Prospectives - IP2I - 2023

Timing activity at IP2I

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cnrs IN2P3 Les deux infinis

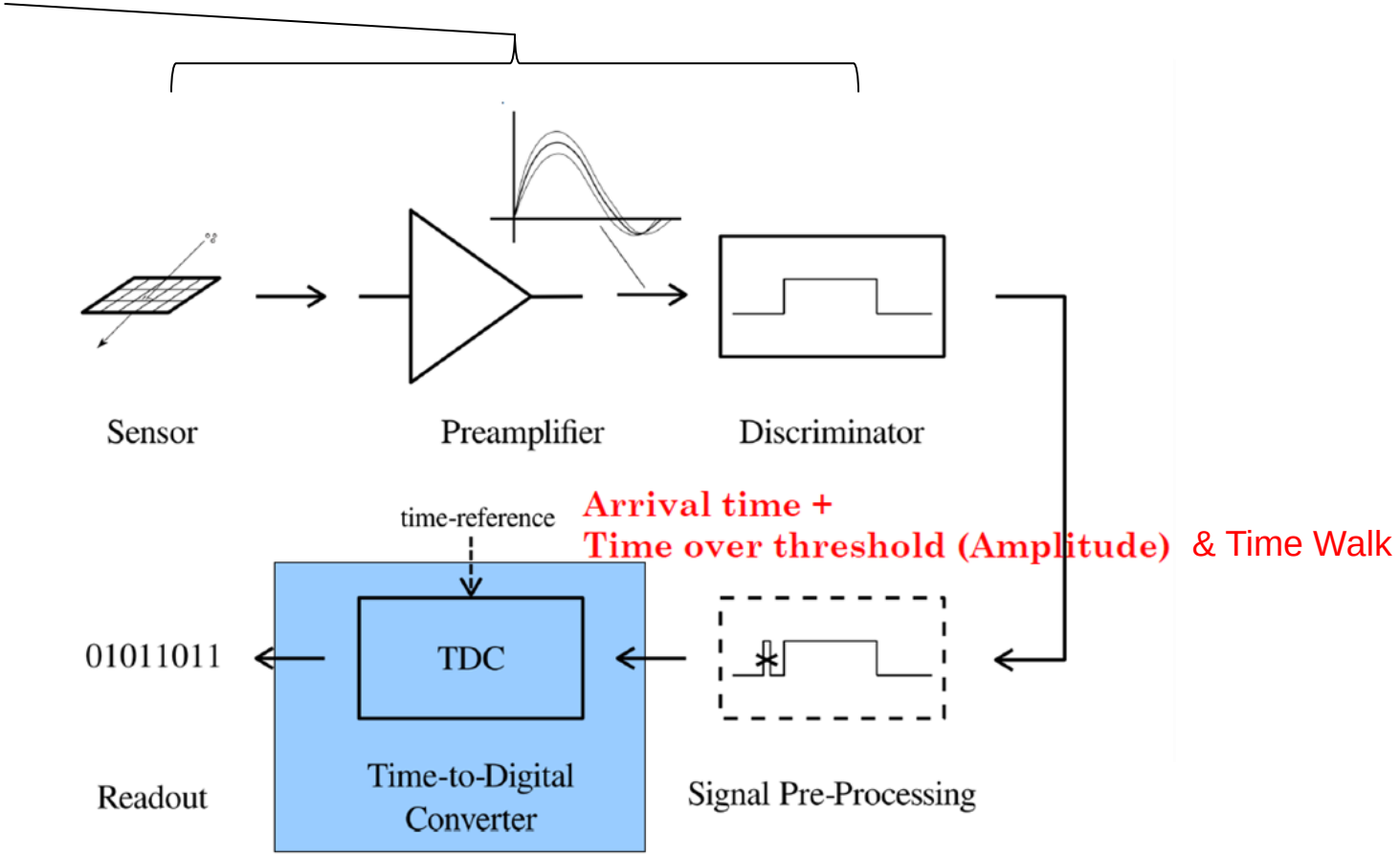
iP2i LES 2 INFINIS LYON

Outlines

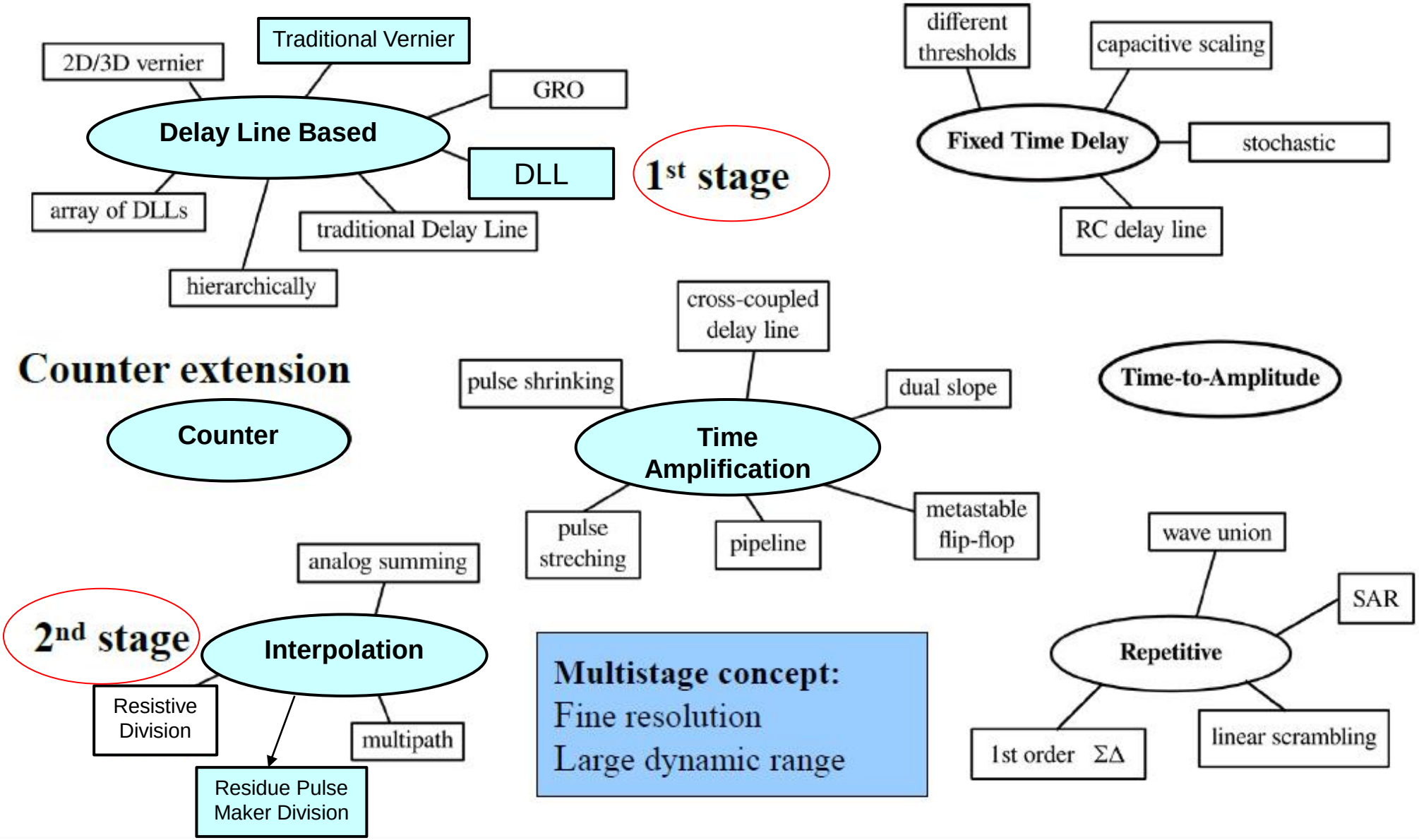
- Introduction
  - Time Measurement Chain
  - TDC Architectures
- Brief State of the Art on TDC Developments :
  - Commercial TDCs
  - TDCs at IN2P3
  - TDCs from others Communities
- TDC Applications :
  - in HEP
  - Other TDC Applications
- Design Constraints in the ps Range
- Skills Developed at IP2I for the Design of Time Measurement Circuits
- Conclusions

Time Measurement Chain

- Detector, Preamplifier and discriminator critical and must be optimized together



TDC Architectures



Commercial TDC Products

Several TDC-Products are commercially available for different applications:

- An example of a low-cost two-channel LiDAR TDC is the Texas Instruments TDC7201 chip which provides **55-ps** resolution
- For applications such as coincidence correlation, a TDC such as Swabian Instrument's Time Tagger, which provides 18 channels with **10-ps** resolution, can be used
- PicoQuant's Picoharp and Hydraharp series, which can provide down to **1-ps** resolution in up to eight channels of operation, are popular TDC products in TCSPC (Time-Correlated Single Photon Counting).
- IdQuantique's ID900 Time Controller is another example of a commercial time tagging box which provides **20-ps** resolution with up to 64-channel operation.

Some TDC ASIC developments

TDC @ IN2P3 (all in tsmc 130 nm) :

- Vernier Ring Oscillator TDC -- Single Phase Detector & Multi Phase Detector TDC @IP2I : ~6 ps rms
- DLL-based TDC for Altiroc @Omega : 20 ps rms (TDC from SLAC group)
- Waveform TDC @IJCLab : ~3 ps rms but very low counting rate (sampling)
- TEAFON TDC @IPHC : has not been tested !
- DiamASICV2 -- DLL-based TDC @LPCCaen : 12 ps rms

TDC examples @ Other communities (65 nm /130 nm):

- PicoTDC/HPTDC@CERN : ~ps rms
- TDCpix for theNA62 Gigatracker hybrid pixel detector) @CERN : ~40 ps rms
- SPAD with TDC ~100 ps binning
- Timepix3 ~1ns binning

FASTIME R&T TDC (Full readout chain: FFE+Discri+TDC+SC+readout… 130 nm):

- ~1 ps resolution simulated for 1pC input charge
- 4 channels including TOA & TOT functionality
- But power and occupied area may be a limitation of this design for some applications
- Characterization is ongoing

TDC applications

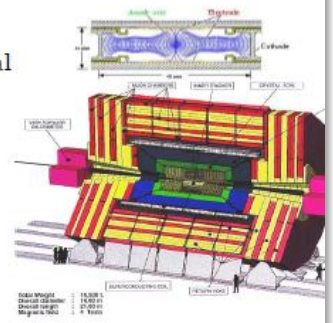
TDC APPLICATIONS IN HEP

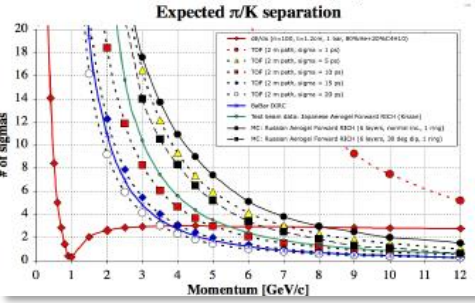
Large systems with many channels: 10k-100k:
Global time resolution/stability across large system critical

- Drift time in gas based tracking detectors
  - **Low resolution: ~1ns**
  - Examples: CMS, ATLAS, LHCb, PANDA drift tubes
- TOF, RICH
  - **High resolution: 5 – 100ps**
  - Example: ALICE TOF
- Background reduction: **5 – 10ps**
- Vertex identification from timing: **5 - 10ps**
- Signal amplitude and time walk compensation: Time Over Threshold (TOT)
  - Or constant fraction discrimination in analog FE
- Triggered or non triggered

New TDC with programmable resolution: 3ps, 12ps, (400ps ?)

- Power consumption highly resolution dependent

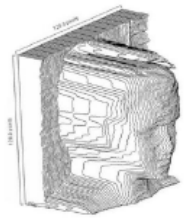


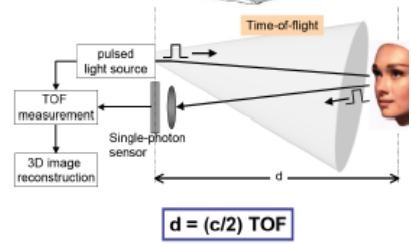


Christiansen @ CERN/PH-ESE

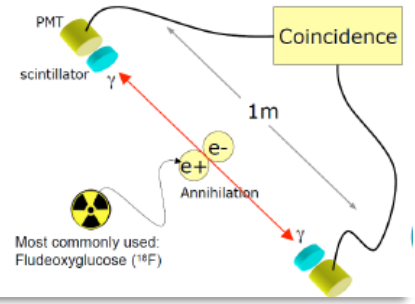
OTHER TDC APPLICATIONS

- Laser ranging
- 3D imaging
- Medical imaging: TOF PET
  - Improve signal/noise, lower radiation
- Fluorescence lifetime imaging
- General instrumentation.
- Differences to HEP systems
  - Small systems - Few channels
    - Time resolution/stability between channels on same chip
  - Averaging can in many cases be used to get improved time resolution





d = (c/2) TOF



Difficulties in the ps range

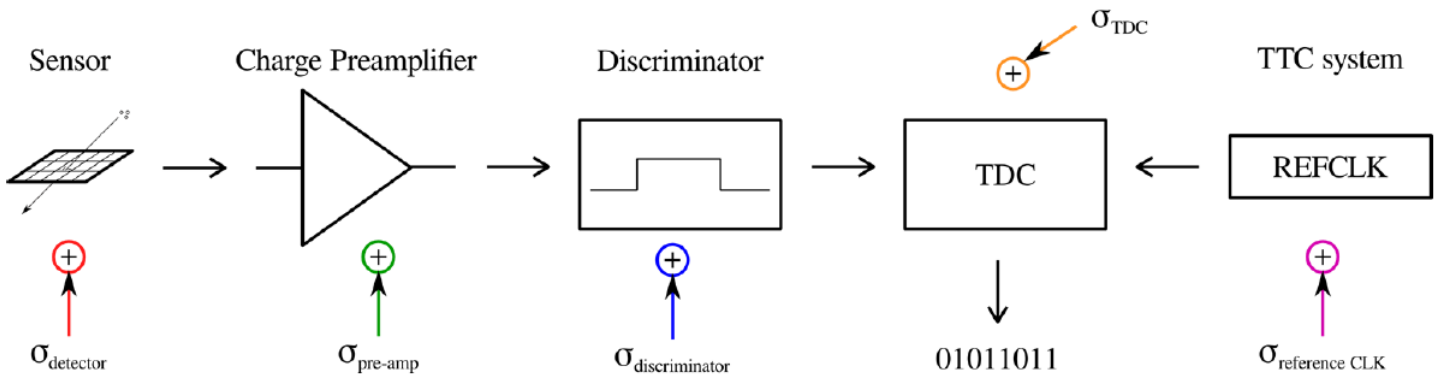
- **Calibration** is a **must**, but at what rate
  - We therefore tend to prefer **auto calibrating** architectures based on DLL's (basic offset calibration still required)
- **Slew rate** of signals much slower than resolution aimed at (digital signals do not exist in the ps domain)
- **Matching** gets critical and **mis-match compensation** becomes a **must** if aiming at **~ps** resolution.
- Distribution of timing signals gets critical (R-C delays in Al, Cu wires, via's, contacts, etc.)
- **Metastability** in timing capturing circuit gets significant/critical.
- **Interpolation** to high ratios gets increasingly **sensitive** to power supply noise (even for the digital approaches), substrate coupled noise, etc.
- Routing delays are significant and difficult to balance (especially for loop feedbacks and parallel load of many registers)
- Phase error across DLL (phase error in PD and end-begin effect)
- Testing a TDC with ps resolution is far from trivial
  - Stochastic testing for linearity (Code Density Test).
  - Fixed delays for jitter and stability.
  - Time sweep if you can find the appropriate instrument (resolution and jitter) and can afford it

System level performance is what counts in HEP !

- Detector, analog front-end, discriminator, time walk compensation, board design, power decoupling, connectors, cables, stability (jitter) across full system, timing distribution across full system, calibration, , ,

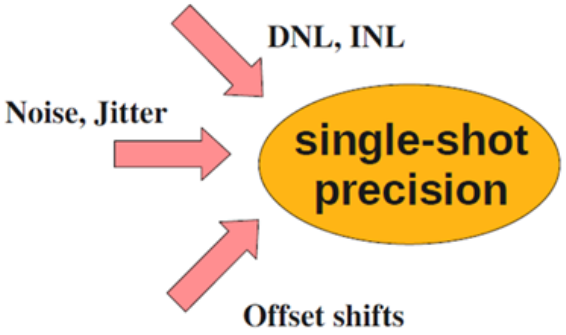
Difficulties in the ps range: System Level resolution

- the overall standard deviation of the chain corresponds to the quadratic sum of the individual jitters of each element of the chain



Complete Measurement Chain

- Detector Noise
- Analog Front End
- Time Walk Correction
- Time Reference Noise
- TDC Noise
- Inter-channel Crosstalk
- PVT variation ...

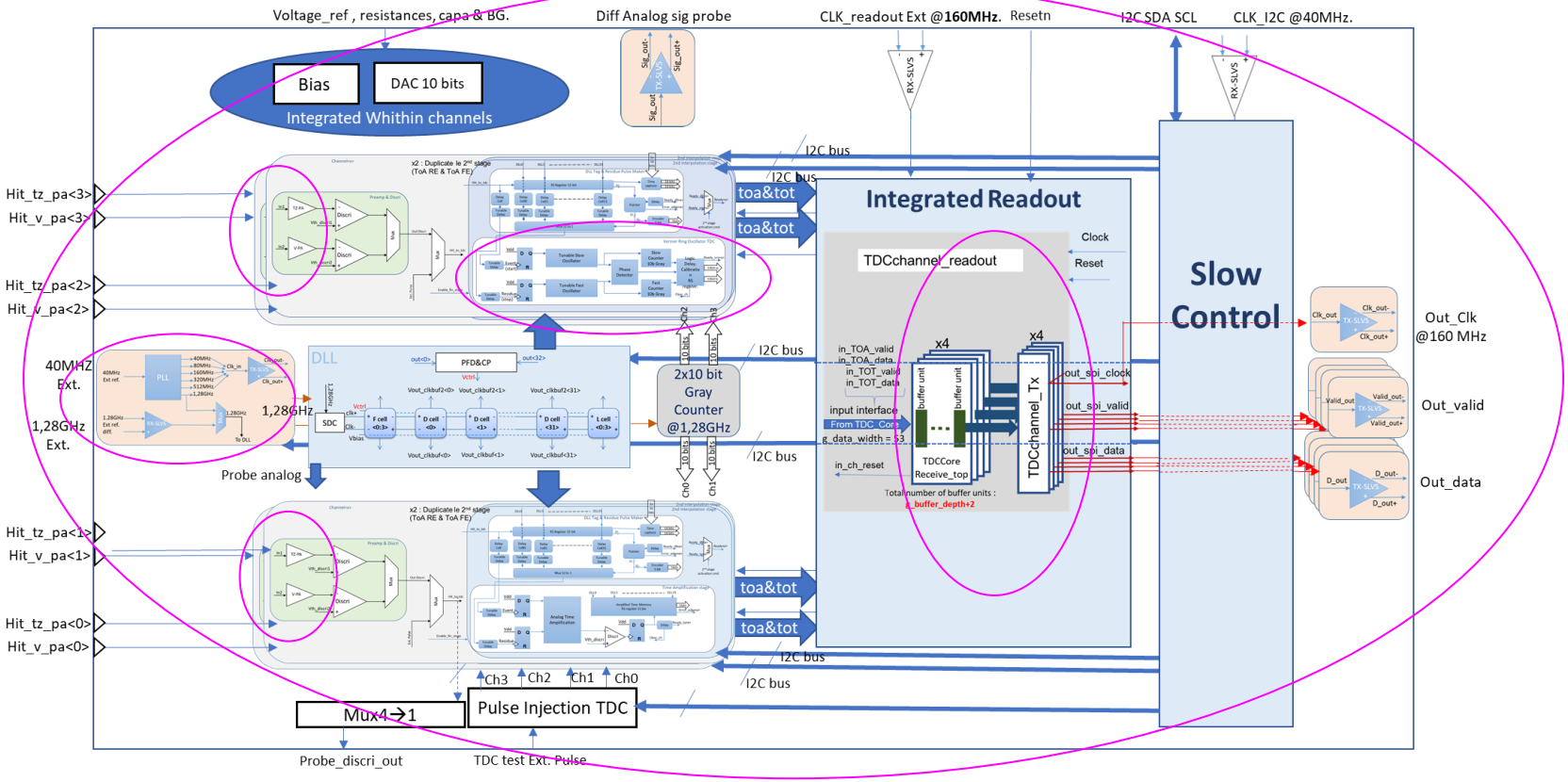


LSB/sqrt(12) ≠ rms

Skills on Timing Developments @ IP2I (Eg. FASTIME ASIC)

- Low jitter PLLs (tsmc65nm and 130 nm).
- Fast Front End : High GBW product and low jitter
- Vernier Ring Oscillator TDC
- System Level TDC : System integration

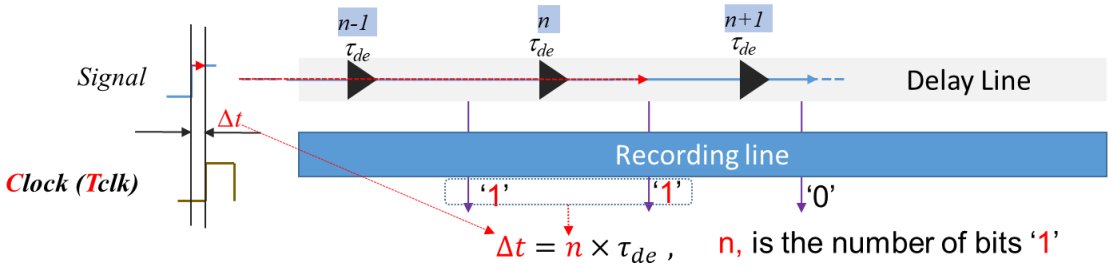
The blocks designated at IP2I Lyon are circled in pink



We could not be abled to design such a complete circuit without collaborating with 5 other laboratories for the design of DLL, Time Ampli TDC, Residue Pulse Maker, Tuning Cells, I2C, Discri, Gray Counters, DACs …

Skills on Timing Developments @ IP2I : TDC on FPGA

TDL interpolator (J.Wu, 2003)



Some realizations

Item	Target FPGA	TDC type	Number of channels	characteristics
1	Cyclone V	TOT (time-to-threshold)	2	Precision (RMS) of TOA (time-of-arrive) :~10,5 ps Precision (RMS) of TOT: ~18 ps Dead time : 10 ns
2	Cyclone V	Multichannel	56	Precision (RMS) of TOA (56 channels): 10 ps et 20 ps Dead time : 7,5 ns
3	Cyclone V	Multichannel	34*3	Precision (RMS) of TOA (56 channels): 10 ps et 20 ps Dead time : 7,5 ns
4	Polarfire	Normal	2	Precision (RMS) of TOA (time-of-arrive) :~3,6 ps Dead time : 10 ns
5	Polarfire	Radiation hardned	2	Precision (RMS) of TOA (time-of-arrive) :~7 ps Dead time : 10 ns

Pros :

- Flexibility and short design time
- Suitable for discreet chains
- Synchronizing discreet systems
- ….

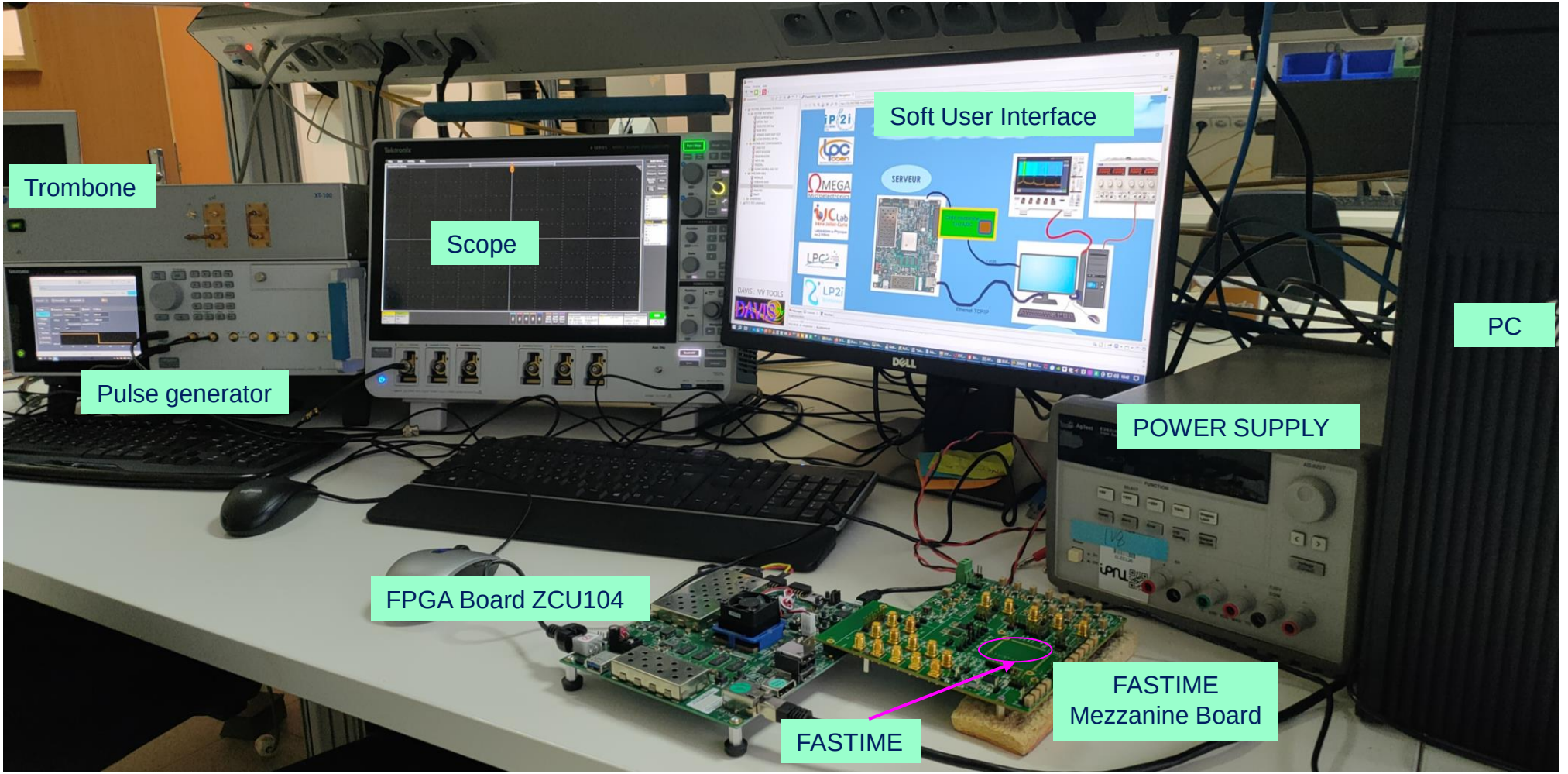
Cons :

- High power consumption
- Less radiation tolerance
- Not suitable for systems or detectors with a very large number of channels
  - Eg. FCCee FCChh etc..

Future activity on FPGA Timing :

- Timing Data analyzing and characterization of ASIC TDCs
- Synchronizing systems/boards
- Etc…
- But FPGA TDC circuit development per se would not be suitable @IP2I

Skills on Timing Developments @ IP2I :Test and characterization of TDCs



FASTIME Characterization Setup

Questions et conclusions :

- Avons-nous une masse critique et toutes les compétences pour prendre en main tout seul (@IP2I) les développements de TDC qui sont de plus en plus complexes et précis
- Dans un design de TDC une grande partie est purement digitale (SC, readout, processing, Buffering…)
  - Avons-nous cette compétence en local ?
  - Si oui serait-elle pérenne
- Nature des développements sur le Timing que l'on souhaite poursuivre et/ou commencer :
  - Ferions-nous des TDCs comme FASTIME, Sampic ou PicoTDC et rester dans « la course » a la résolution sub-picoseconde *(FASTIME diffère des deux autres exemples car il intègre une chaine complète de mesure)*
    - Dans ce cas, vers quel type de technologies migrons-nous
      - Asic Hybride (FFE et TDC dans deux techno différentes puis intégration 3D, stitching etc
      - Aurions-nous les financements pour des MPW RUN dont le prix augmente selon la finesse de gravure
  - Ou bien orientons-nous vers des briques de tdc relativement simples à intégrer dans des gros capteurs monolithiques (eg. MAPS+timing)
    - Dans ce cas, nous engageons-nous à faire du R&D sur les architectures de readout qui puissant intégrer le timing de fait (de point de vue architectural de la matrice de pixel par exemple)
  - Avons-nous les moyens de suivre des activités sur les deux fronts
  - Nous sommes équipés d'un matériel de très grandes précision (le meilleur à l'in2p3)
    - Acceptons-nous de servir de plateforme de caractérisation des circuits TDC de la communauté ?
  - Etc…

THANK YOU