Prospectives IP2I

Futur Collisionneurs FCC: Forum 2, Trajectographie

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Challenges in the design of ASICs for future colliders tracking detectors

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Motivation (and disclaimer)

Disclaimer: the following aims at briefly summarizing the topic from a designer (personal) point of view

- The microelectronics group at IP2I had a leading role in the design of a fully digital ASIC for the front-end electronics of a tracker system in CMS:
  - this design experience ended in 2021
  - currently getting experience in the design of a MAPS pixel detector
  - expression of interest in some of the ECFA DRD7 sub-topics
- Microelectronics (still) play a fundamental role in HEP research
- ASIC R&D is justified by commercial microelectronics technology evolution (steady pace) and new HEP detectors requirements:
  - integration of increasingly complex features progress at the same pace
- Major drivers for the innovation of microelectronics in HEP are the tracking detectors:
  - tracking algorithms are among the most time consuming and computation intensive aspects of event reconstruction and tracker detectors are vital elements of collider-based HEP experiments
  - requirements for future trackers (future trackers) are significantly more demanding than currently available technologies
- More intelligence is required in the FE electronics when particle density increases

Requirements

Pixel detectors are (today) the technology of choice in high-rate and radiation applications
Readout architectures are mostly specific to the target application

Challenges:
Increase in data density
Precision timing resolution (in tracker environment) (Mokrane slides)
Segmentation and position resolution
Tolerance to fluence
Total detector surfaces and fabrication costs
Mass budget
Cooling

Possible targets:
65n MAPS
28n hybrid ASICS
Large-area sensors
Coping with increased data desity and high data rates with highly configurable, AI/ML driven, FE electronics
Power management
4D/5D techniques
Emerging technologies

Methodology (see Benedetta slides)

Technology boosts (0.25um → 130n → 65n → 28n) drive design complexity

- long and careful characterization of new technologies to minimize the effects of increased radiations levels
- adoption of new technologies by the HEP community is a difficult trade-off between:
  - radiation hardness
  - frequency and cost of MPW runs
  - market presence
  - circuit density/speed
- Evolution of the physics requirements demands an increase of complexity: high-level (system) design languages are now commonly adopted for the design and verification of those ASICS
  - the increased abstraction level in design methodologies permits multiple chip description levels
- The largest part of the design effort is dominated by the verification process
  - direct testing often only detects foreseen bugs having specific features
- Data (design) management:
  - team design, integration with the existing workflows, tracking of variants and releases, access permissions, reusing of IPs and PDKs
  - text files are the digital designer data: software management techniques are largely adopted but still complex
- Development of sensor readout:
  - 4D tracking includes timing information in the pattern recognition and parameter estimation
  - 5D and pixel-clusters shape provide an additional dimension for the track seeding
  - unified design of full systems

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- standard methodology consists in system-level modeling of the design and development of reusable verification environments to be used by multiple designers with different needs and goals
- the keys are: constrained random stimuli generation + functional coverage +layered and reusable testbenches

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- on chip data reduction using AI/ML techniques
- neuromorphic Front-End Solution Dynamic vision sensor DVS based pixels for SNN algorithms
- on-chip inferences still require algorithms development