Quels développements en électronique pour la physique des hautes énergies ?

La perspective de CERN-EP-ESE

Francois Vasey, 14 septembre 2023

Agenda

1. Contexte
2. Trois piliers et un cadre pour la R&D
3. Les choix de CERN-EP-ESE

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1. Contexte
   a. Programmes scientifiques
   b. Compétences et activités
   c. Environnement collaboratif
2. Trois piliers et un cadre pour la R&D
3. Les choix de CERN-EP-ESE

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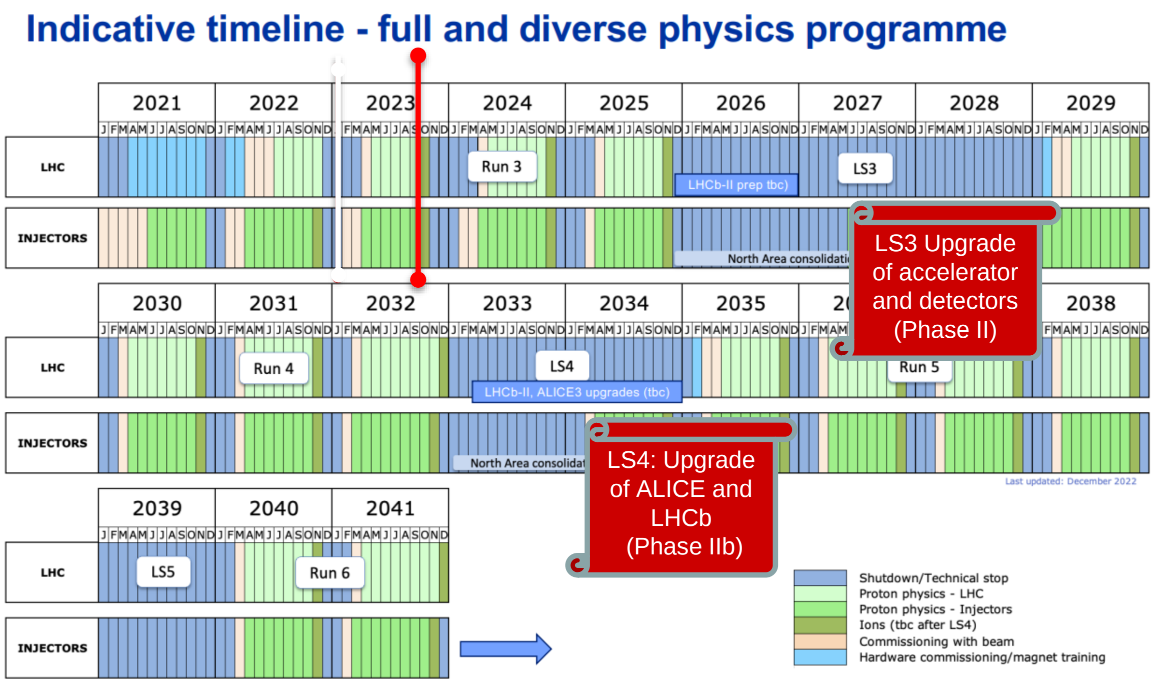
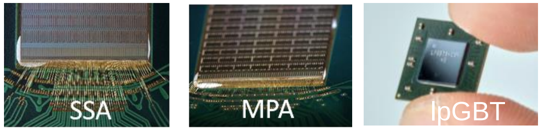
Au programme: LHC et HL-LHC

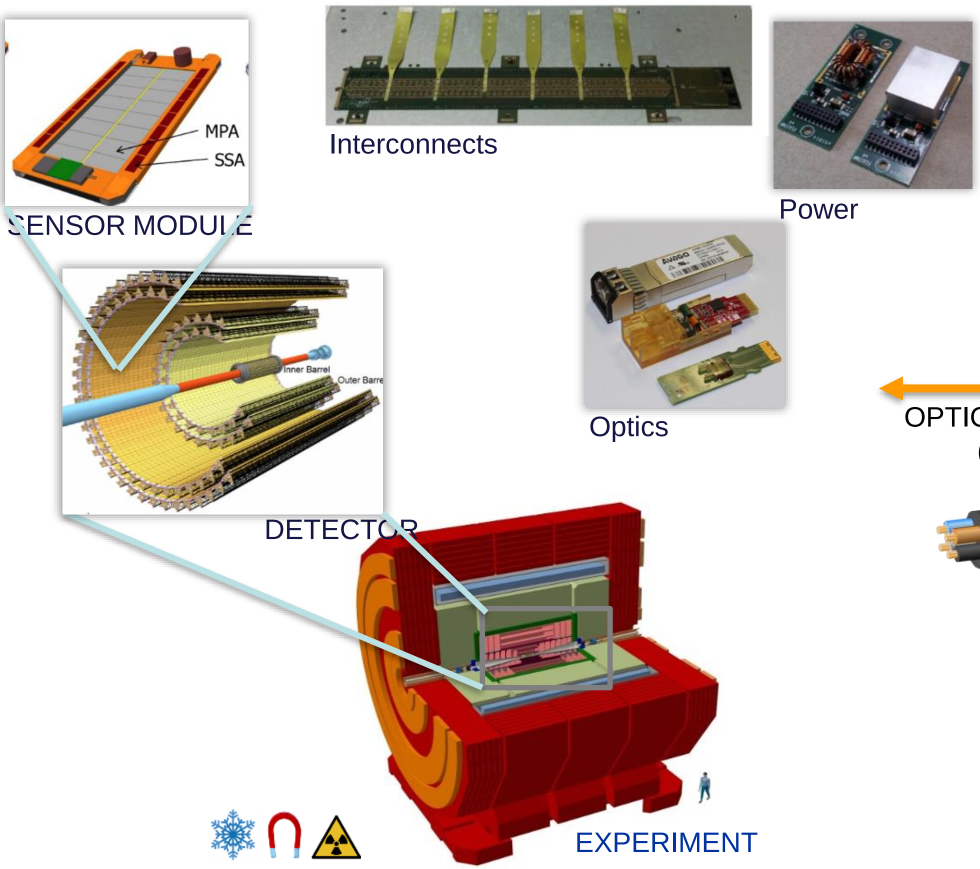


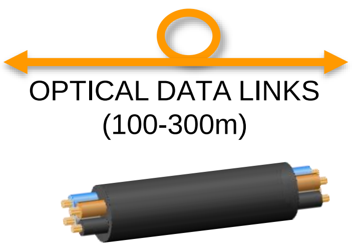
Compétences et activités



ON DETECTOR ELECTRONICS (FRONT-END)

OFF DETECTOR ELECTRONICS (BACK-END)





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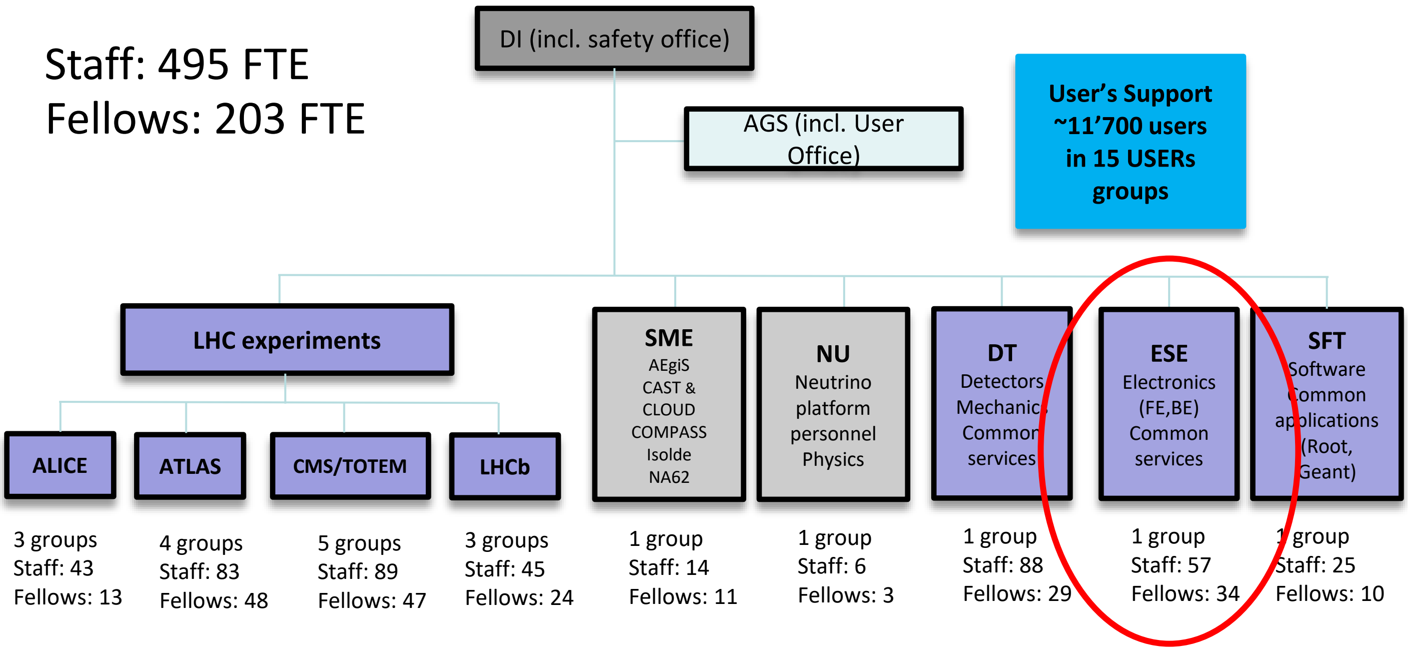
L'environnement collaboratif

CERN-EP Department Structure

Staff: 495 FTE
Fellows: 203 FTE



~90% of resources are focused on LHC experiments and their upgrades

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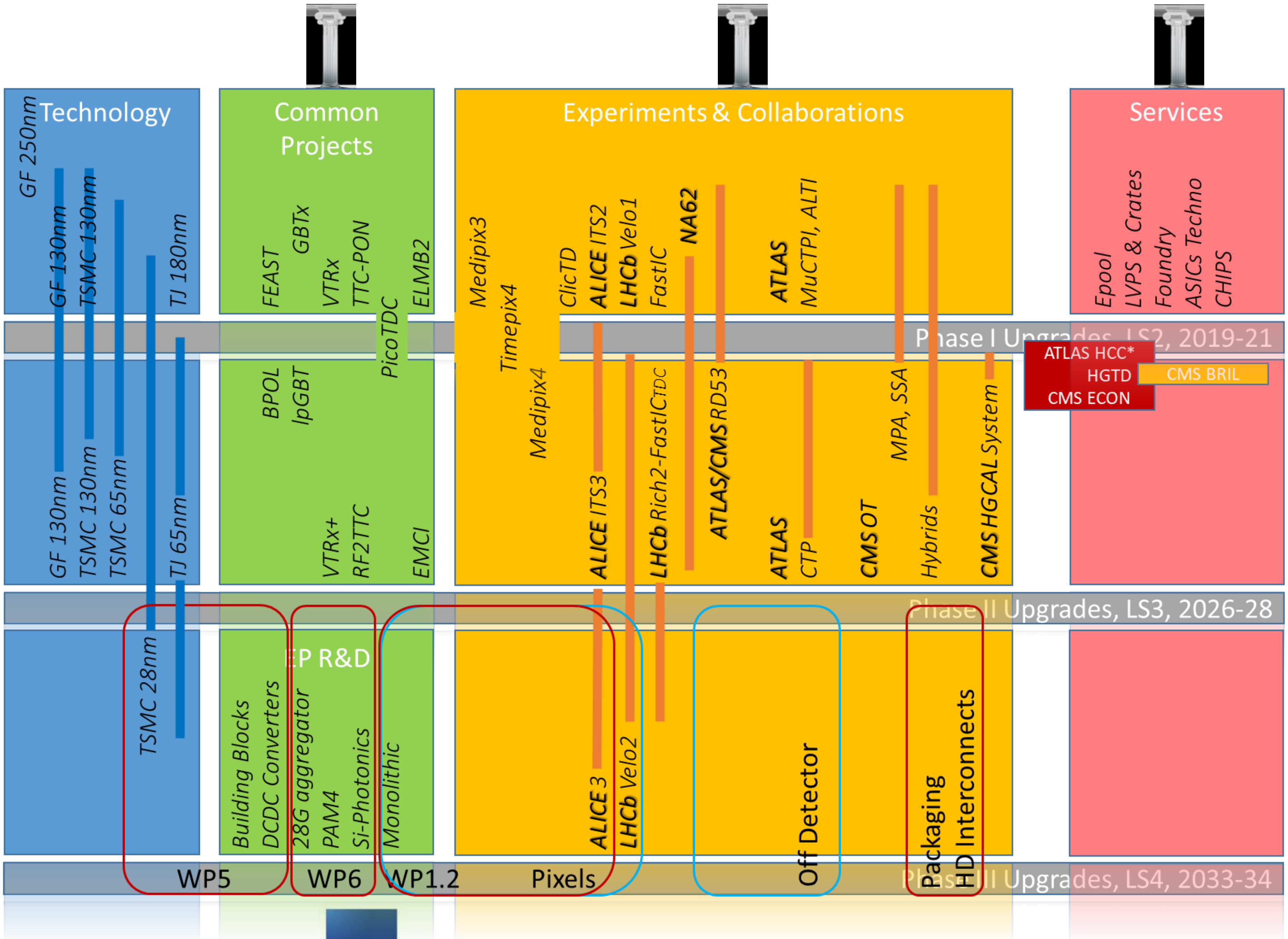
Les trois pilliers

- Experiments
- Common projects for experiments and R&D
- Services

ESE Activity Portfolio and Evolution

EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS



EP R&D

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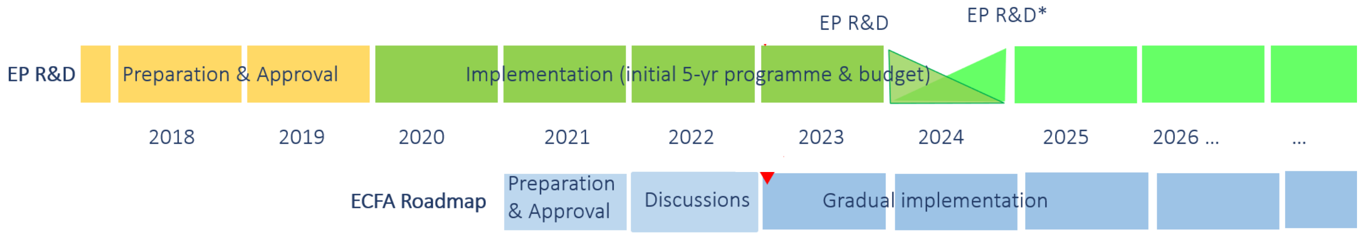
Un cadre pour la R&D



- LOCAL: EP R&D, CERN strategic programme on technologies for future experiments
  - Being continued (requests approved for 2024-2028) and expanded
  - ESE has projects for WP1.2 (monolithic CMOS), WP5 (IC developments) and WP6 (Links)
    - Will be the ESE research arm, in synergy with detector-specific developments

- GLOBAL: ECFA Detector R&D, international programme on strategic R&D for future detectors
  - Being implemented for gradual start in 2024, to reach full speed in 2026
  - CERN's contribution via EP R&D workpackages
  - Community is self-organizing as Detector R&D collaborations (DRDs)
    - DRD7: Electronics
    - A unique opportunity to adapt structurally to the evolving technology landscape
    - DRD7 Workshop on 25-26 Sep

A Roadmap for which Facilities ?

Future Facilities Timeline

< 2030	2030-2035	2035-2040	2040-2045	> 2045
SPS fixed target Other fixed target; FAIR (hep) Belle II ALICE LS3 PIP-II/DUNE/Hyper-K	ALICE 3 LHCb (≥ LS4) EIC LHeC	ILC	FCC-ee CLIC	FCC-hh FCC-eh Muon Collider Plasma Collider

- 'Chicken-and-egg' problem
  - Cannot define an R&D timeline without knowing the approximate dates of future facilities
  - Cannot predict dates of future facilities without knowing R&D needs
- Detector / accelerator roadmaps have used a common timeline
  - Highly approximate, and not to be used out of context
  - Dates represent the 'earliest feasible date', driven by both technical considerations and the processes of approval
  - The goal on both sides is that R&D shall not be the rate-limiting step

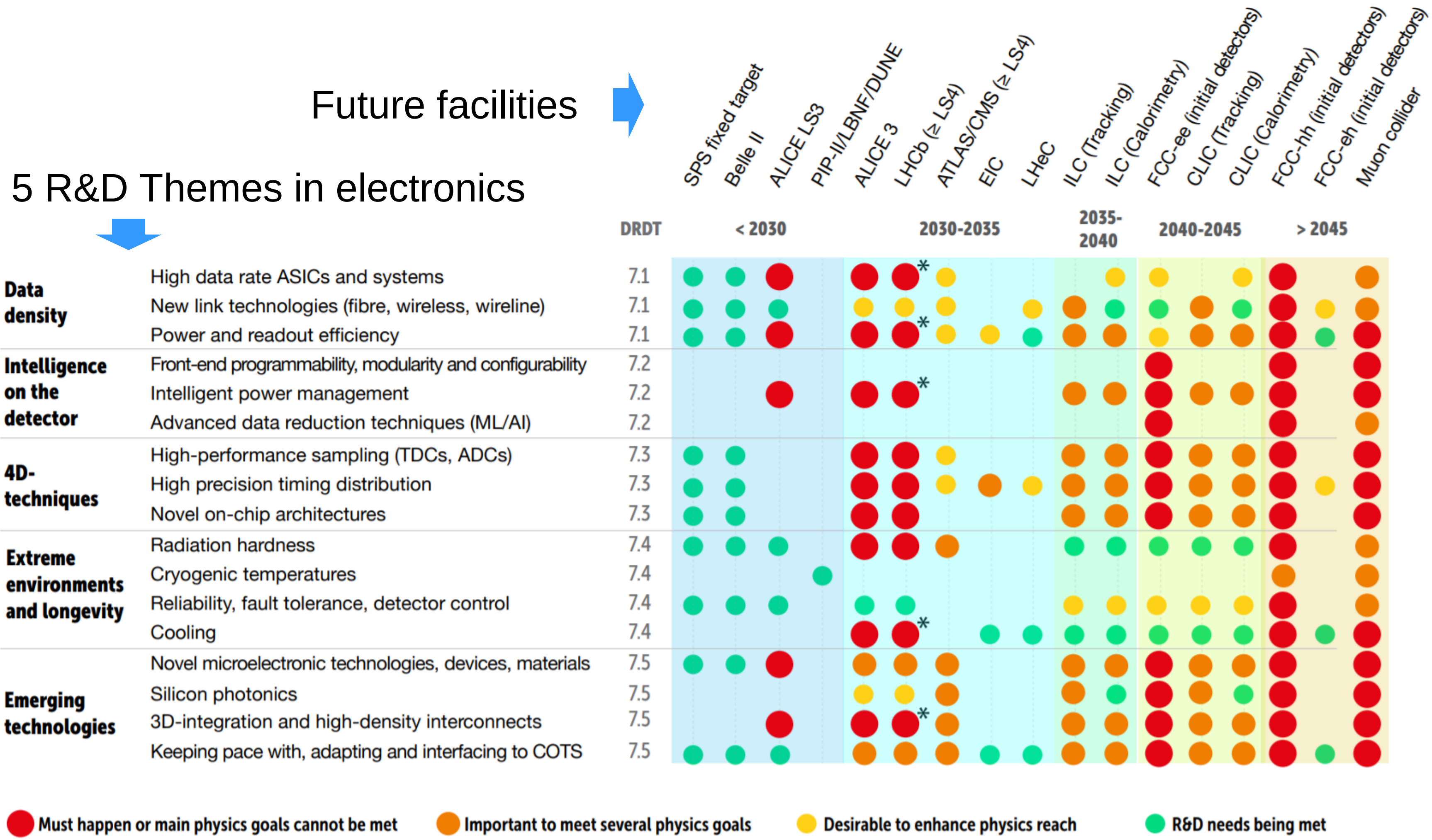
21 ECFA, 18th November 2021 Dave.Newbold@stfc.ac.uk UKRI Science and Technology Facilities Council

TF7 Recommendations

a) Detector R&D Themes, Electronics

Future facilities

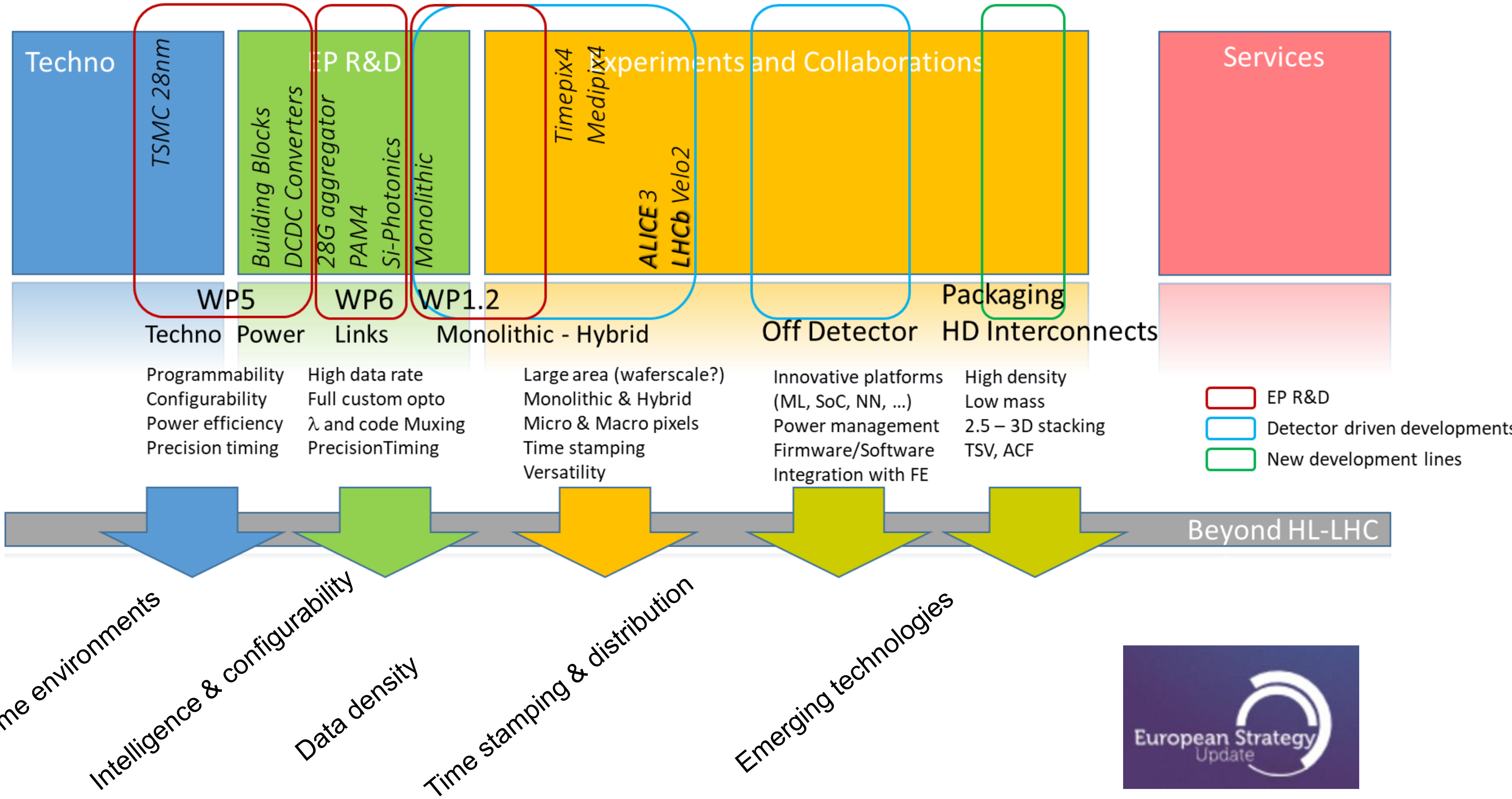
5 R&D Themes in electronics



* LHCb Velo

ESE Activity Evolution

WP1.2: 1.3M, 16.5FY, 8SY
WP5: 2.3M, 14FY, 14SY
WP6: 0.8M, 12FY, 8SY
over 5 yrs (2020-2024)



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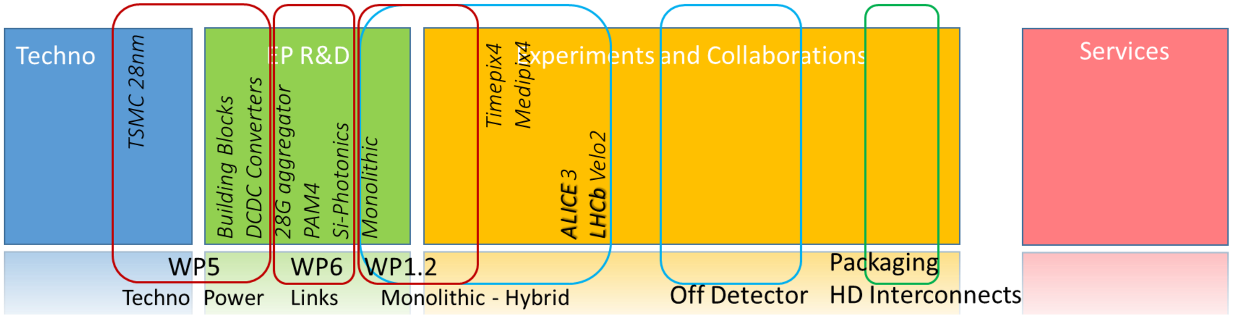
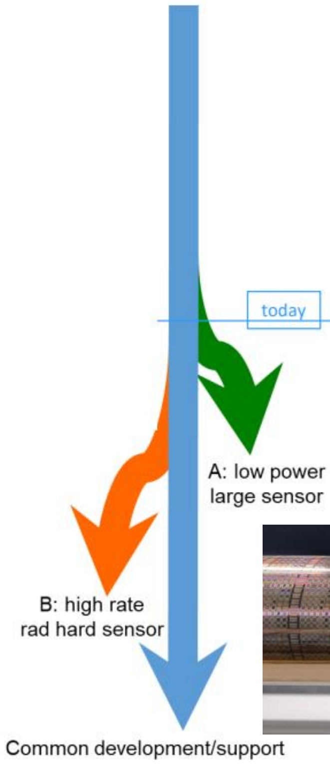


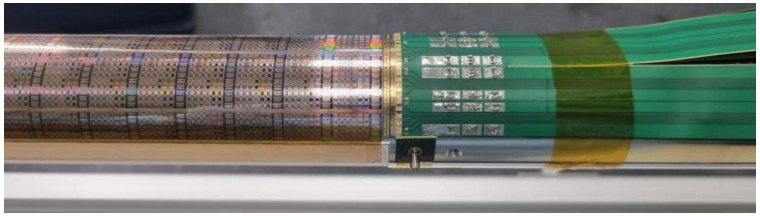
WP1.2 Monolithic Si Pixel Detectors

WP1.2 Timeline, Scope and Results

EP R&D



Time	*Scope*	*Submissions* TPSCo ISC 65nm
Phase I 2020-21	Technology Test structures Collaboration Framework	MLR1 Dec20
Phase II 2021-22	Technology iterations Test demonstrators Dissemination	ER1 Nov22
Phase III 2023-24	Technology iterations Full chips	ER2 Exp. 2024
		MLR2



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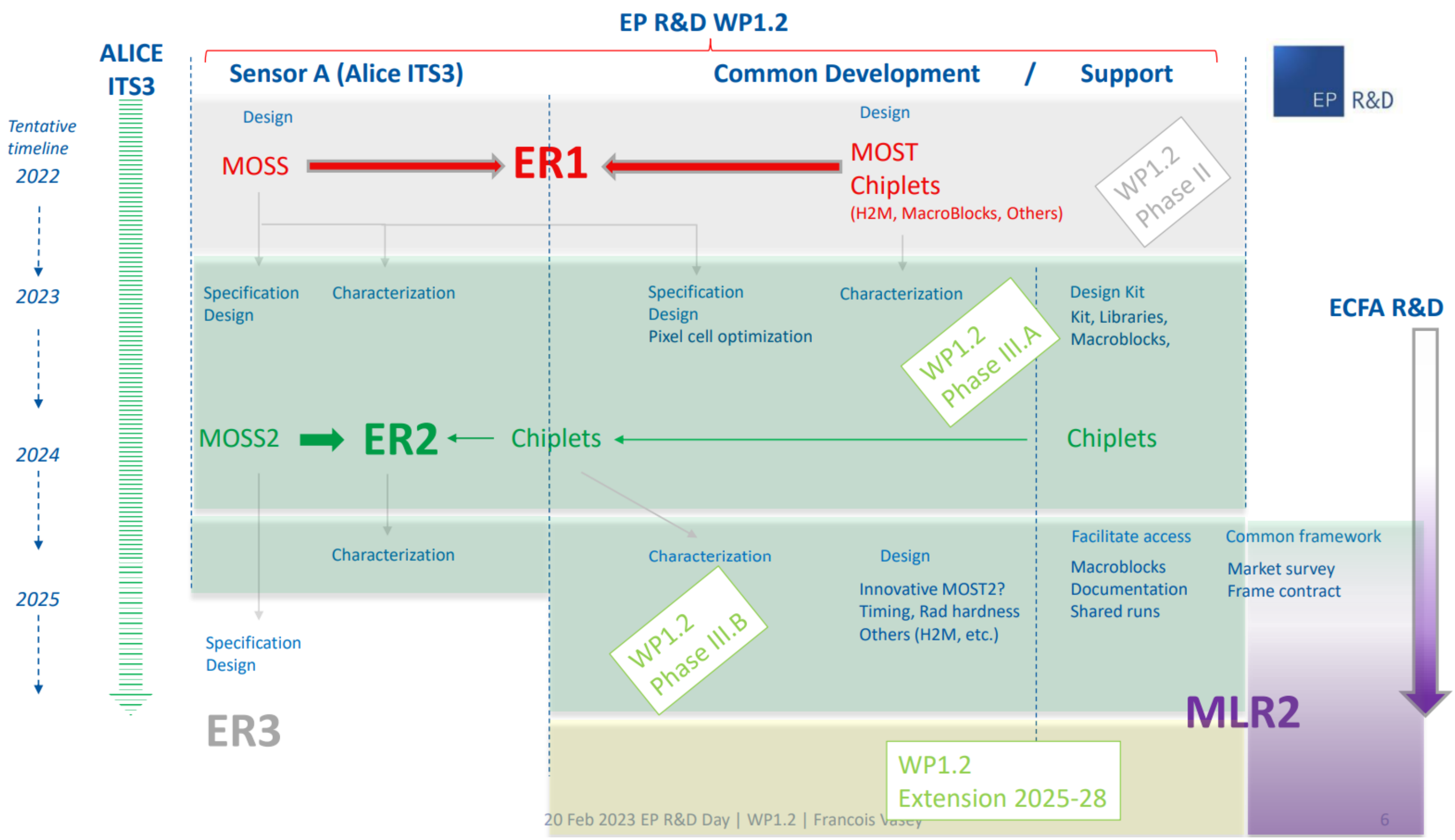
WP1.2, continuation



EP R&D

WP1.2 deliverables

	2024	2025	2026	2027	2028
Deliverables:		Des.Kit & Libraries	Report ER2	Report MLR2	Report MLR3
Tape-out dates:	ER2	MLR2		MLR3	MLR4

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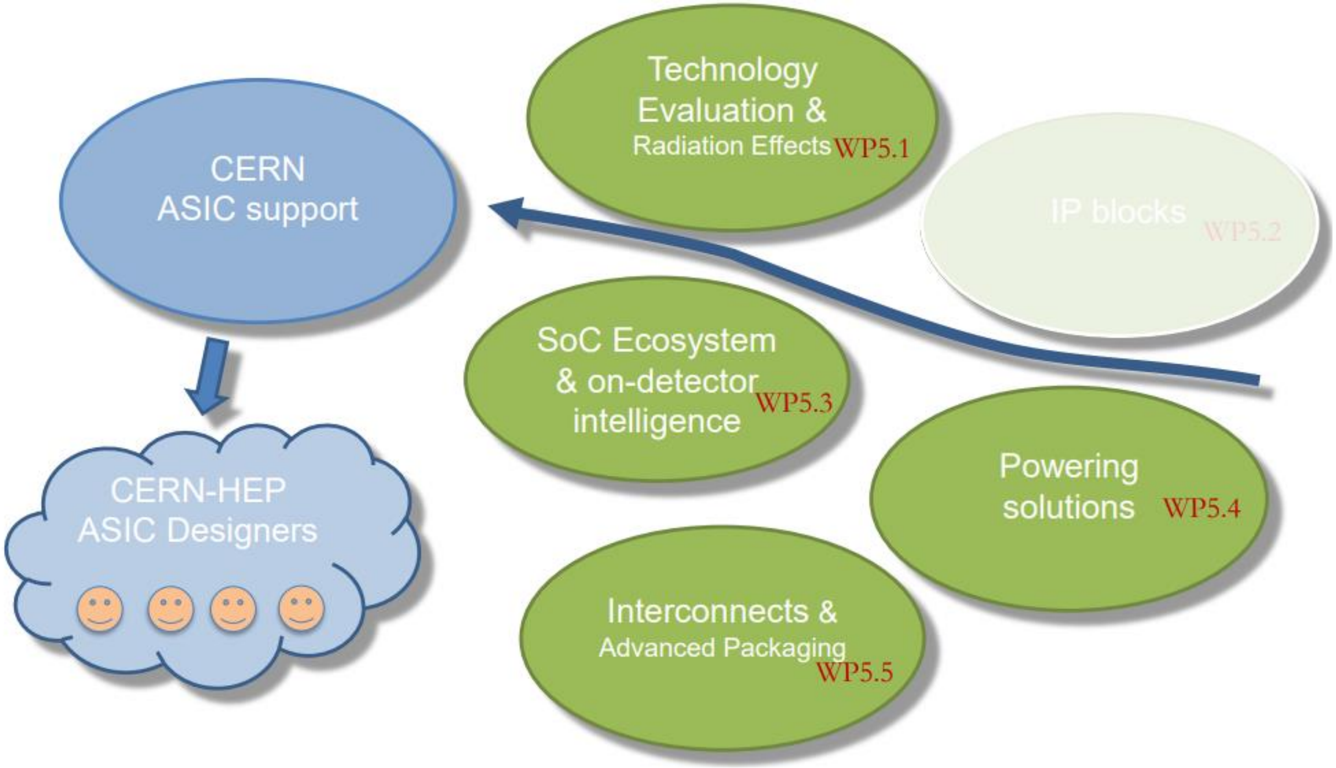
WP5: IC Technologies



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WP5.3 SoC & Data Processing

TWO COMPLEMENTARY R&D ACTIVITIES:

CONTROL & MONITORING

RISC-V BASED

- STANDARDIZED SOLUTION
- OPEN SOURCE
- FULLY RADIATION TOLERANT
- ECO SYSTEM OPEN TO HEP THE COMMUNITY
  - RT SOC IP BLOCKS
  - RT SOC INTERCONNECT

Stand alone applications of Control & Monitoring

DATA PROCESSING

ASIP BASED

- APPLICATION SPECIFIC INSTRUCTION SET PROCESSOR
- COMMERCIAL TOOL – ASIP DESIGNER BY SYNOPSIS
- CUSTOM ISA
- CUSTOM MICROARCHITECTURE

IP blocks to support the implementation of Data Processing applications

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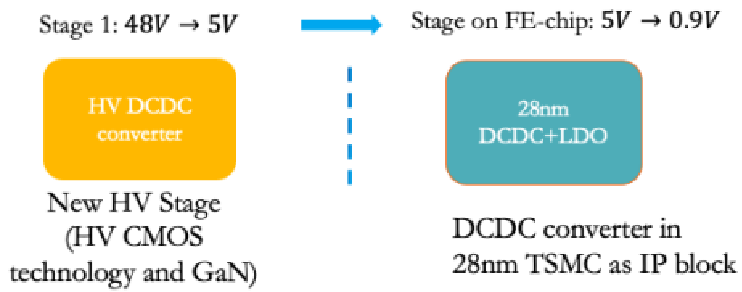
WP5.4 Powering Solutions



Slide by: S. Michelis

Stage 1: 48V → 5V

Find a new CMOS HV technology (old one no longer available) ⎫ Full radiation characterization
Explore the new upcoming GaN commercial technologies ⎭ (TID, DD, SEE)

Find a suitable architecture for this high conversion ratio with main specification
low volume, low noise, high efficiency, higher radiation hardness (bPOL48 only rated up to 5e14 n/cm2)

Power module design: provide to the experiment a small and optimized "brick"
with all active and passive elements included.

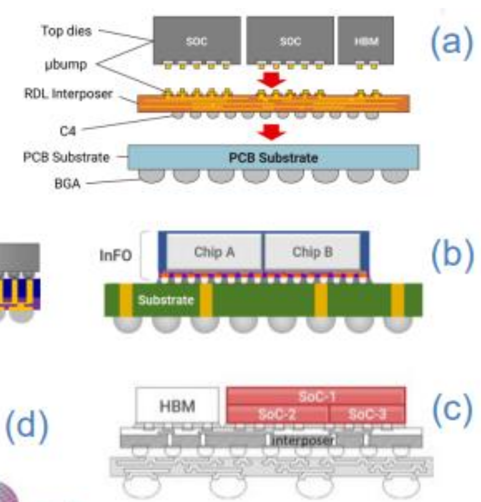
Stage 2: 5V → 0.9V

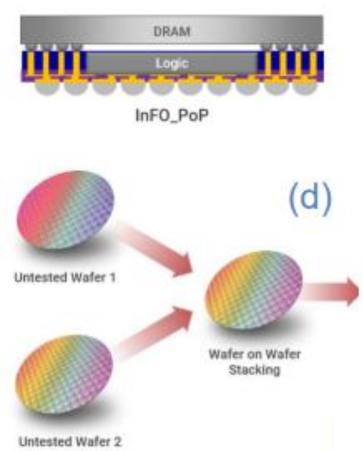
Continue the recently started R&D activity to:

- reach production readiness
- improve the design for a modular approach where designers can easily connect blocks for higher output current (>3A)
- design a linear regulator from 5V → 0.9V - 1.2V necessary for some I/O pads
- explore derived topologies for higher output voltages

WP5.5 Interconnects & Packaging

- Advanced packaging & 3D Interconnects
  - Technology survey, access and evaluation
    - Silicon Interposer (a)
    - Wafer Level Packaging & TSVs (b)
    - Chip on Wafer (c)
    - Wafer on Wafer (d)
  - Enabler for many applications
    - Hybrid detectors
    - Si Photonics
  - Timeline
    - Phase A
      - Identify industrial collaborators
      - Comparison between the ‘third-party’ and ‘turn-key’ approaches
    - Phase B
      - Invest R&D funds to test the viability of the technologies
      - Test vehicle ASICs (ex. TimePix4)



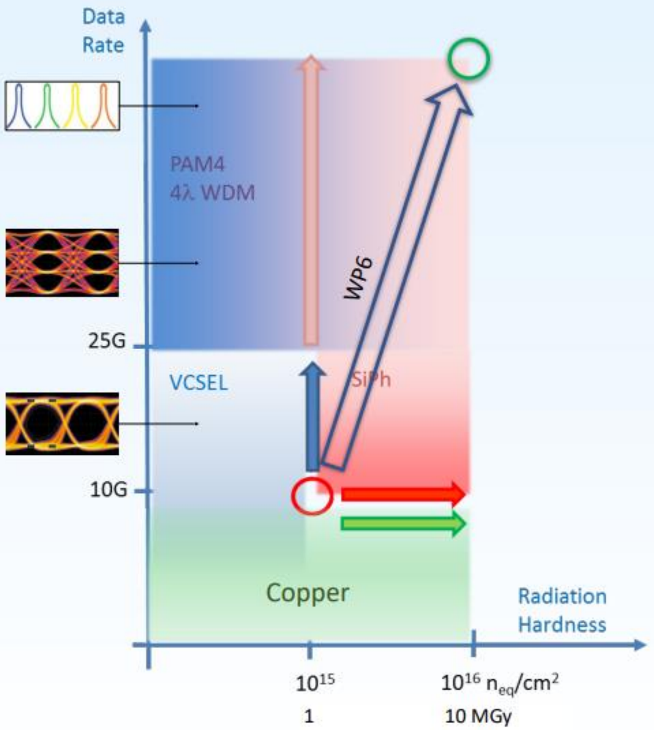


WP6 High Speed Links

WP6 Goals

EP R&D
WP6 High Speed Links

- Provide the future HEP systems with:
  - High bandwidths: ~25 Gbps / lane
  - High radiation tolerance *c.f. ECFA roadmap*
  - Low power, low mass
- FPGAs
  - Compatible with the state-of-the-art
- ASICS
  - Advanced technologies 28nm CMOS
  - High order modulation formats (PAM4)
  - Drivers for SiPh optoelectronics
- Optoelectronics
  - Silicon Photonics (SiPh)
  - External Modulators
    - Ring & MZ
- Wavelength Division Multiplexing (WDM)



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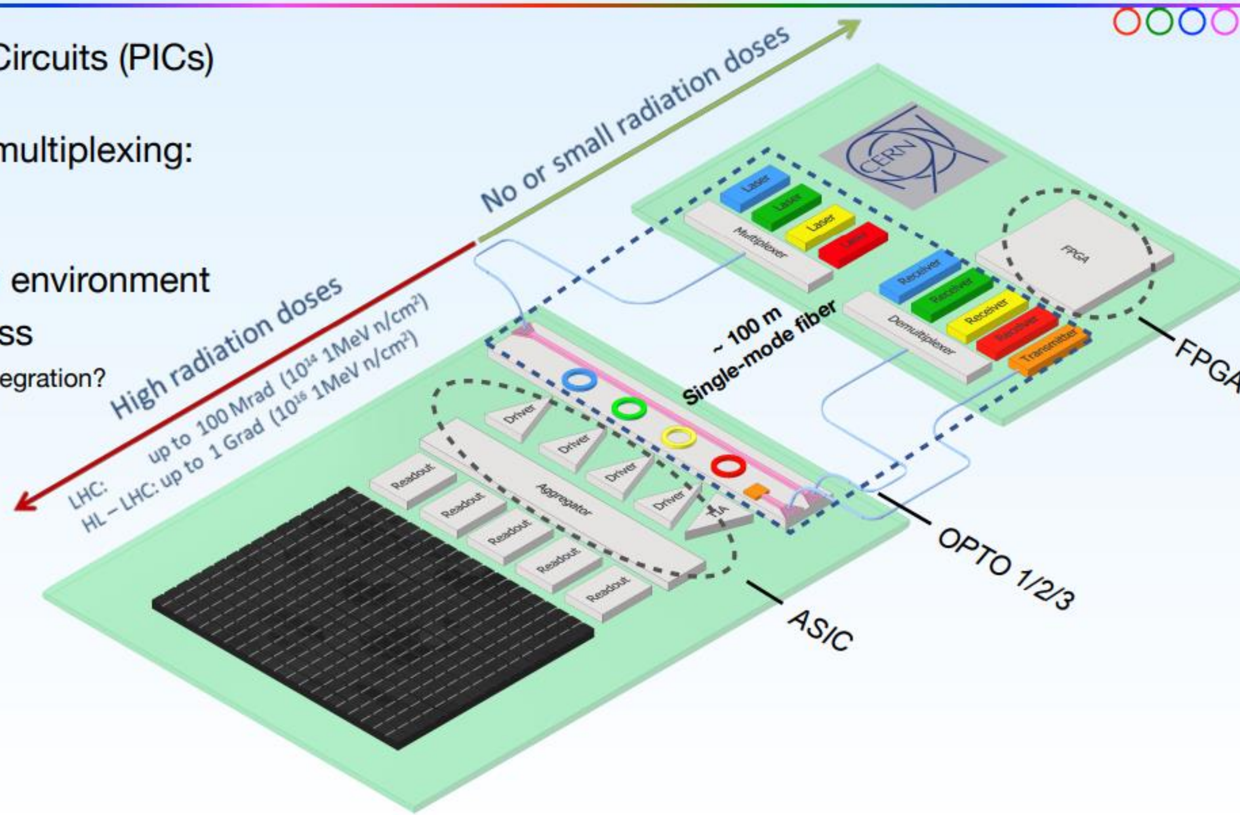
WP6 vision

WP6 Project updated breakdown

EP R&D
WP6 High Speed Links

- Photonic Integrated Circuits (PICs)
  - RadHard "promise"
- Wavelength division multiplexing:
  - Lane: 25 Gbps NRZ
  - Fibre: 100 Gbps
- Laser out of radiation environment
- Low power / Low mass
  - How far can we push FE integration?



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WP6-addition 1

ASIC-3: RH FPGA

EP R&D
WP6 High Speed Links

- FPGAs have been enablers of HEP off-detector systems
- Rad-Hard FPGAs that can be installed inside HEP detectors are not available
- Some on-detector functions would benefit from embedded programmable logic:
  - Data concentrators/aggregators
  - Trigger algorithms
- We propose to study the feasibility of developing a moderate complexity (realistic for our community) Radiation-Hard FPGA (RH-FPGA)
  - But, nonetheless, useful for embedded detector systems
- The study should answer questions like:
  - Which detector systems could benefit?
  - Which architectures are best suited for data concentrators, data compression and trigger algorithms?
- It will propose:
  - Architectures
  - Software and firmware tools
  - Minimum hardware set
- Depending on the study conclusions, a proposal for a demonstrator ASIC will be made

WP6-addition 2

FPGA-3: Ethernet Link for Front-Ends

EP R&D
WP6 High Speed Links

- Streaming data directly from detector front-end to the DAQ processing farm is very attractive for trigger-less DAQ architectures
  - Would require sending output of FE datalink directly into a commodity network switch
- Propose to study the feasibility of implementing a standard-compliant 100G Ethernet link for on-detector deployment
  - Buffering
  - Asynchronous to LHC collisions
- To be carried out in close collaboration with future Back-End and DAQ developers

Conclusions

- The vital importance of electronics to High Energy Physics is acknowledged at the highest levels:
  - Innovation in hardware and software will disrupt the way we build detectors
  - Complexity in technologies and tools will disrupt the way we work
- An R&D program must address the above two points, keeping in mind that:
  - No team can cover the full spectrum
  - Collaboration is key to survival
- R&D lines must build on:
  - Focused expertise
  - Above-critical-mass teams
  - Mid-term applications

- It is important to carefully guide the R&D program to maintain achievable goals
  - The national R&D programs support developments for the mid-term future
  - The ECFA R&D roadmap for detectors extends this support-promise to the long-term

- In electronics, the role of CERN EP-ESE is central to the community
- For complex projects, a new balance is being sought between CERN, central institutions and distributed resources: Hub model for ASIC developments

- Register to, and attend the upcoming DRD7 workshop on 25-26 Sep at CERN
  https://indico.cern.ch/event/1318635/