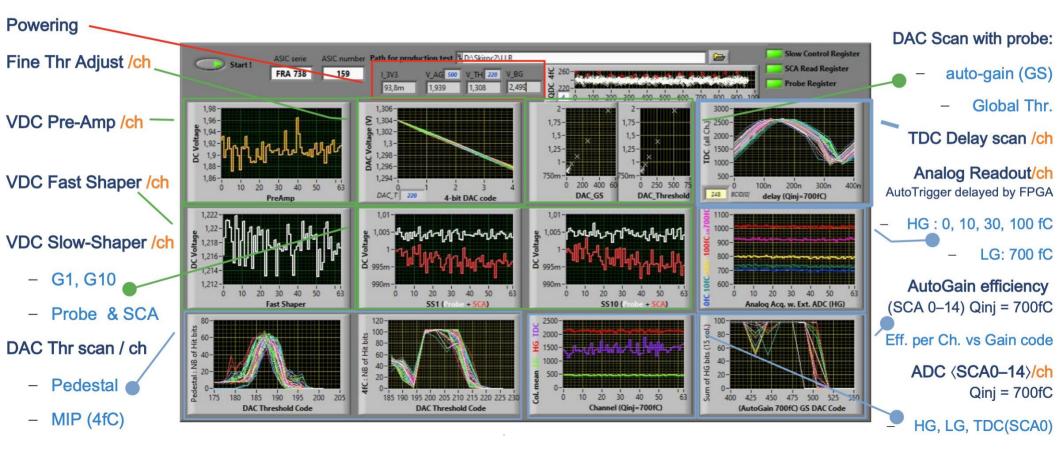
#### SK2A Test results analysis

# Yeqín CHeng Institut Polytechnique de Paris



#### Measurements

LabView testing SW : Digital & Analogue probing @ 9 mins per ASIC (optim) © S. Callier



#### Retrieved data file: Chip # FRA 738-159

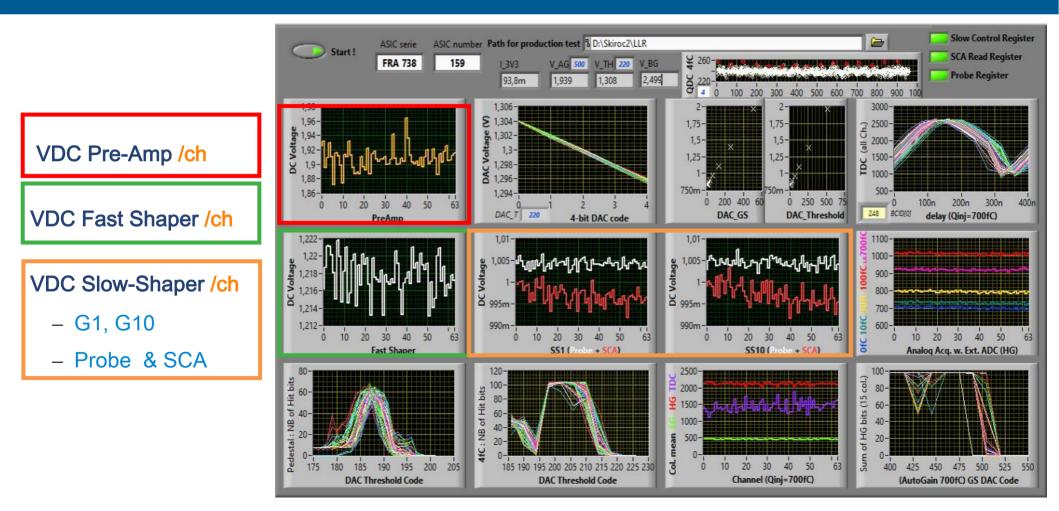
42

43

data > = Test SK2A BGA FRA 738-159.data Slow\_Control\_Register 5 0K SCA Read Register 0K 6 Probe Register 0K 7 9 I 3V3 V BG V TH V GS 10 0,0937976 2,4989200 1,3079803 1,9394339 11 12 VDC FS 13 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 14 1.2161662 1.2186568 1.2211954 1.2211390 1.2201431 1.2180445 1.2150118 1.2218660 1.2199741 1.2147174 1.2182692 1.2210182 15 VDC SS10 16 17 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 1,0028281 1,0049861 1,0061333 1,0052725 1,0049275 1,0038300 1,0038774 1,0053356 1,0045272 1,0041886 1,0052986 1,0039053 18 19 VDC SS1 20 21 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 22 1,0049201 1,0042521 1,0060671 1,0047835 1,0035045 1,0028111 1,0046542 1,0024921 1,0047438 1,0031069 1,0049574 1,0038115 23 VDC PA 24 25 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 26 1,9249406 1,9312833 1,8951288 1,9088952 1,9294705 1,9108778 1,8721739 1,9158122 1,9111444 1,8988010 1,8742716 1,9141055 27 28 VDC SCA10 29 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 30 0,9991411 1,0001048 0,9995381 0,9989773 0,9967898 1,0012201 0,9964449 1,0015977 1,0000934 0,9974055 1,0004141 1,0032151 31 32 VDC\_SCA1 33 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 34 0.9994429 0.9994854 0.9999536 1.0002390 0.9980254 0.9991362 0.9994906 0.9953494 0.9975675 0.9957655 1.0008029 0.9987904 35 36 DAC linearity V TH 37 0 1 2 4 8 16 32 64 128 256 512 38 0,8154298 0,8176452 0,8198520 0,8241404 0,8326749 0,8507235 0,8876501 0,9597801 1,1026122 1,3905303 1,9663821 39 40 DAC linearity V AG 41 0 1 2 4 8 16 32 64 128 256 512

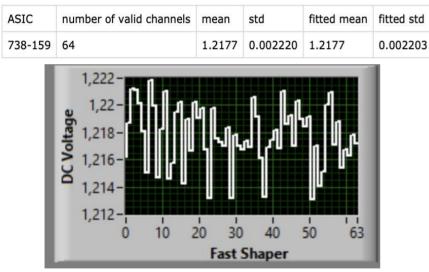
0,8276091 0,8297366 0,8318541 0,8365022 0,8451735 0,8619108 0,8989854 0,9687146 1,1116212 1,3978217 1,9652133

# **Channel Scans:**



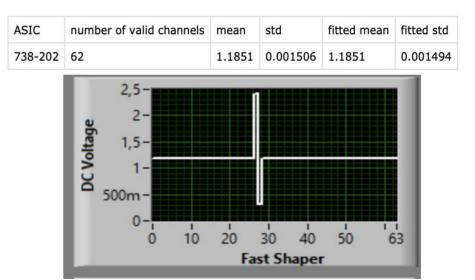
#### Channel Scans: Output csv files: stats and outliers

- single measurements from 64 channels
- Find mean and standard deviation
- · Fit to Gaussian by MLE method, extract fitted mean and std



Outliers (outside 3 std from the mean)

ASIC	channel	distance	ASIC	channel	distance
738-261	34	3.4829	2127-251	34	-3.4044



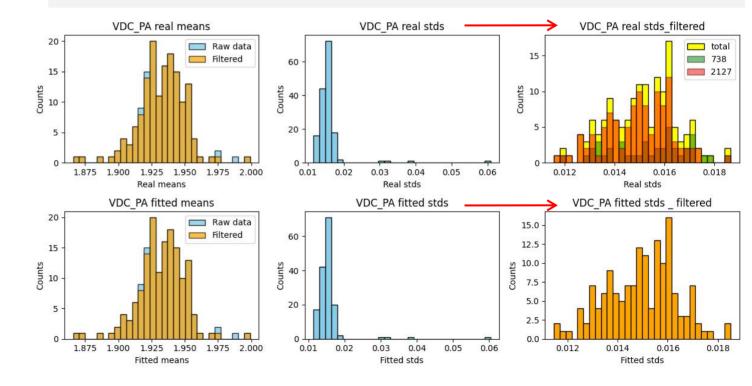
Distance = (value - mean)/std

# Channel Scans: Summary VDC\_PA

Filter by standard deviation

- Total no. of ASICs: 156
- valid ASICs: 152

ASICS of filtered std outliers: ASIC std 27 2127-209 0.039015 55 738-264 0.029789 61 2127-178 0.031462 2127-264 0.060818 143 total no. of ASICs: 156 number of excluded ASICs: 4 number of valid ASICs: 152



# Channel Scans: Summary VDC\_SS1

Filter by standard deviation

ASIC

738-167

2127-415

2127-390

.

20

87

114

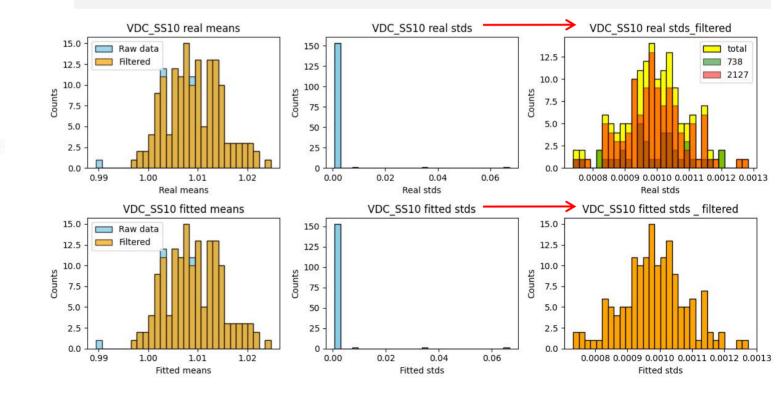
150

std range = {'VDC FS': [0,0.003], 'VDC SS10': [0,0.002], 'VDC SS1': [0,0.02], 'VDC PA': [0, 0,02]. 'VDC SCA10': [0,0,004]. 'VDC SCA1': [0.math.inf]}

VDC SS1 real means VDC SS1 real stds VDC SS1 real stds filtered 150 Raw data total 15 Total no. of ASICs: 155 20 Filtered 738 125 2127 15 Counts 10 100 valid ASICs: 151 Counts 10 Counts 75 ASICS of filtered std outliers: 50 5 std 5 25 0.095356 0 0 0.093840 0.97 0.98 0.99 1.00 1.01 1.02 0.00 0.02 0.04 0.06 0.08 0.10 0.12 0.0008 0.0009 0.0010 0.0011 0.0012 0.0013 0.118829 Real means Real stds Real stds 2127-391 0.065169 VDC SS1 fitted means VDC SS1 fitted stds VDC SS1 fitted stds \_ filtered total no. of ASICs: 155 150 . Raw data number of excluded ASICs: 4 15 20 Filtered 125 number of valid ASICs: 151 15 Counts 10 100 Counts 10 Counts 75 50 5 5 25 0 0 0.99 1.00 1.01 0.02 0.04 0.06 0.08 0.10 0.0008 0.0009 0.0010 0.0011 0.0012 0.0013 0.97 0.98 1.02 0.00 0.12 Fitted stds Fitted means Fitted stds

# Channel Scans: Summary VDC\_SS10

Filter by standard deviation



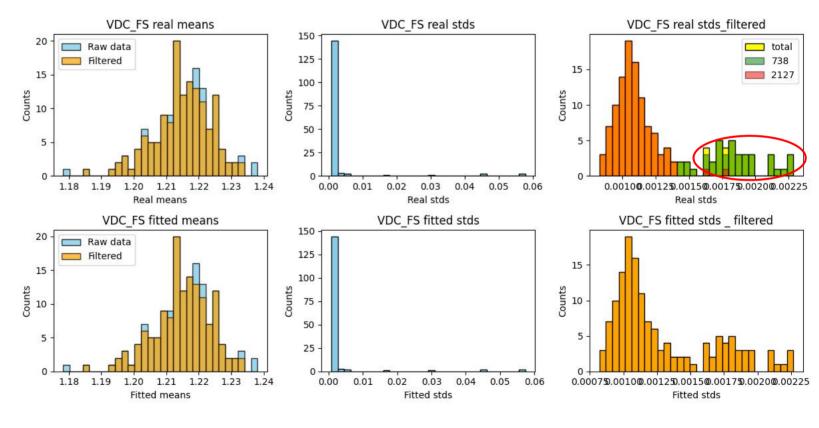
• Total no. of ASICs: 156

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# Channel Scans: dependence on packaging VDC\_FS

- Particular VDC\_FS
- 39 ASICs "outside" the Gaussian in filtered std
- Different packaging
- Total no. of ASICs: 155
- valid ASICs: 144

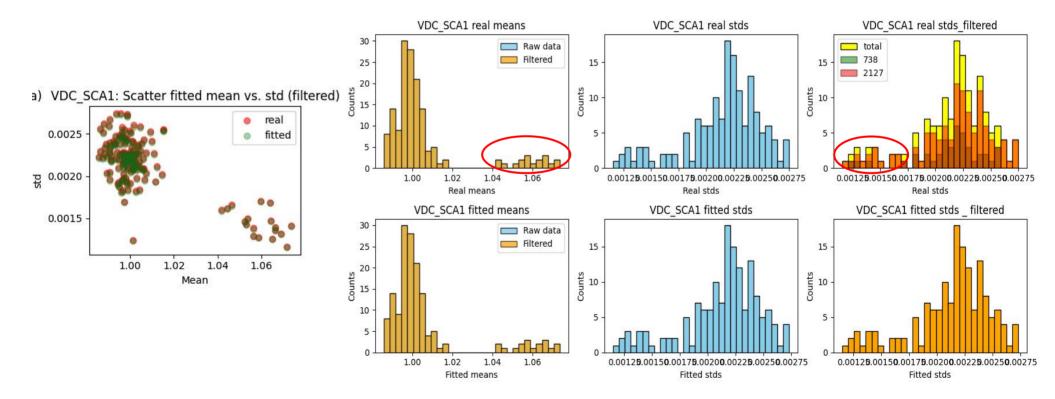
ASICS of filtered std outliers: ASIC std 2127-254\_chn62off 0.003949 34 37 2127-264\_chn41off 0.045919 43 2127-282 0.005098 63 738-264 0.016618 70 2127-129 0.057840 2127-254 0.003949 80 85 2127-177 0.004103 94 2127-264 0.046293 2127-129\_chn6off 0.057476 103 117 2127-262 0.030707 149 2127-256 0.006103 total no. of ASICs: 155 number of excluded ASICs: 11 number of valid ASICs: 144



# Channel Scans: 2 groups of mean data SCA1

- Notch of data that is "outside" Gaussian in mean and filtered std as in red circle
- Scatter plots show correlation between mean and std.

• valid ASICs: 155

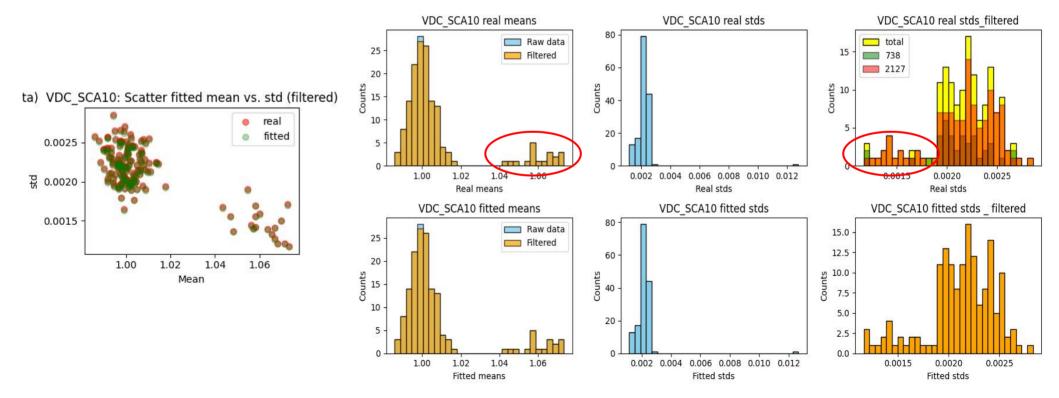


<sup>•</sup> Total no. of ASICs: 155

# Channel Scans: 2 groups of mean data SCA10

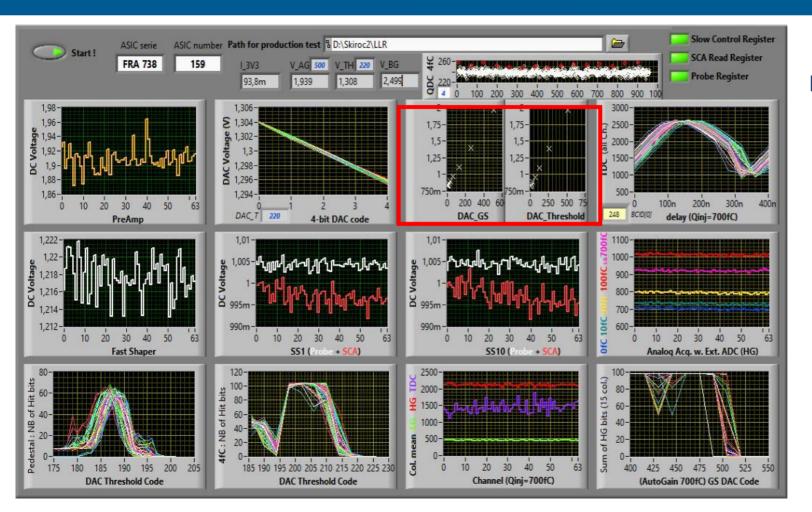
- Notch of data that is "outside" Gaussian in mean and filtered std as in red circle
- Scatter plots show correlation between mean and std.

• valid ASICs: 155



<sup>•</sup> Total no. of ASICs: 156

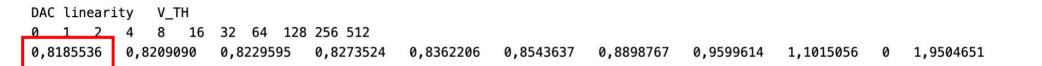
## Parameter Scans:



#### DAC Scan with probe:

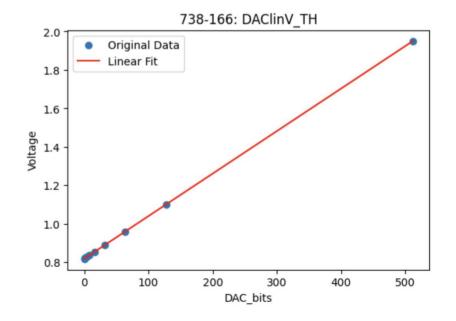
- auto-gain (GS)
- Global Thr.

#### Parameter scan: retrieved data file



- Linear fit with y-intercept = voltage value at DAC = 0
- excluding zeros (if V0 = 0, extrapolate)
- Extract slope

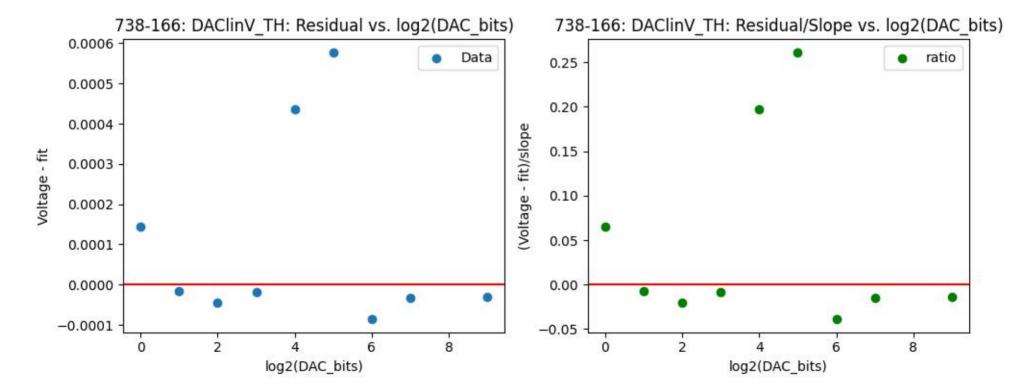
```
738-166: DAClinV_TH
Equation of the linear fit:
Voltage = 0.0022108238079647283 * DAC + 0.8185536
```



#### Parameter scan: Analysis of a single chip

- Plot residual vs. log2 of DAC
- residual = data fit

- Ratio = residual/slope: how well the fit is
- slope = smallest step of voltage when changing DAC value



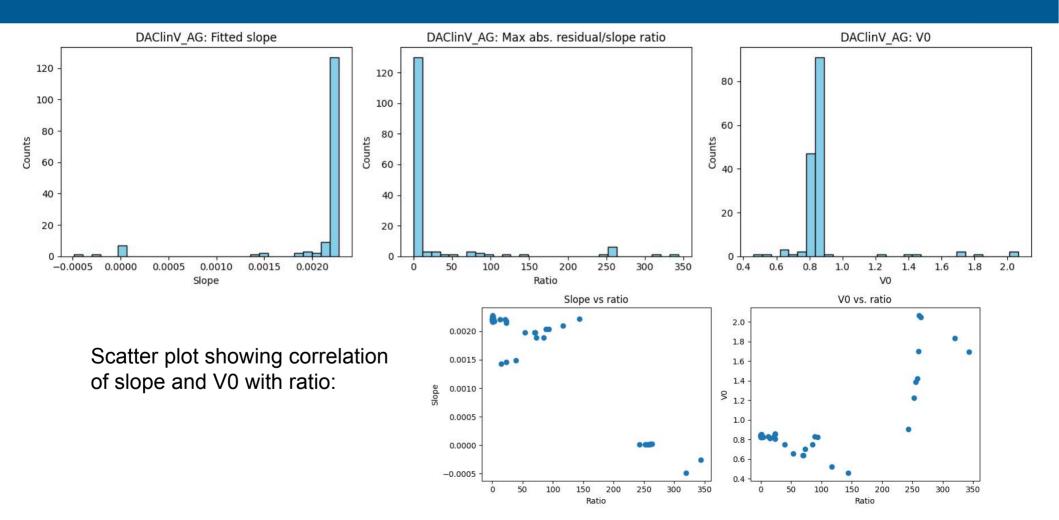
#### Parameter scan: output file

ASIC	V0 != 0	Fitted slope	Max abs. residual/slope ratio	V0(intercept)
738-159	TRUE	0.002247538	0.327114922	0.8154298

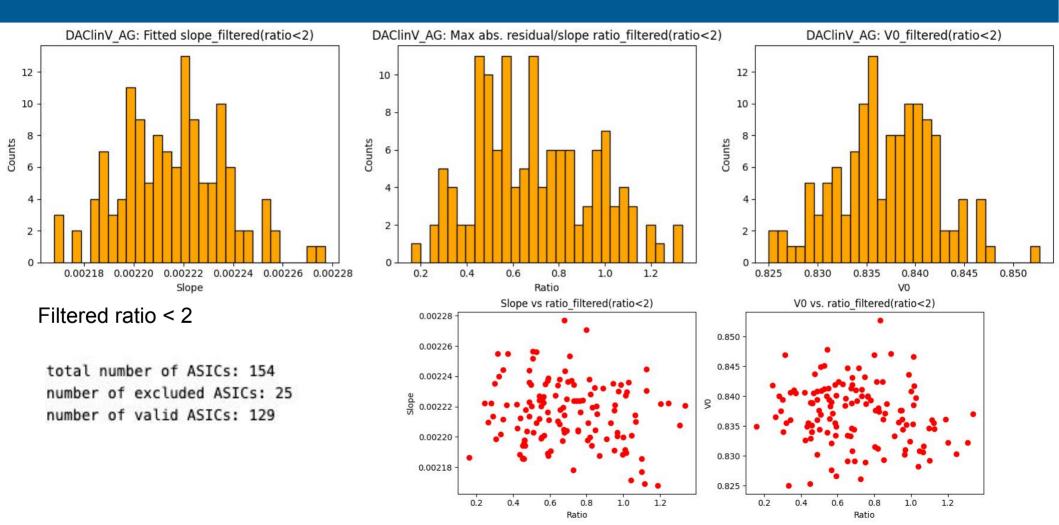
• Steps of voltage to reconstruct scan

Step: V1-V0	Step: V2-V0	Step: V3-V0	Step: V4-V0	Step: V5-V0
0.0022154	0.0044222	0.0087106	0.0172451	0.0352937
Step: V6-V0	Step: V7-V0	Step: V8-V0	Step: V9-V0	Step: V10-V0
0.0722203	0.1443503	0.2871824	0.5751005	1.1509523

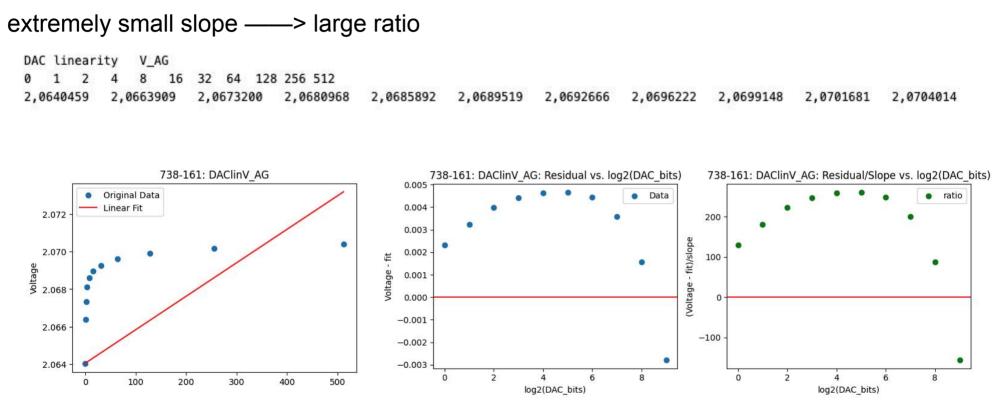
# Parameter scan: Summary analysis of DAClinV\_AG



### Parameter scan: Summary analysis of DAClinV\_AG

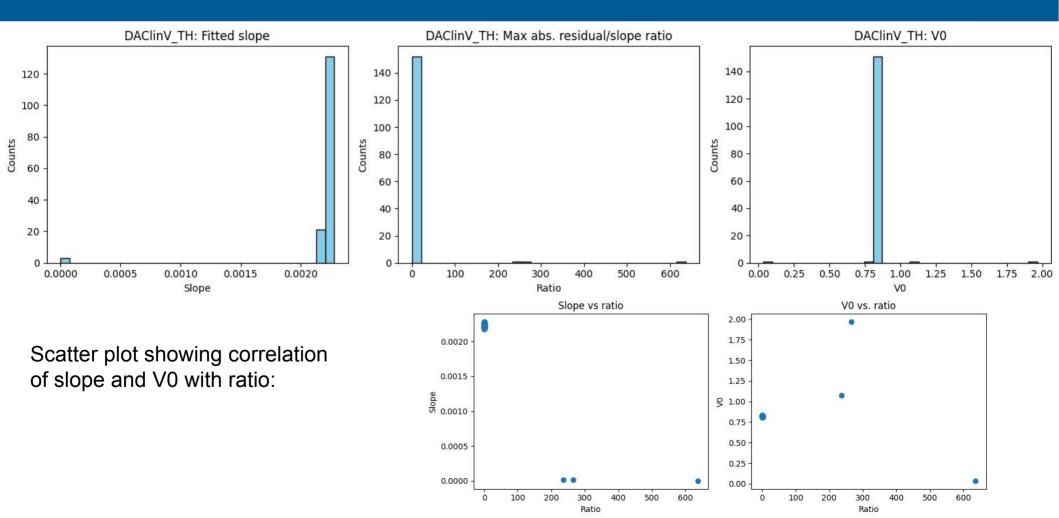


#### Parameter scan: Problem shoot (738-161: DAClinV\_AG)

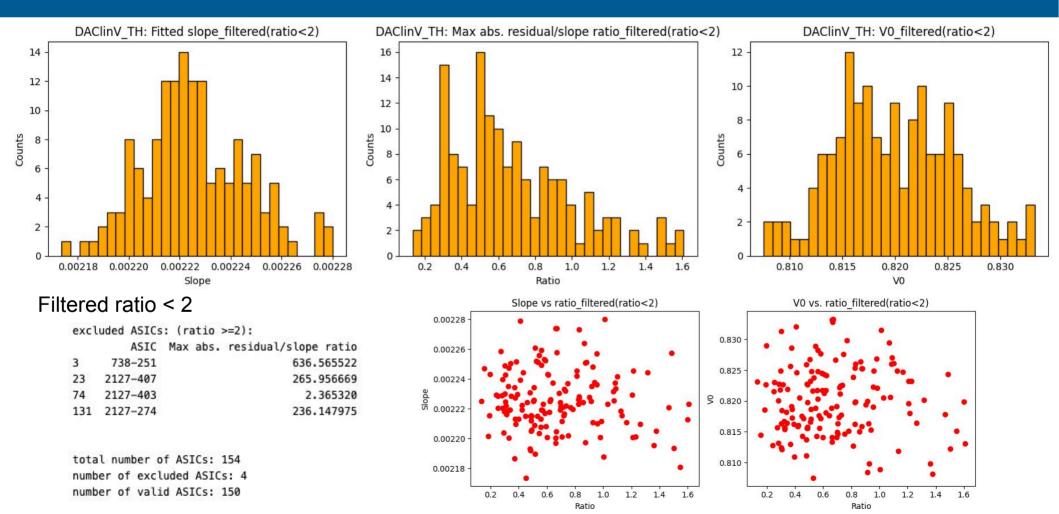


738-161: DAClinV\_AG Equation of the linear fit: Voltage = 1.7842507510690275e-05 \* DAC + 2.0640459

# Parameter scan: Summary analysis of DAClinV\_TH



# Parameter scan: Summary analysis of DAClinV\_TH



# **Conclusion:**

- Data analysized from 158 chips
- Channel Scans (single measurement by external device from 64 channels)
  - Non Gaussian distribution of std in VDC\_FS,
    - Fast shaper -----> packaging 738 twice the std of 2127
  - VDC\_SC1 and VDC\_SC10: two groups of mean and std -----> correlations
- Parameter scan
  - Auto-gain: measurements completely off (values almost the same)