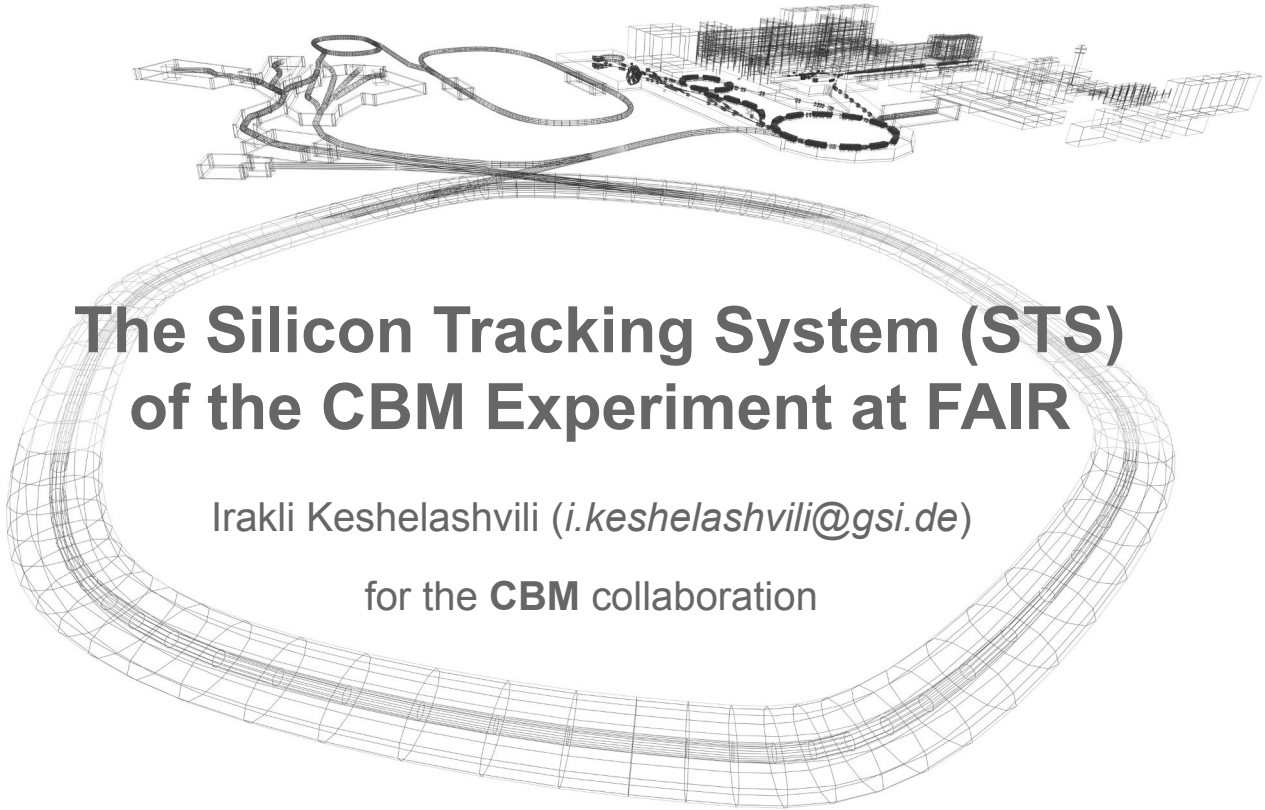
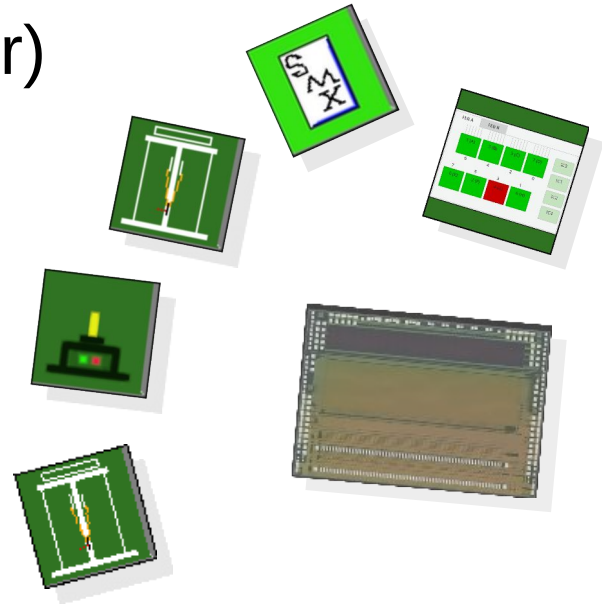


The Silicon Tracking System (STS) of the CBM Experiment at FAIR

Irakli Keshelashvili (*i.keshelashvili@gsi.de*)

for the **CBM** collaboration

- **Introduction**
  - **FAIR** (**F**acility for **A**ntiproton and **I**on **R**esearch)
  - **CBM** (**C**ompressed **B**aryonic **M**atter)
  - **STS** (**S**ilicon **T**racking **S**ystem)
- **Q&A Test and Assembly Setup**
- **Summary**



Introduction

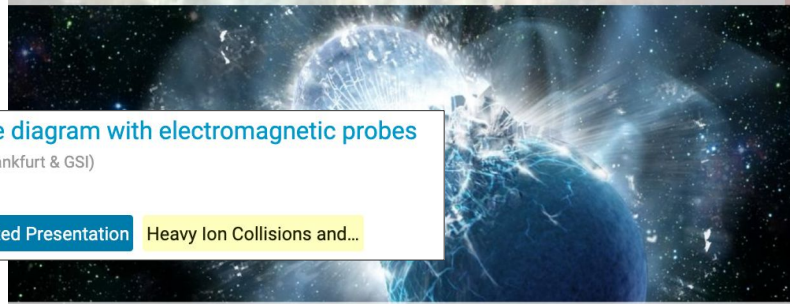
347. The FAIR/GSI facility - Status and future perspectives
Prof. Thomas Nilsson (GSI/FAIR)
26/09/2025, 09:00
Hadron Structure, Spectr... | Invited Presentation | Plenary Session

334. High Precision Measurements with Stored Highly Charged Radioactive Ions
Yury Litvinov (GSI Darmstadt)
22/09/2025, 11:00
Nuclear Structure, Spect... | Invited Presentation | Plenary Session

288. Exploring the phase diagram with electromagnetic probes
Alberica Toia (Goethe Uni. Frankfurt & GSI)
23/09/2025, 14:50
Heavy Ion Collisions and... | Invited Presentation | Heavy Ion Collisions and...

Synthesis of chemical elements in the cosmos

Building blocks of life: Production of carbon and oxygen in stars



Neutron star mergers: equation of state, strong force, neutron rich nuclei

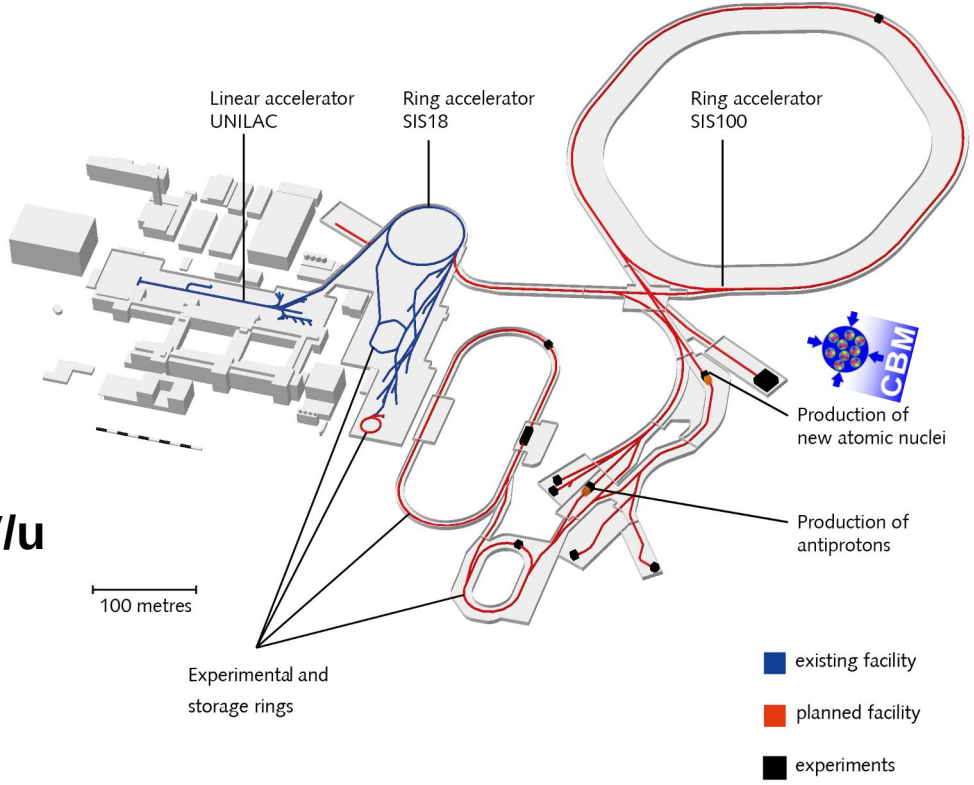
Matter in the interior of Earth and of large planets

Facility for **A**ntiproton and **I**on **R**esearch

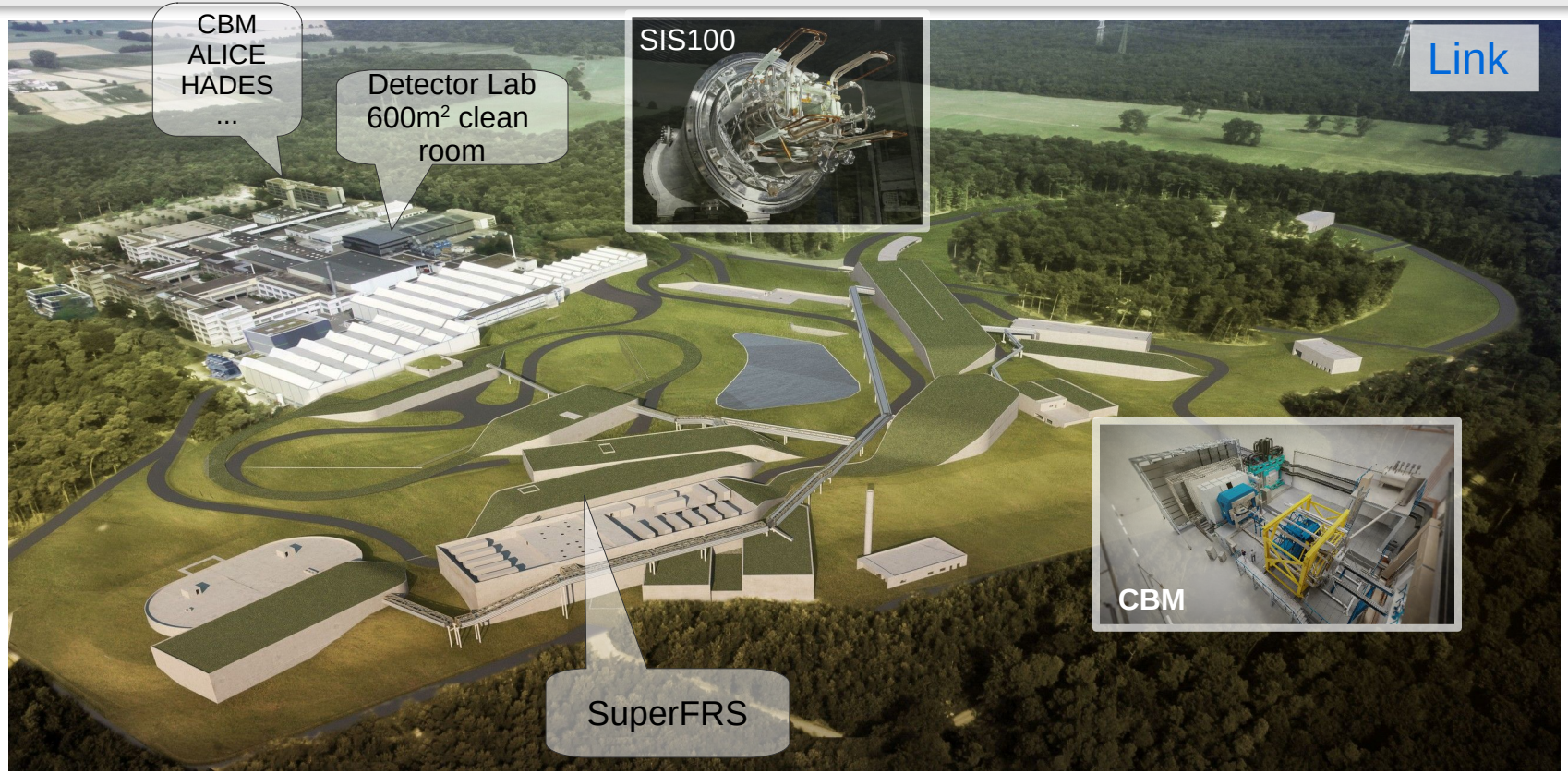
SIS100

- Circumference **1100m**
- Underground 17m
- Superconducting to -269°C
- Superconducting superferric **1.9 T**
- Fast-ramped up to 4 T/s
- 4×10^{13} protons at **29 GeV**
- 5×10^{11} Uranium (28+) ions at **2.7 GeV/u**

- Investments 3.3 billion euros.
- 3000 researchers from 50 countries



Facility for **A**ntiproton and **I**on **R**esearch



CBM (**C**ompressed **B**aryonic **M**atter)

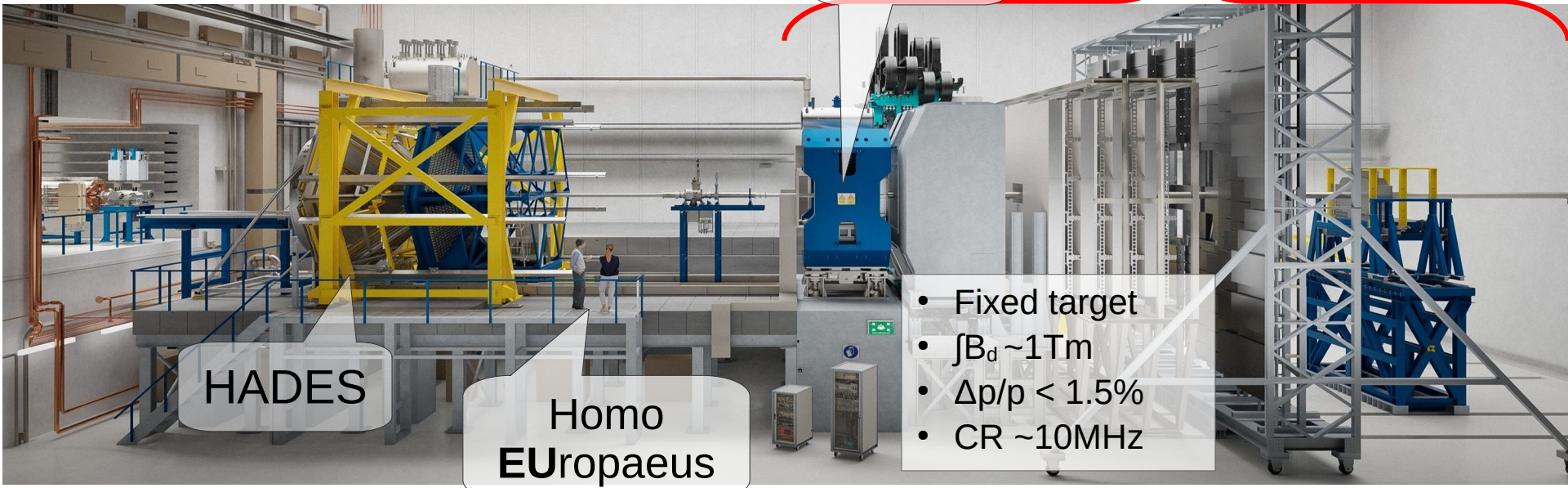
260. New timing Multi-Strip Multi-Gap Resistive Plate Chamber architecture with aging suppression for high counting rate experiments

Mariana Petris (Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH))

22/09/2025, 18:40

Accelerators and Instru... | Oral Presentation | Accelerators and Instru...

Silicon
Tracking
System



HADES

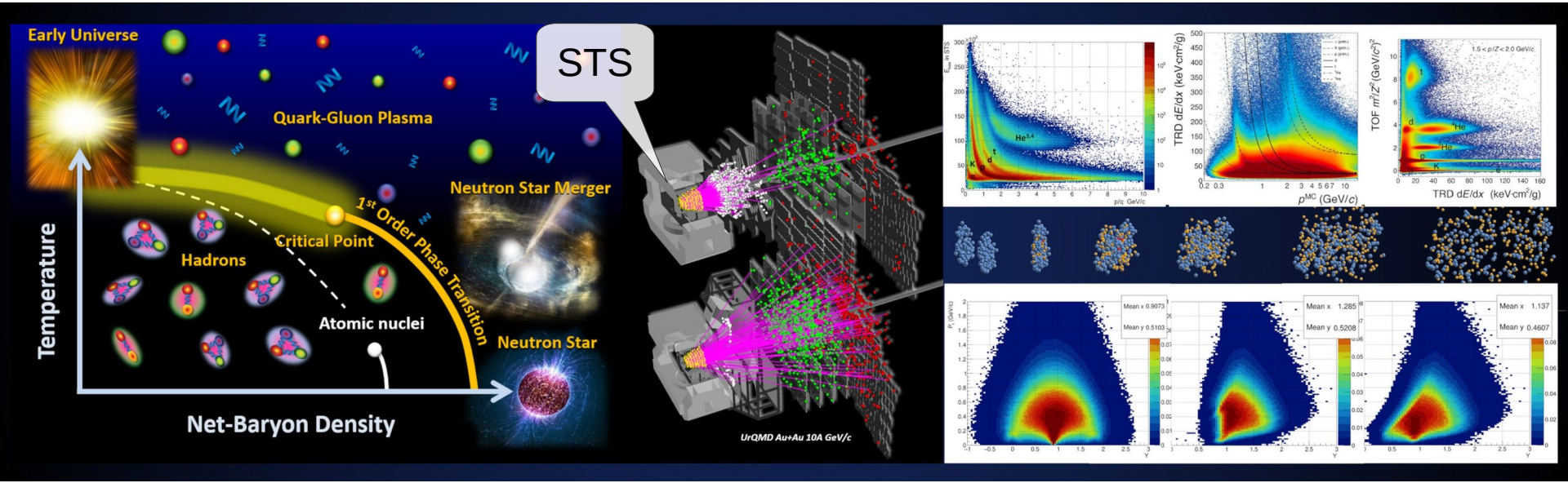
Homo
EUropaeus

- Fixed target
- $\int B_d$ ~1Tm
- $\Delta p/p < 1.5\%$
- CR ~10MHz

CBM (**C**ompressed **B**aryonic **M**atter)

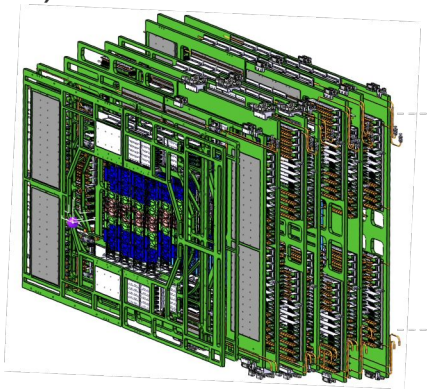
288. Exploring the phase diagram with electromagnetic probes
Alberica Toia (Goethe Uni. Frankfurt & GSI)
23/09/2025, 14:50
Heavy Ion Collisions and... | Invited Presentation | Heavy Ion Collisions and...

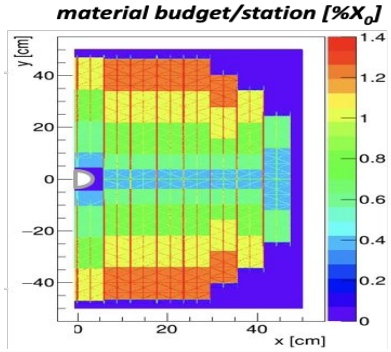
Au+Au 2-11 AGeV,
CBM aims at multi-ρ_0 matter **(~3–6 ρ_0)** in the hottest, densest stage of the collision



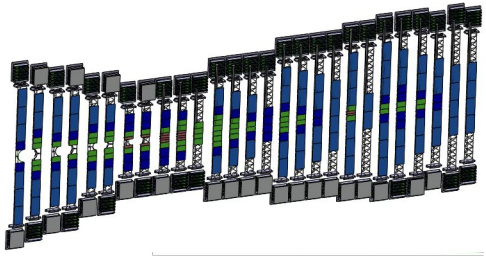
STS (**S**ilicon **T**racking **S**ystem)

- In Total **1.8 Million** channels
- **Assembled to guarantee < 1.5% Δp/p**
- **876** *(910)* silicon strip detector modules
- **106 Ladder** with up to 10 modules
- 2x(3+5) separate C-Frames / Stations
- 4 different sensor sizes (22; 42; 62; 124 x 62 mm)
- **2x1024 strips** per side; **58 um strip pitch**;
- Double-metallization on p side
- Electronics outside acceptance



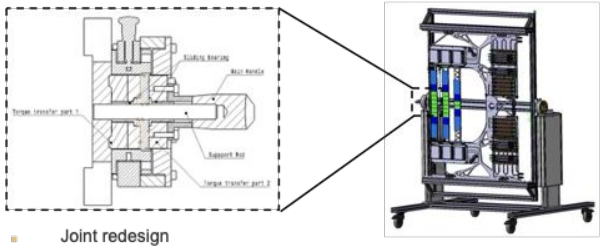


STS (Silicon Tracking System)

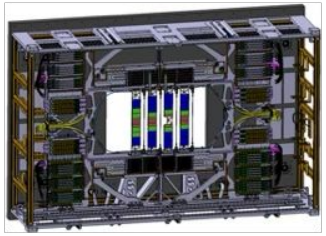


27 ladder variants

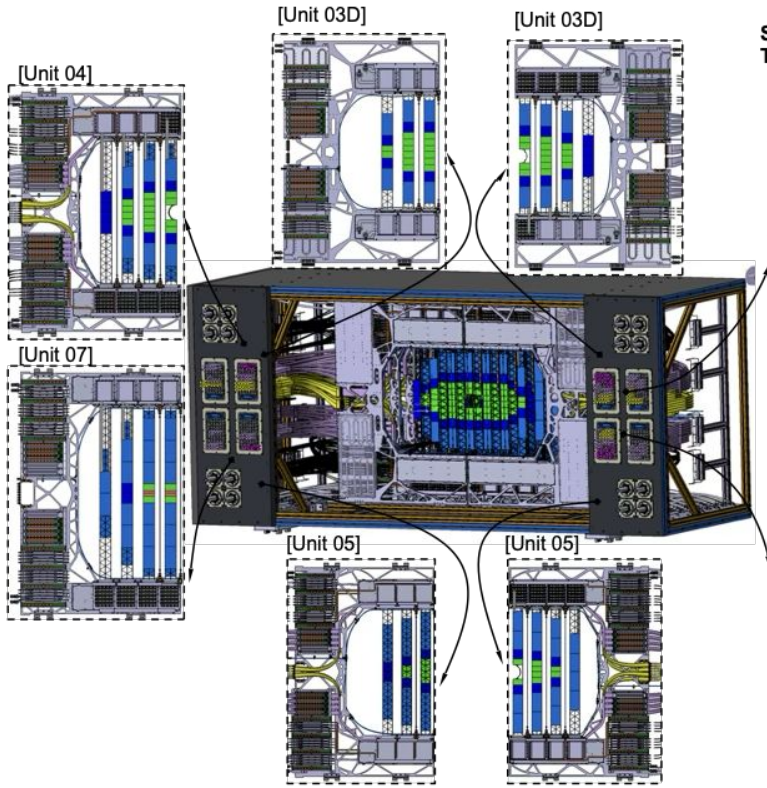
Central ladders with cut-out for beam pipe



- Joint redesign
- Increased stiffness and fixation point amount
- 3D Printed prototype
- Production soon



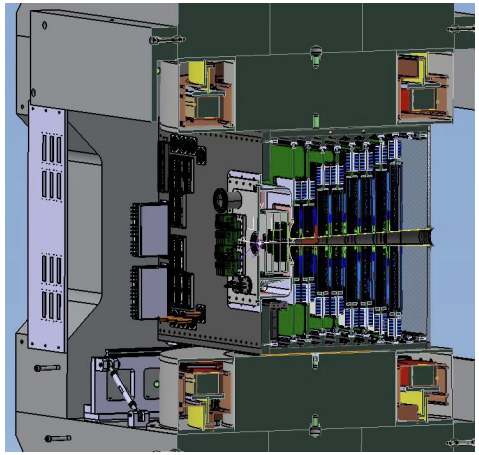
STS U
Topology optimization

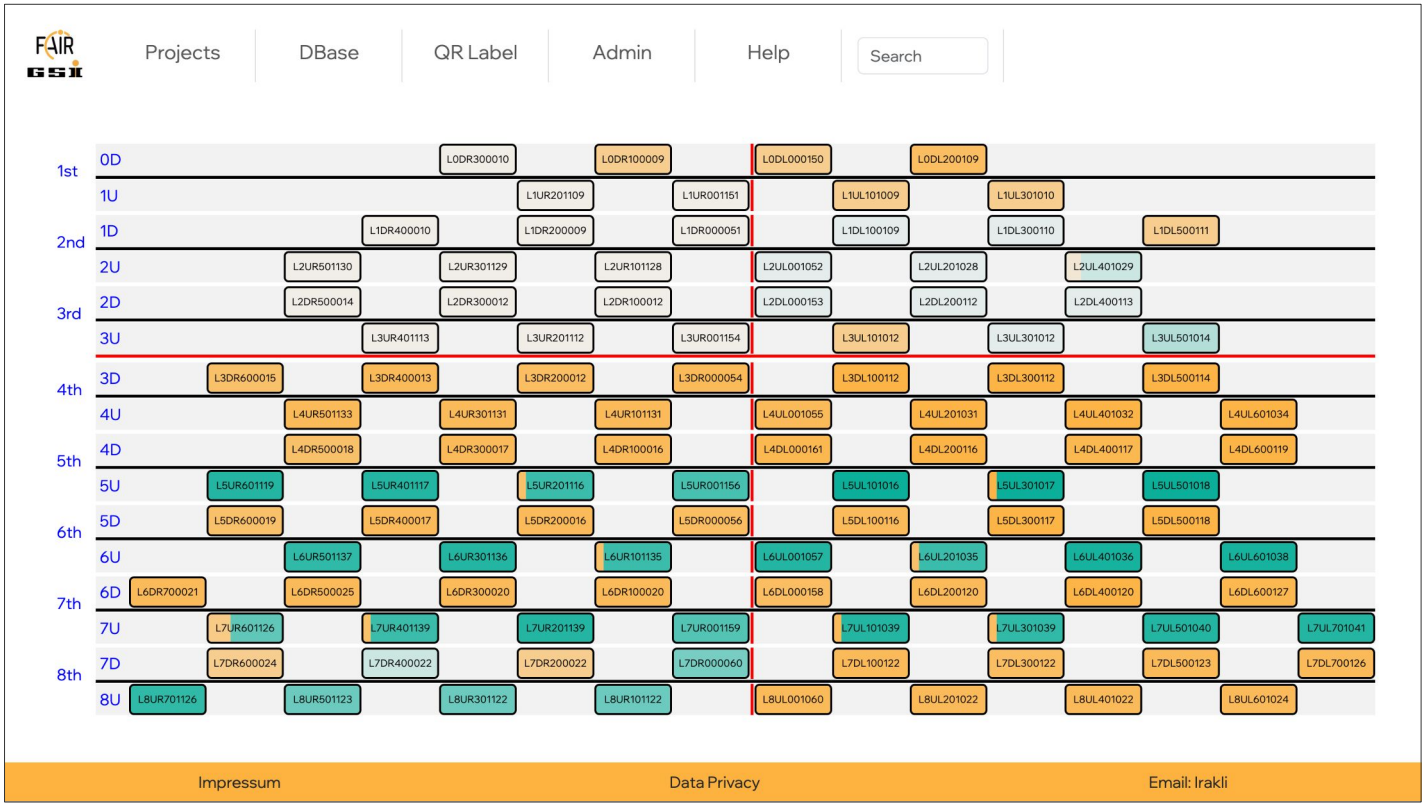


STS D
Topology optimization

Ladders Top View

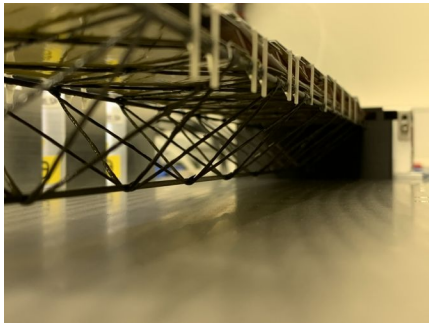
- **106** Ladder
- 2x(**3+5**) separate C-Frames / Stations

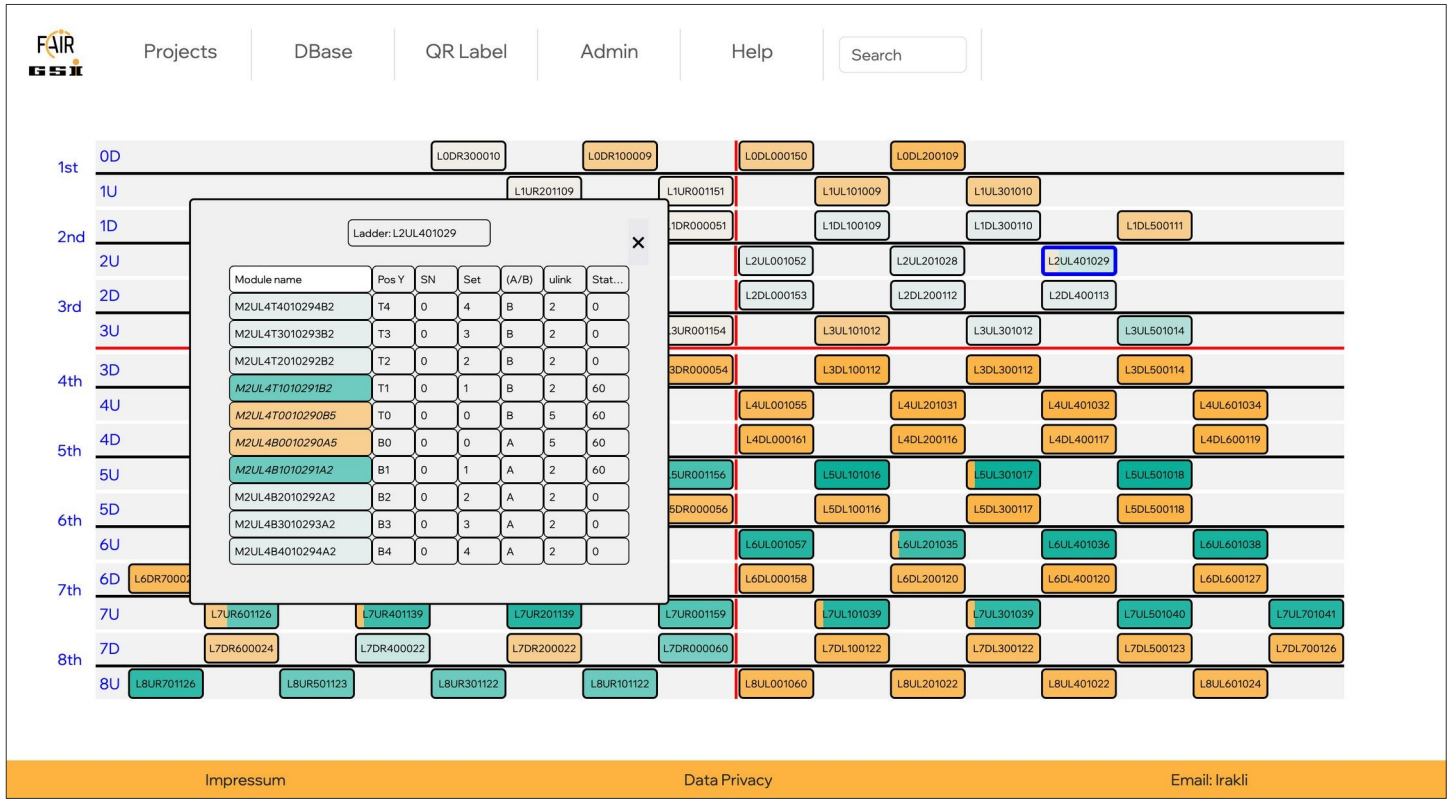




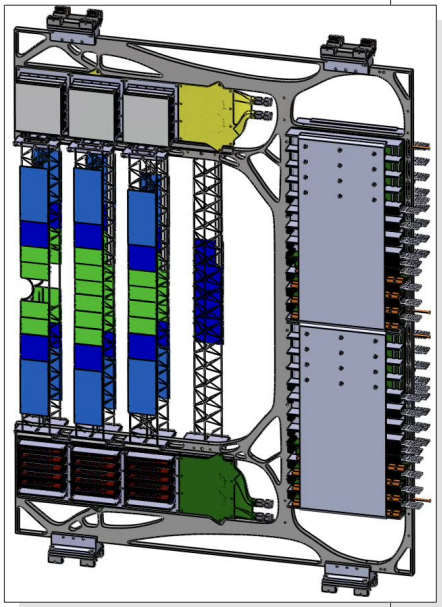
Ladders Progress Overview

Ladder 8 to 10 modules

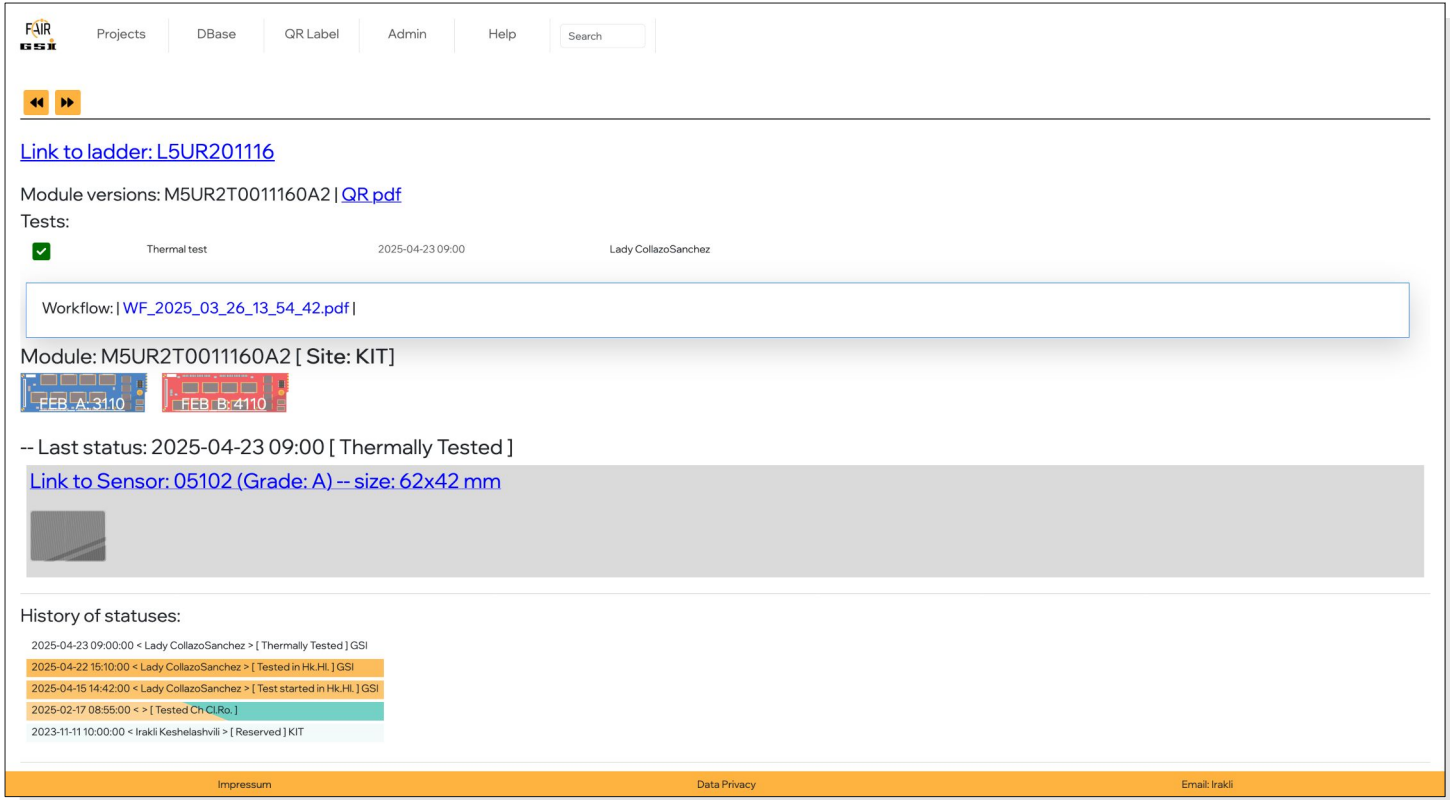




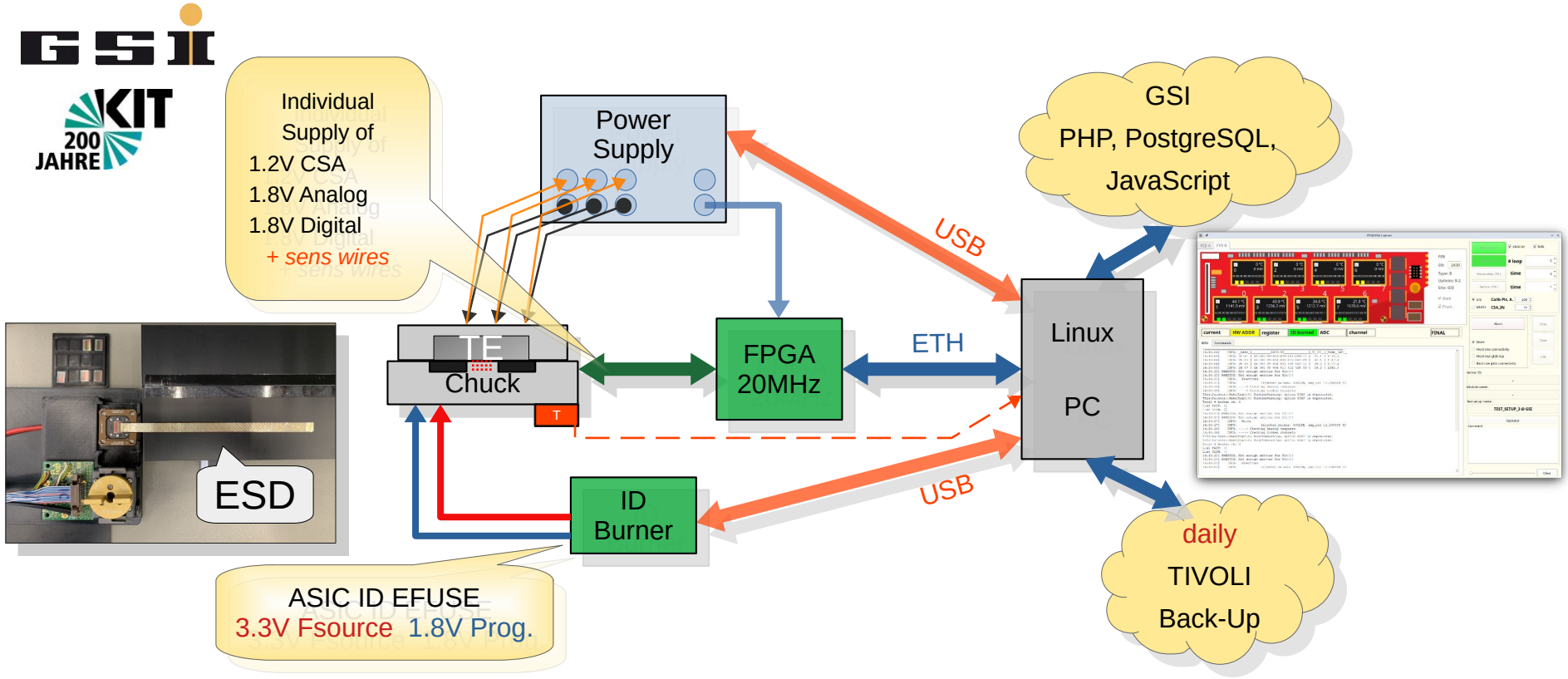
C-Frame Monitoring Web Page



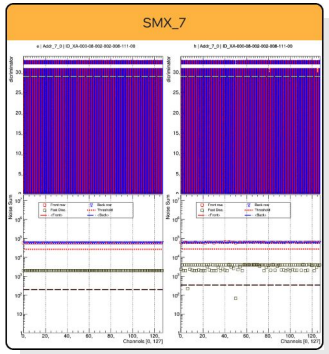
Module Test Web Page

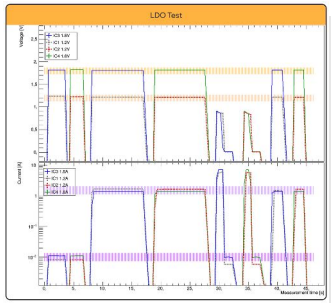


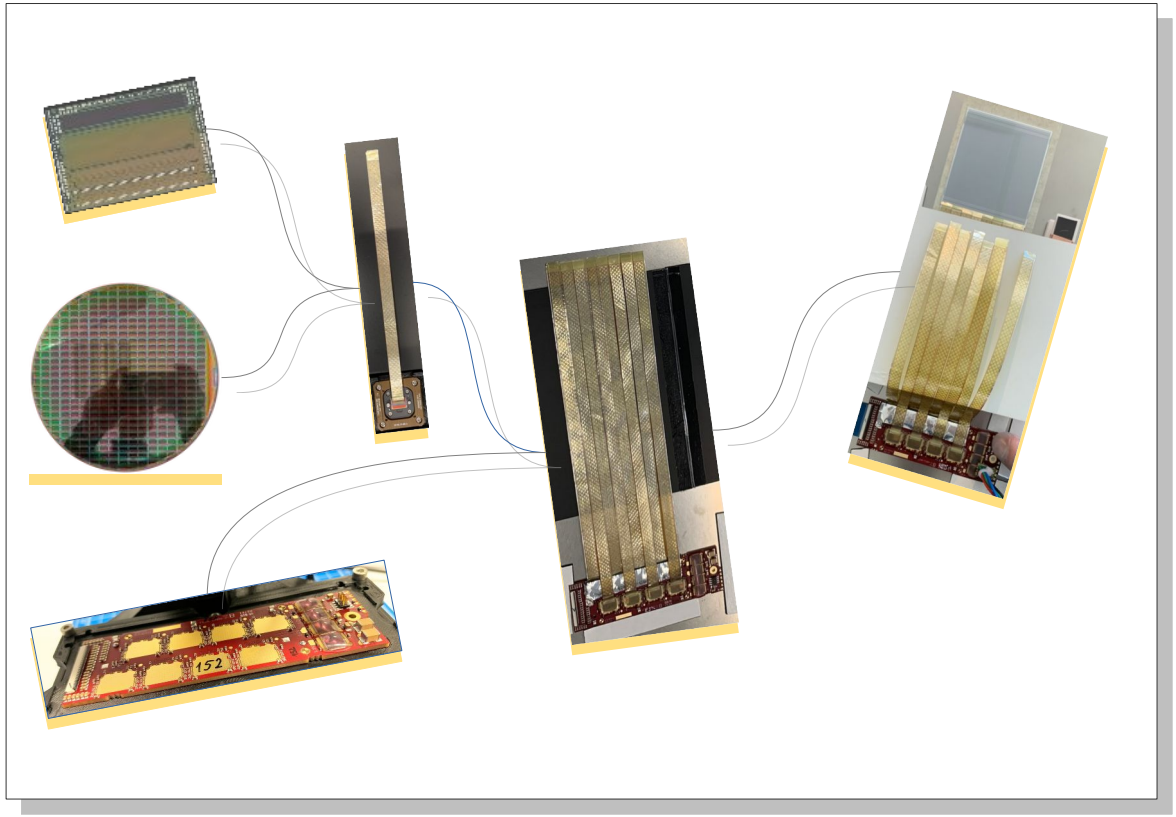
How Test Setup Is Working?

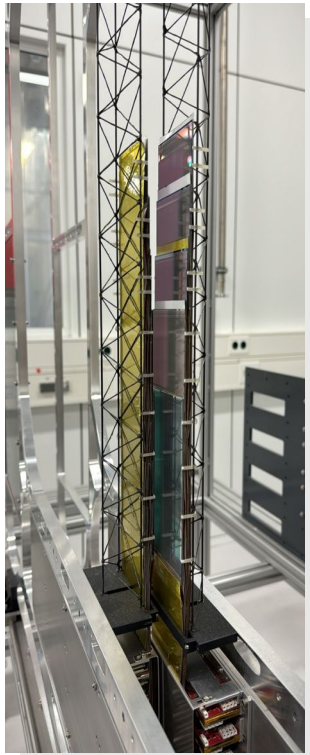


Module Assembly Procedere









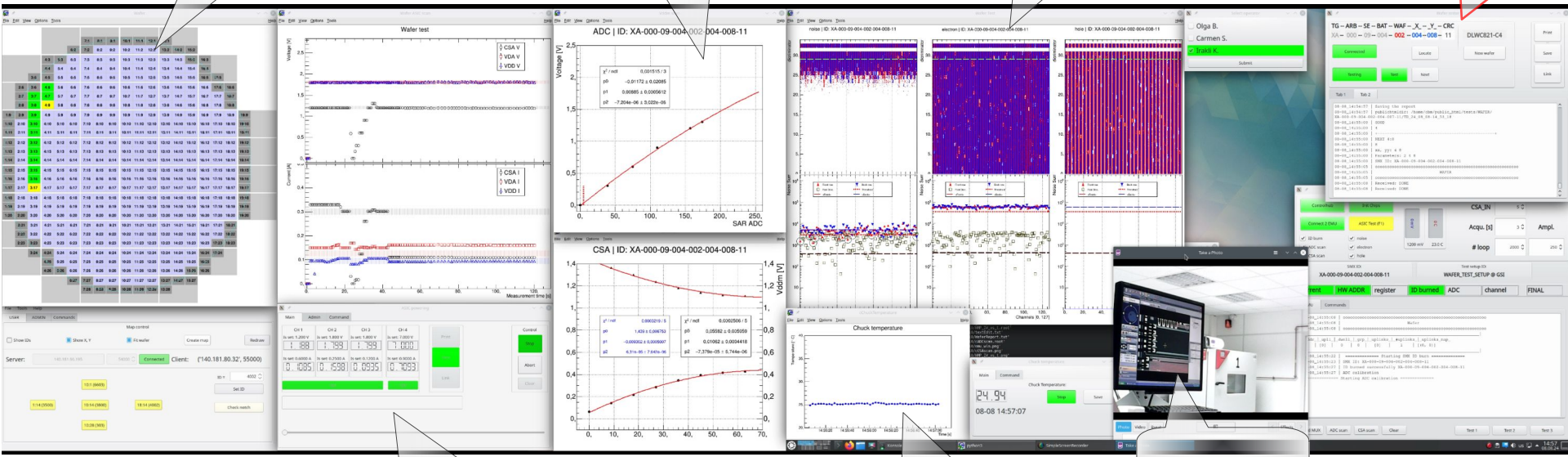
Test Software (5 x module/server)

WAFER
Prober server

ADC calib.
CSA calib.

Channel test
Noise, Neg., Pos.,

MAIN
server



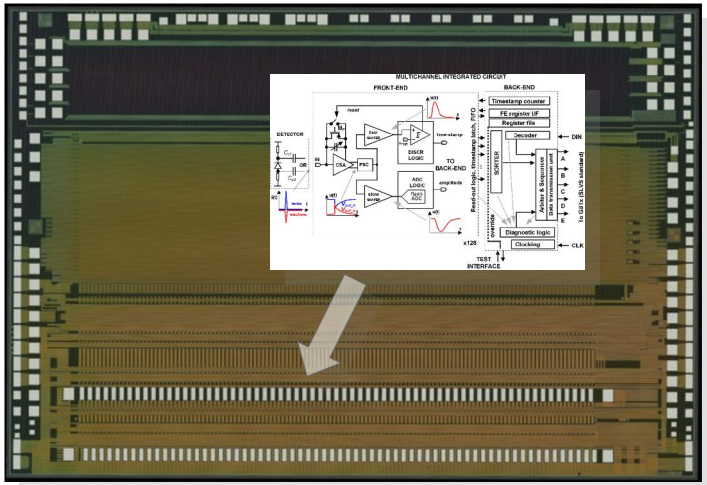
Power supply
server

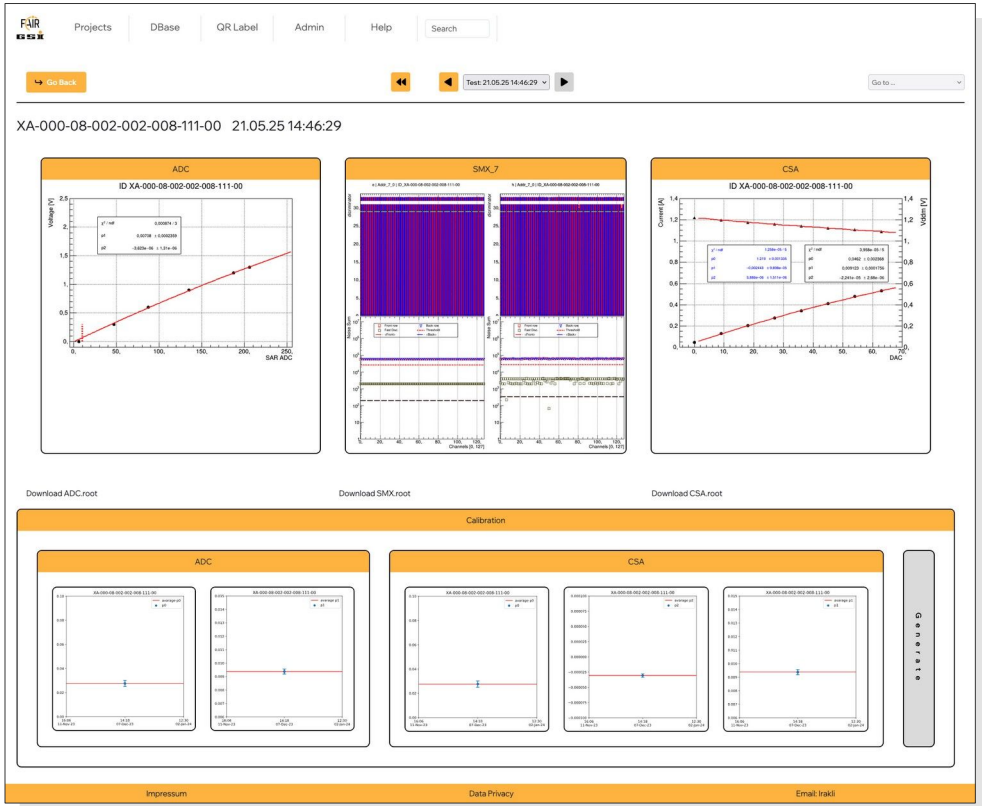
WAFER/Chuck
Temperature

Test card

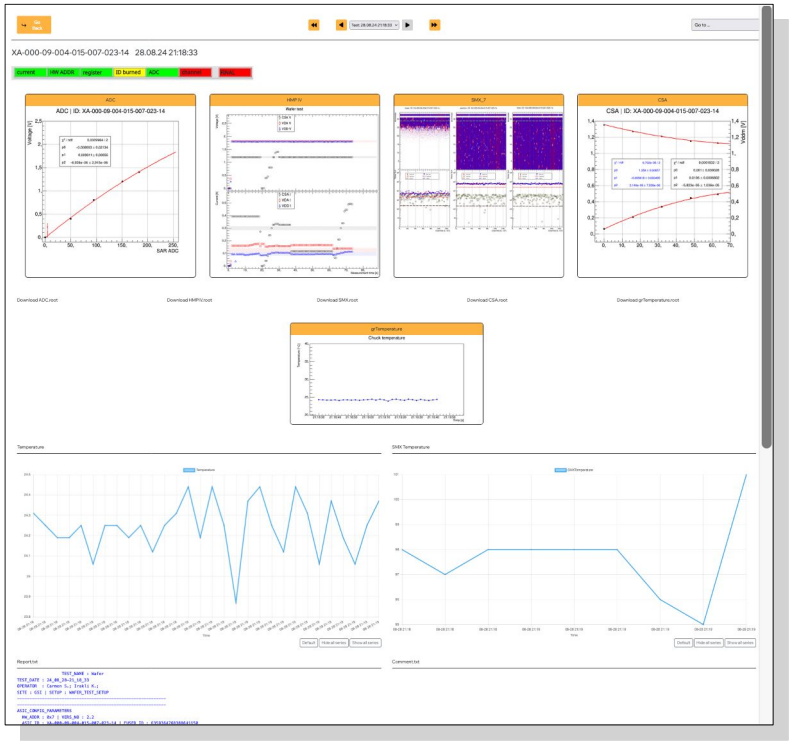
Test of XYTER 2.2 Readout ASIC

- **128** analog readout channels
- 5x**320 Mbit/s** data transfer
- Analog+Digital circuit
- STS and MUCH
- 5 bit Amp, 14 bit Time res.

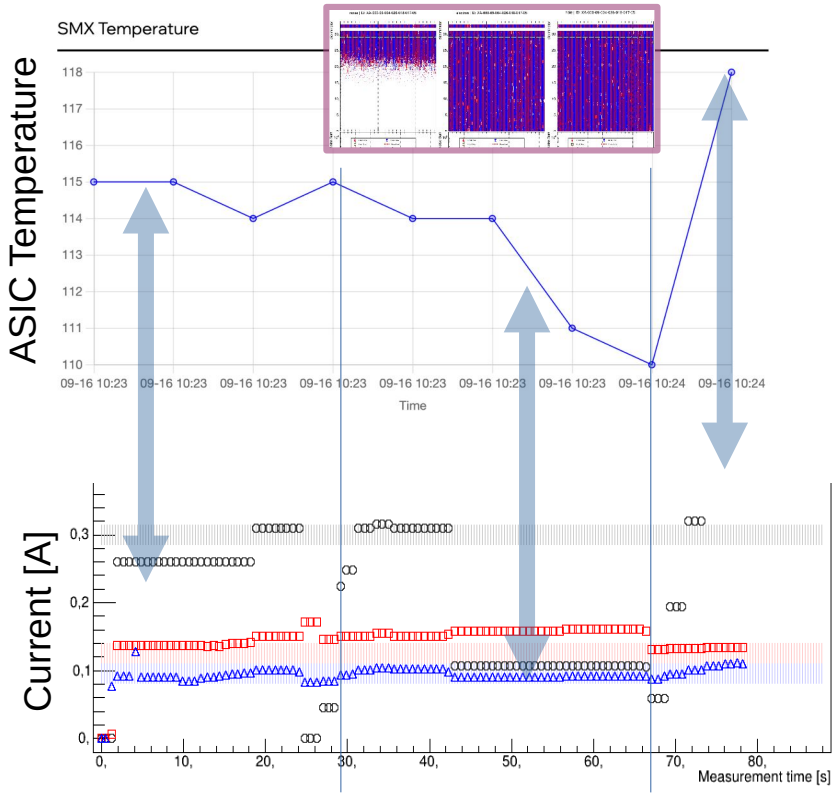


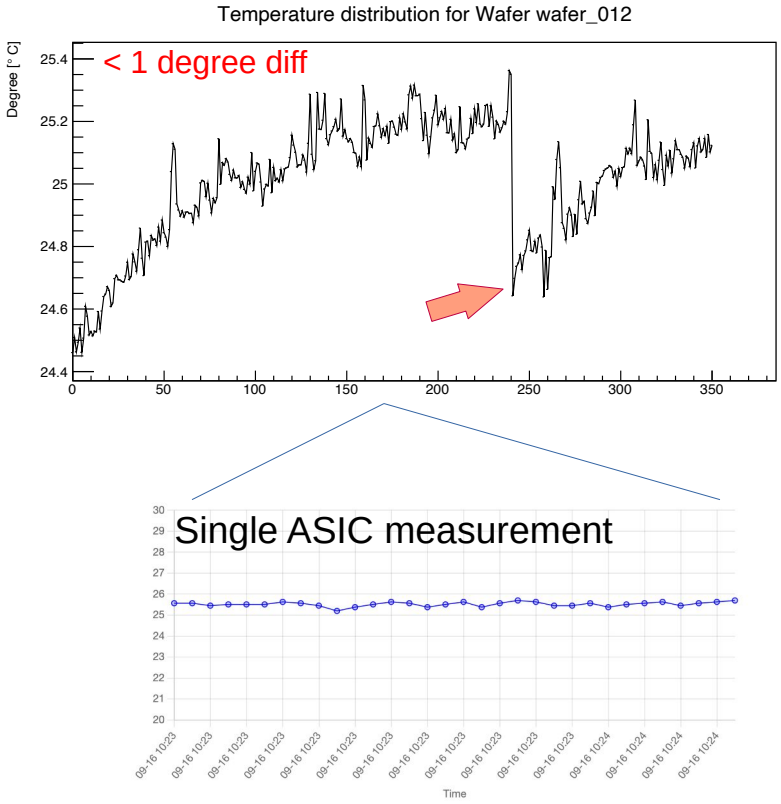


Wafer ASIC / Microcable Test Page

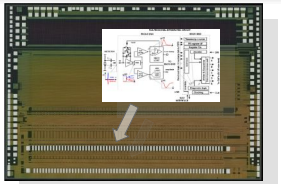


Chuck / Wafer / ASIC Temperature

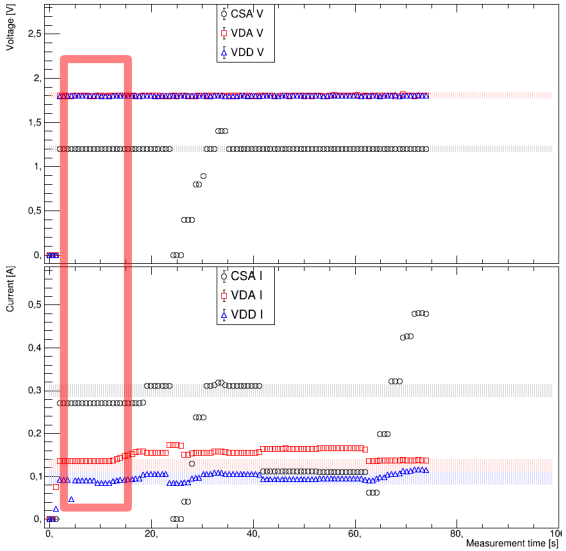


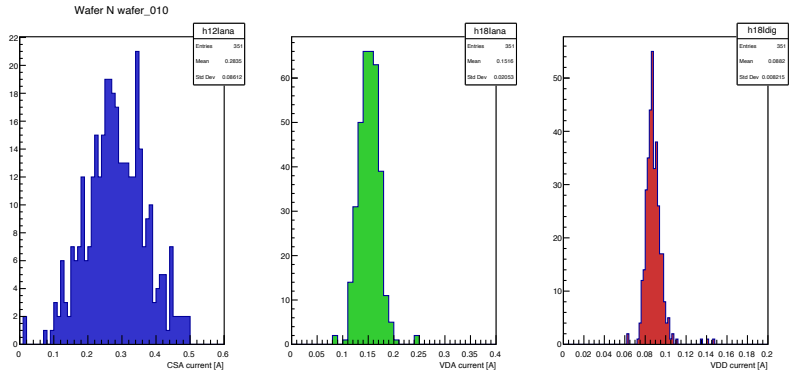


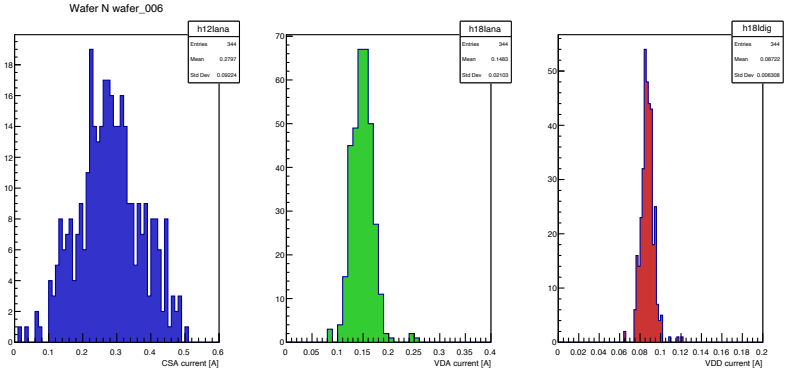
Current consumption before Init



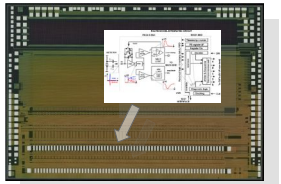
Wafer test



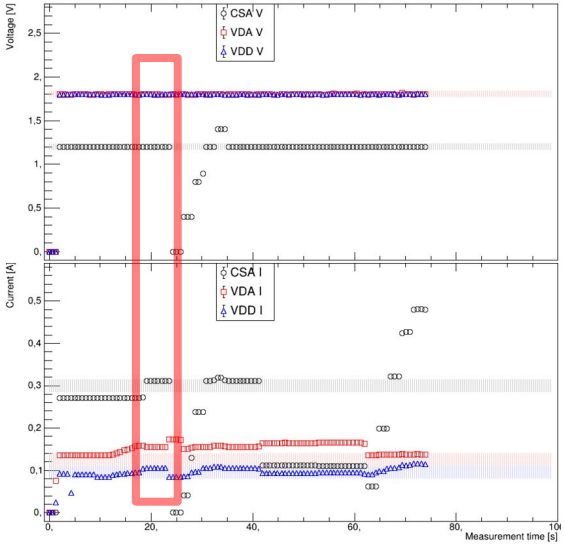


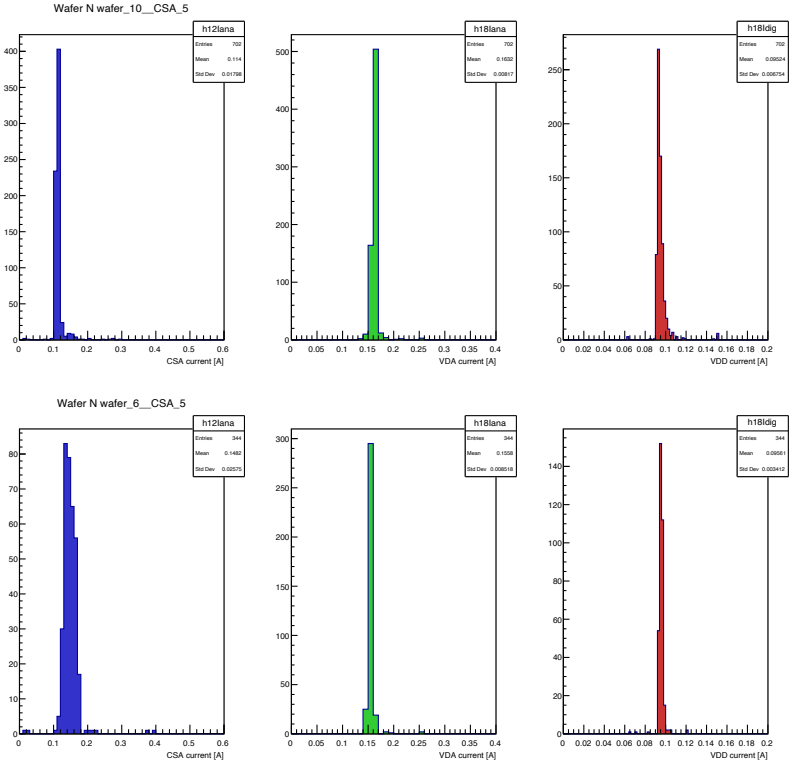


Current consumption after Init

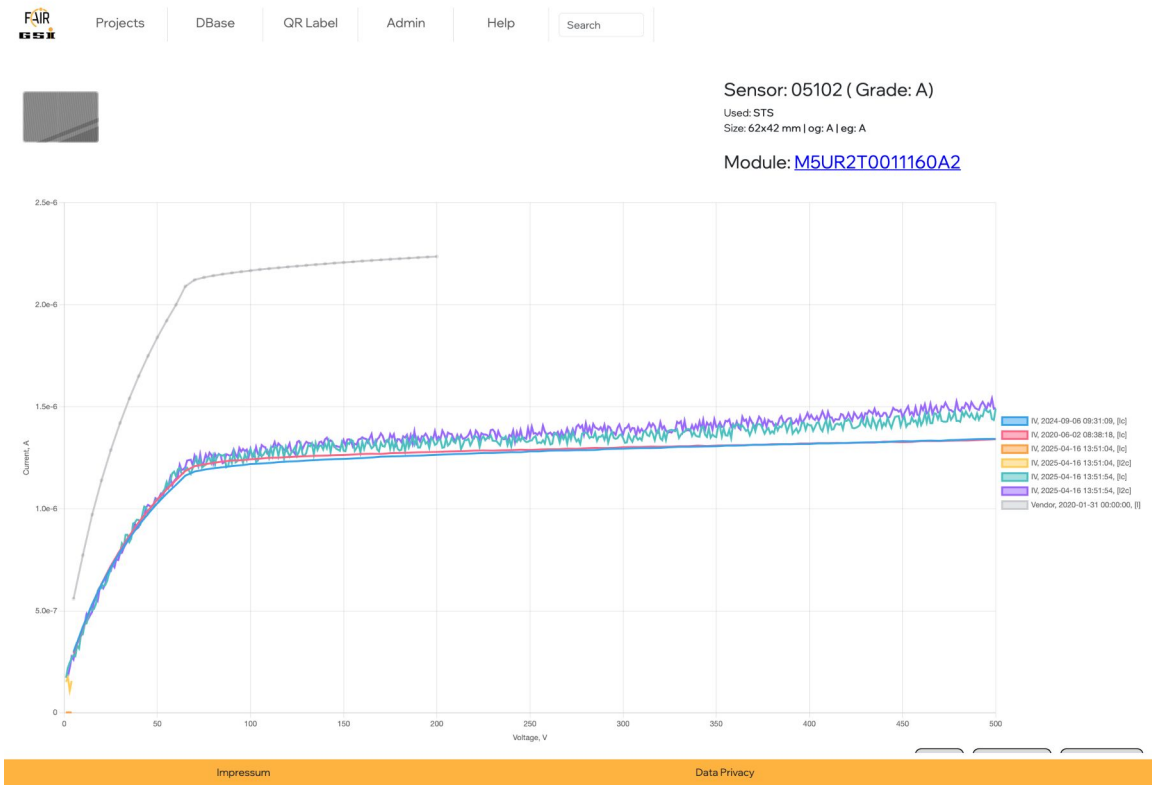


Wafer test

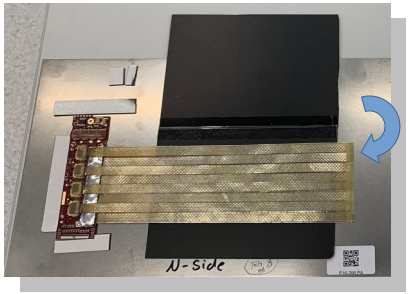


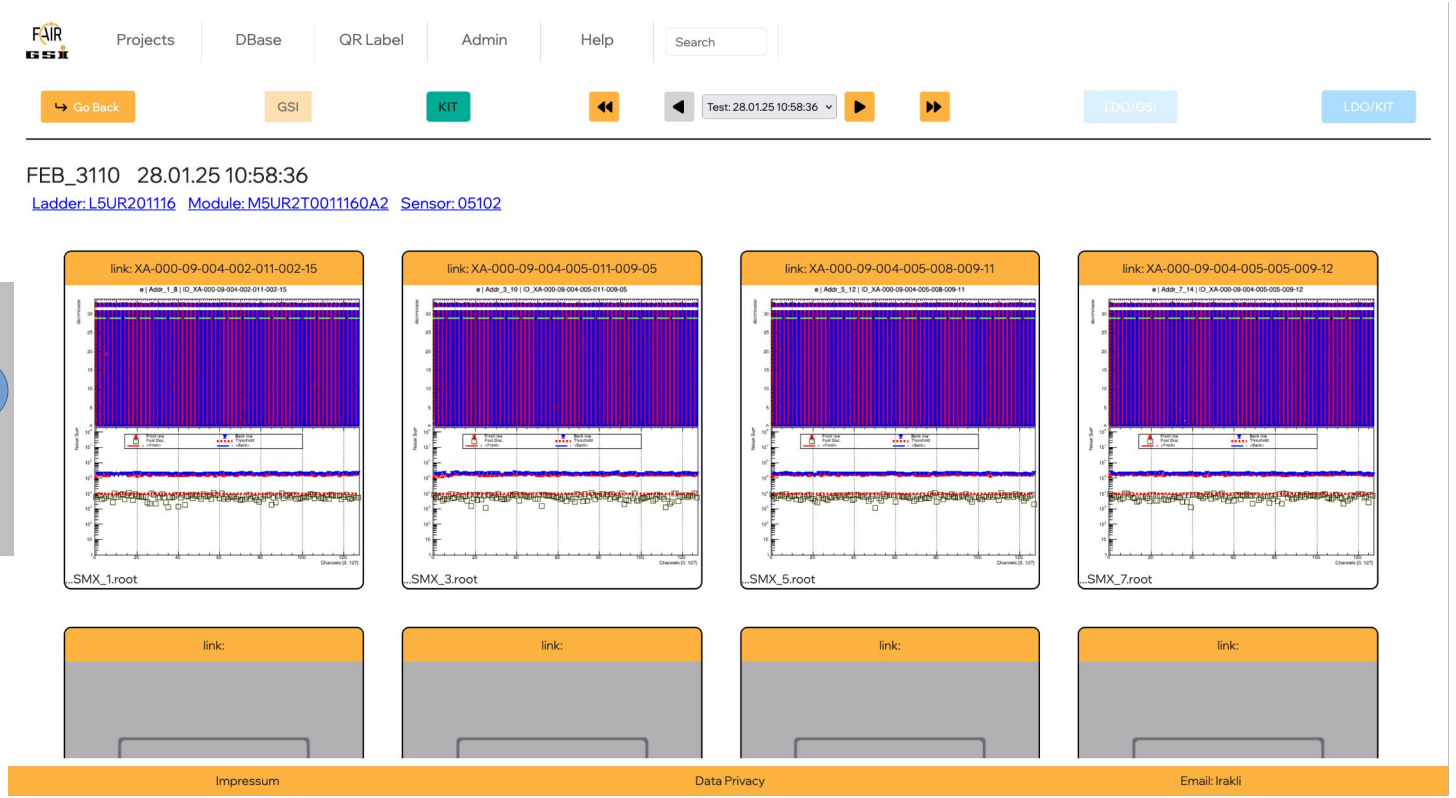


Sensor Test Web Page



Front End Board Test Page

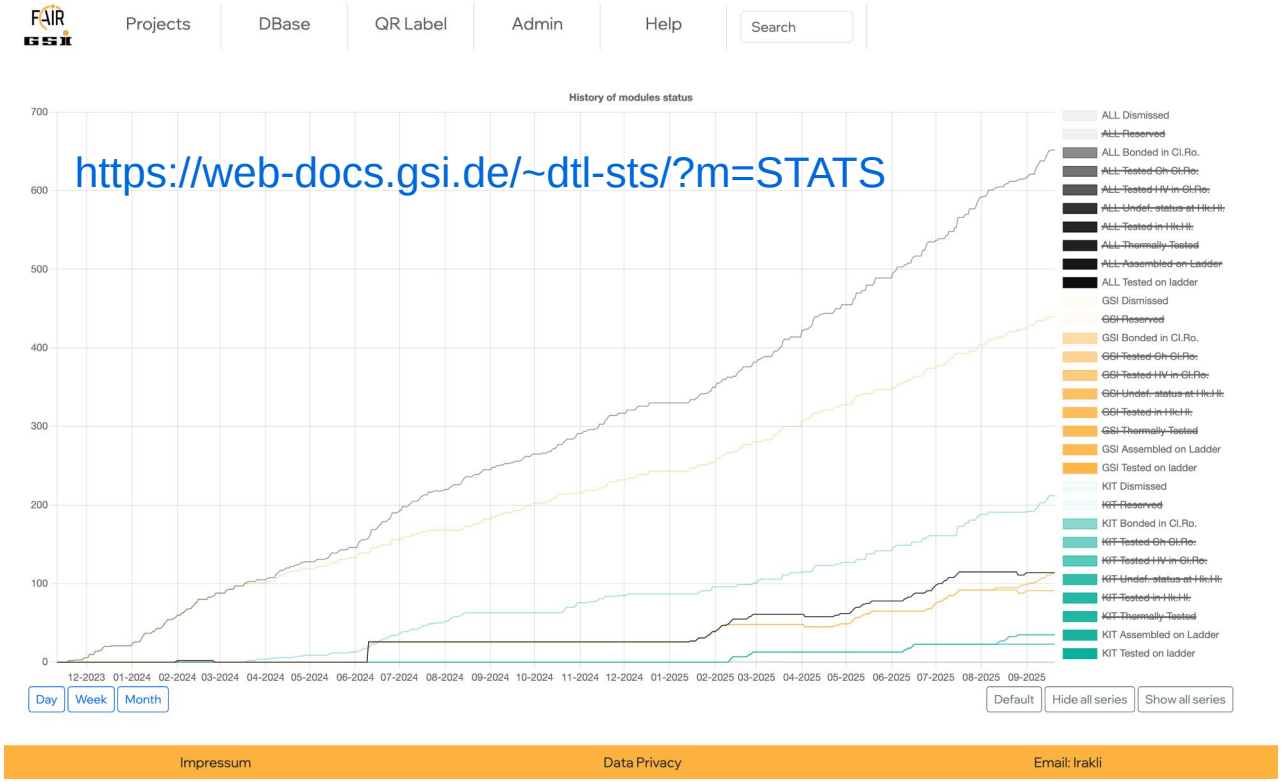




STS Assembly Monitoring

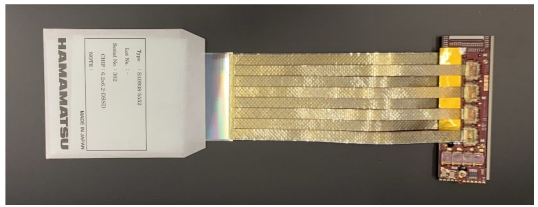
Module statuses - All (GSI, KIT)

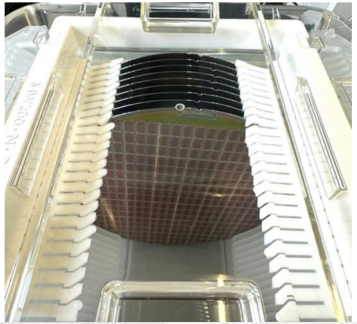
Total		GSI		KIT		
#	%	#	%	#	%	
114	13	91	80	23	20	Tested on ladder
148	17	113	80	35	20	Assembled on Ladder
512	58	358	70	154	30	Tested in Hk.Hl.
513	58	359	70	154	30	Undef. status at Hk.Hl.
519	59	363	70	156	30	Test started in Hk.Hl.
519	59	363	70	156	30	Tested HV in Cl.Ro.
656	74	447	70	209	30	Tested Ch Cl.Ro.
659	75	447	70	212	30	Bonded in Cl.Ro.
34	4					Rebuilt modules
224	25	134	60	90	40	Reserved



Summary

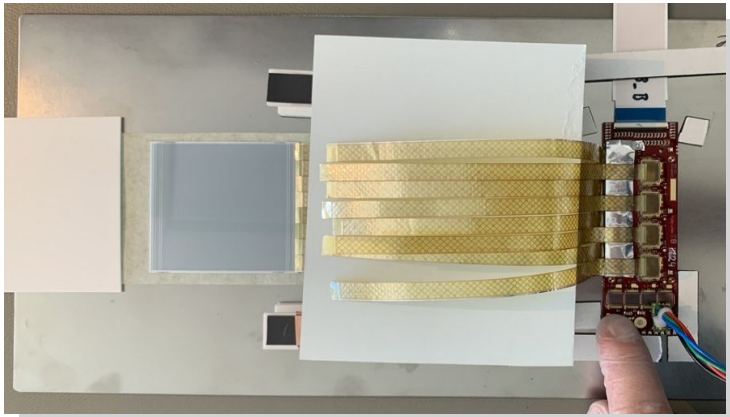
- **75%** of the modules are produced
- 13% of the modules tested on the ladder
- 80 Wafers, each with 360 ASICs tested
- Extremely successful Q&A procedure
- Assembly teams at GSI and KIT
- Universal testing and storing software
- Experimental success at **miniCBM**



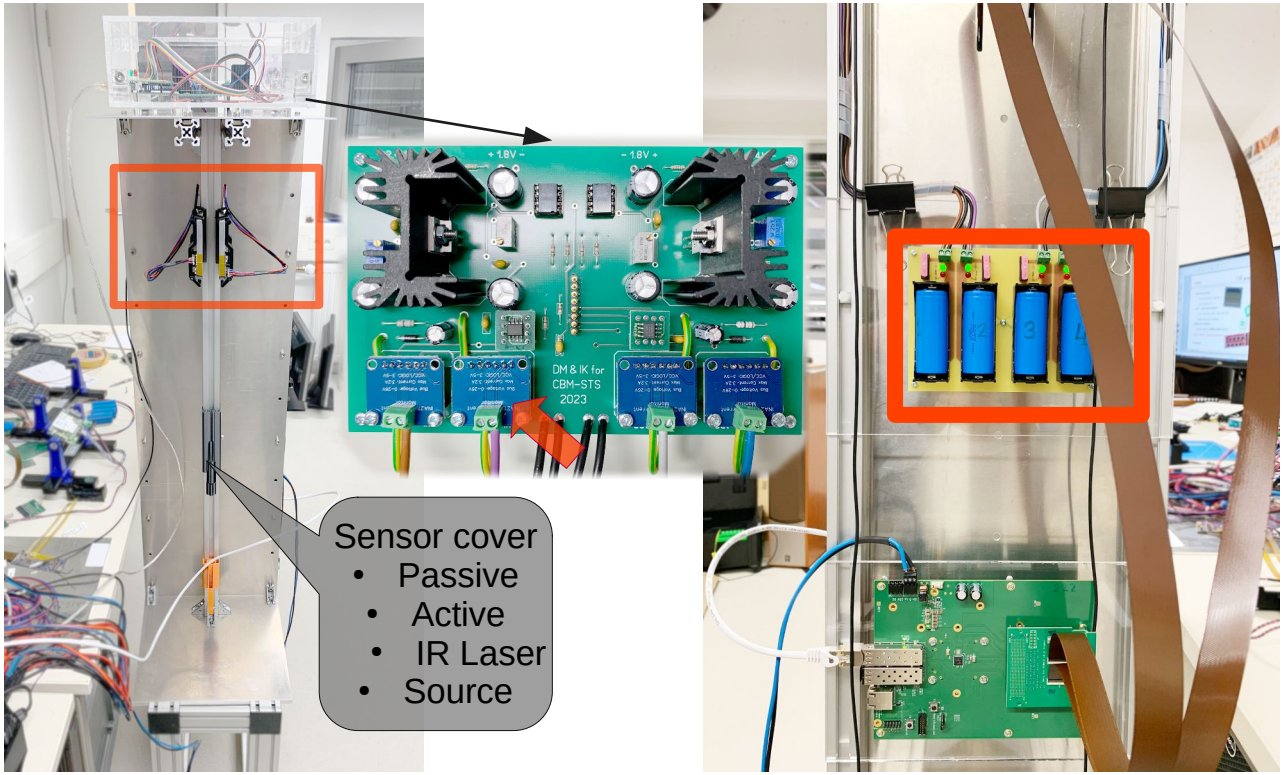


Total		GSI		KIT		
#	%	#	%	#	%	
114	13	91	80	23	20	Tested on ladder
146	17	111	80	35	20	Assembled on Ladder
512	58	358	70	154	30	Tested in Hk.HI.
513	58	359	70	154	30	Undef. status at Hk.HI.
519	59	363	70	156	30	Test started in Hk.HI.
519	59	363	70	156	30	Tested HV in CI.Ro.
655	74	451	70	204	30	Tested Ch CI.Ro.
658	75	452	70	206	30	Bonded in CI.Ro.

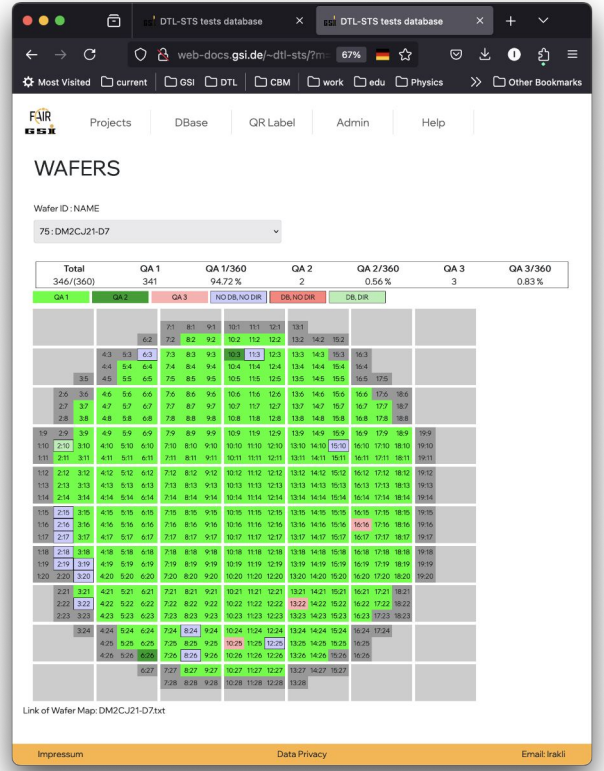
Sensor test

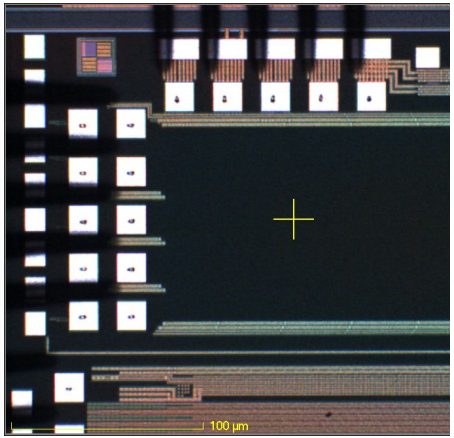


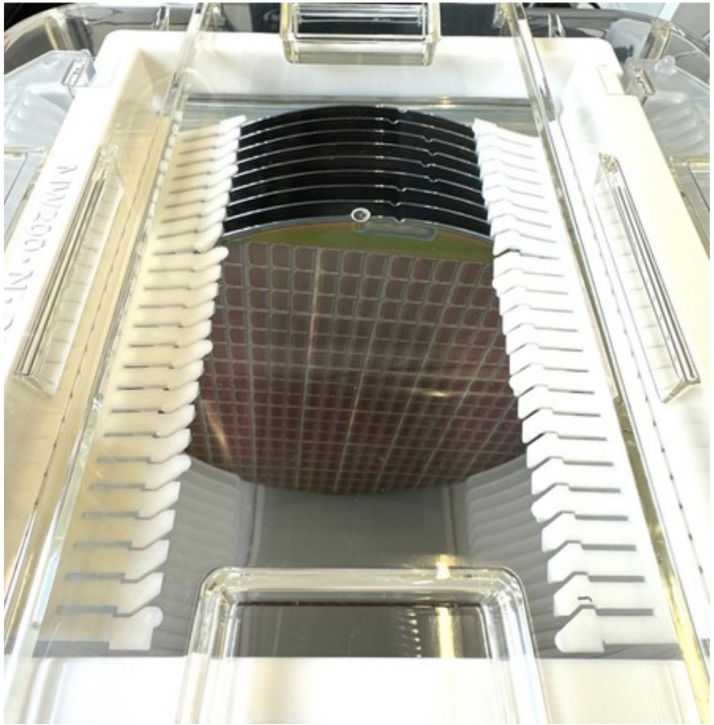
Module test setup



ASIC Wafer 80 x 360 chips







Wafer level ASIC test