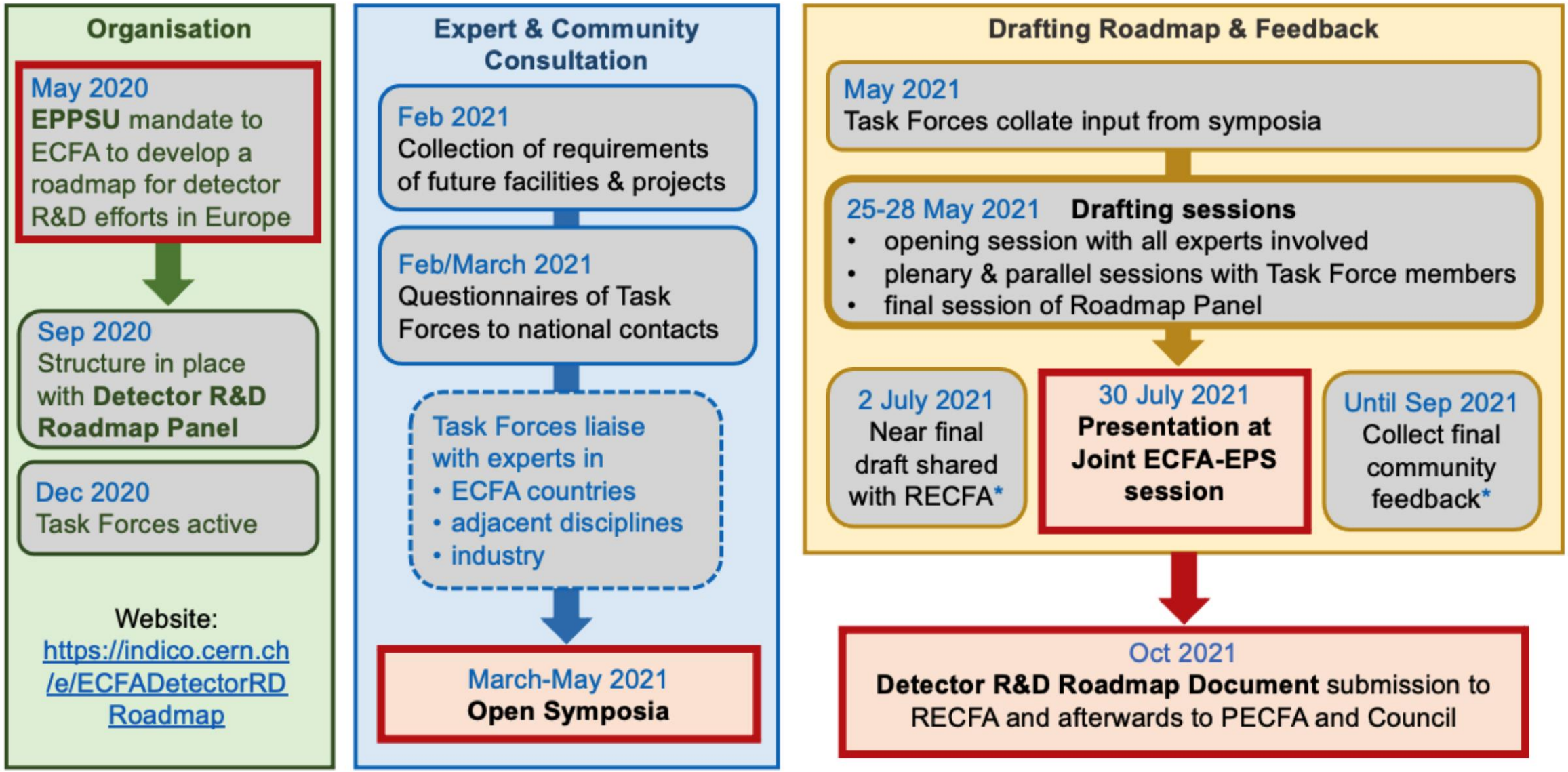
ECFA DRD7: Electronics

Francesco Crescioli – 28/06/2023

ECFA Detector R&D Roadmap Process



https://cds.cern.ch/record/2784893

*community feedback via RECFA delegates and National Contacts

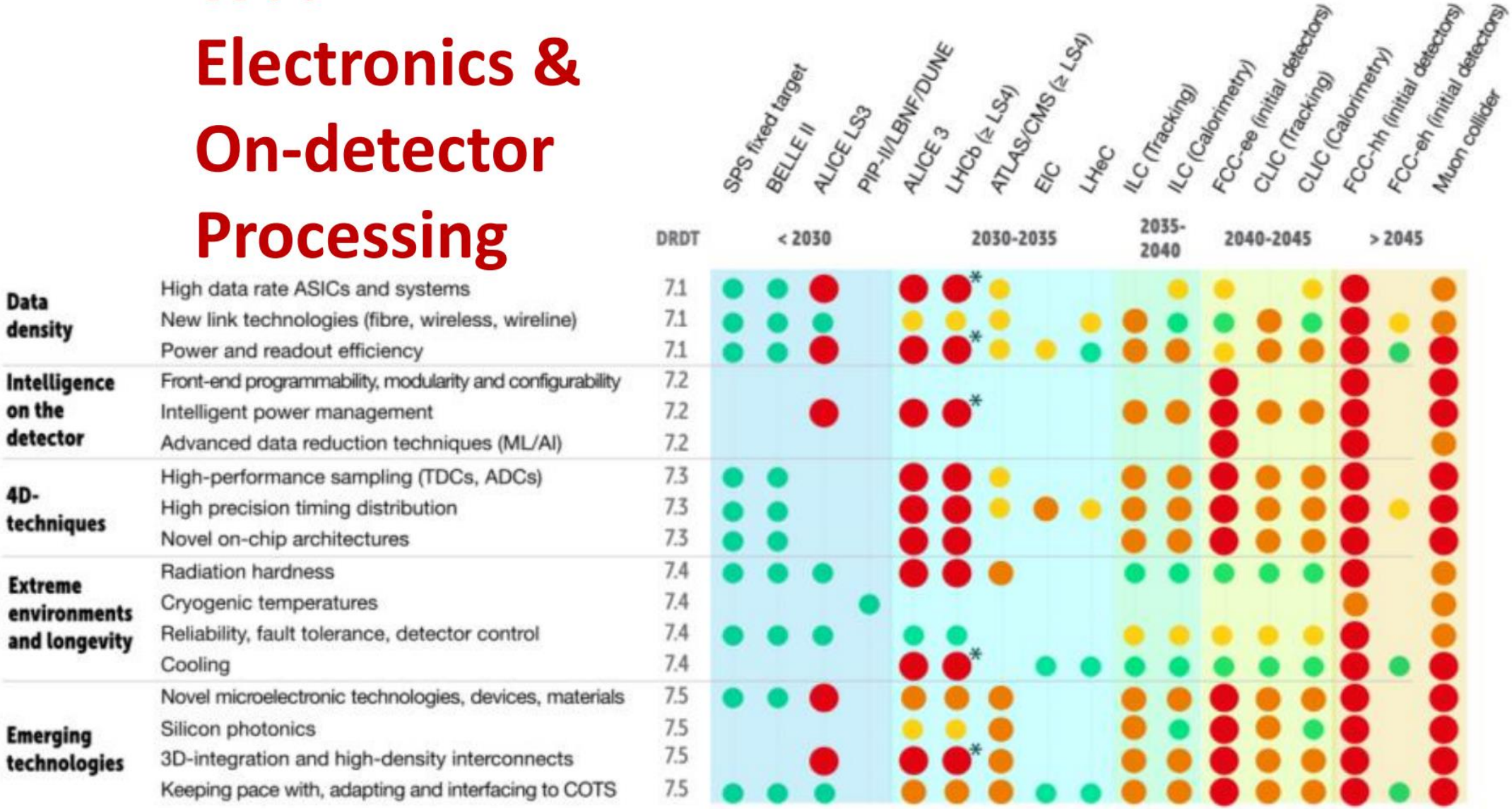
ECFA DRD7 Workshop - 14-15/03/2023

- Qu'est-ce que l'ECFA ?

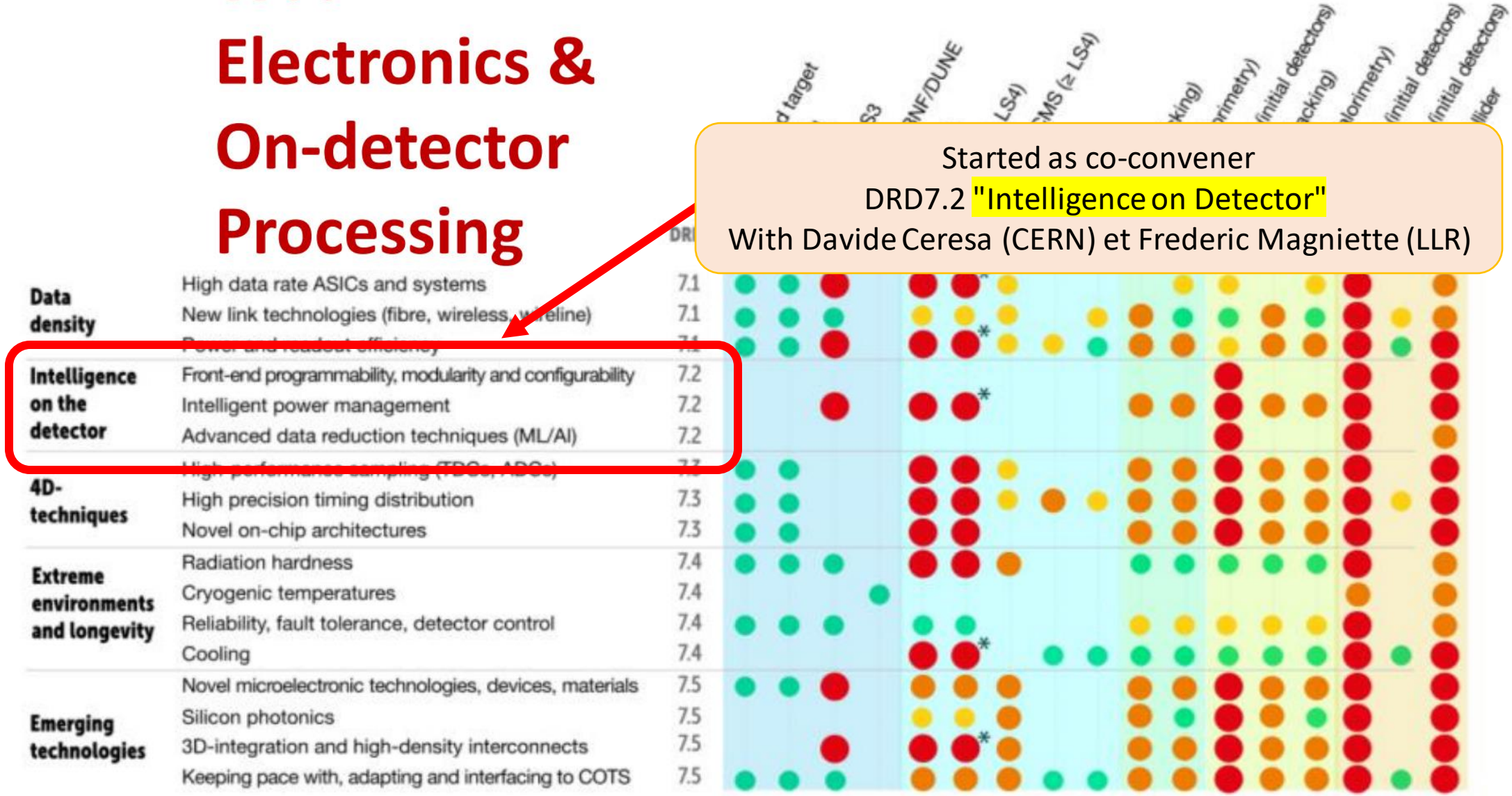
https://ecfa.web.cern.ch/

- Qu'est-ce que DRD7?
  - Detector R&D Roadmap
  - DRD7 = Detector R&D Themes 7 "Electronics & On-Detector Processing"

TF7: Electronics & On-detector Processing



TF7: Electronics & On-detector Processing



7.1: **Data density and power efficiency**

Szymon Kulis (CERN), Jeffrey Prinzie (KU Leuven), Jan Troska (CERN)

- High data-rate ASICs and systems
- New link technologies, including silicon photonics technology
- Power conversion and efficiency optimisation

7.2: **Intelligence on the detector**

Davide Ceresa (CERN), Francesco Crescioli (IN2P3-LPNHE), Frédéric Magniette (IN2P3-LLR)

- Front-end programmability and modular design
- Intelligent power management
- Advanced data reduction techniques

7.3: **4D and 5D techniques**

Sophie Baron (CERN), Marek Idzik (AGH-Kracow), Adriano Lai (INFN-Cagliari)

- High-performance sampling
- High-precision timing distribution
- Novel on-chip architectures

7.4: **Extreme environments**

Giulio Borghello (CERN), Oscar Francisco (Uni-Manchester), Manuel Rolo (INFN-Torino)

- Cryogenic technology and operation
- Thermal management of ASICs
- Radiation hardness

7.5: **Backend systems and COTS**

Conor Fitzpatrick (Uni Manchester), Niko Neufeld (CERN), NN

- Use and adaptation of advanced COTS technologies
- Real-time software and firmware development
- System-level control and readout

7.6: **Complex imaging ASICs and technologies**

Marlon Barbero (IN2P3-CPPM), Michele Caselle (KIT), Iain Sedgwick (RAL), Walter Snoeys (CERN)

- Common access framework to selected imaging technologies
- Common IP for imaging ASICs
- 3D integration and interconnects

7.7: **Tools and technologies**

Kostas Kloukinas (CERN), Xavi Llopart (CERN), Mark Willoughby (RAL)

- Access and support to qualified technologies and tools
- Investigation of emerging microelectronics technologies
- Support and training for device and systems development and verification
- Common IP and design reuse

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Continuing as co-convener
WG 7.2 "Intelligence on Detector"
With Davide Ceresa (CERN) et Frederic Magniette (LLR)

Proto-projects: *Ideas that have the potential to aggregate the community in projects. Representative of interests expressed by the community during the last workshop and after it. Not exhaustive nor exclusive.*

WG 7.1: **Data density and power efficiency**
Data density and power efficiency are key to developing the next generation of front-end
electronics. Projects being proposed so far include:
7.1.a: **Si-photonics based links, including IP blocks for timing distribution**
Contact: jan.k.troska@cern.ch
7.1.b: **High efficiency DCDC converters**
Contact: szymon.kulis@cern.ch, jeffrey.prinzie@kuleuven.be

Proto-projects: *Ideas that have the potential to aggregate the community in projects.*

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Not exhaustive nor exclusive.

WG 7.2: **Intelligence on the detector**
Two types of projects are envisaged in WG7.2: support projects based on tool or knowledge exchange, promoting collaboration between developers and users; and specific projects based on defined deliverables but with a potential for common and shared use in the community.
Four proto-projects are highlighted below to seed feedback:
7.2.a: **Radiation tolerant processors**
Contact: davide.ceresa@cern.ch
7.2.b: **Evaluation of radiation tolerant design techniques**
Contact: francesco.crescioli@lpnhe.in2p3.fr
7.2.c: **System-level architectural modelling**
Contact: davide.ceresa@cern.ch
7.2.d: **Benchmarking platform for advanced reduction techniques (ML, AI), and associated hardware testing**
Contact: frederic.magniette@llr.in2p3.fr

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WG 7.3: **4D and 5D techniques**

Two types of projects are considered by WG7.3: the design and architecture of ASIC macrocells on the one hand (7.3.a and 7.3.d) and time distribution techniques, tools and components on the other hand (7.3.b and 7.3.c).

7.3.a: **High performance TDC and ADC blocks at ultra-low power**

Contact: idzik@ftj.agh.edu.pl

7.3.b: **Timing methodologies and infrastructures**

- Common, generic approach for simulating timing in detectors
- Precise timing measurement and calibration

Contact: sophie.baron@cern.ch

7.3.c: **Timing distribution techniques**

- Components design and characterization (COTS and Custom)
- Distribution architectures and systems

Contact: sophie.baron@cern.ch

7.3.d: **Novel architectural solutions for ASICs with precision timing capabilities**

Contact: adriano.lai@ca.infn.it

Proto-projects: *Ideas that have the potential to aggregate the community in projects.*

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WG 7.4: **Extreme environments**
CMOS technologies operating at cryogenic temperatures (7.4.a) and/or in radiation environments (7.4.b and 7.4.c) and investigations on cooling technologies (7.4.d).
7.4.a: **Modelling and development of an ASIC Process Design Kit (PDK) for operation at cryogenic temperatures**
Contact: darochar@to.infn.it
7.4.b: **Radiation resistance of advanced CMOS nodes**
7.4.c: **Survey and access to test facilities**
Contact: giulio.borghello@cern.ch
7.4.d: **Silicon microchannels cooling plates**
Contact: cogan@cppm.in2p3.fr and oleroy@cppm.in2p3.fr

Proto-projects: *Ideas that have the potential to aggregate the community in projects.*

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WG 7.5: **Backend systems and COTS**
backend data processing, connectivity and the need to keep pace with Commercial, off-the-shelf hardware as it evolves. 7.5a: capture frequently updated benchmarking of COTS processing technologies is considered. Related to this, in 7.5b, a method of hosting and maintaining benchmark algorithms as a resource for 7.5a and for the community in general is provided. 7.5c proposes R&D into removing the need for dedicated backend hardware using COTS solutions.
7.5.a: **Benchmarking of Heterogeneous COTS Architectures for Physics (BOHCAP)**
Contact: conor.fitzpatrick@cern.ch
7.5.b: **DAQ Overflow**
Contact: conor.fitzpatrick@cern.ch
7.5.c: **No Backend**
Contact: Niko.Neufeld@cern.ch

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7.6: **Complex imaging ASICs and technologies**
Providing support to other areas in the broader DRD programme.
To support these high level goals, DRD 7.6 is interested in receiving submissions in the following areas:
7.6.a: **Setting up joint access to selected imaging technologies**

- Candidate technologies might include but are not limited to:
  - Tower Semiconductor (65 and 180nm)
  - LFoundry
  - TSI
- Proposals for IP blocks developed in the above technologies such as pixels, ADCs, data transmission blocks, bias circuits etc

Contact: : Walter Snoeys, Marlon Barbero
7.6.b: **Shared access to 3D technologies**
Contact: Michele Caselle, Walter Snoeys
7.6.c: **Development of a common QA/ASIC development framework**
Contact: Marlon Barbero, Iain Sedgwick

Proto-projects: *Ideas that have the potential to aggregate the community in projects.*

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7.7: **Tools and technologies**
providing support to foundry, process, tools and design related tasks. Its importance is such that the community is encouraged to engage with the experts into common projects to develop and spread this crucial expertise. Projects may include dedicated funding schemes for recruiting and training specialists working for the community.

7.7.a: **Expand existing ASIC and Foundry support service to advanced nodes, develop and distribute IP blocks (fitting digital on top flows)**
Contact: Kostas.kloukinas@cern.ch

7.7.b: **Support EDA tools, develop seamless IP exchange across community**
Contact: mark.willoughby@stfc.ac.uk

7.7.c: **Complex digital on top design and verification: develop and implement a model for supporting the community and disseminating the expertise**
Contact: Xavier.Llopart@cern.ch

7.7.d: **Survey 3D wafer stacking options, explore access possibilities, implement framework for community**
Contact: Kostas.kloukinas@cern.

Interested scientists, groups or collaborations are invited to express their interest in participating to R&D projects in DRD7 by contacting the conveners of the relevant Working Group:

If interested in joining one of the proto-projects highlighted in section 2, please describe:

- Contributor and area of competence
- Available material and human resources
- Existing R&D framework and available funding
- Rough estimate and time profile of to be requested resources, if needed in addition to existing resources

If interested in proposing a new project, please submit your proto-project as a group, as conveners will not be able to organise projects based on individual suggestions. The following elements will be needed to evaluate your proposal:

- Proto-project description
- Innovative/strategic vision
- Performance target, deliverables and timeline
- Multi-disciplinary, transversal content
- Contributors and area of competence
- Available material and human resources
- Existing R&D framework and available funding
- Rough estimate and time profile of to be requested resources, if needed in addition to existing resources

DEADLINE 30th JUNE

An example: IN2P3's THINK R&T project

- 2020-2022 THINK: "*On propose dans ce projet d'évaluer l'implémentation de techniques neuronales temps réel dans les étages les plus amonts de la chaîne d'acquisition. Plusieurs types de hardwares seront évalués : GPUs, FPGAs, chips neuromorphiques, chips MPPA tant sur le plan des performances que de la facilité de mise en œuvre.*"
- THINK collaboration is going to ask funding for a THINK2 phase
  - This is independent of ECFA
- Similar projects exists basically in every FA
- THINK2 idea will be submitted to DRD7 in the context of 7.2 and 7.5
  - What I expect: being able to coordinate/aggregate similar local projects in an EU-level big project (= more funding...)

Another example: PCIe400

- Funded R&T project in the context of LHCb DAQ
  - Started in 2022 lasting for 3 years, 5 IN2P3 labs (+ CERN)
- Big FPGA from Intel to analyse real-time Velo data using NN
  - 400 GBps link to PCIe!
  - HW/FW/SW challenge
- Applied for DRD 7.2 (probably also relevant for 7.5)

What about LPNHE?

- Personally unavailable until ITk production end is in sight
  - I would like to study radiation induced errors in digital logic, potential synergy with other future R&D (e.g. integrated CMOS sensors), which is 7.2b
- Inquired informally some colleagues
  - Potential interest for timing methodologies (DRD 7.3)
  - Interest in the topics of 7.5 (mainly) and 7.2d for the AI/ML part on hardware accelerators
    - Not willing to participate in this phase, maybe a future call?

Backup material

Proto-projects: *Ideas that have the potential to aggregate the community in projects.*

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WG 7.2: **Intelligence on the detector**

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Possible interest from our ML/AI group?

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This is implicit in all recent microelectronics for radhard environment developments. Could be an explicit topic.