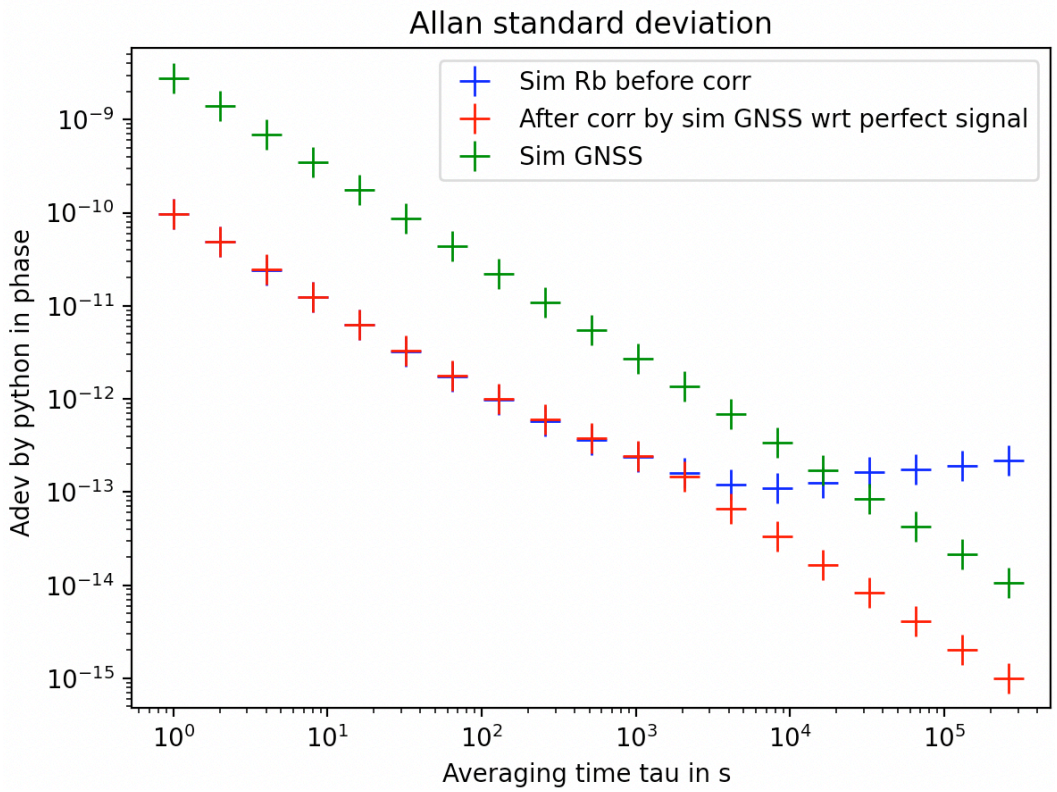
Status of the Time Distribution System for Hyper-Kamiokande

stefano russo LPNHE 29/06/2023

Time Generation Status

Online correction : first implementation with simulated data

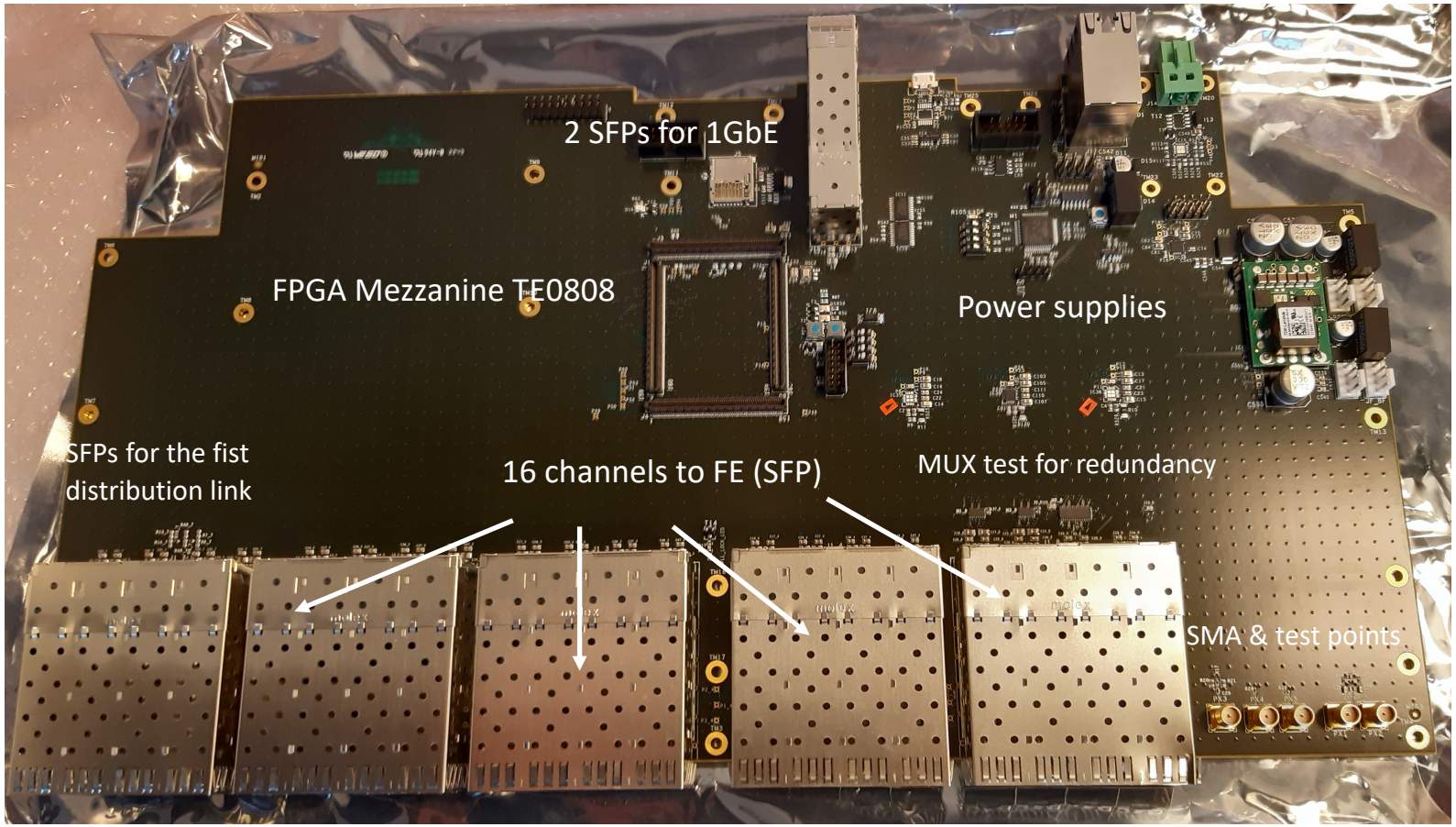


We obtain very satisfying results even by taking the corrections from the previous interval :

- Because the length of the interval L is optimized
- The tendency of the drift does not change fast with respect to L

Test of the time drift correction has giving good results on simulation. The same algorithm is now applied on raw data

TDM Prototype Tests



Before the board was delivered, most of the core firmware was developed on EVB so the tests are going fast.

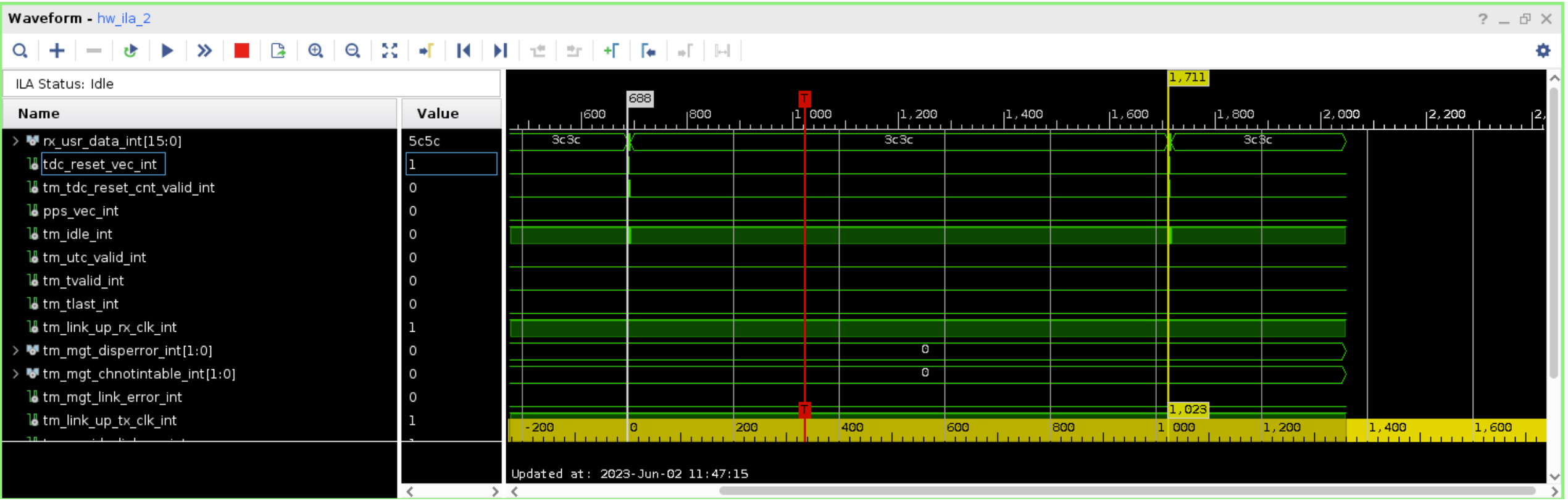
TDM Prototype Tests

With the first round of tests several good results has been achieved. Here is the list:

- Linux Boot from SD card ✓
- Establishing Ethernet connection via PS serializer (GTR) and an SFP to RJ45 converter ✓
- Test of I2C busses to control the SFP power and critical lines and the onboard PLL ✓
- Test of the sync link against the DPB mockup on ZCU102 (10/16 channels) ✓
- Test of timing signal transmission from TDM to ZCU102 (10/16 channels) ✓

These results show that the board is operational and can be used for the interface tests with other boards (vertical slice test).

Test of Timing Signals Exchange Between TDM and DPB on ZCU102



The two markers are set on two subsequent TDC reset received on the DPB. The distance between them is 1024 clk cycles at 62.5 MHz = 16.384 us.

The space between the TDC resets can be used to send async data. When there is none idles are sent (3C3C = to K28.1)

TDM Prototype Tests

Next test to be done:

- Timing performance characterization
- Time link redundant scheme test
- On board microcontroller and environmental sensors test
- Integration with the first distribution stage and real DPB

All the remaining checks will be done in the next month. We count to finish by end of September.

TDM Development Plan

In light of the current results, we think we can produce only one other prototype (instead of the two envisioned in the schedule). It will have few new features that are tested in this version. Most notably the time link redundant scheme.

The board submission is scheduled for the end of September.

Vertical Slice Test

This year and the next we plan to finalize and validate the design on the distribution board to start the production by the end of 2024 (according to the schedule).

The validation process will be done with the stand-alone tests and in the Vertical Slice Test that we are organizing at CERN. This is an essential milestone for us and for the HK project.

I’m in charge of coordinating the whole vertical slice test effort.

Vertical Slice Test

The vertical slice test is an evolving test stand in which we'll include all the electronics and DAQ elements as soon as they are ready. It stated two weeks ago and will go on until the integration will begin. It will be very useful to test all the interfaces and check the HK readout chain "as a system". It will be useful also to prepare the tests during integration.

Every subsystem needs to provide the elements for which it is responsible. In our case we need to bring:

- First Distribution board (CEA)
- Second distribution board (we'll use prototypes we have/will build)
- Power supplies (to be bought)
- Atomic clock and GNSS receiver (to be bought)

Spending Profile – 2023/2024

The spending profile we envision for the end of 2023 and 2024 reflects what said up to now:

2023:

- Two second distribution prototype v2
- A power supply (for the vertical slice test)
- An atomic clock, a GNSS and an antenna (for the vertical slice test)

2024:

- Boards production
- …

Due to the total amount expected we need to follow the European tender procedure for the production. LPNHE CTA group has given guidance and suggestion to prepare it. The estimated time to completion is about 3 months. We would like to start the procedure in September 2024

Spending Profile – 2025/2026

2025:

- Two GNSS receivers + one antenna and splitter + atomic clock (main chain)
- UPS (main chain)
- Boards power supplies

2026:

- Two GNSS receivers + one antenna and splitter + atomic clock (spare chain)
- UPS (spare chain)

We would like to defer the time generation instruments purchase to the end of installation/start of data taking. This because the atomic clocks age and the GNSS receivers now on the market could become obsolete before HK starts.

Some power supplies can be purchased in advance, if needed.

We would like to buy the instruments asking for a delivery in Japan to save custom fees. Is this acceptable?

BACKUP

Test of Sync Link to DPB on ZCU102

Thanks to all the work done on the EVB it was possible to quickly test the sync link link between the TDM and the DPB mockup realized with a ZCU102 board.

The link was successfully established and the clock passed with data on one channel.

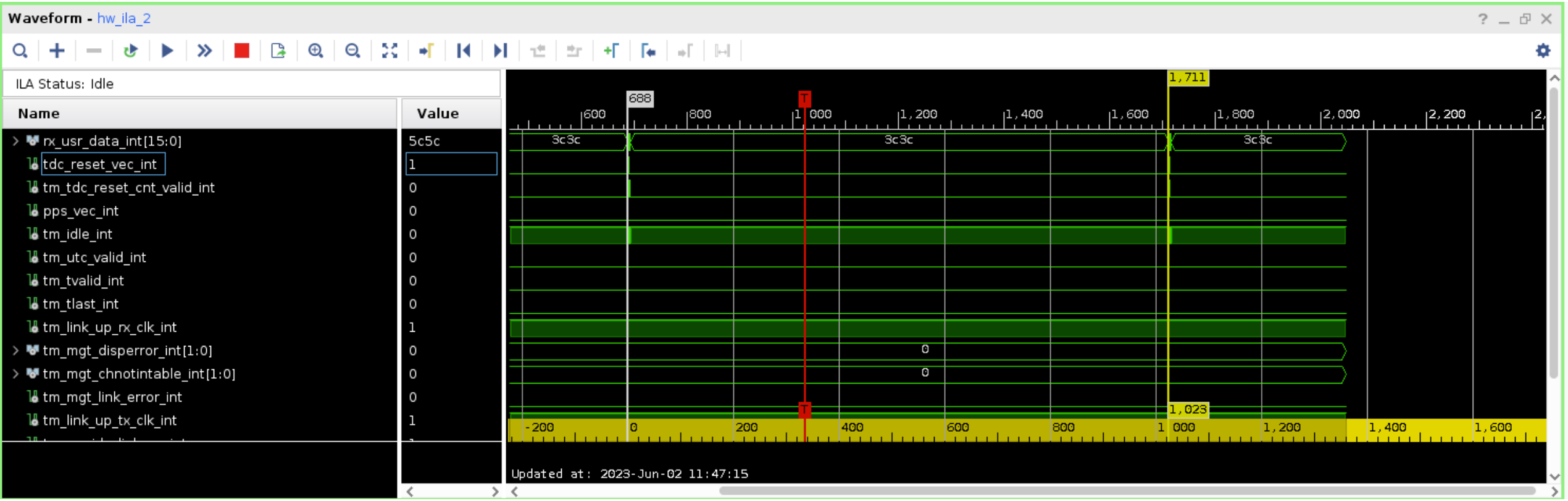
Test of Timing Signals Exchange Between TDM and DPB on ZCU102

Once the timing link was test the code to pass the timing signals (TDC reset, TDC reset counter, sync “trigger”, PPS etc.) was integrated. It performs the following tasks:

- Aligns the link so the clock received on the DPB is phase aligned with the one on the TDM.
- On the TDM it encodes the time information in serial stream using K-characters creating a frame
- On the DPB, it extracts the time information from the serial link, decodes it and present to the logic with a specific interface.
- On the DPB it echoes the same info to the TDM so the master can check that the system is working properly

All the presented tests has been done with the xilinx virtual logic analyzer which spies the internal FPGA lines. (This is not a simulation but real hw signals)

Test of Timing Signals Exchange Between TDM and DPB on ZCU102



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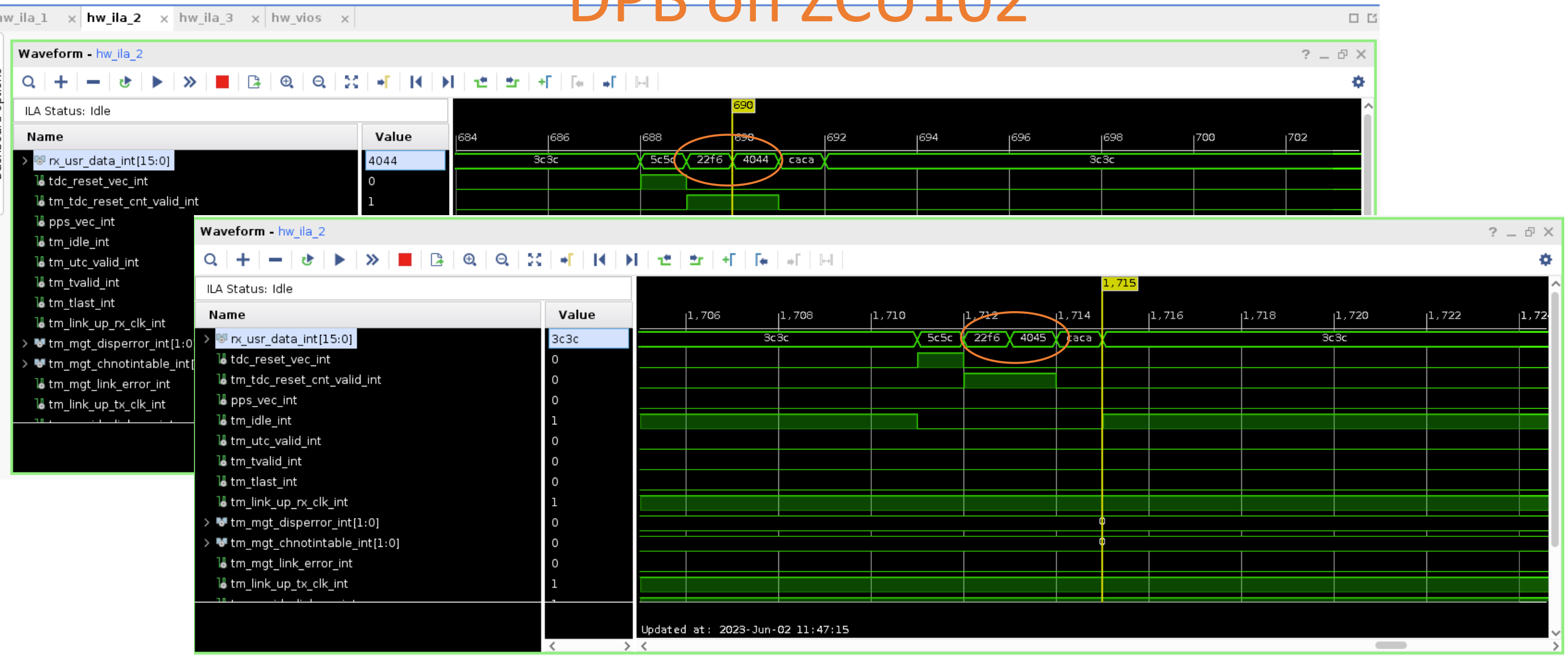

The packet structure is the one presented some time ago: 5C5C is the word that signals the TDC reset, followed by the TDC reset number and the “trigger” info. The lines below the parallel data are moved by the decoder to mark the different data.

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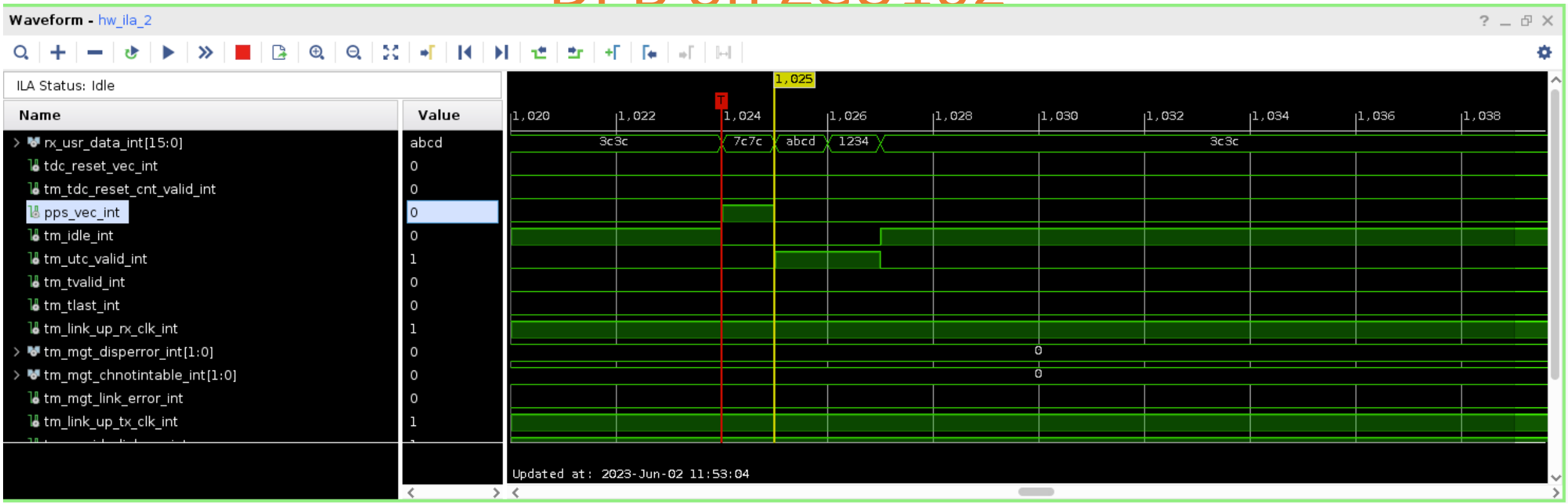
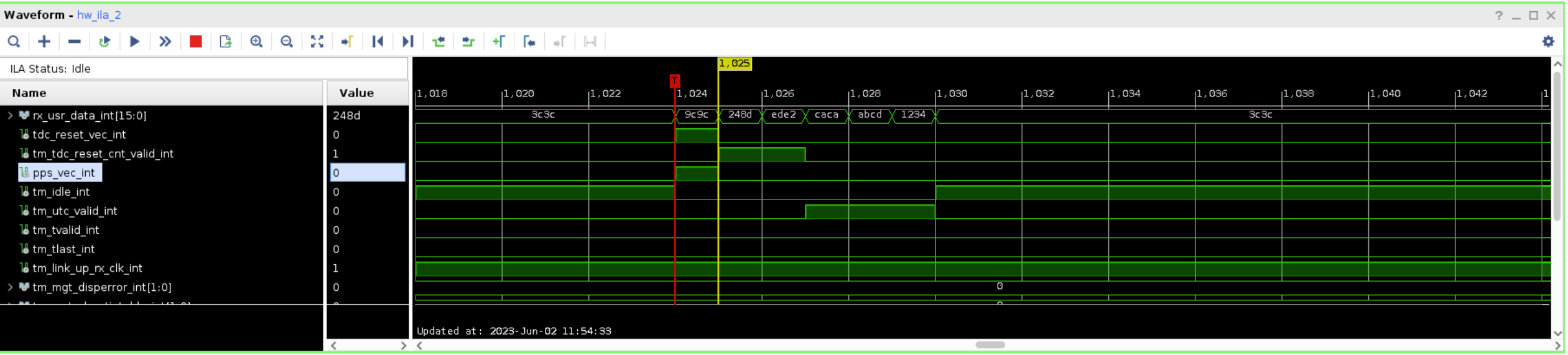


The system sends also the PPS signal followed by the UTC. In this case is a dummy word. Also here, corresponding flags are generated by the decoder.

Test of Timing Signals Exchange Between TDM and DPB on ZCU102



This is the case when the PPS and the TDC reset coincide. As visible both the UTC time, the TDC reset number and “triggers” are included in the sync packet.

Next Tests

In the next weeks other test will be performed:

- Measure the signals time distance with the oscilloscope;
- Measure the jitter on the reconstructed clock;
- Test the DMA communication with the processor and the user data packet in the serial stream (work in collaboration with digitizer group);
- Perform a multilane test.

This results have been obtained with the help of Fabrizio Ameli and Gennaro Tortone (INFN Napoli)