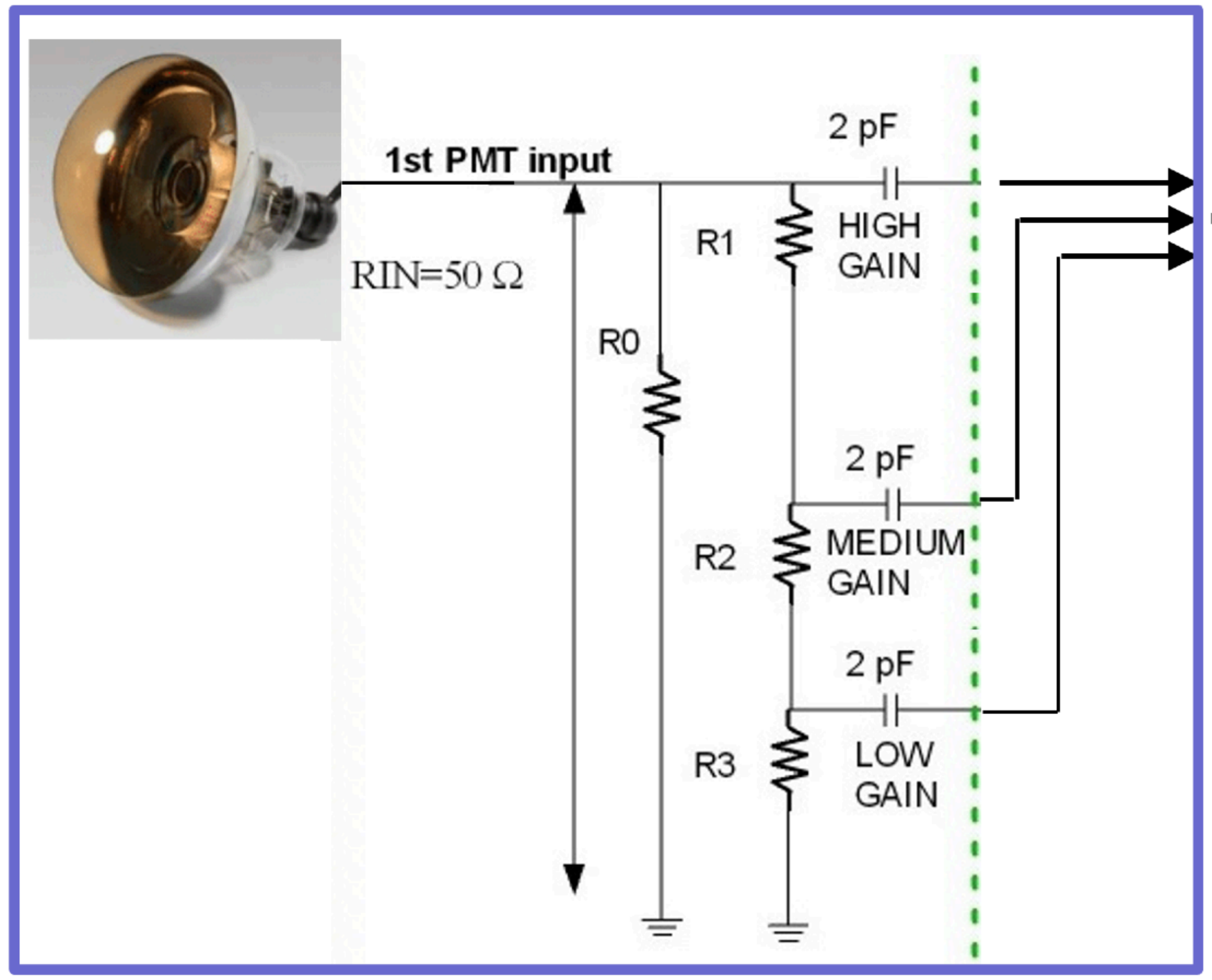
HKROC Tests & Results

A. Beauchêne, D. Carabadjac, S. Conforti, F. Dulucq, J. Nanni & R. Rogly - May 2nd, 2023

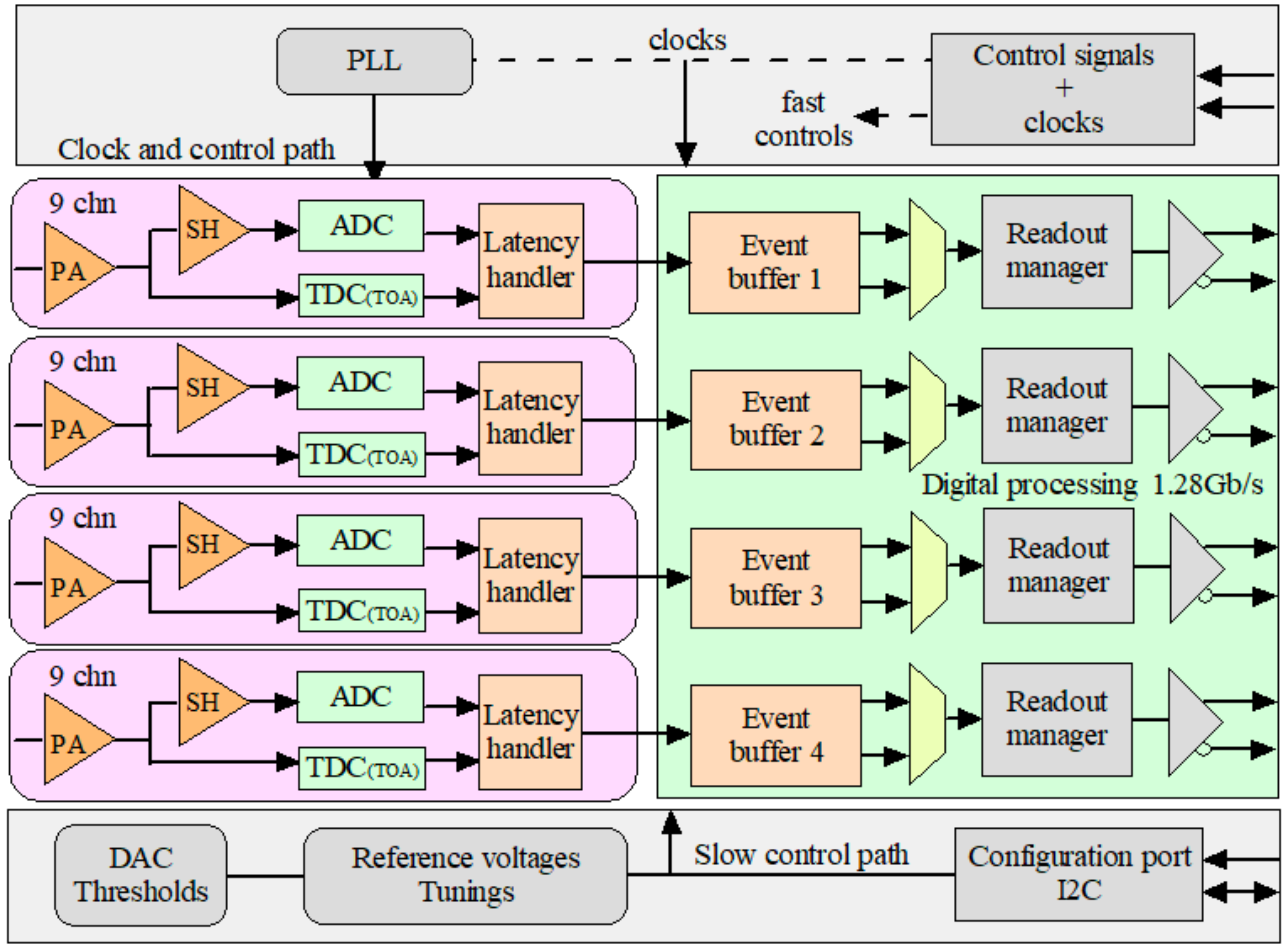
Introduction

The HKROC ASIC

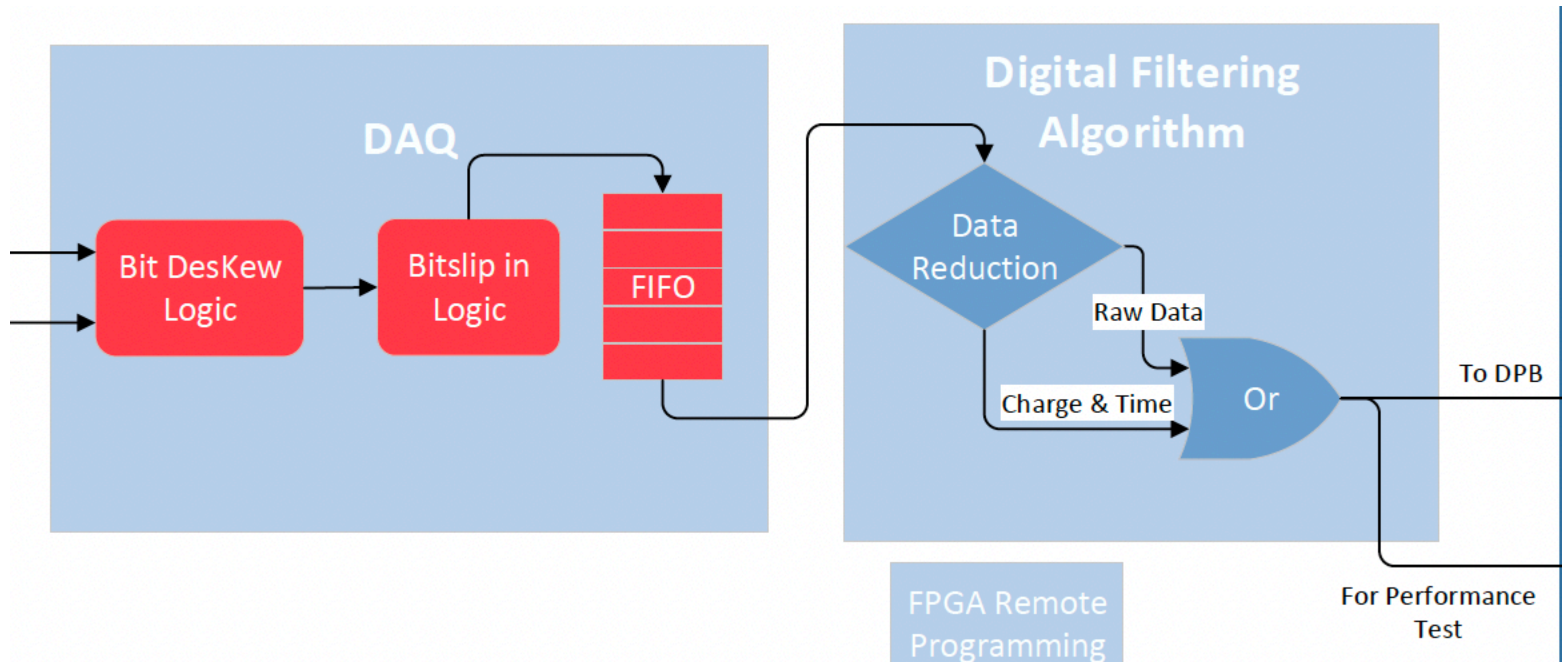
Block Diagram



On-board analogous signal input

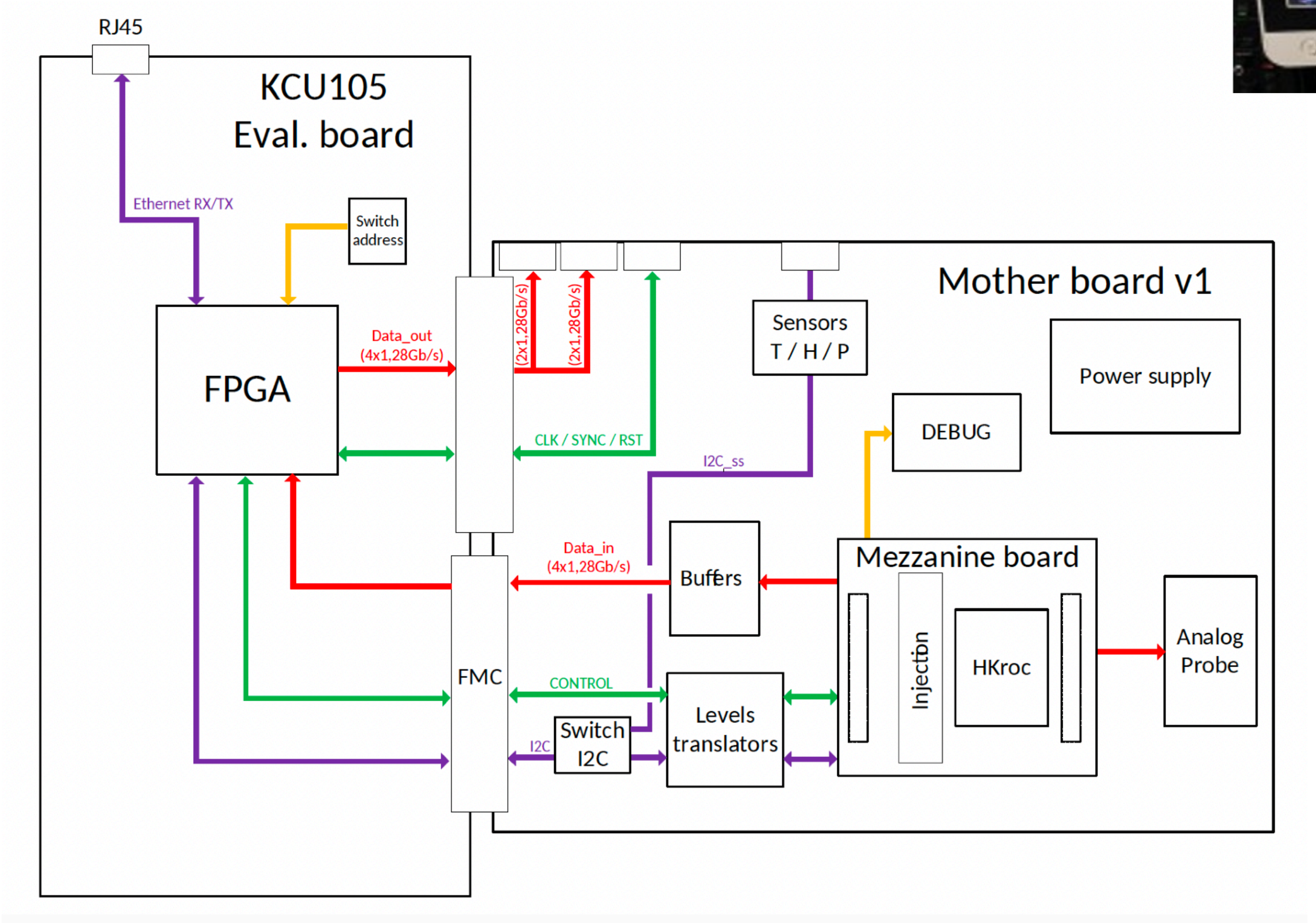


HKROC digitization

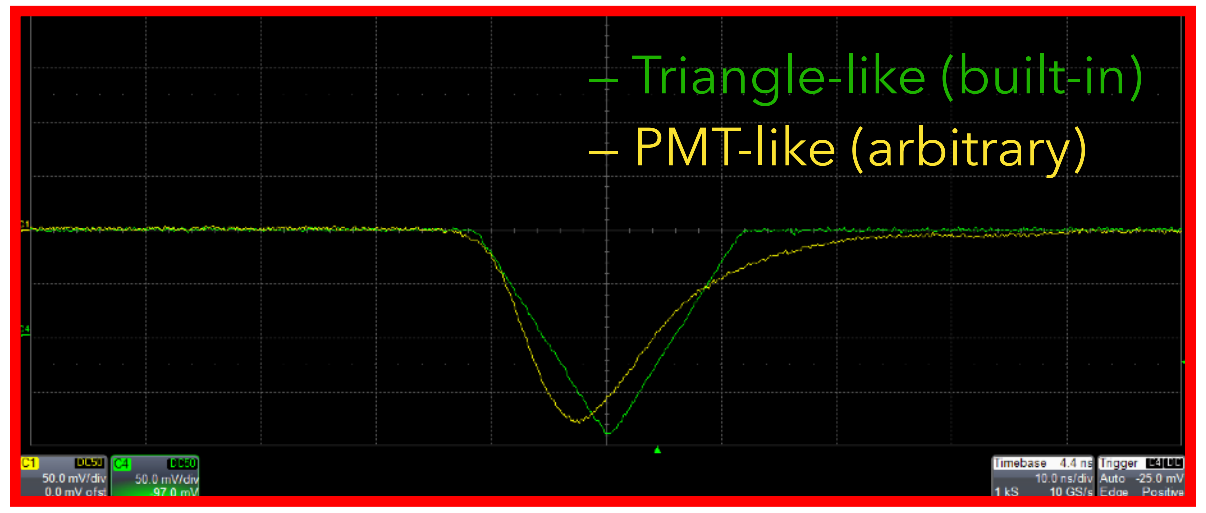


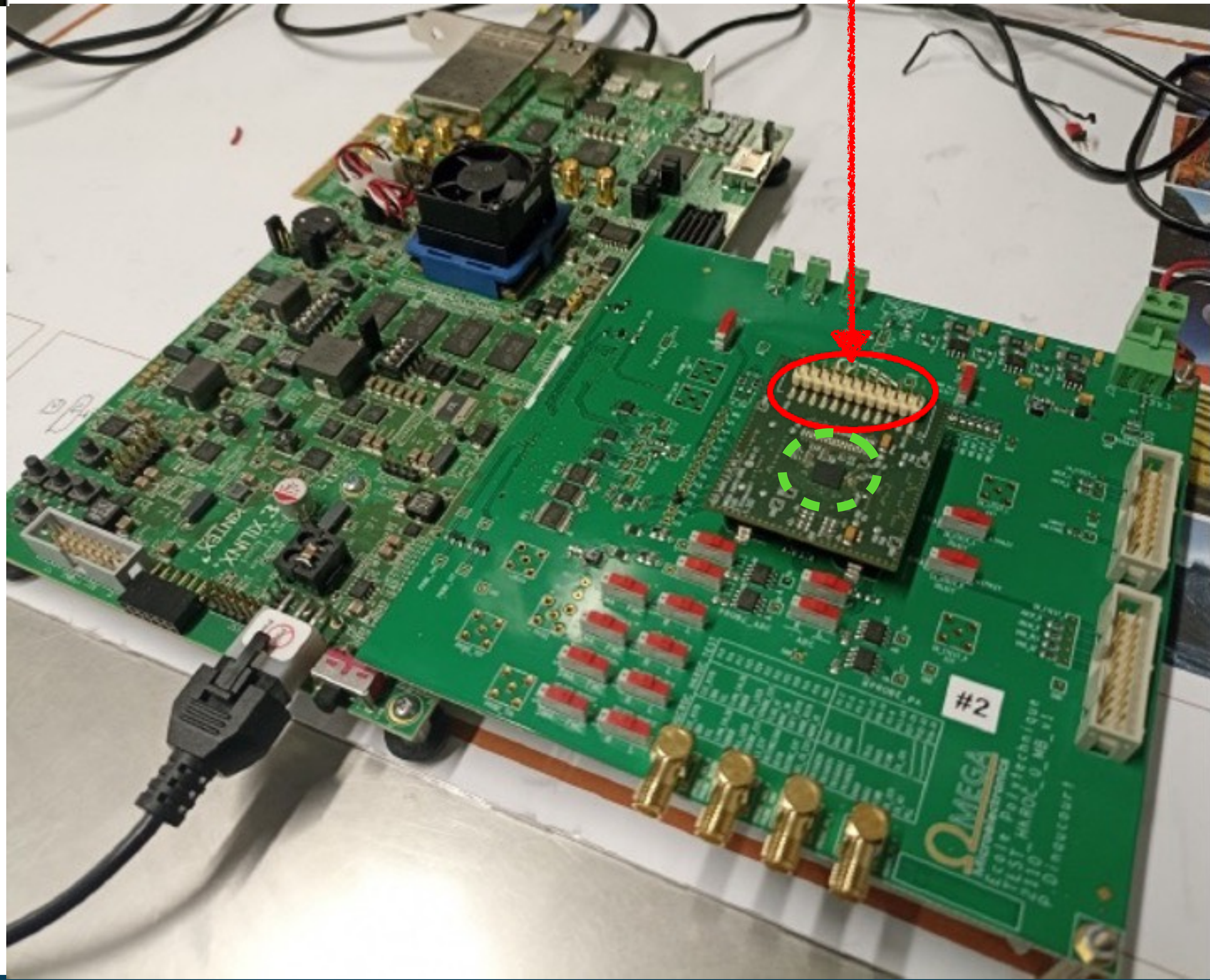
FPGA
(Charge + Time output)

HKROC digitizer architecture

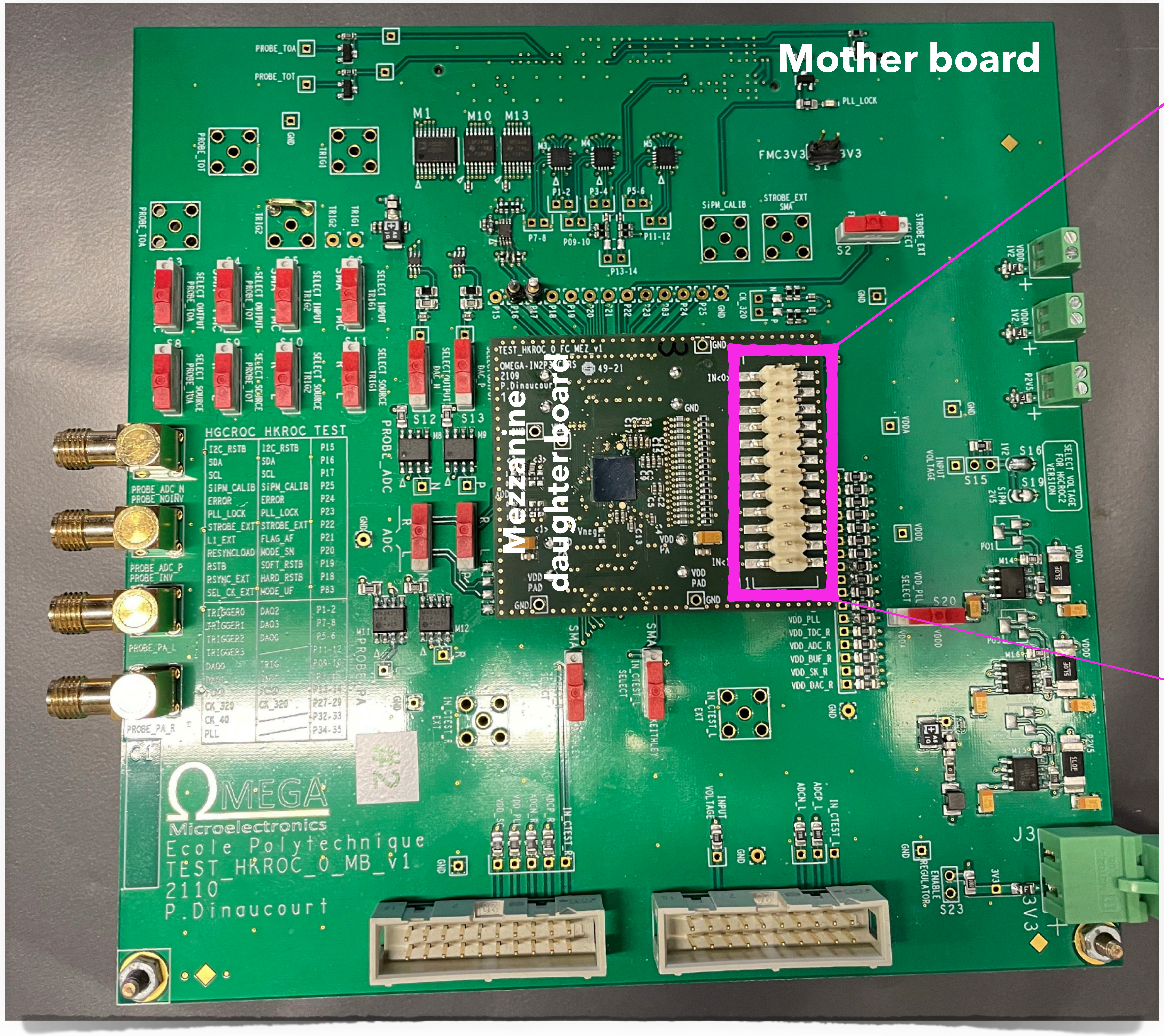


Block diagram



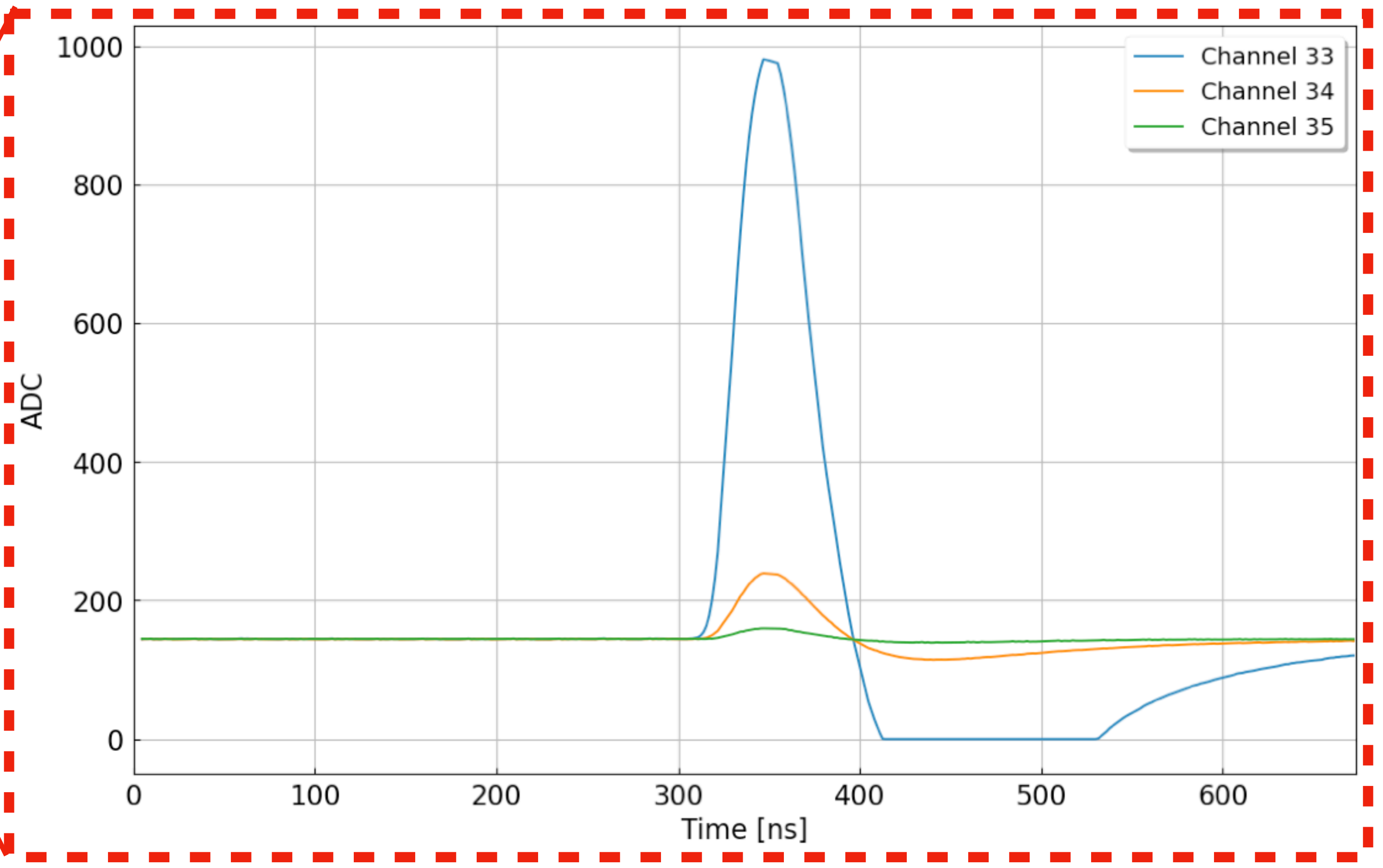


HKROC on Mezzanine daughter board



HG - MG - LG

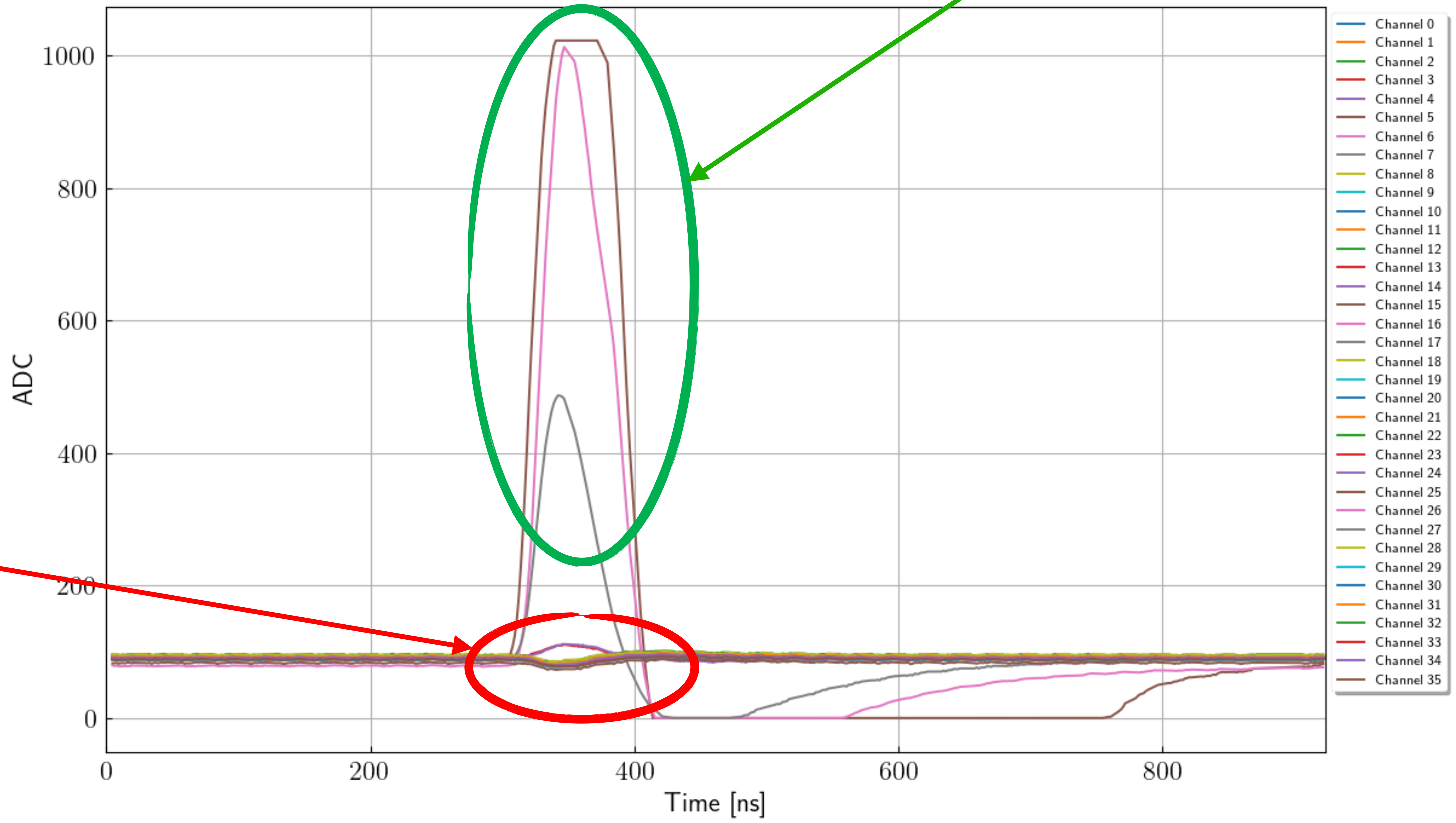
Pin 0 ↔ Ch. 0-1-2
Pin 1 ↔ Ch. 3-4-5
Pin 2 ↔ Ch. 6-7-8
Pin 3 ↔ Ch. 9-10-11
Pin 4 ↔ Ch. 12-13-14
Pin 5 ↔ Ch. 15-16-17
Pin 6 ↔ Ch. 18-19-20
Pin 7 ↔ Ch. 21-22-23
Pin 8 ↔ Ch. 24-25-26
Pin 9 ↔ Ch. 27-28-29
Pin 10 ↔ Ch. 30-31-32
Pin 11 ↔ Ch. 33-34-35



Where we initially stood..

∼ 800 p.e. input signal in one injection pin (HG, MG and LG channels)

Signal in the other channels



Identified Cross-talk

1. Diffuse cross-talk (negative), ASIC-wise.

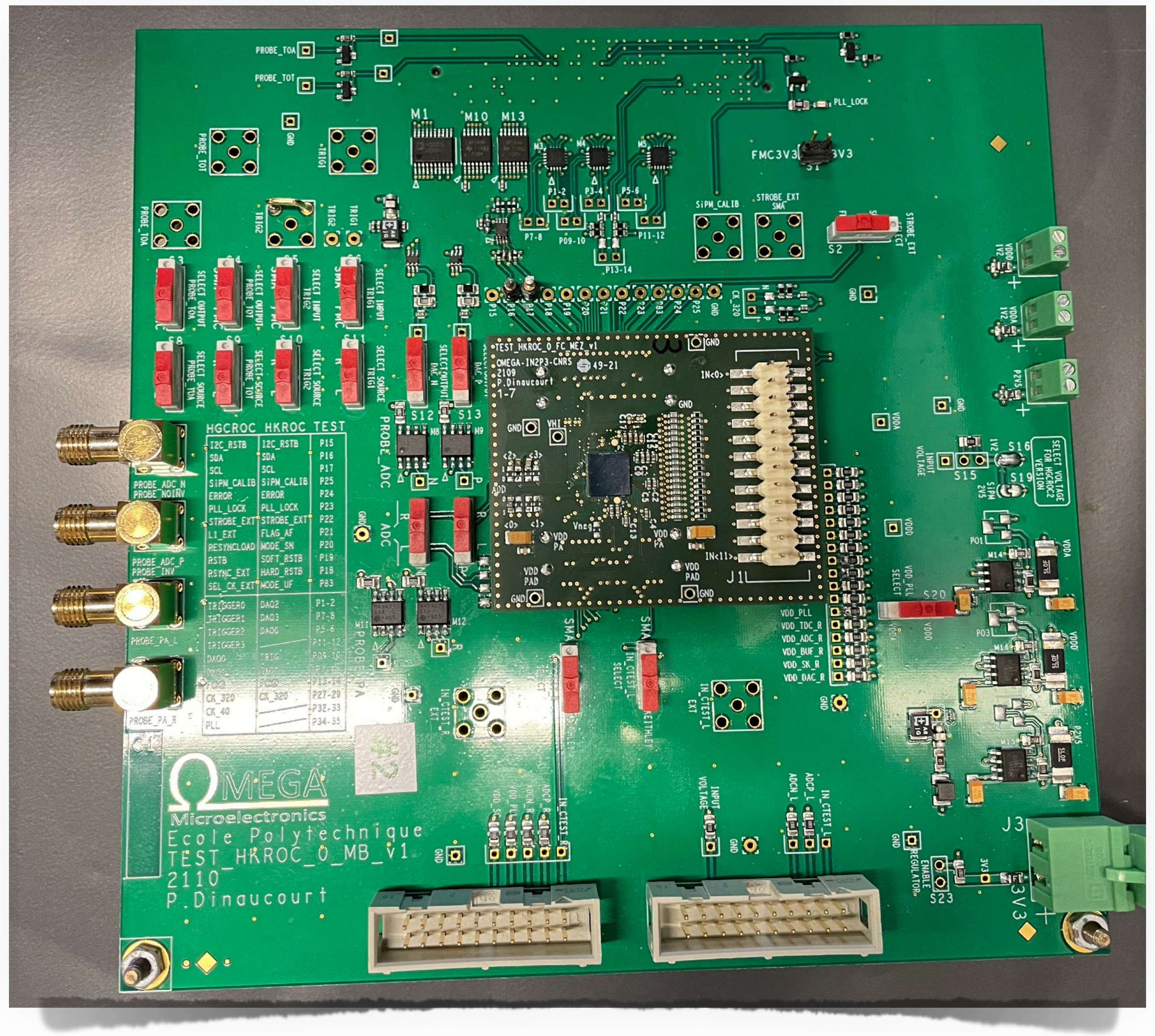
   ✓ Decoupling capacitances added: **HKROC v0** → **HKROC v1b**.

2. Close cross-talk (positive), board-wise.

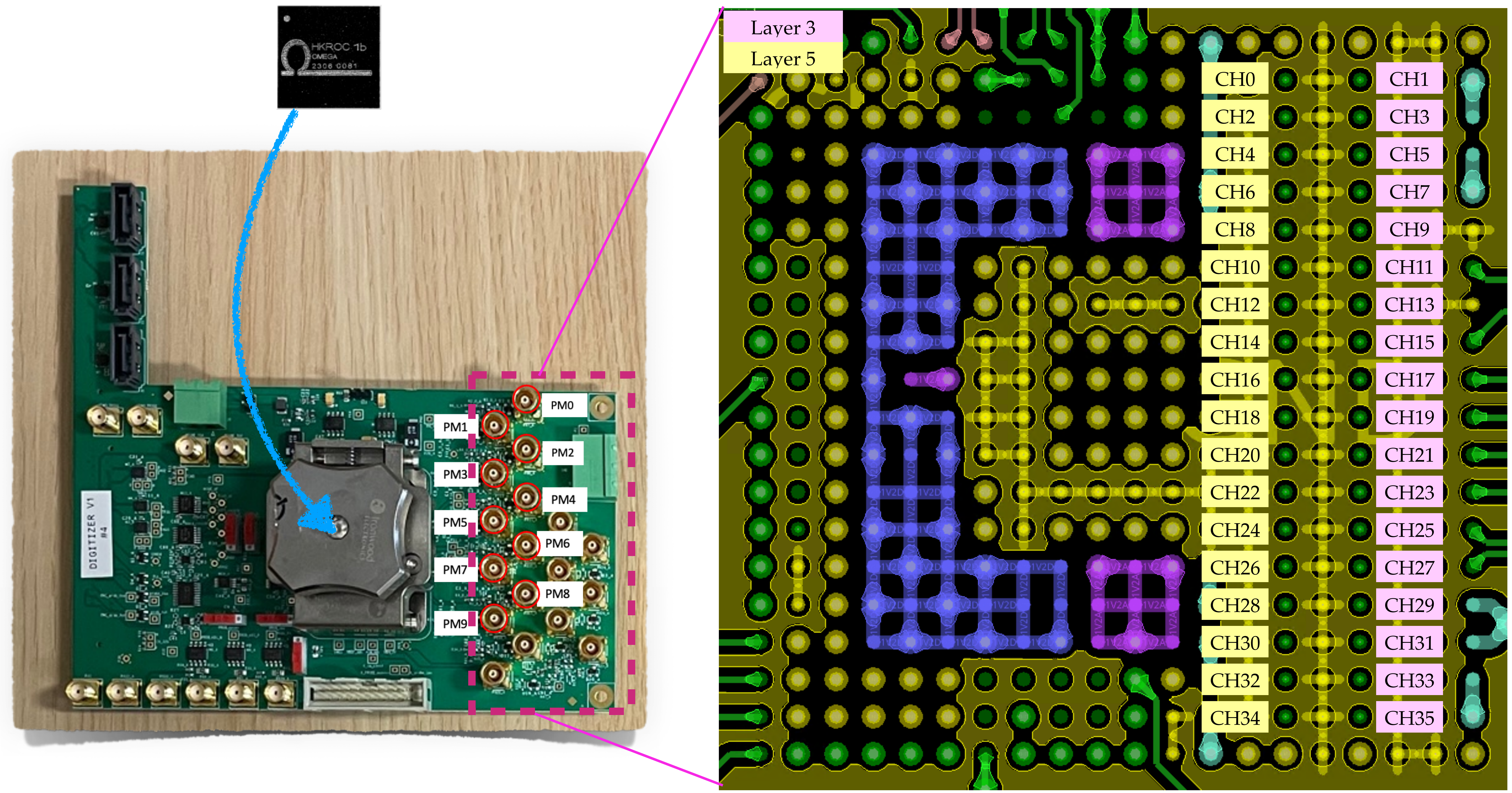
   ✓ **Mezzanine single-layer** daughter board → **BGA multi-layer** mother board.

From Mezzanine to BGA

From single-layer to multi-layer



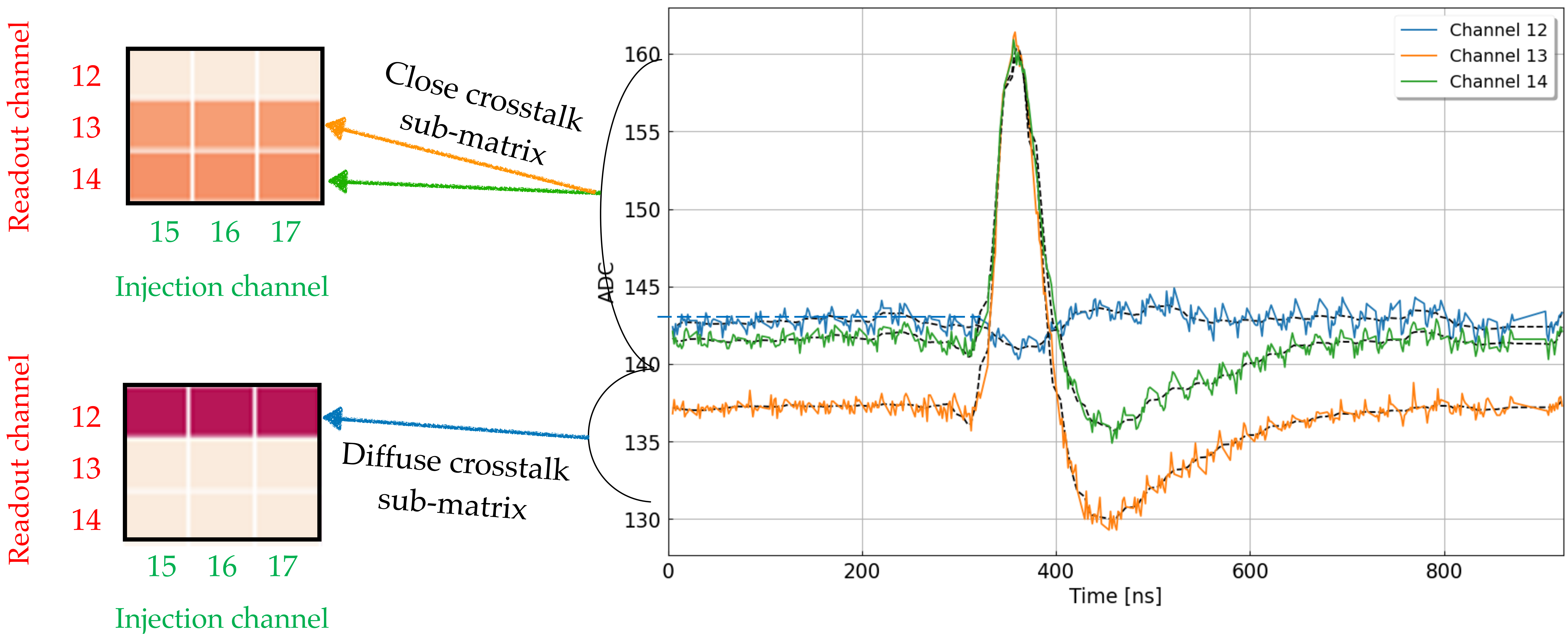
Mezzanine daughter board
on Mother board



BGA mother board

Crosstalk measurements

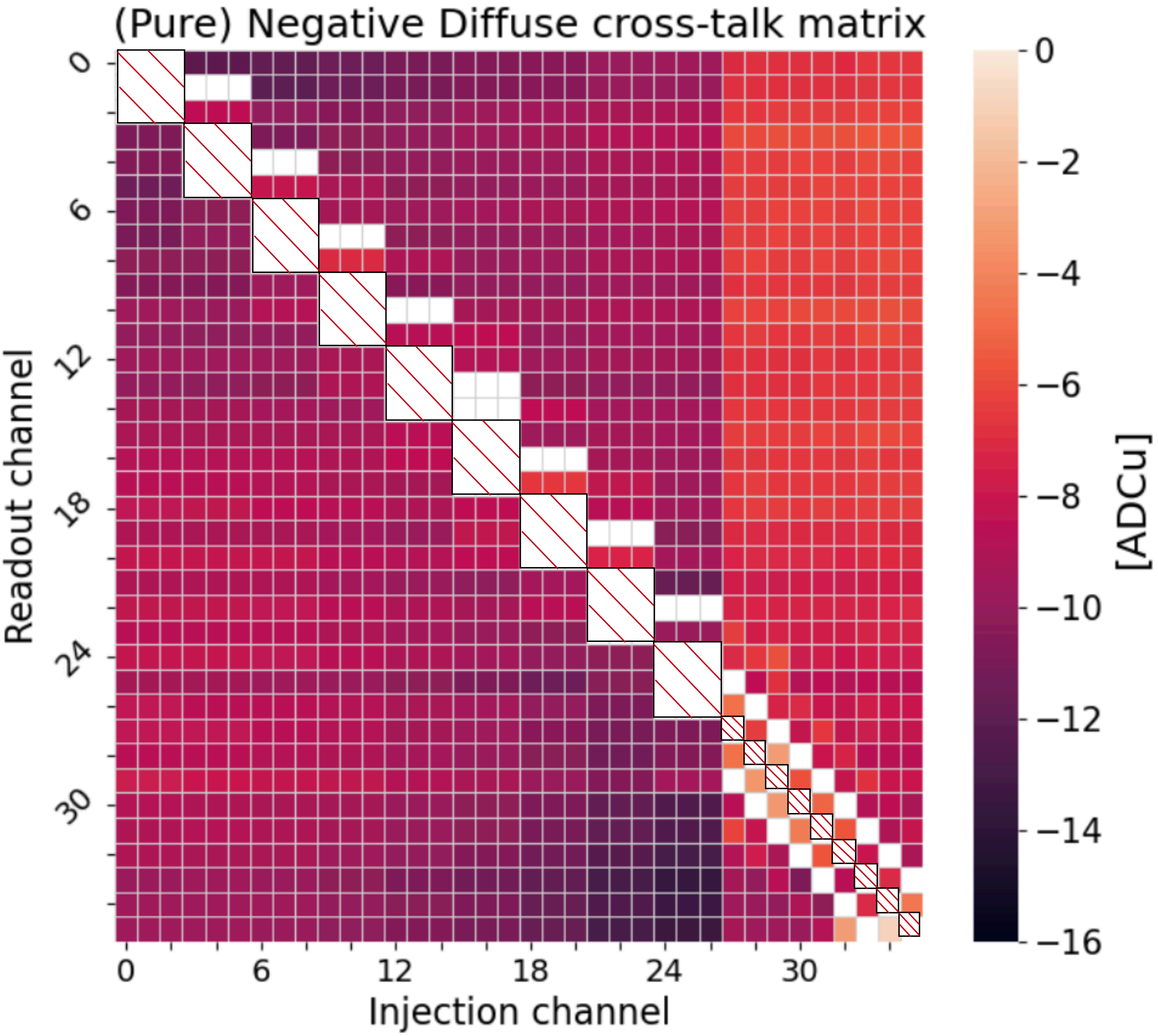
Example (injection in channels 15-16-17)



(Negative) Diffuse Crosstalk Matrices – Board v2 (BGA)

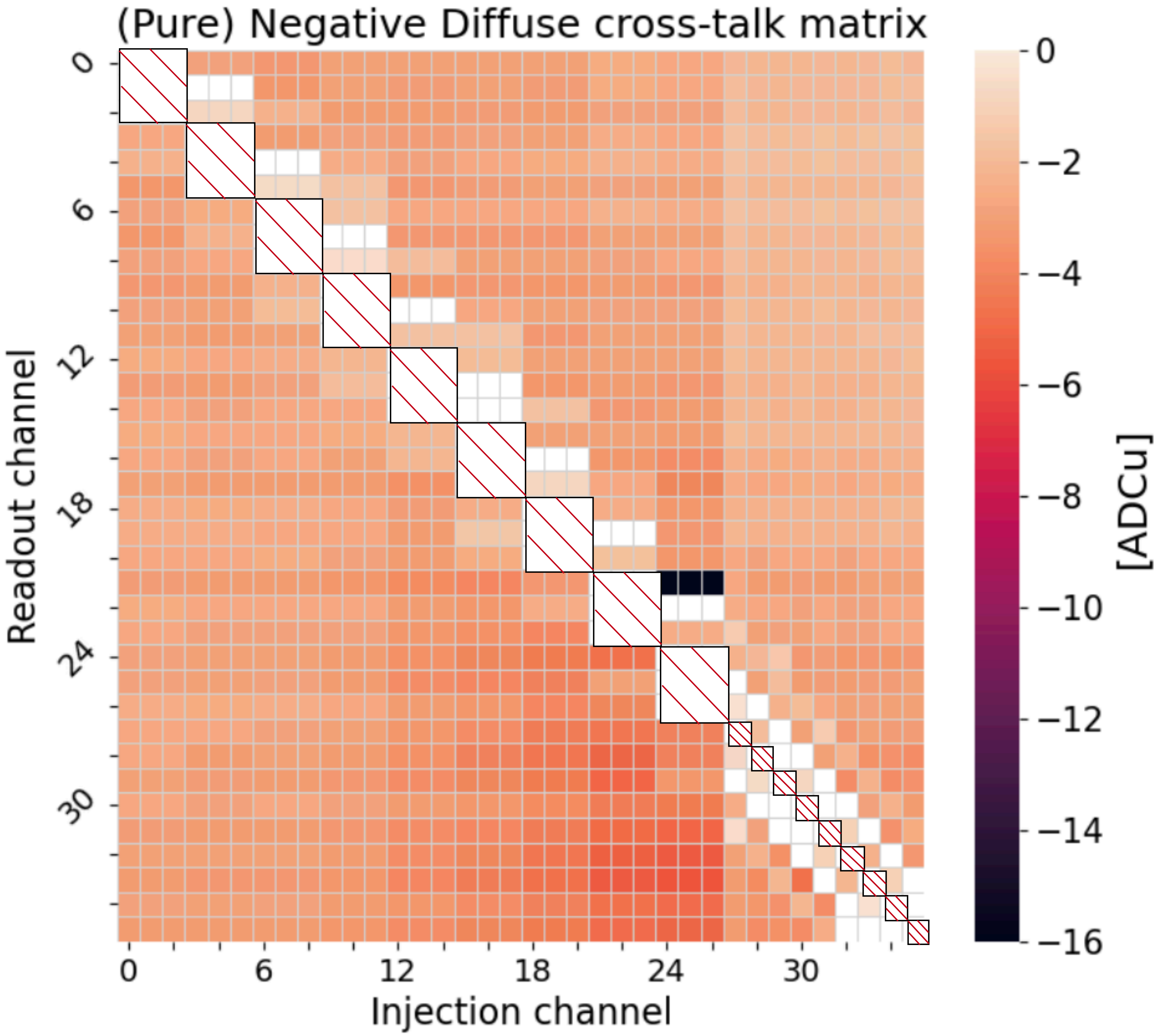
Courtesy of Antoine

HKROC v0



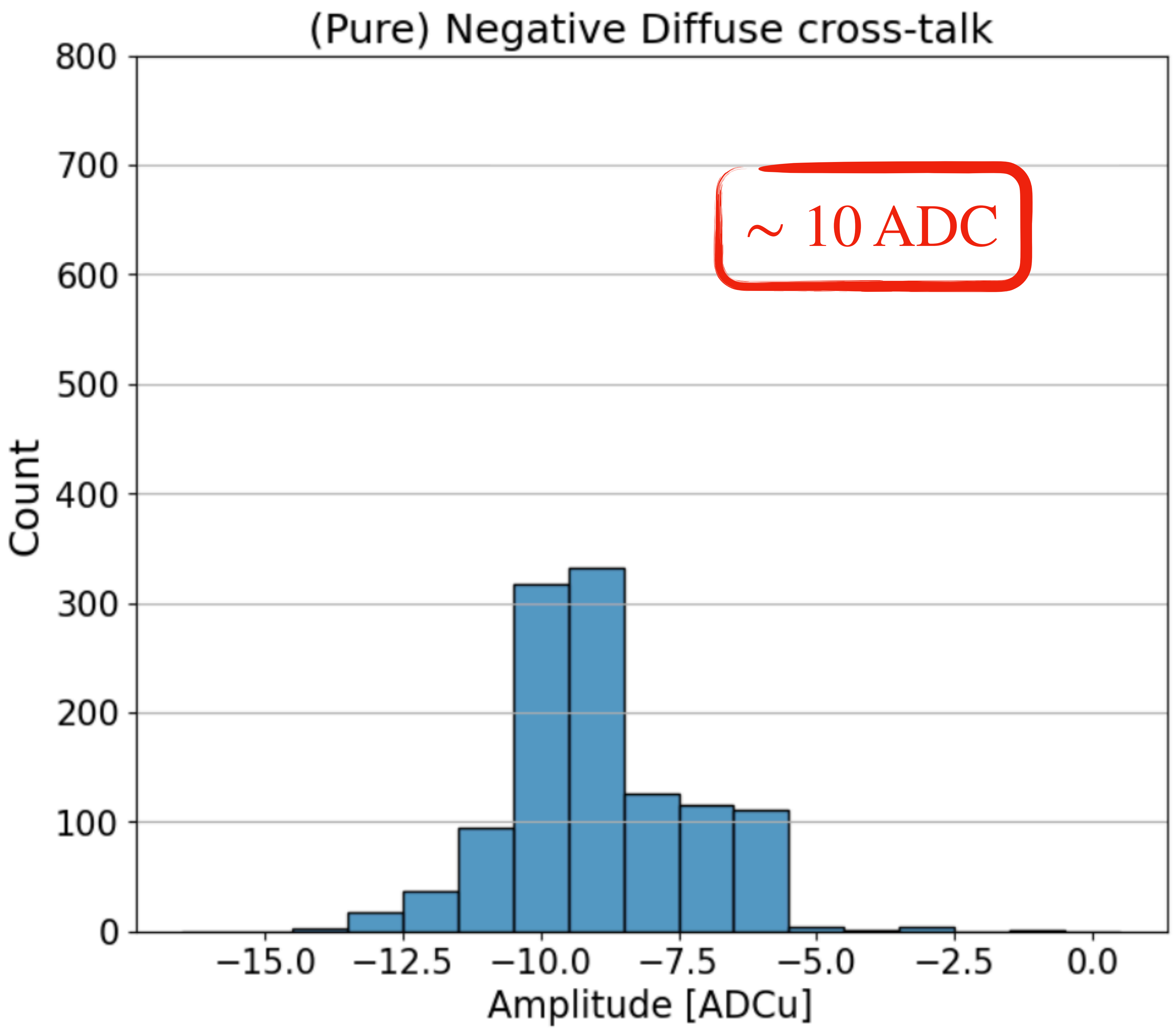
Diffuse XT Reduction from v0 to v1b (ASIC-to-ASIC)

HKROC v1b



(Negative) Diffuse Crosstalk Histograms – Board v2 (BGA)

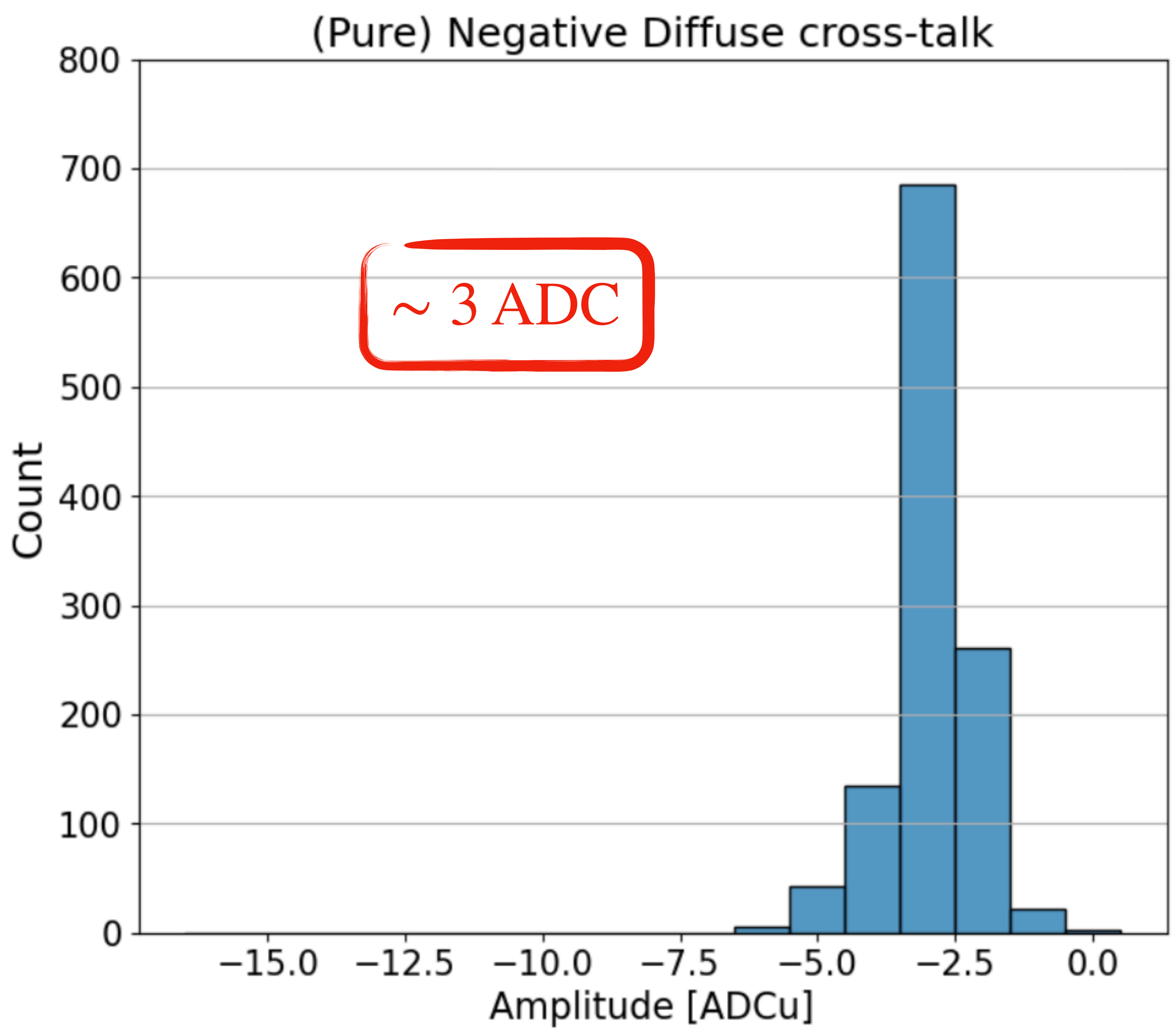
HKROC v0



Diffuse XT Reduction

by a factor ~ 3

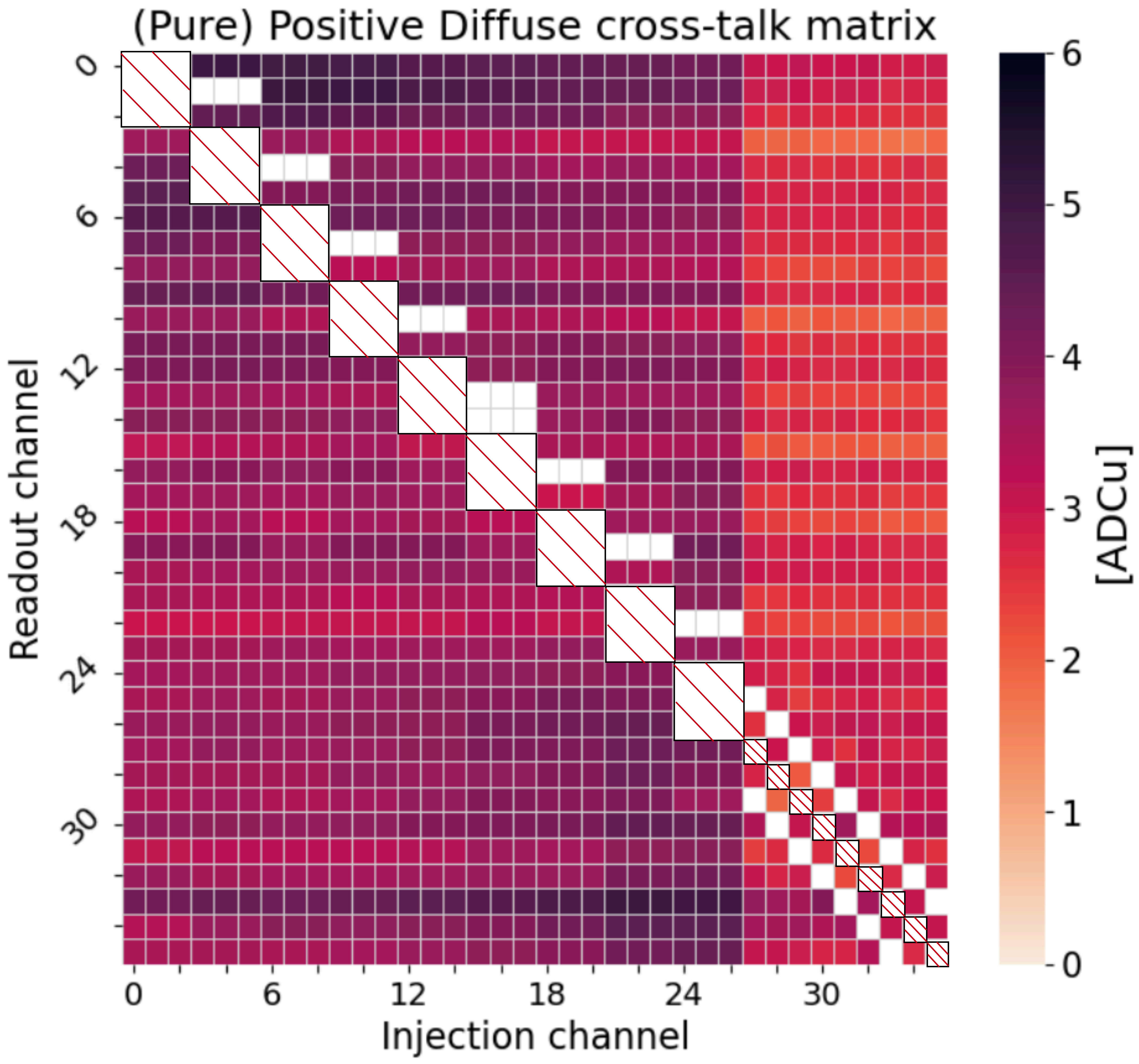
HKROC v1b



From HKROC v0 → v1b: **Factor ~ 3 reduction** of neg. diffuse cross-talk.

(Positive) Diffuse Crosstalk Matrices – Board v2 (BGA)

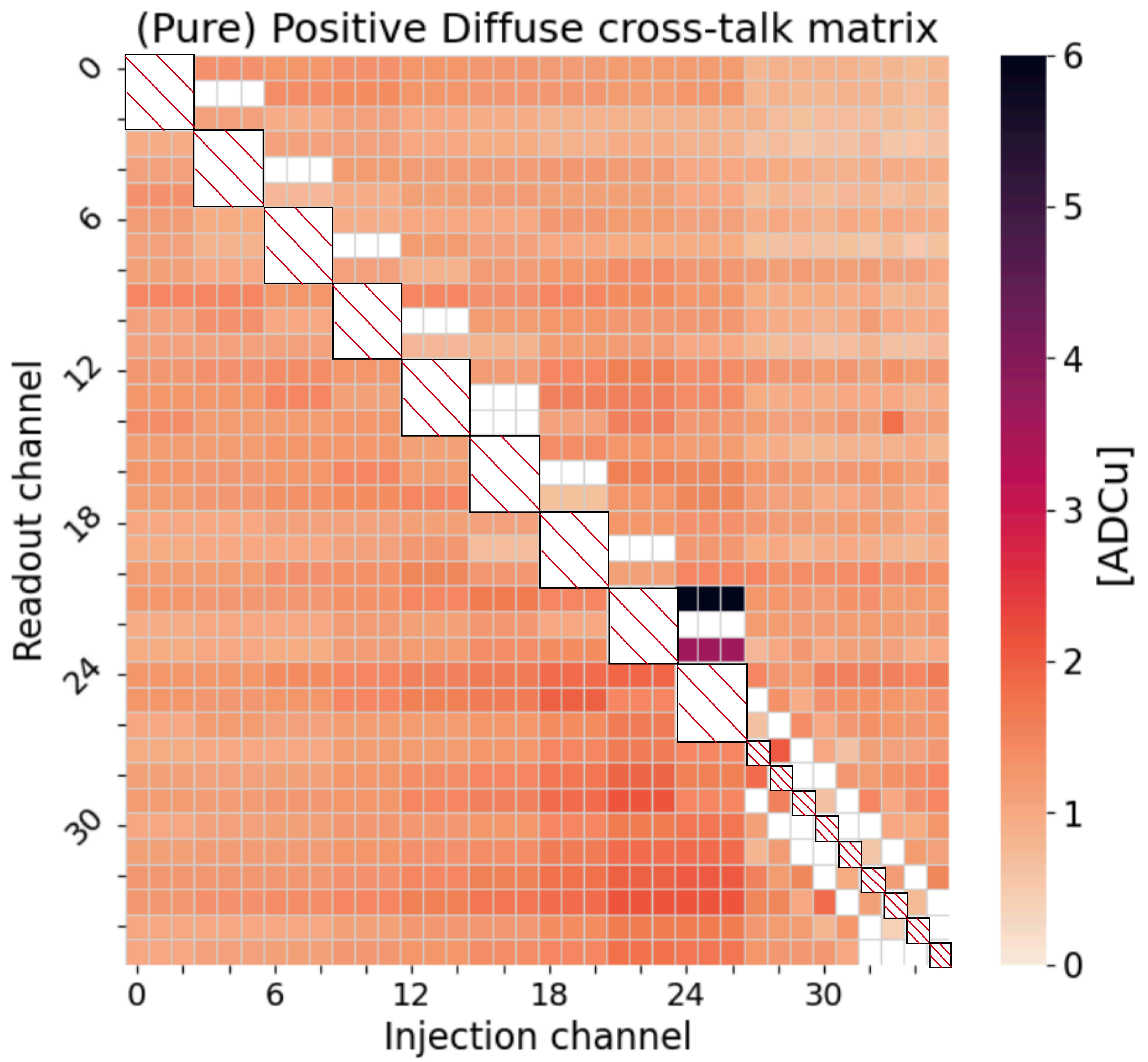
HKROC v0



Diffuse XT Reduction

from v0 to v1b (ASIC-to-ASIC)

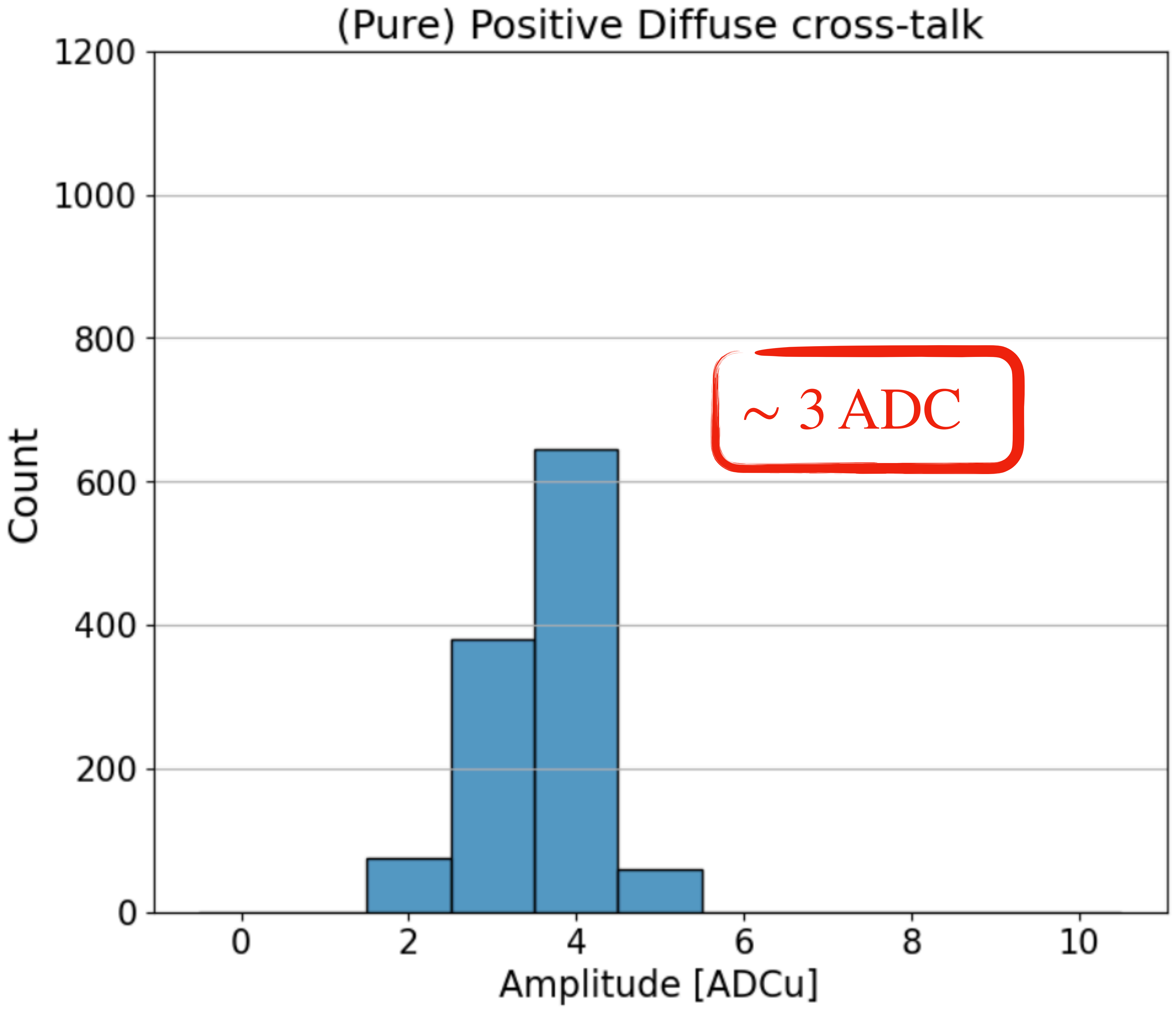
HKROC v1b



Diffuse Crosstalk Reduction

(Positive) Diffuse Crosstalk Histograms – Board v2 (BGA)

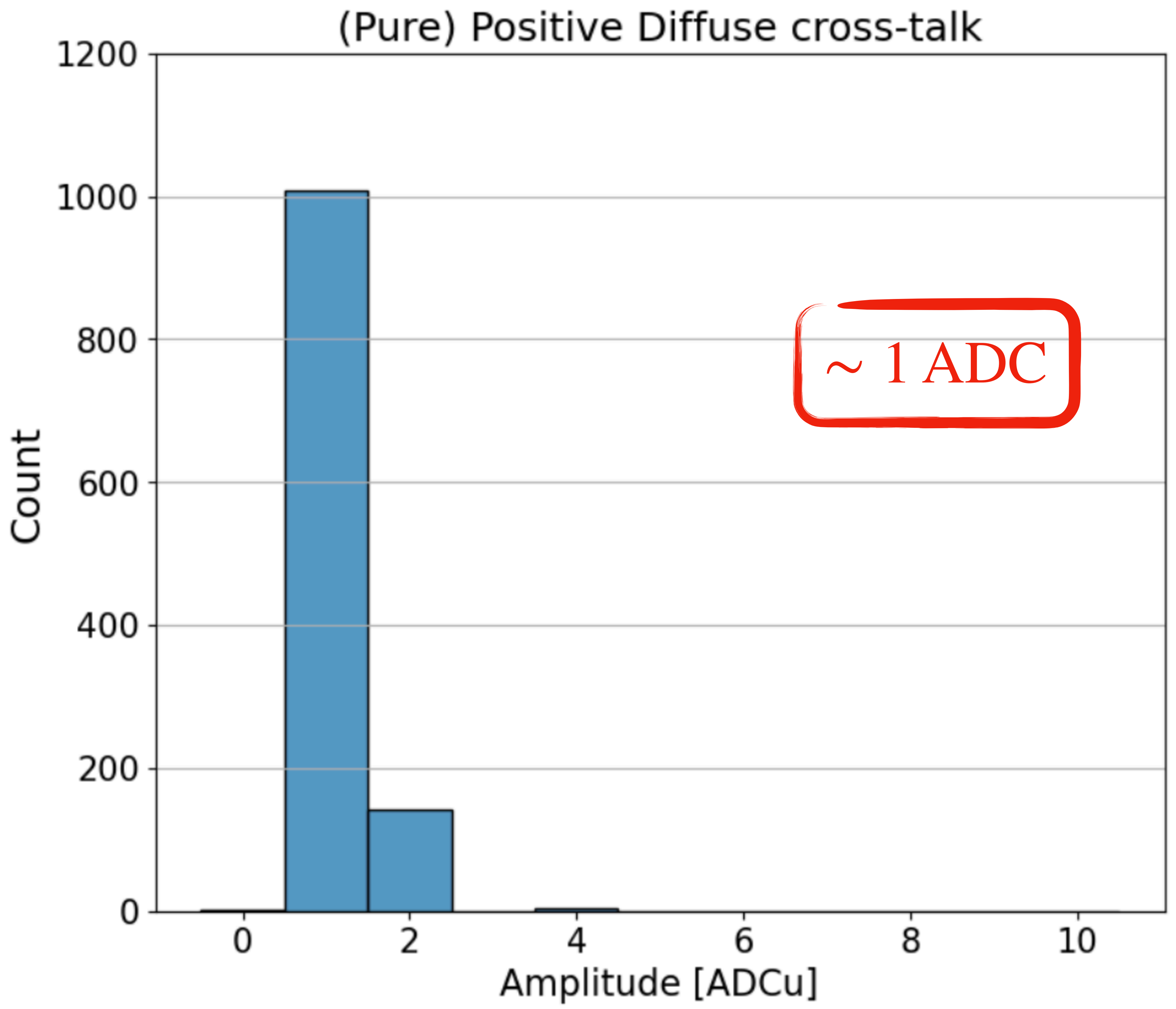
HKROC v0



Diffuse XT Reduction

by a factor ~ 3

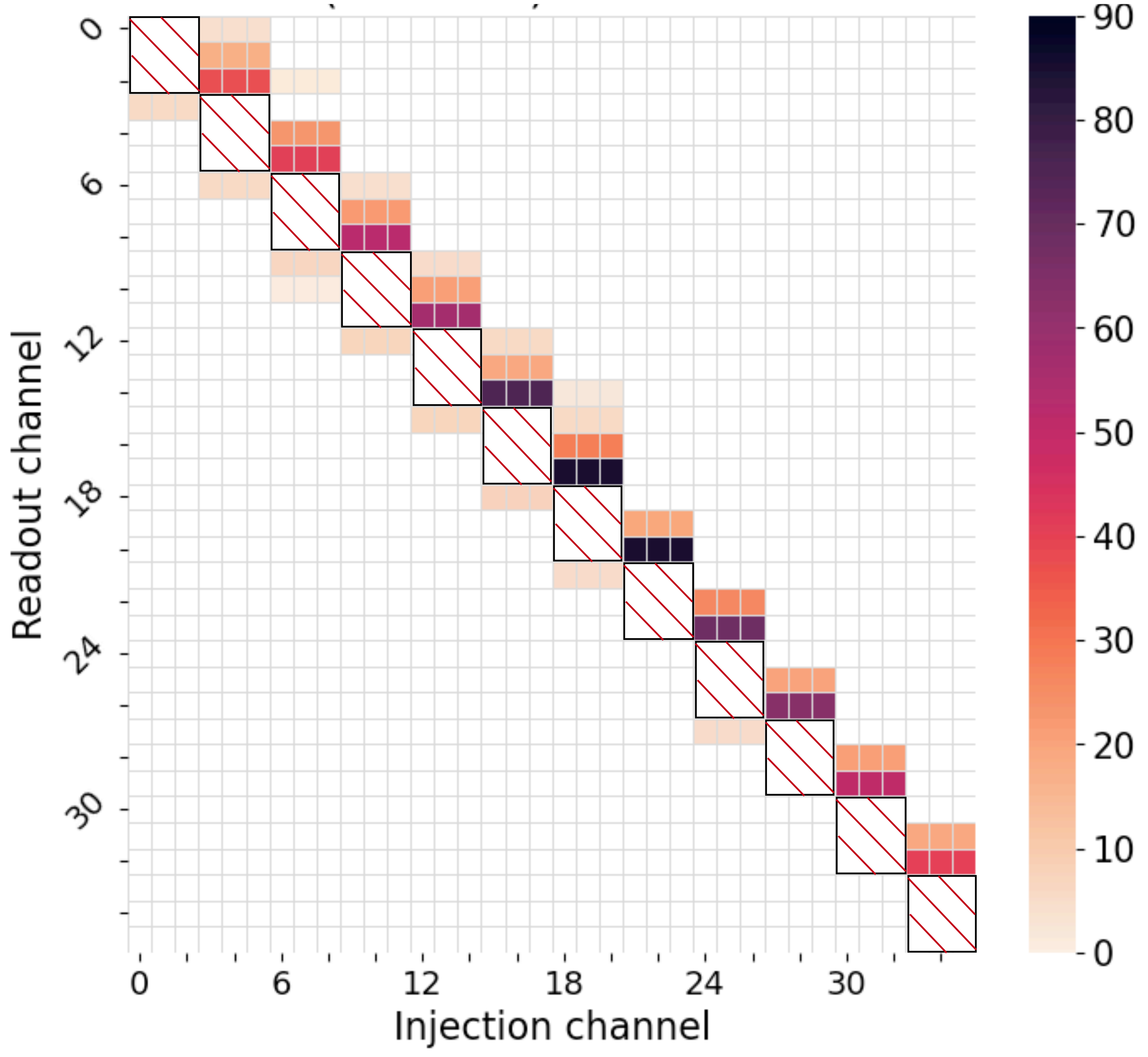
HKROC v1b



From HKROC v0 → v1b: **Factor ~ 3 reduction** of pos. diffuse cross-talk (~1/15 p.e. on HG).

Close Crosstalk Matrices - HKROC v1b

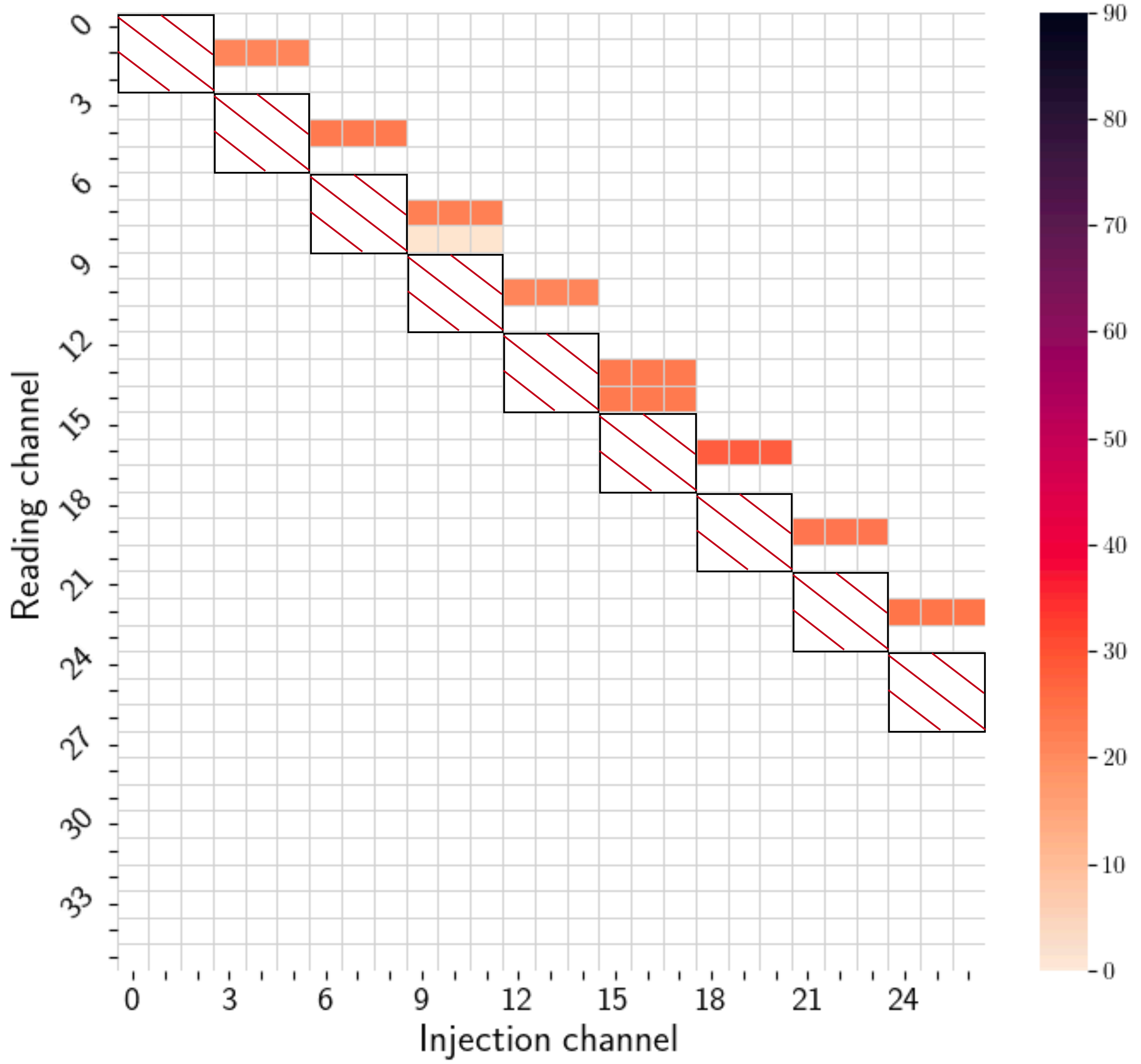
Board v1 (Mezzanine) [ADC units]



Close XT Reduction

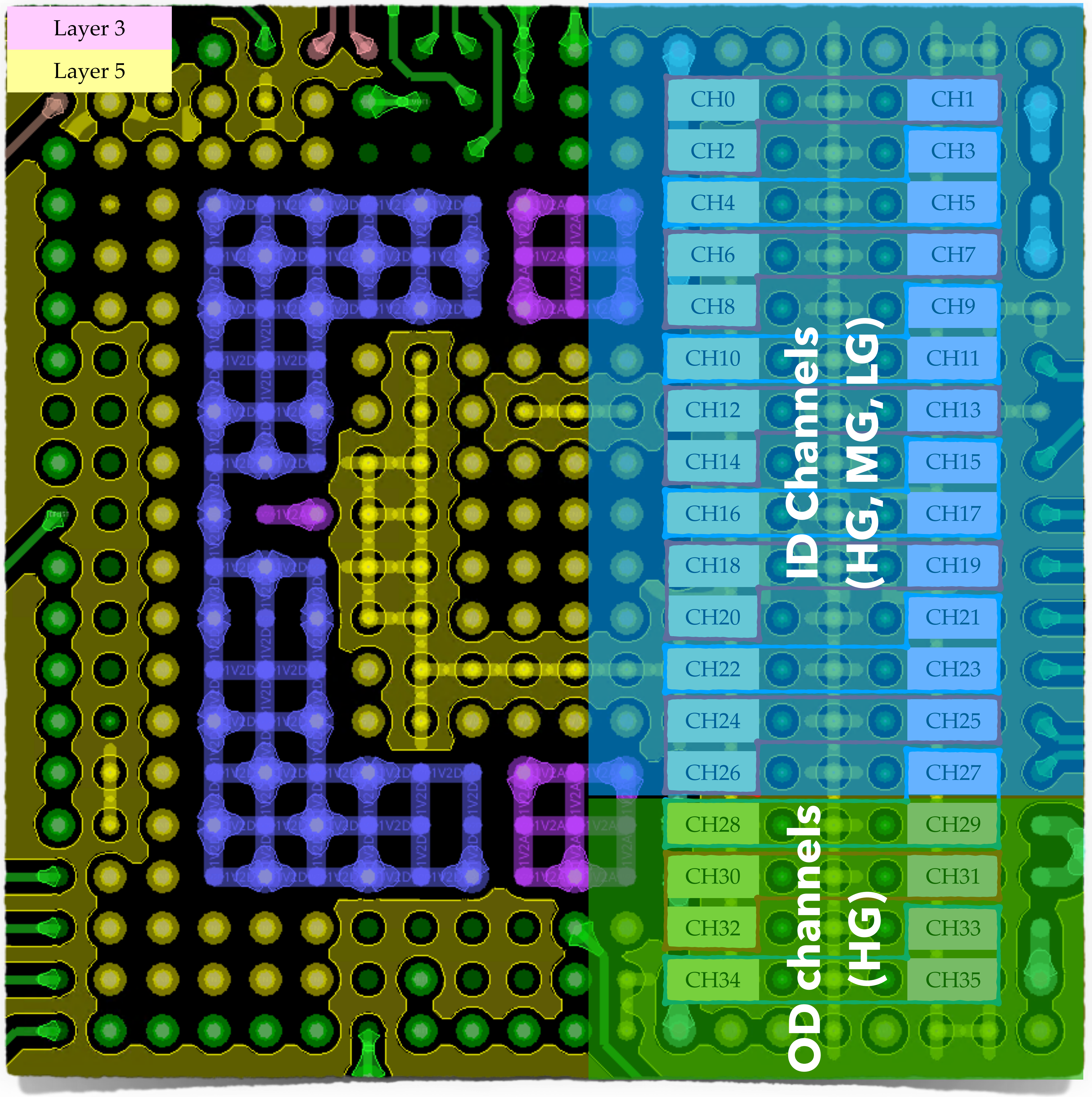
from v1 to v2 (board-to-board)

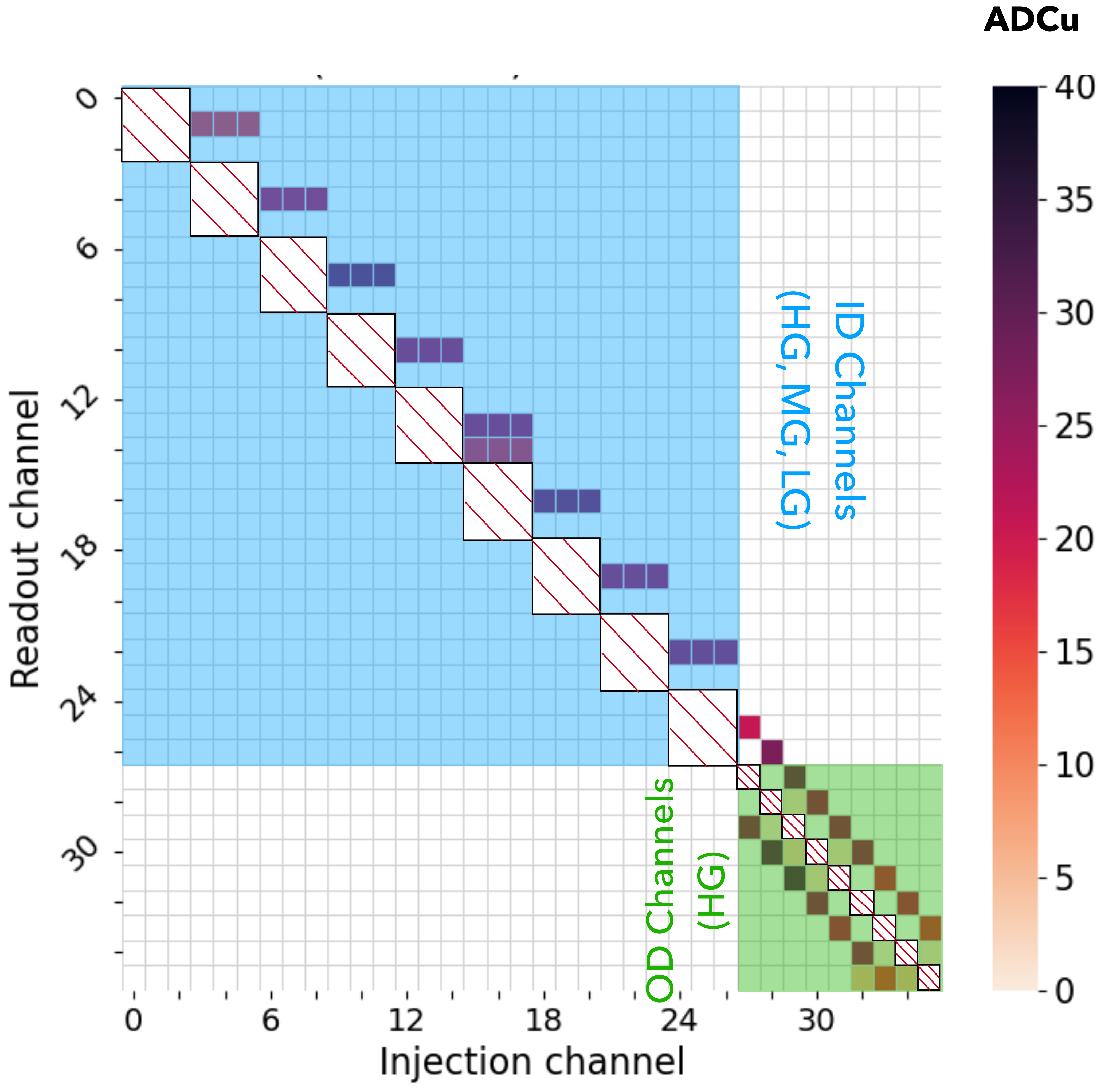
Board v2 (BGA) [ADC units]



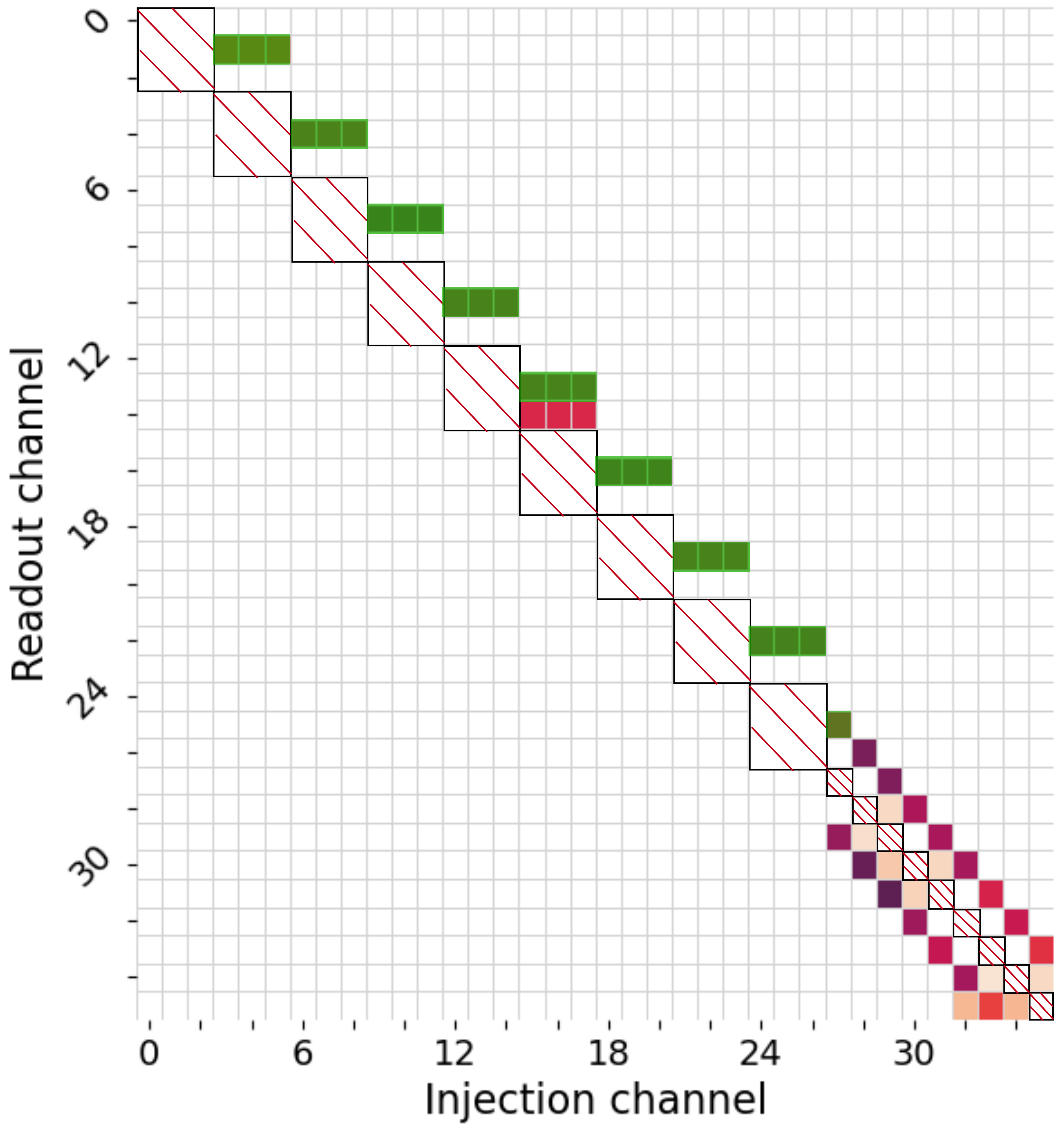
From Board v1 → v2: **Suppression** of the close cross-talk :

HG ch.⟶ HG + LG ch.

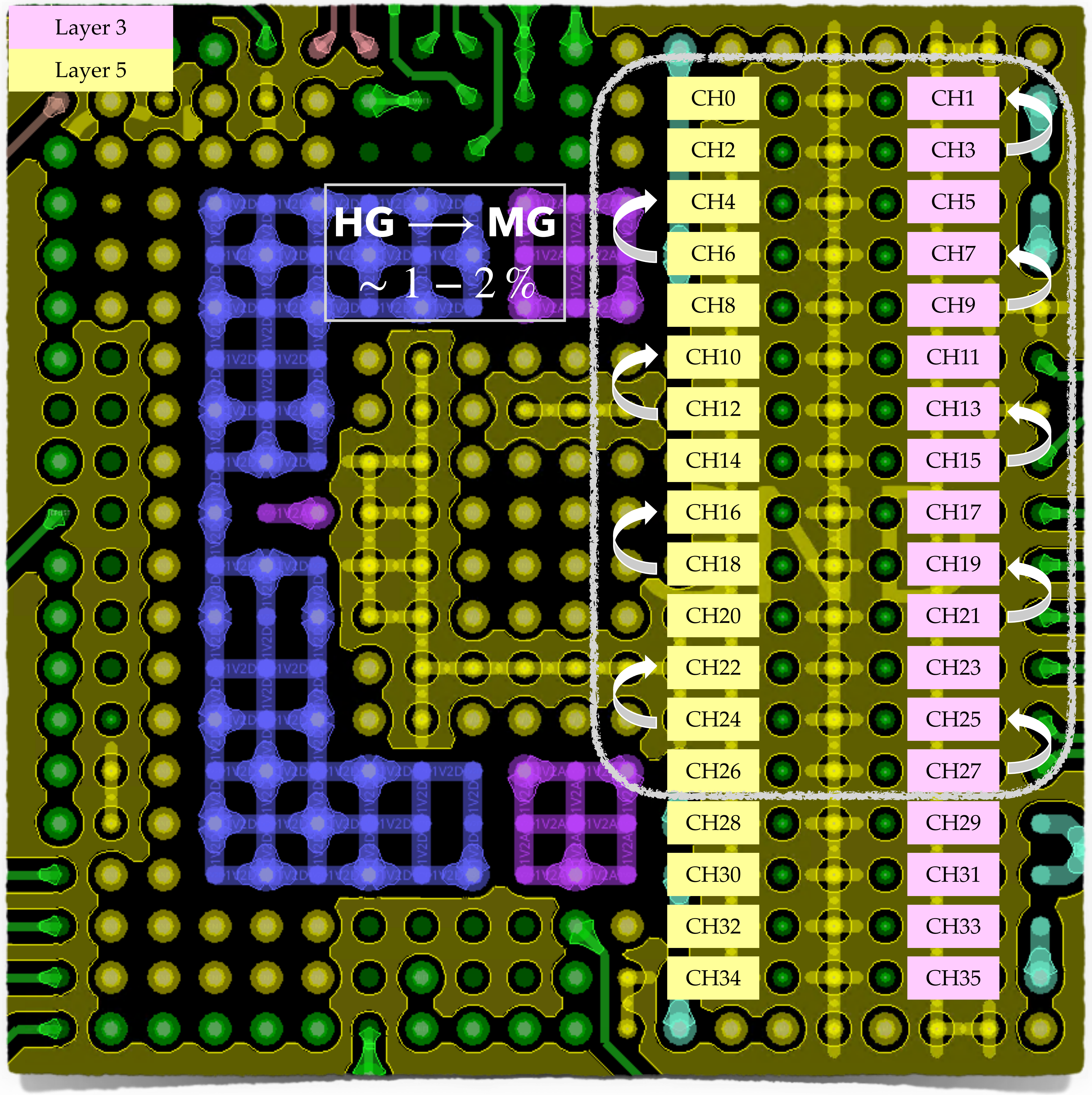

Layer 3
Layer 5
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
CH9
CH10
CH11
CH12
CH13
CH14
CH15
CH16
CH17
CH18
CH19
CH20
CH21
CH22
CH23
CH24
CH25
CH26
CH27
CH28
CH29
CH30
CH31
CH32
CH33
CH34
CH35
ID Channels (HG, MG, LG)
OD channels (HG)


ADCu
40
35
30
25
20
15
10
5
0
Readout channel
Injection channel
0
6
12
18
24
30
ID Channels (HG, MG, LG)
OD Channels (HG)

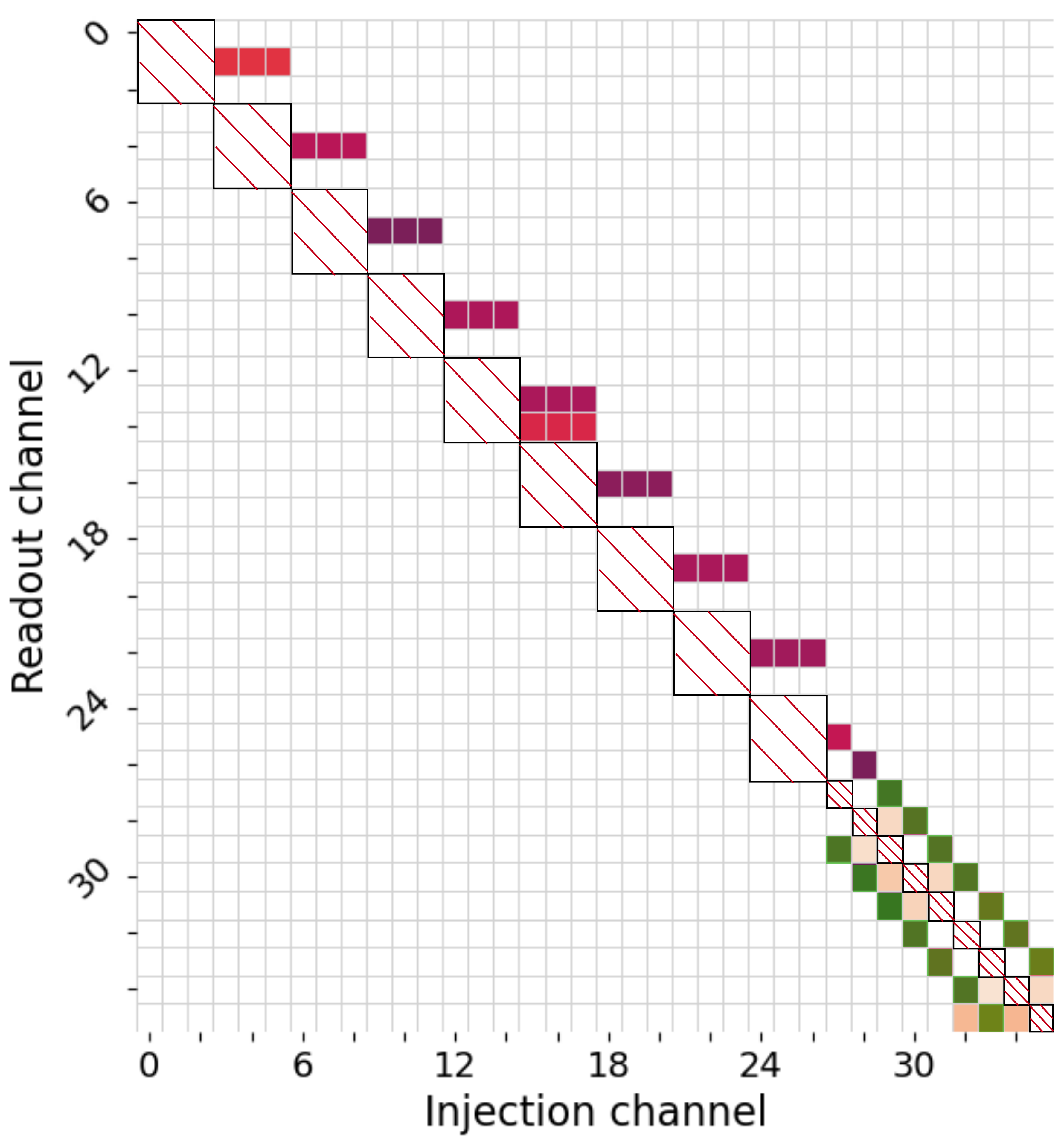
Close Crosstalk Matrix



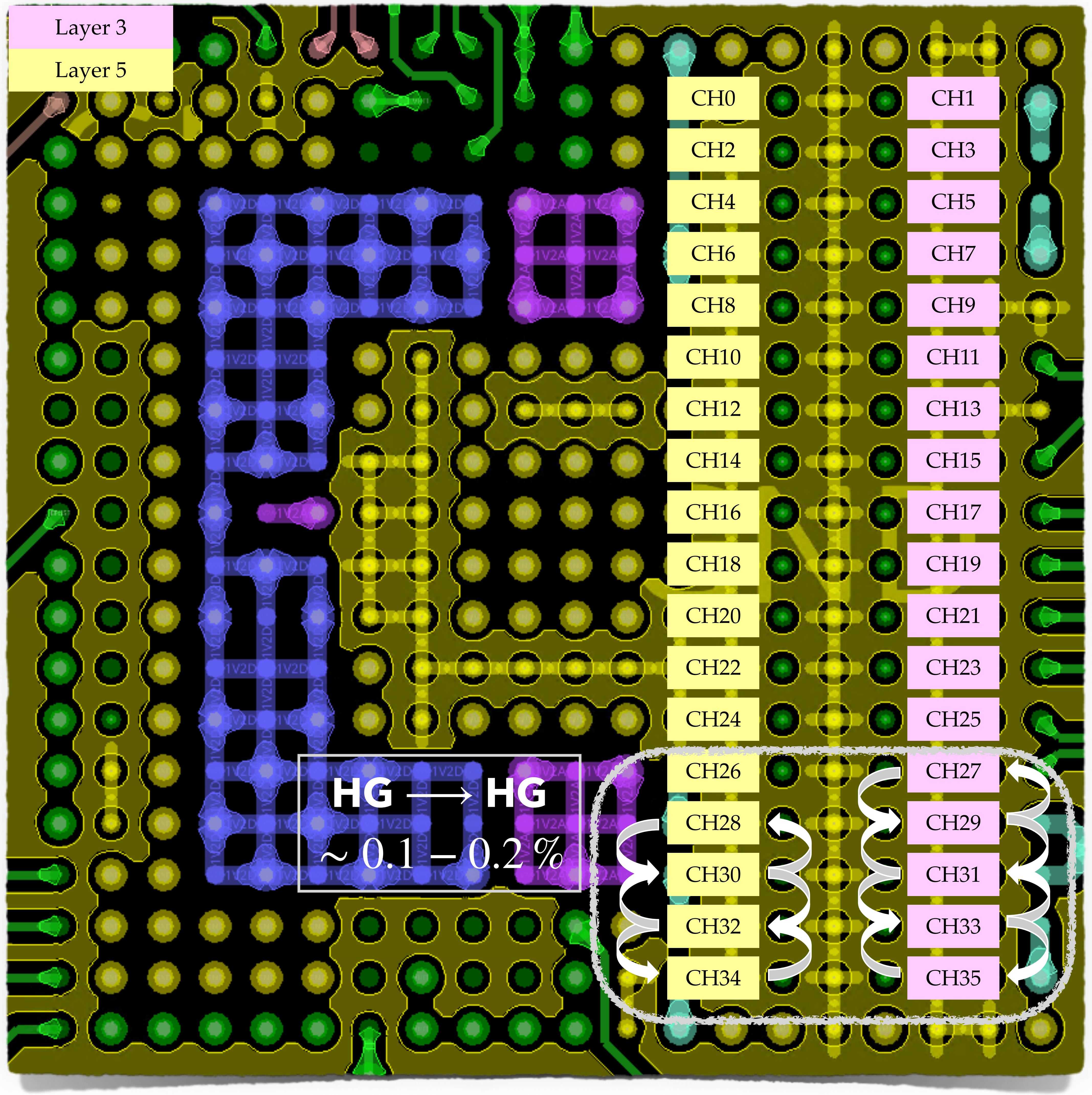
Expected in-layer cross-talk



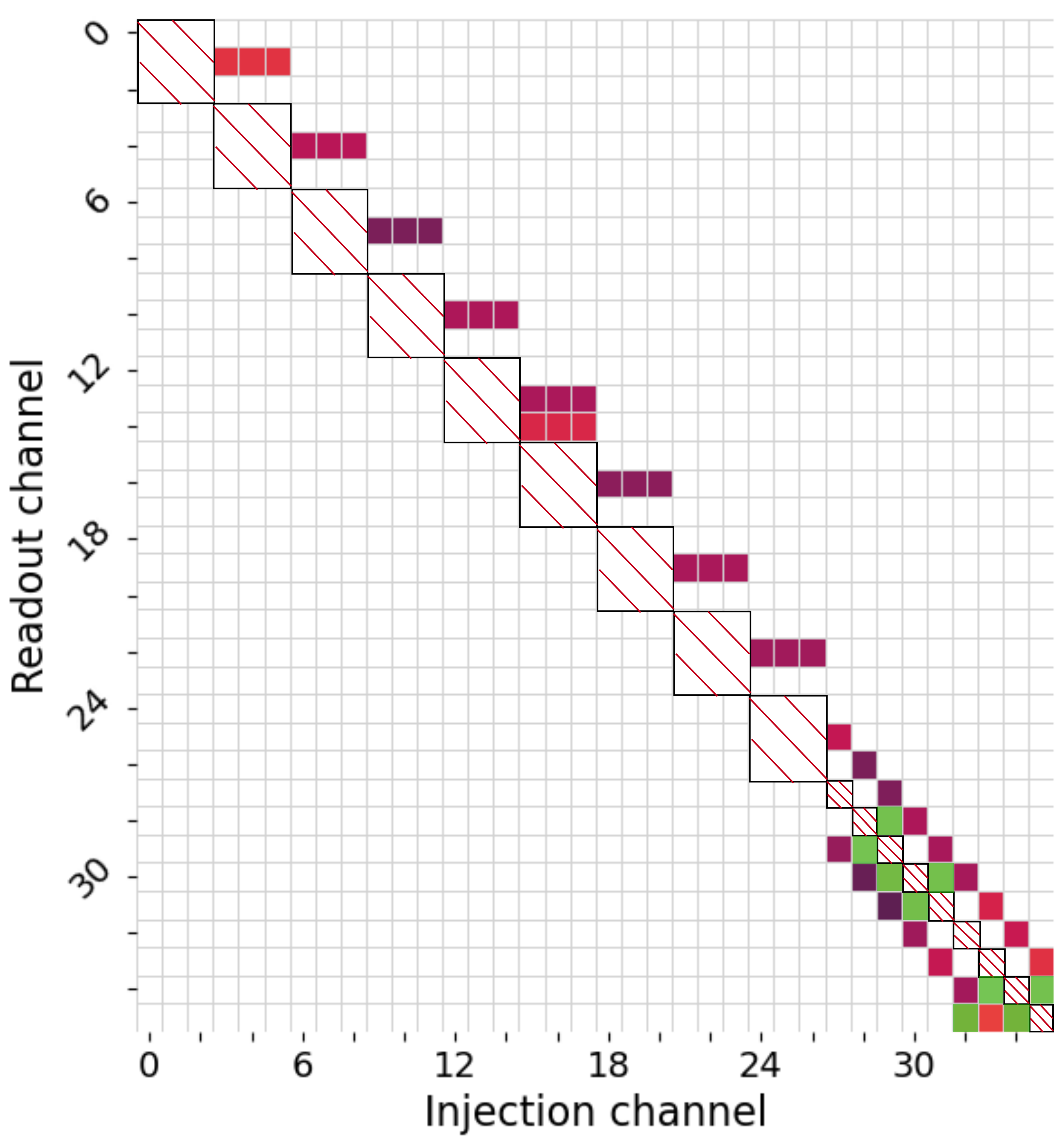
Close Crosstalk Matrix



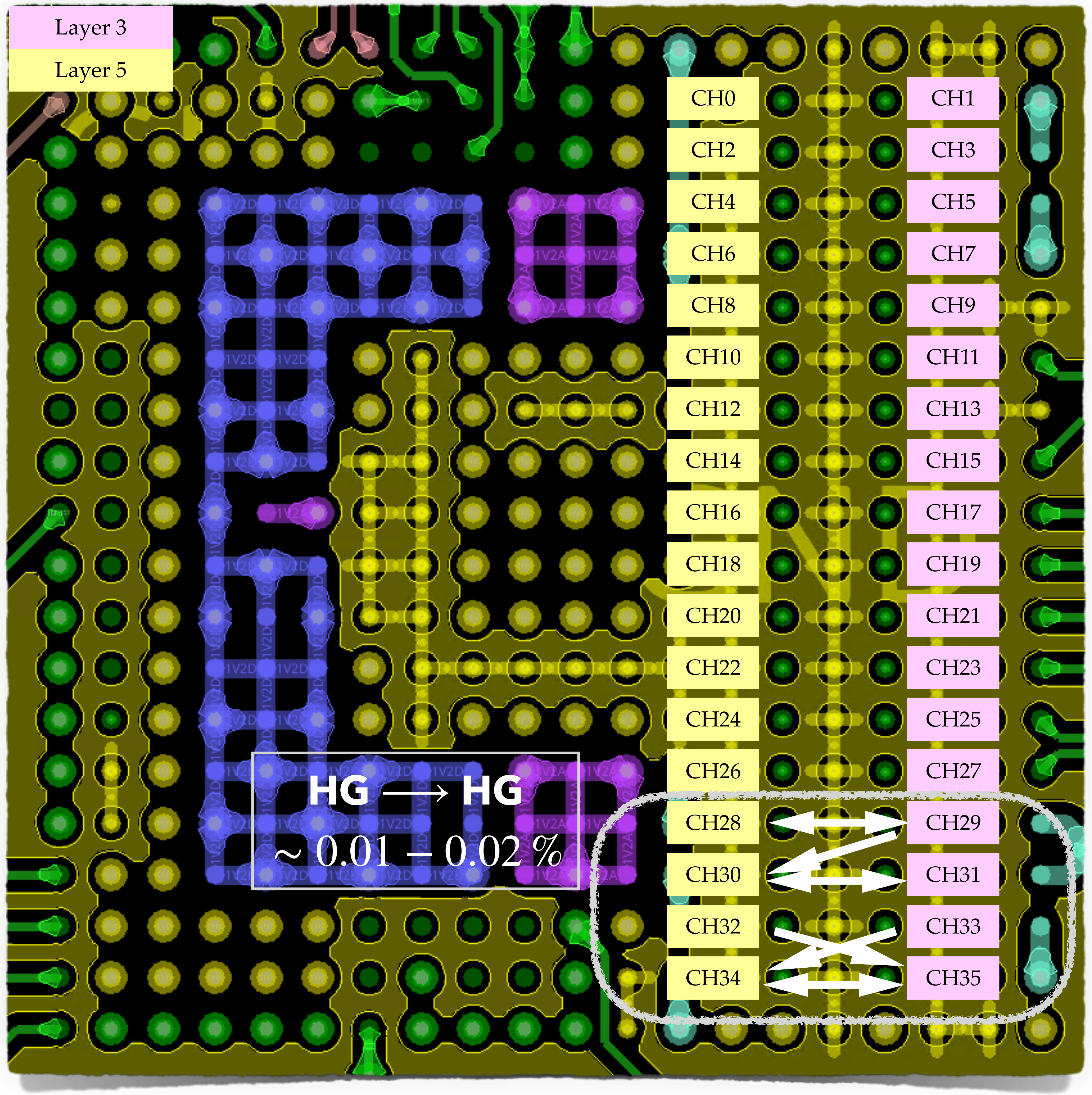
Expected in-layer cross-talk



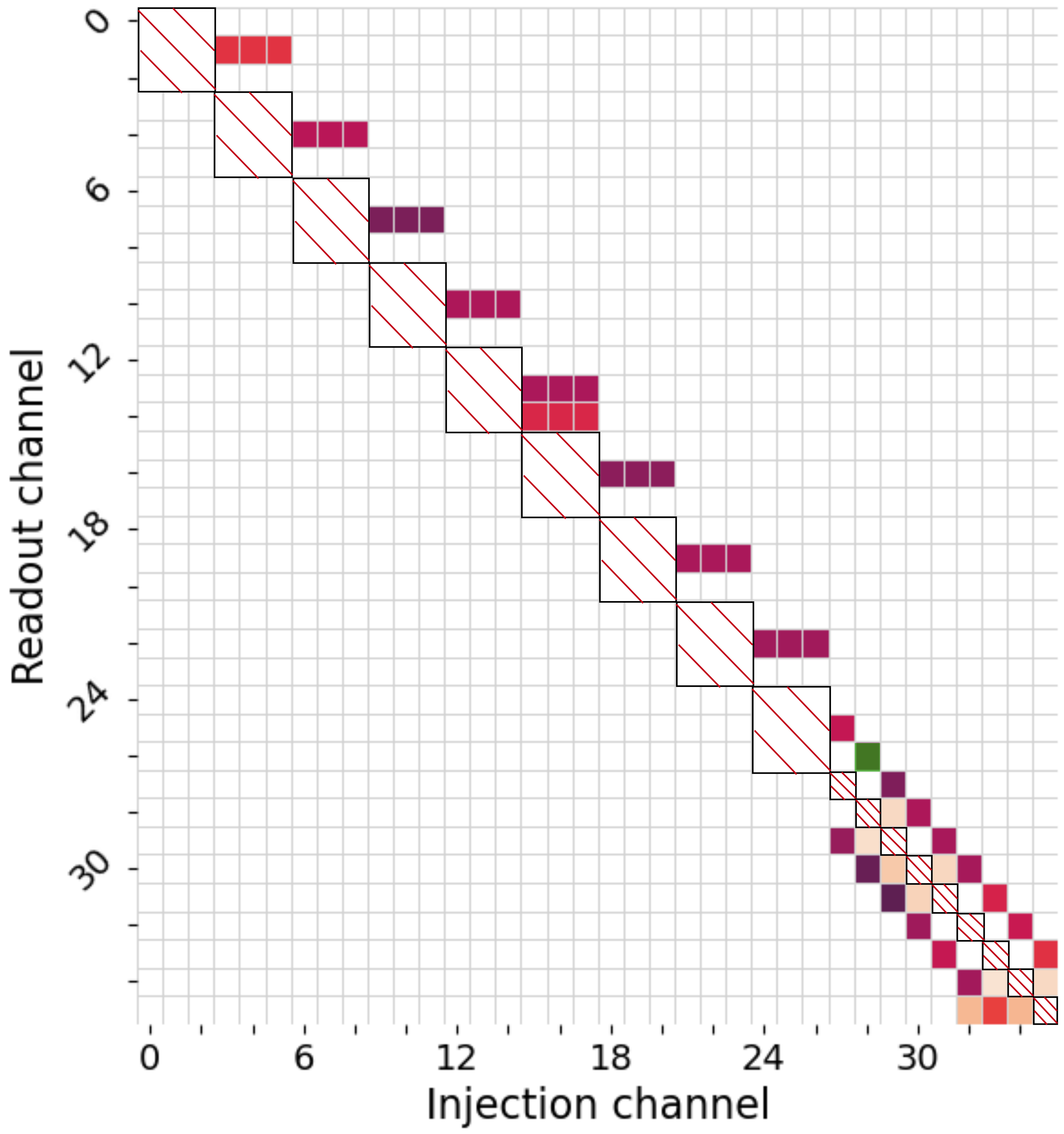
Close Crosstalk Matrix



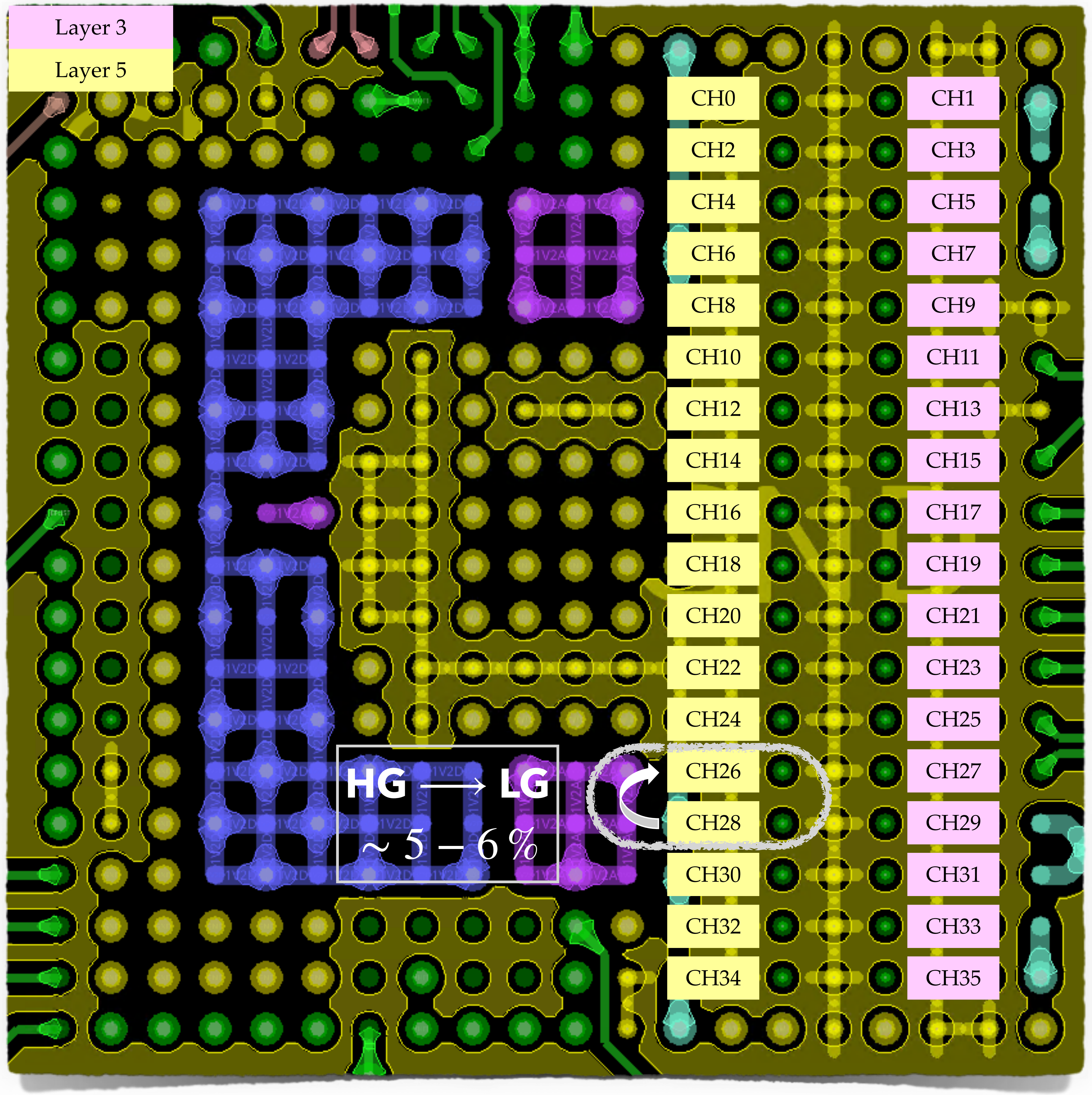
Abnormal cross-layer cross-talk



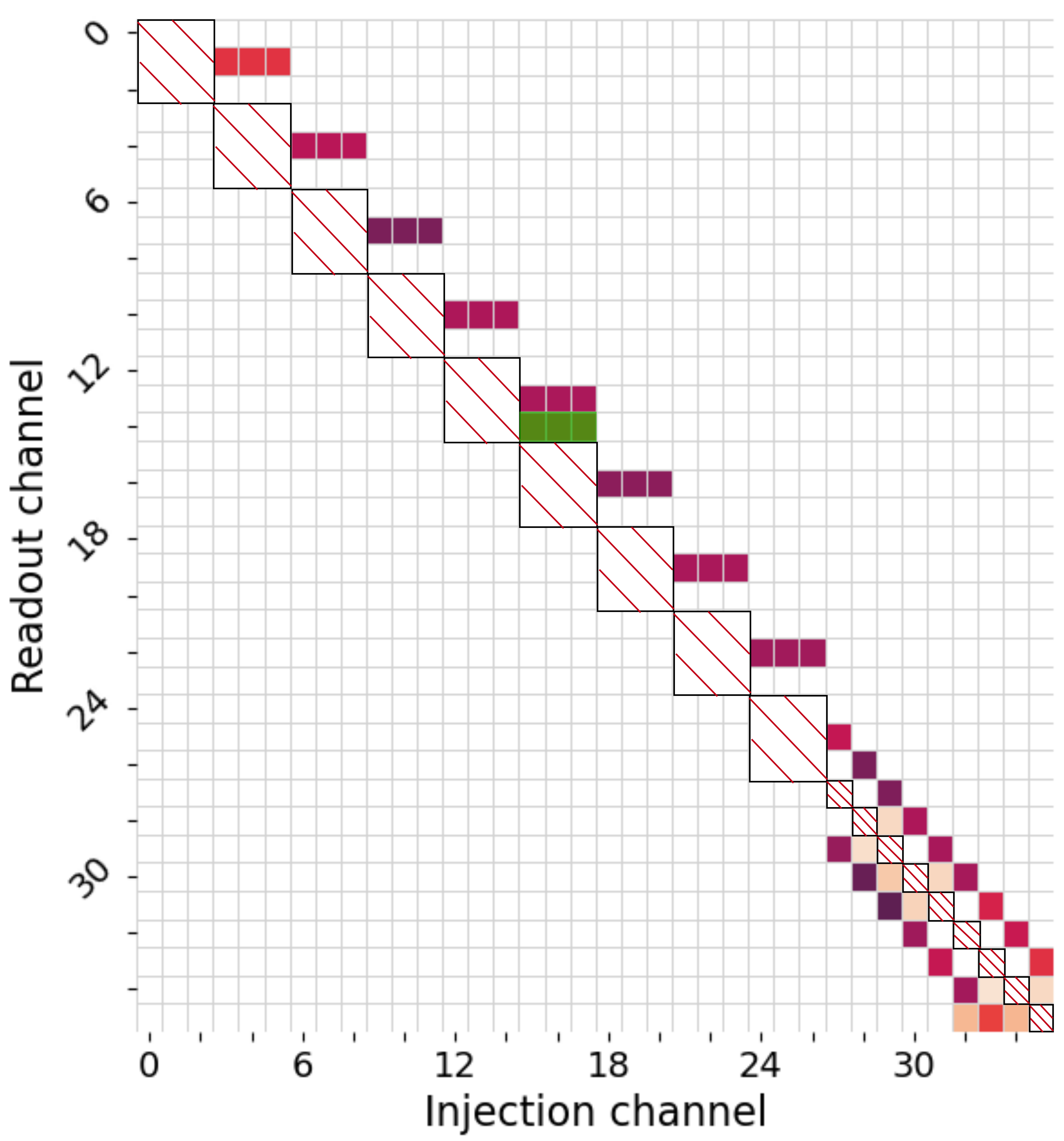
Close Crosstalk Matrix

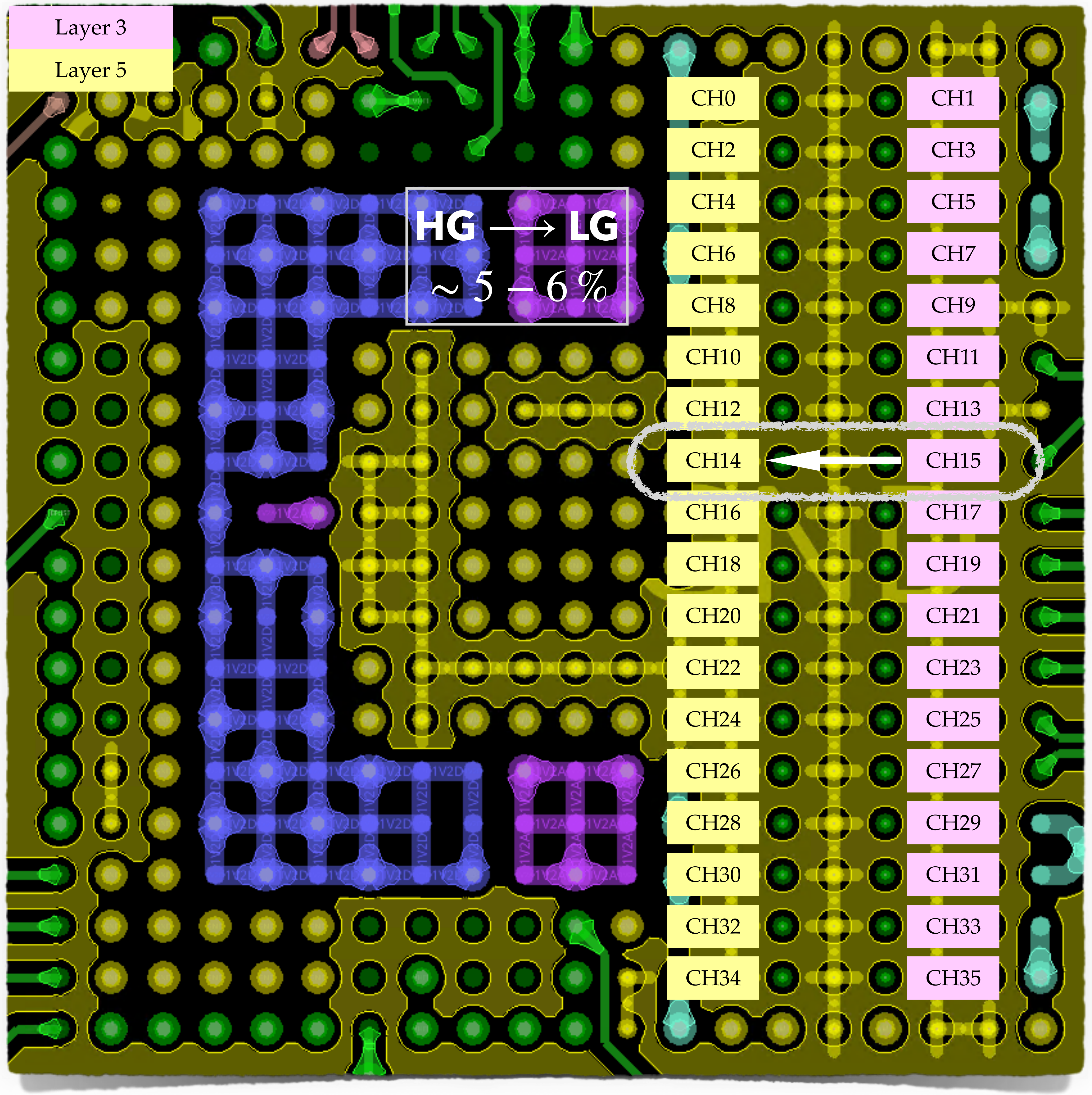


High in-layer cross-talk



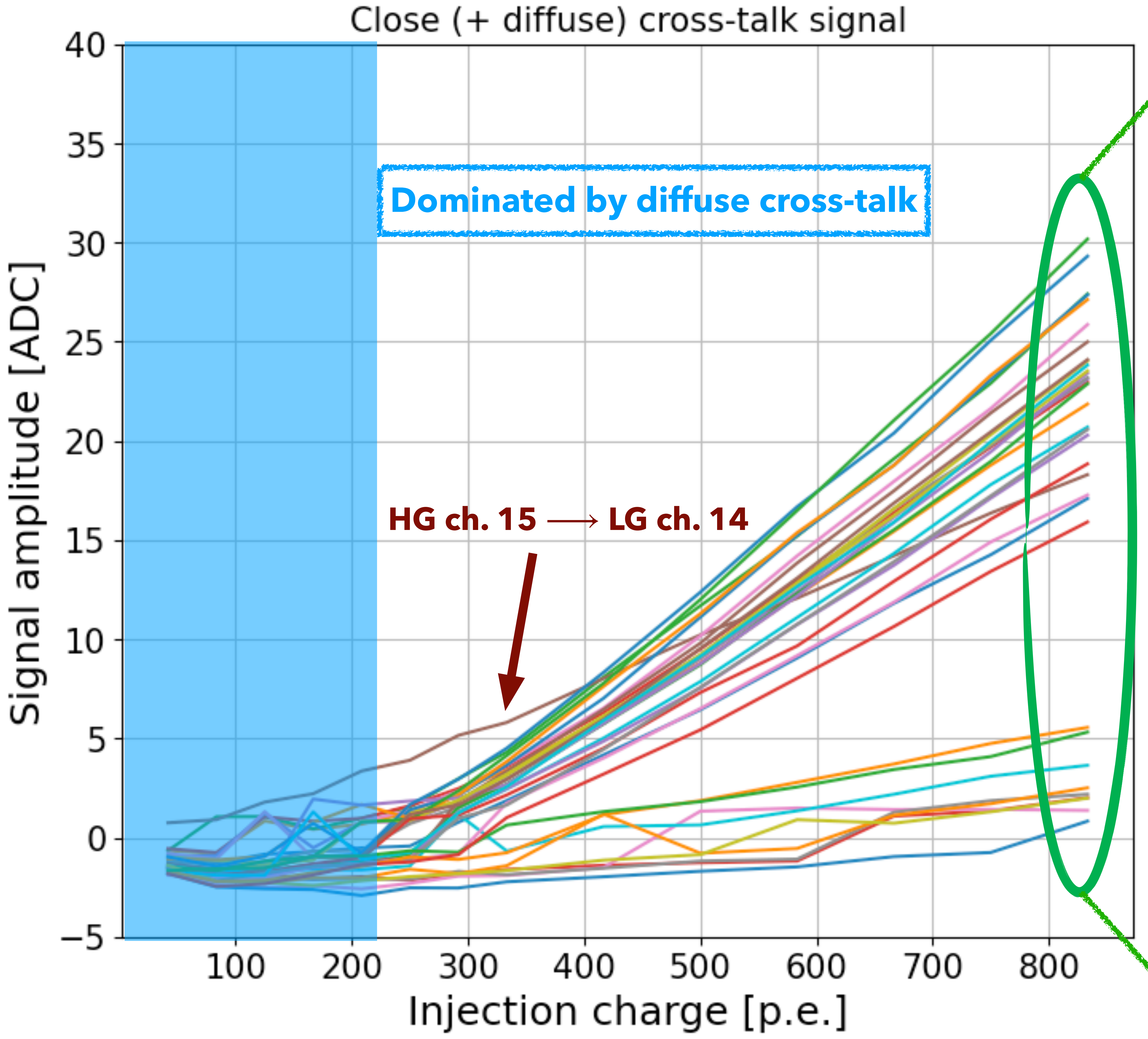
Close Crosstalk Matrix

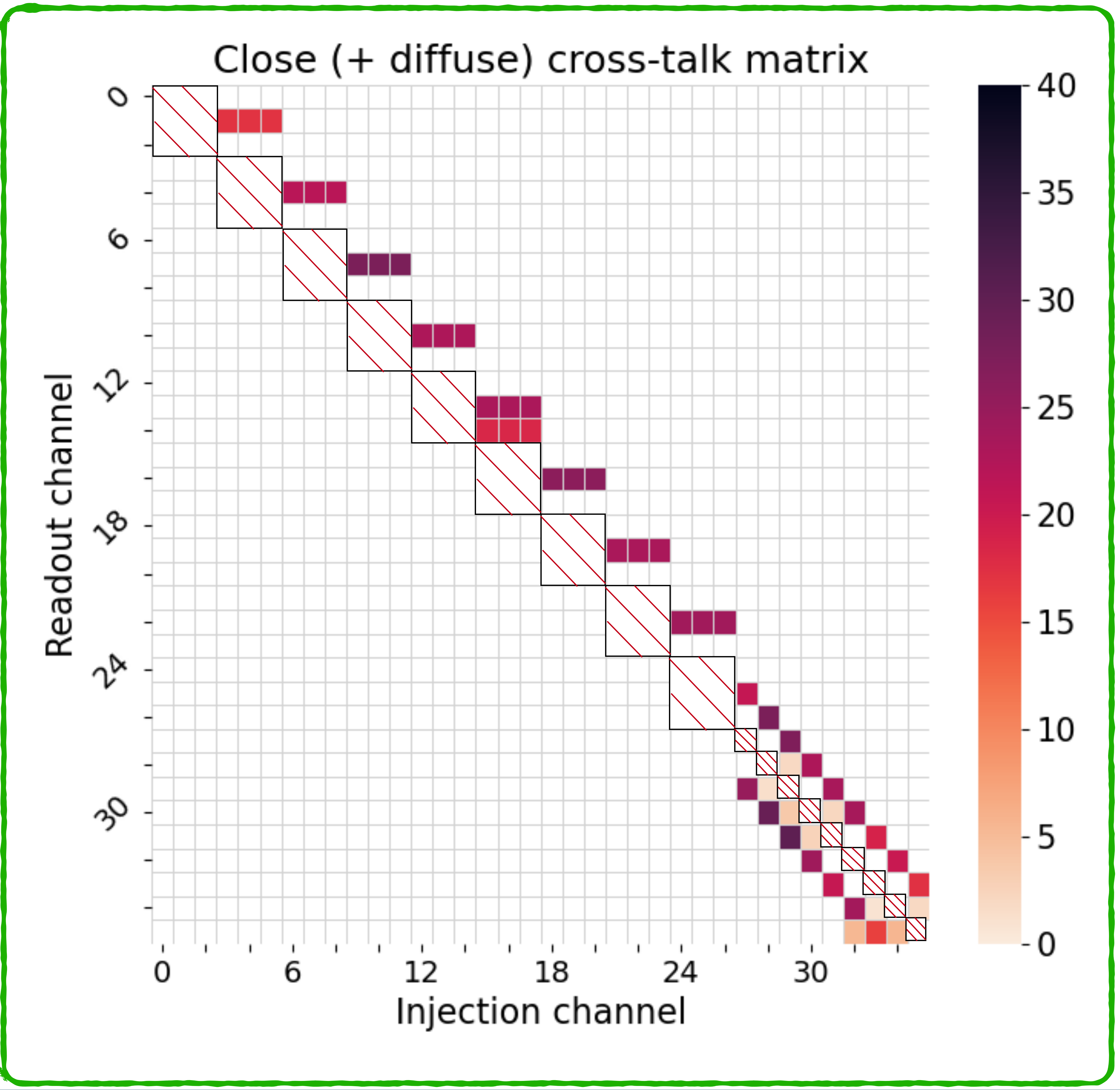




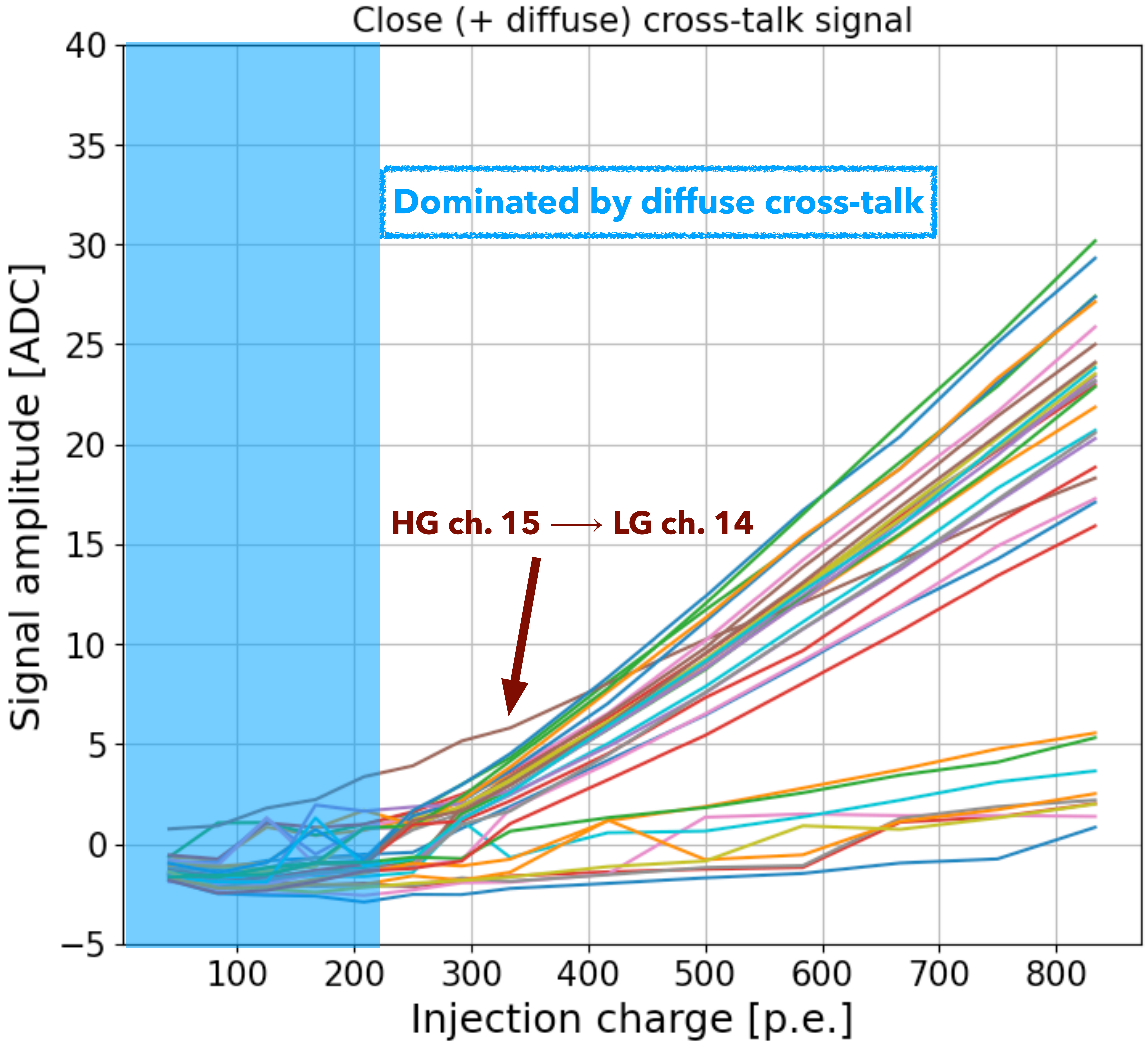
High cross-layer cross-talk

Linearity measurements





Linearity measurements



➡ Linear dependance of the close cross-talk with injected charge.

➡ Threshold at ∼ 200 p.e. for the close cross-talk ?

Conclusions on Crosstalk

- Validated the reduction (factor ~3) of diffuse crosstalk: **HKROC v0** → **HKROC v1b**.

- Validated the reduction of close crosstalk: **Mezzanine board** → **BGA board.**

  ➡ Survival 1-2% HG → MG close crosstalk.

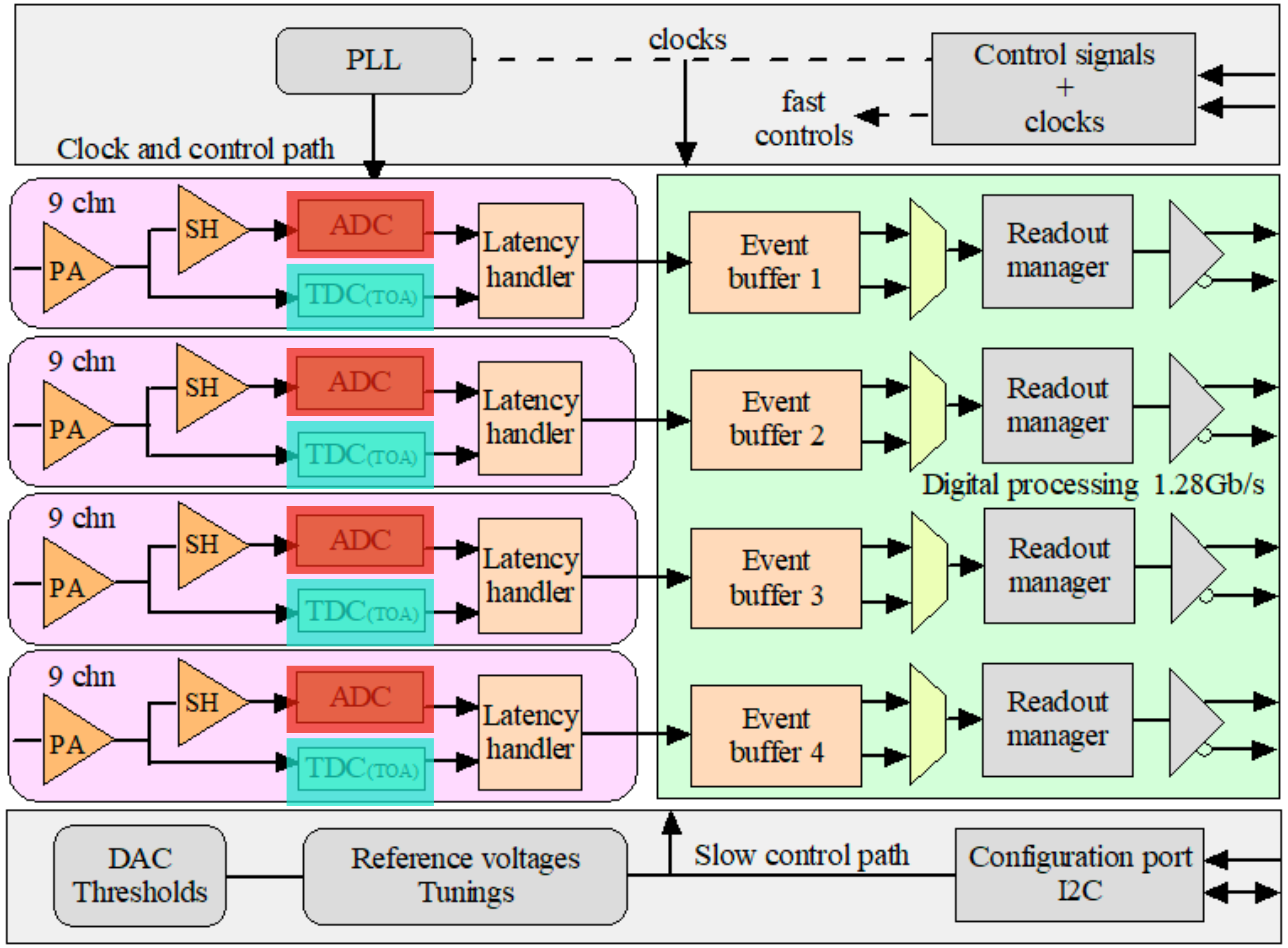
  ➡ Unexpected cross-layer close crosstalk + threshold ?

Time measurements

What we looked at so far…

Before: Crosstalk measurements
Now: Time measurements

➡ **Measure the Time of Arrival (ToA) of the signal.**

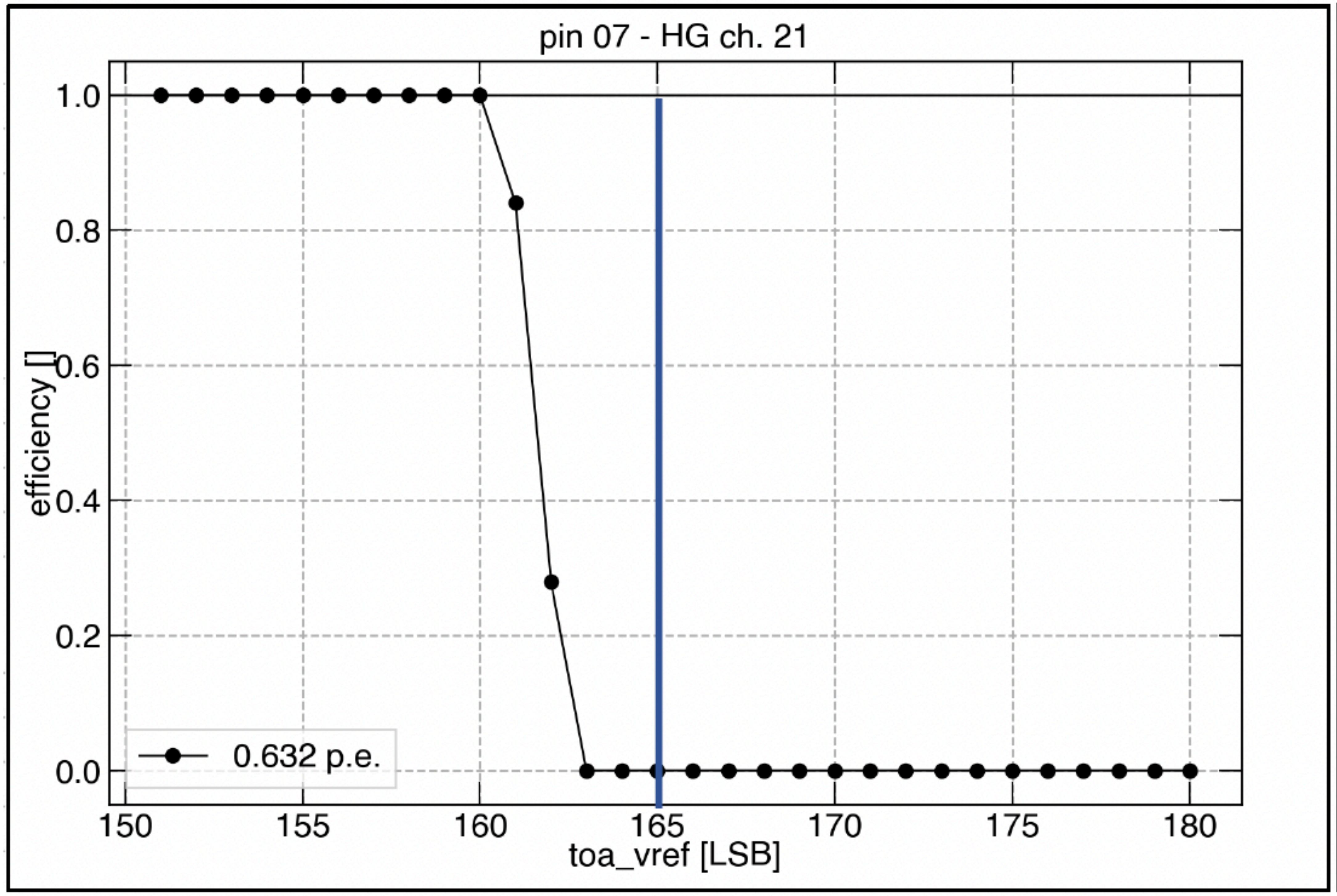


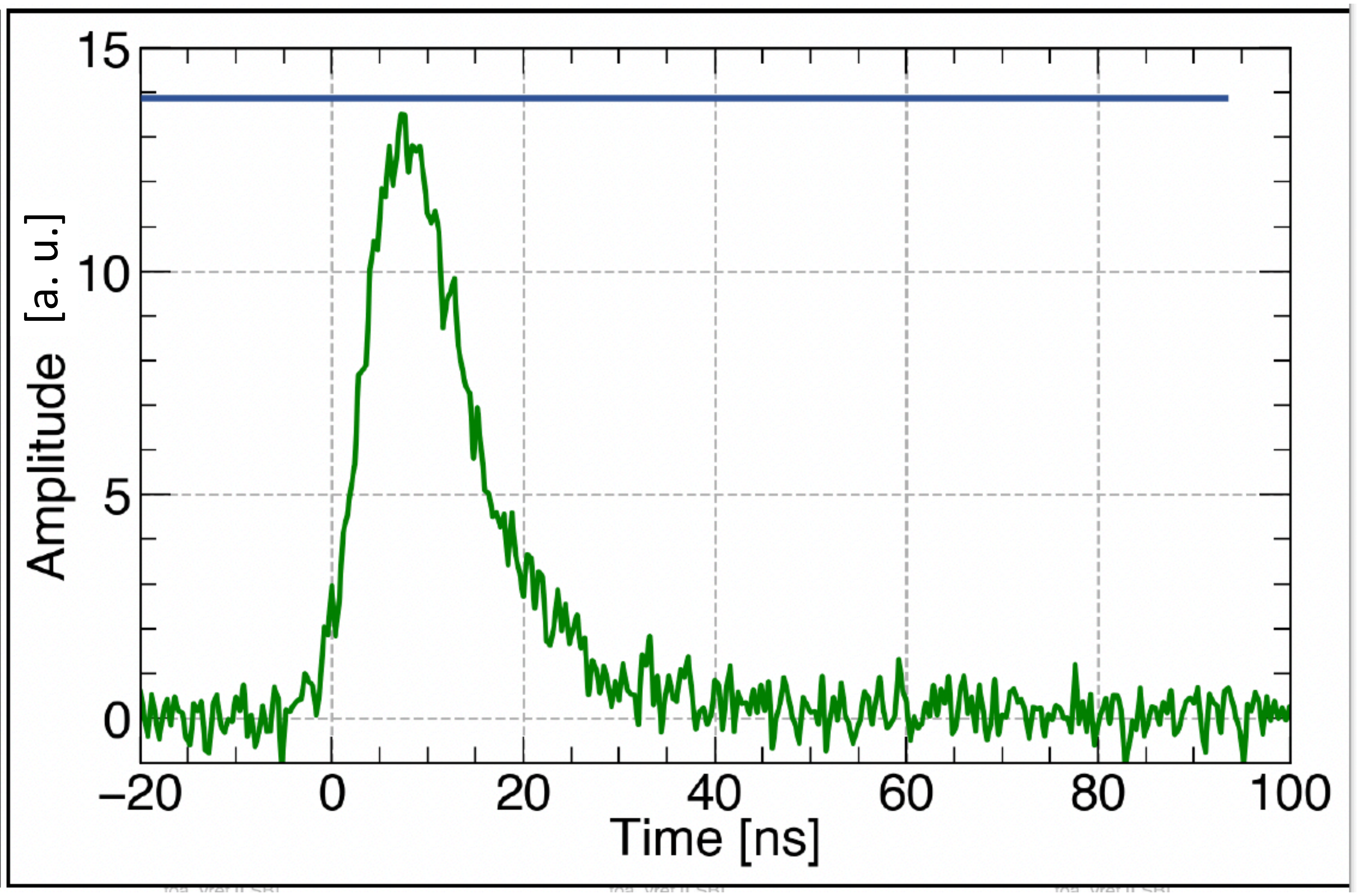
HKROC digitization

S-curves for Time of Arrival (ToA)

ToA_threshold = toa_vref<9:0> - trim_dac_toa<5:0>

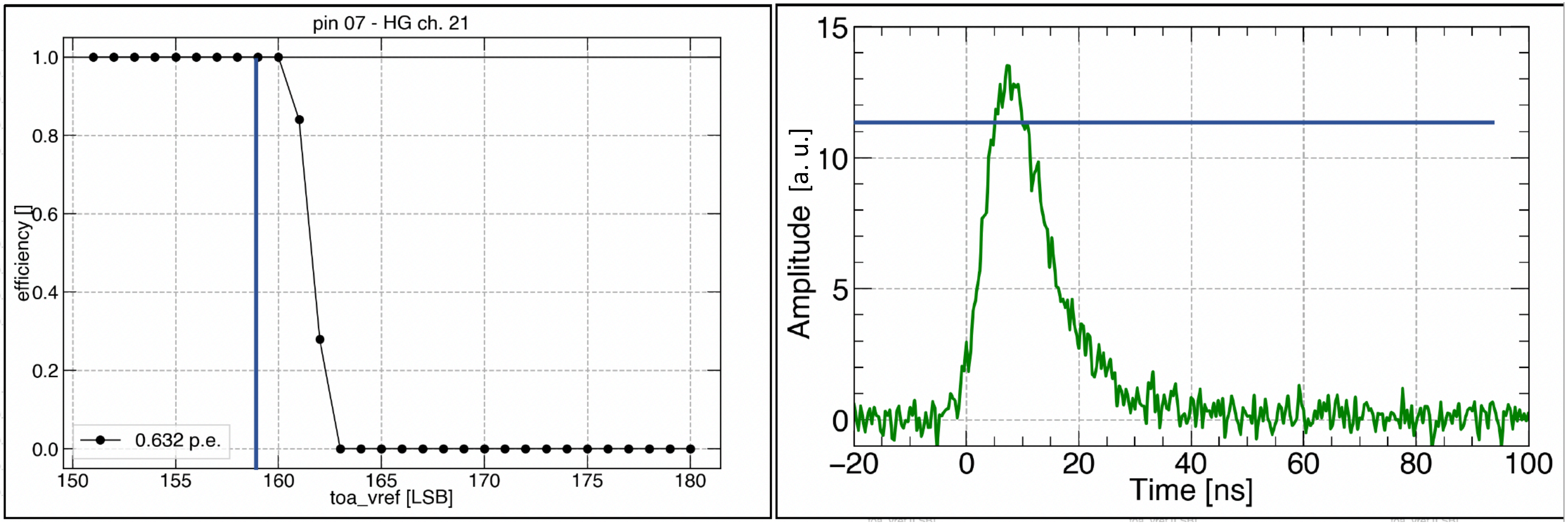
Courtesy of Denis





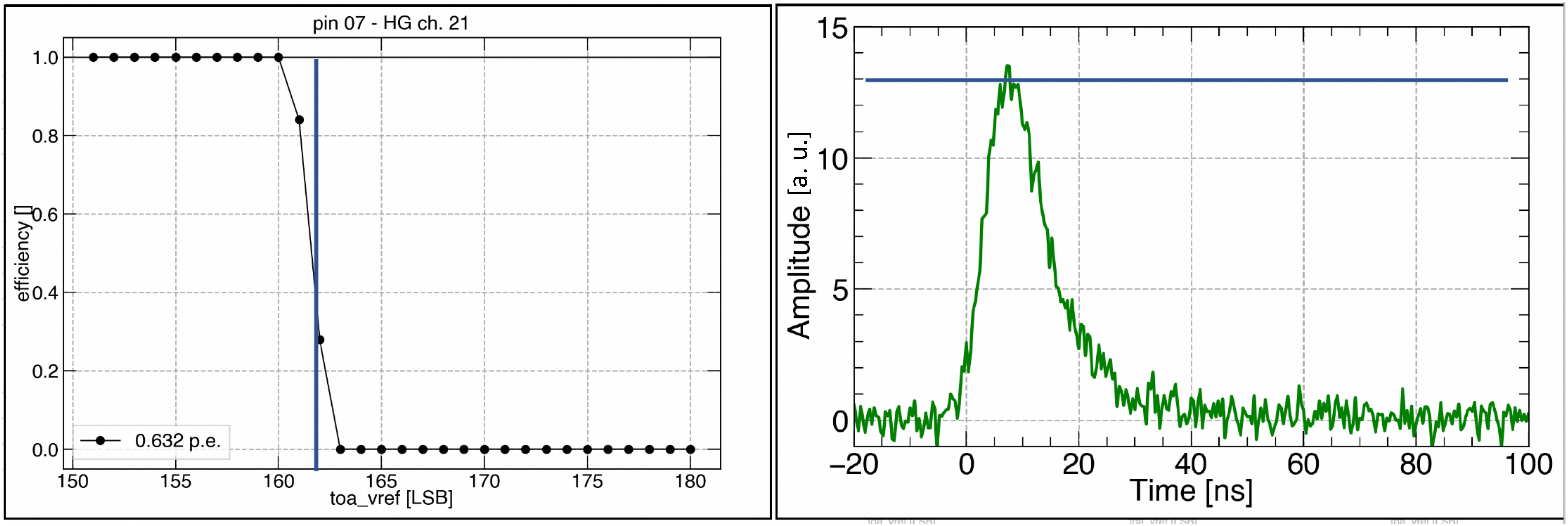
No trigger ⟷ Efficiency = 0%

ToA_threshold = toa_vref<9:0> - trim_dac_toa<5:0>



Only triggers ⟷ Efficiency = 100%

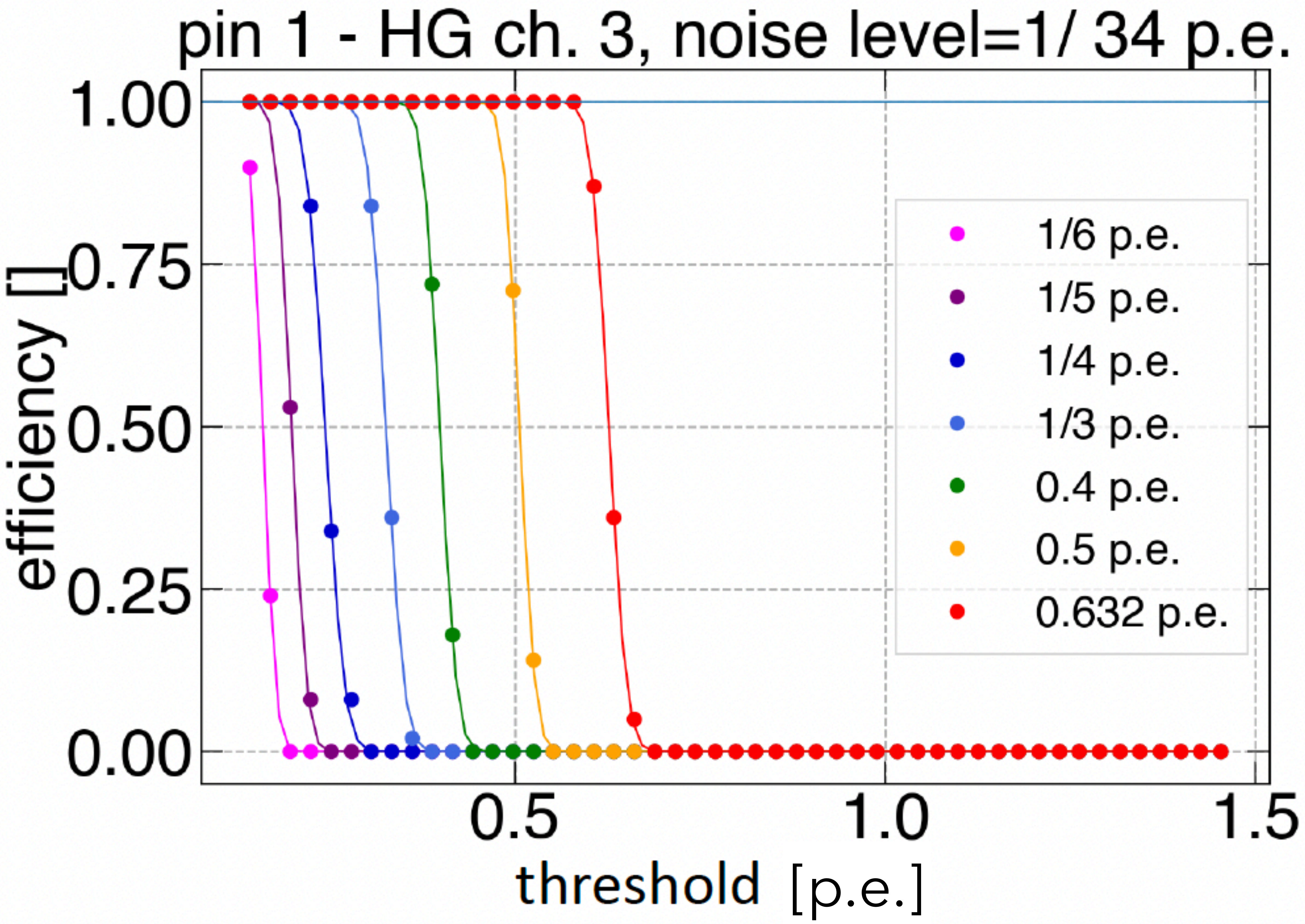
ToA_threshold = toa_vref<9:0> - trim_dac_toa<5:0>



Signal peak height ⟷ Efficiency = 50%

Here toa_vref = 162 ⟷ threshold = 0.632 p.e.

Courtesy of Denis



Fit by error function on the 36 channels to extract the noise level:

< 1/22 p.e. for all channels!

(Target threshold = 1/6 p.e.)

ToA measurements (threshold scan)

ToA mean (PMT waveform)

ToA std (PMT waveform)

Around 1/6 p.e. threshold:

✦ **Even pin/channel**: explosion of the std for **1 p.e.** injected charge (PMT waveform)

✦ **Odd pin/channel**: explosion of the std for **10 p.e**. injected charge (PMT waveform)

➡ **Correspond to a « kink » in ToA mean, i.e. deformation of the pre-amp. signal feeding the TDC.**

ToA measurements (threshold scan)

ToA std (PMT waveform)

Further investigations suggested a coupling to the clock as an explanation

Without this coupling → well within the requirements to have ToA resolution < 300 ps for 1 p.e.

Conclusions on ToA

- If not for the clock coupling, ToA resolution well within HK requirements (< 300 ps at 1 p.e.)

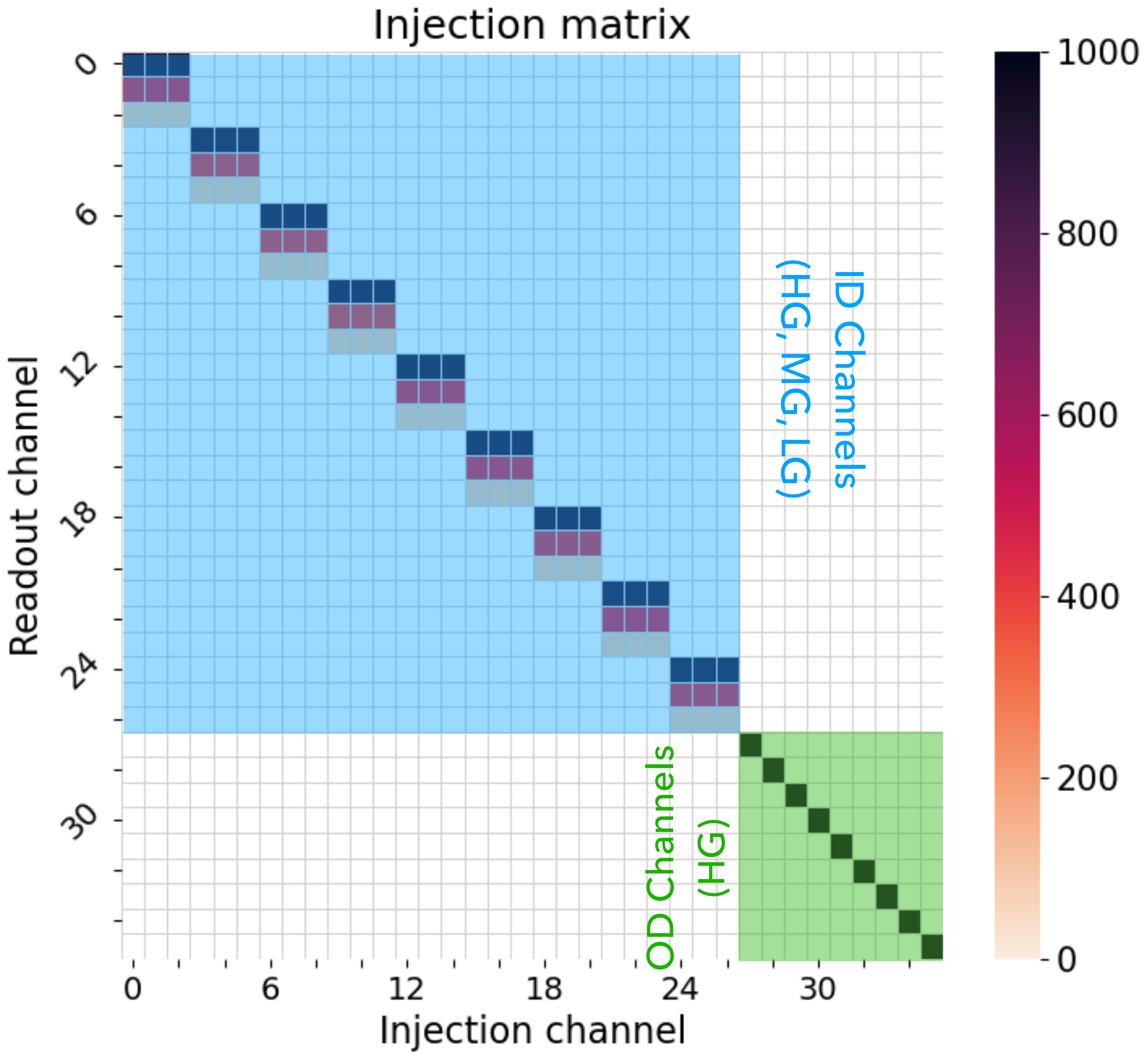
  ➡ Continue investigation on the coupling.

- Noise level confirmed to be moderate.

  ➡ Check impact on noise trigger rate at $1/6$ p.e. Required to be < 1 Hz.

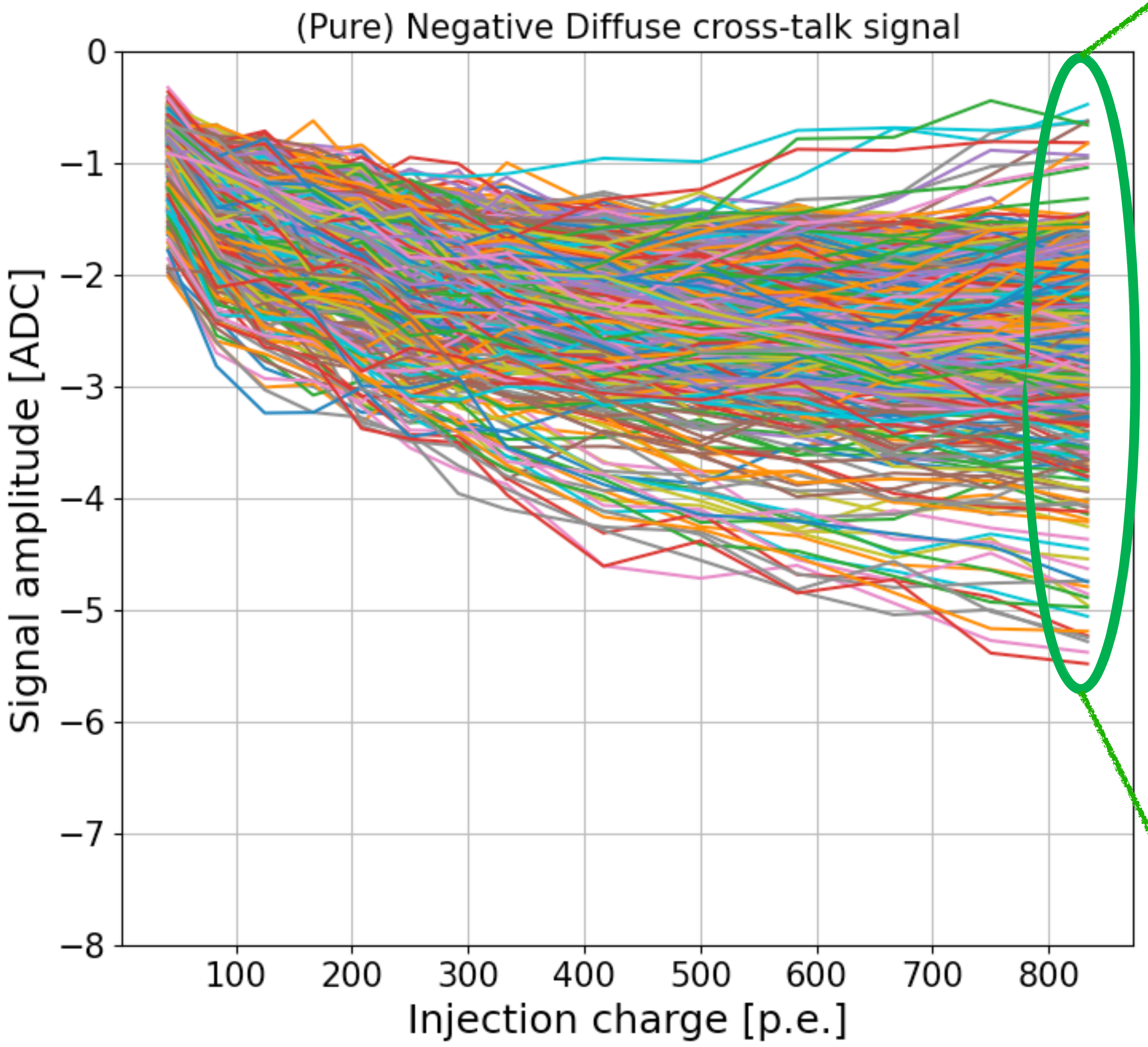
Appendix

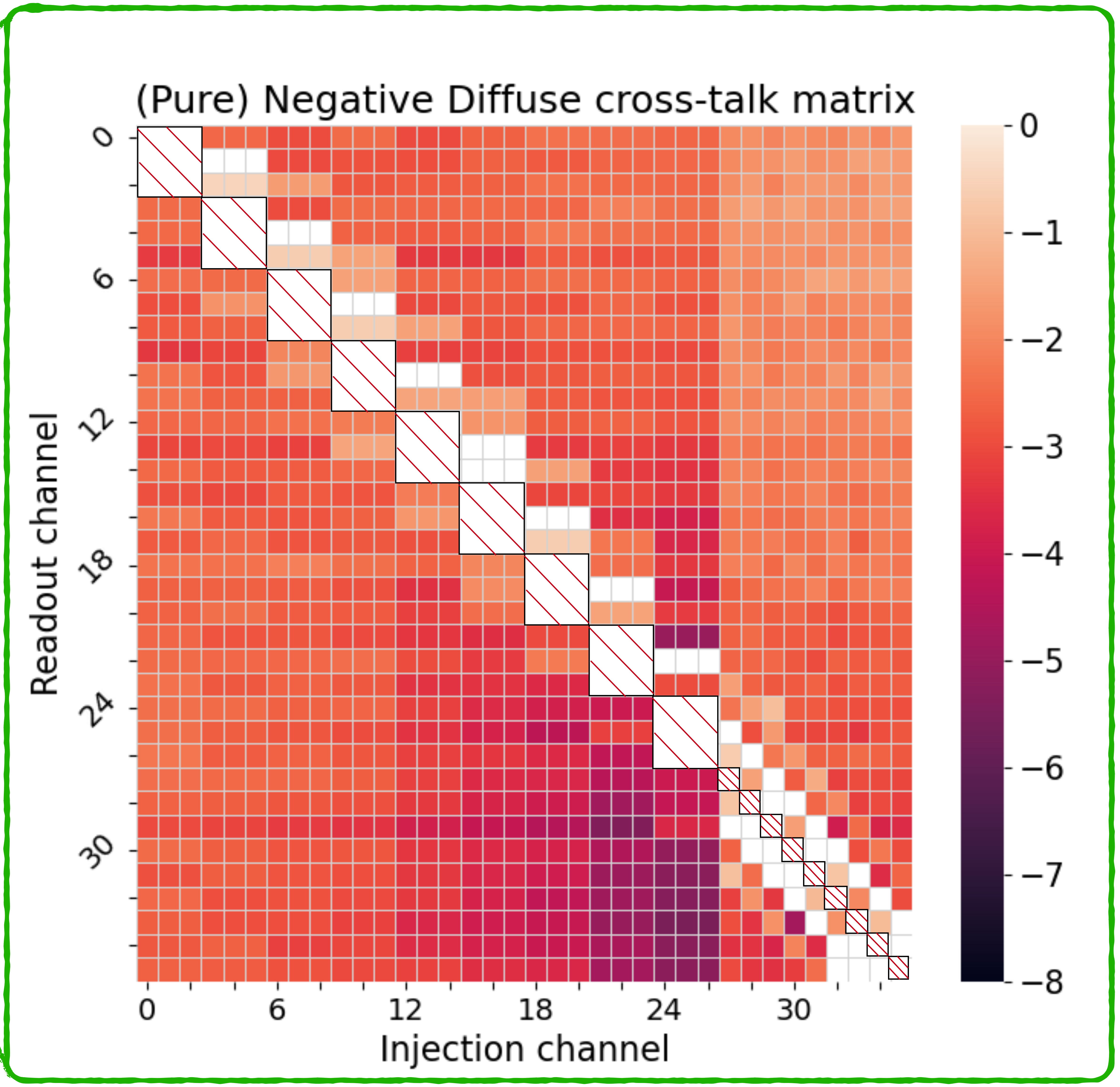
Injection Matrix - Chip v1b + Board v2 (BGA)



Input signal ~ 200 *p.e.*

Linearity Measurements





ToA histograms (PMT waveform)

ToA measurements (threshold scan)

ToA mean (Triangular waveform)

ToA std (Triangular waveform)

Around 1/2 p.e. threshold:

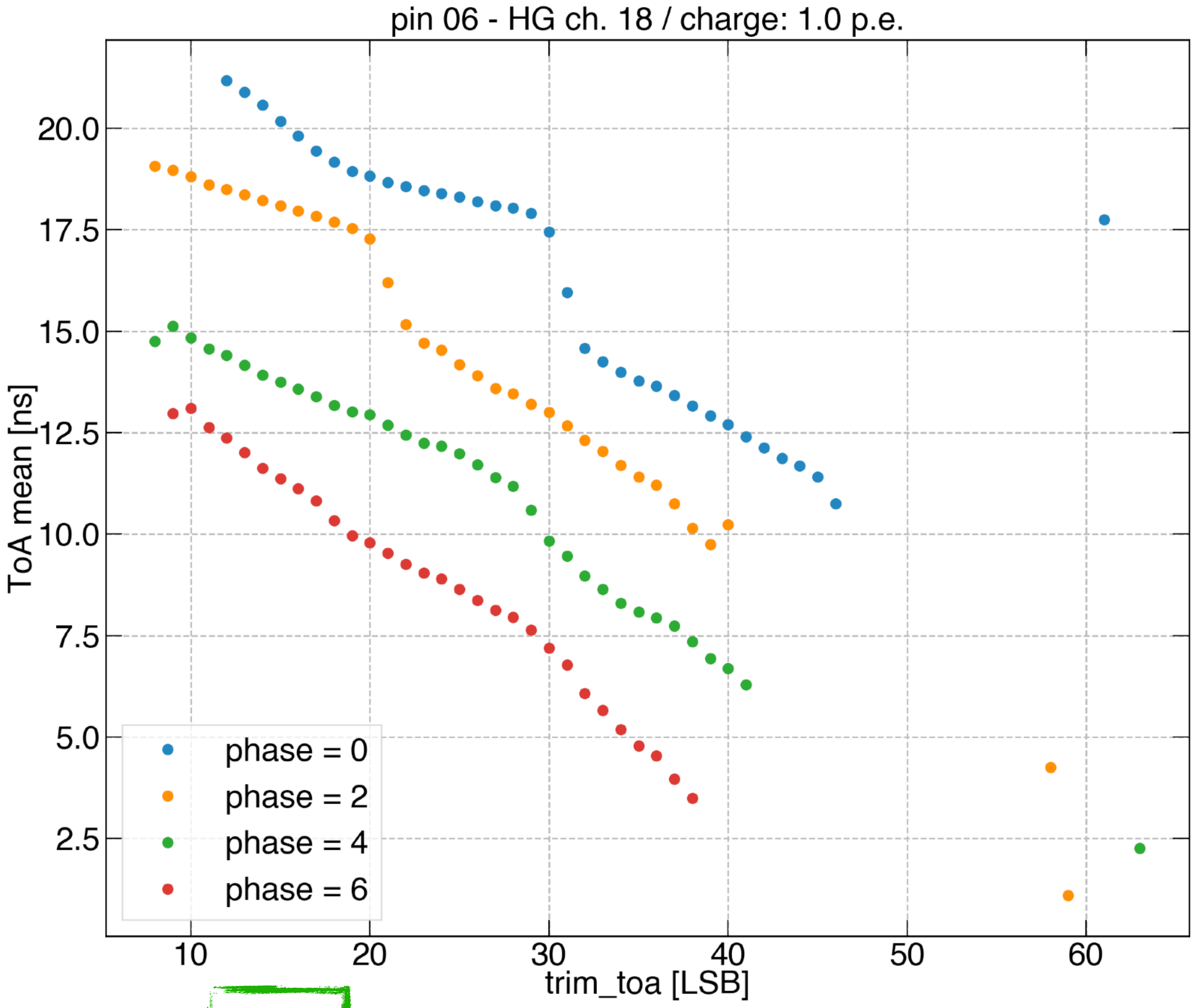
✦ **Even pin/channel**: explosion of the std for **1 p.e.** injected charge (PMT waveform)

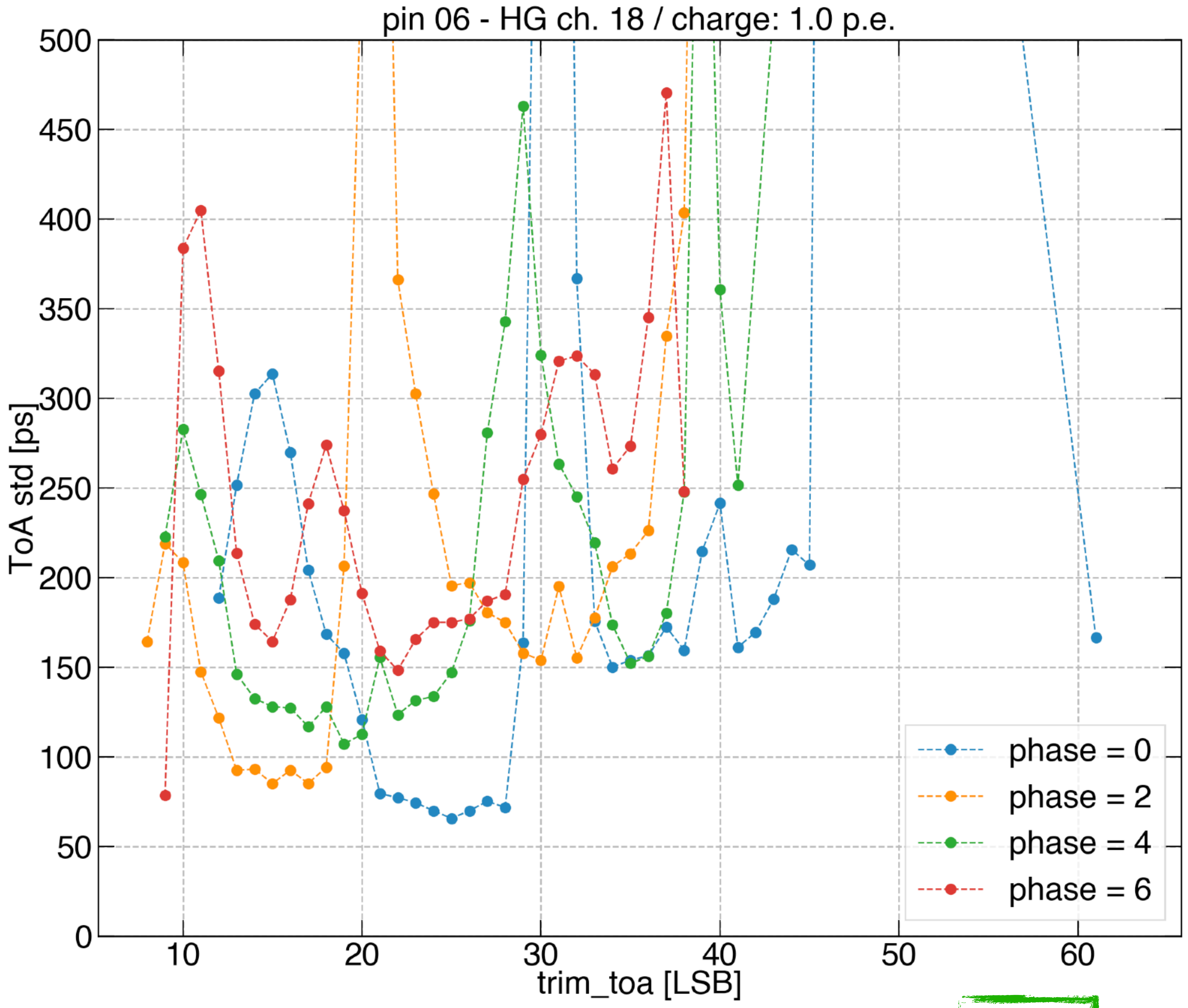
➡ **Correspond to a « kink » in ToA mean, i.e. deformation of the pre-amp. signal feeding the TDC.**

ToA histograms (Triangular waveform)

Phase scan for 1 p.e. signal

1 p.e. Triangle signal / Injection pin n°6 (HG ch. 18)





1. p.e.

0. p.e.