HKROC: digitizer description and test results

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LLR group meeting 02.05.2023

Outline

Part I: Introduction

- HK physics program
- General description of HKROC
- HKROC history
- Key characteristics

Part II: The HKROC ASIC

- General description
- Block scheme
- Operating principle

Part III: Test results

- Calibration
- Noise evaluation
- Cross-talk measurements
- Time measurements
- Charge measurements

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See Rudolph's presentation

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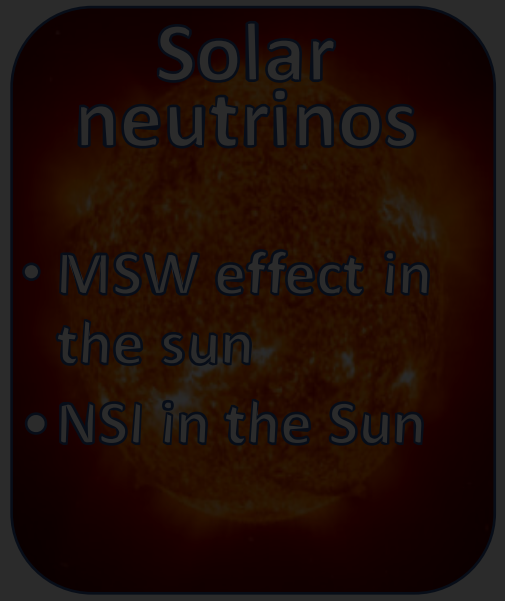
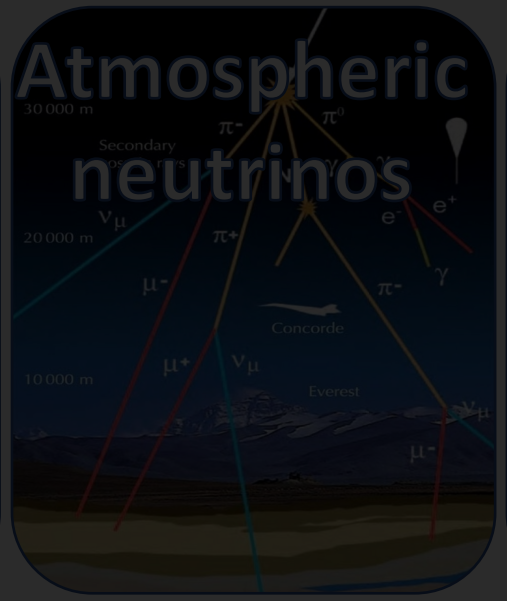
HyperK has an extensive physics program





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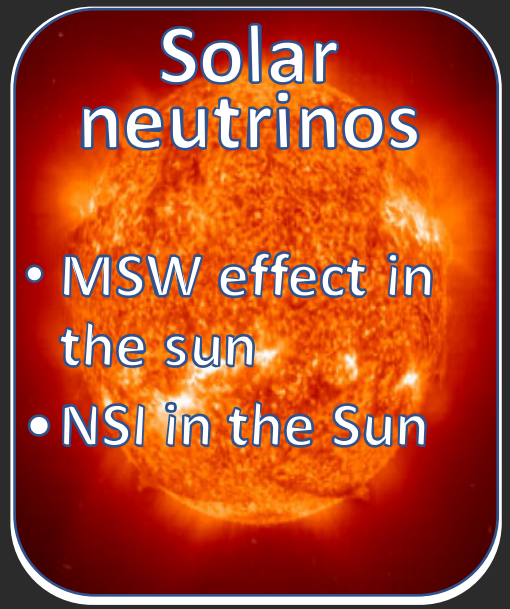

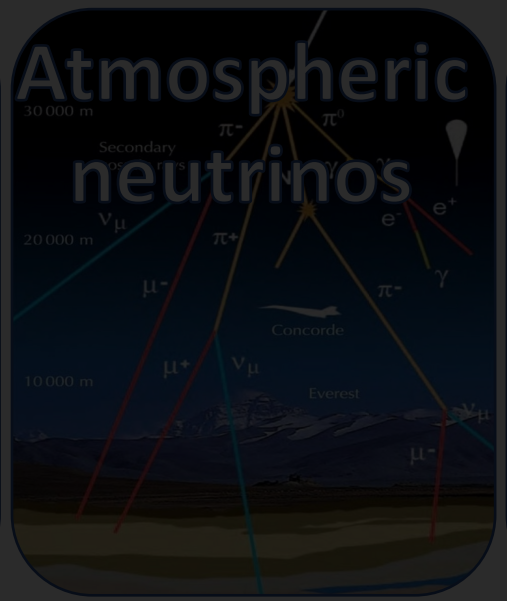

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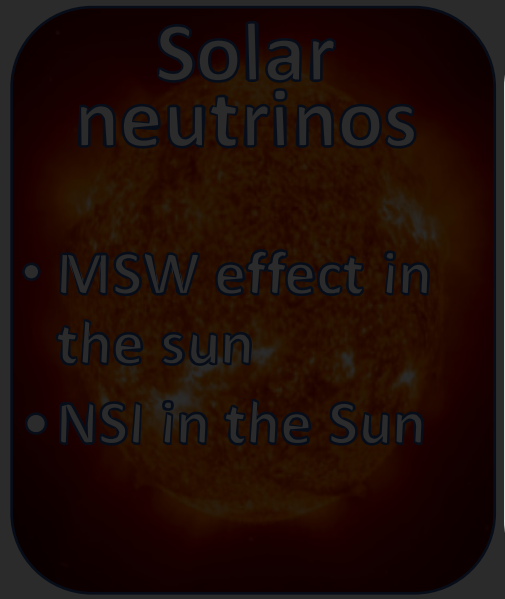
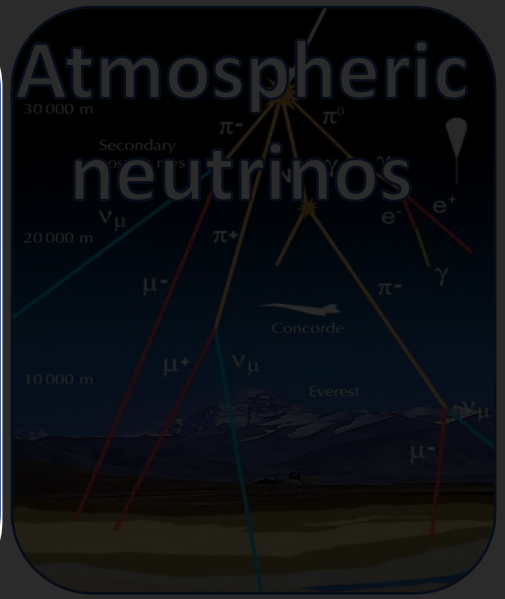
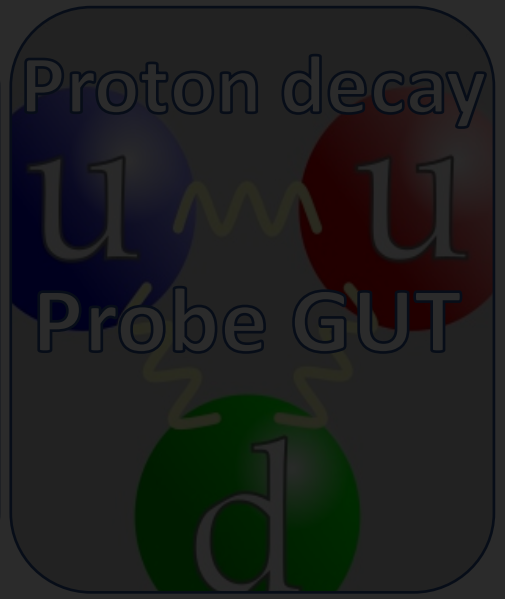






HyperK has an extensive physics program

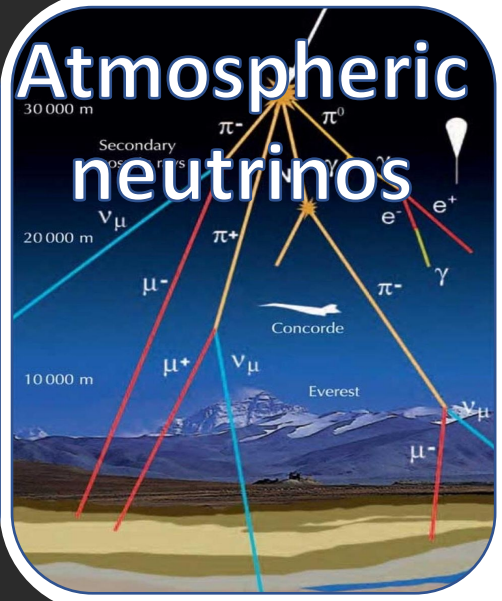
Solar neutrinos

- MSW effect in the sun
- NSI in the Sun

Supernova neutrinos

- Direct SNv :
- Relic SNv :

Atmospheric neutrinos



Accelerator neutrinos

Proton decay

Probe GUT

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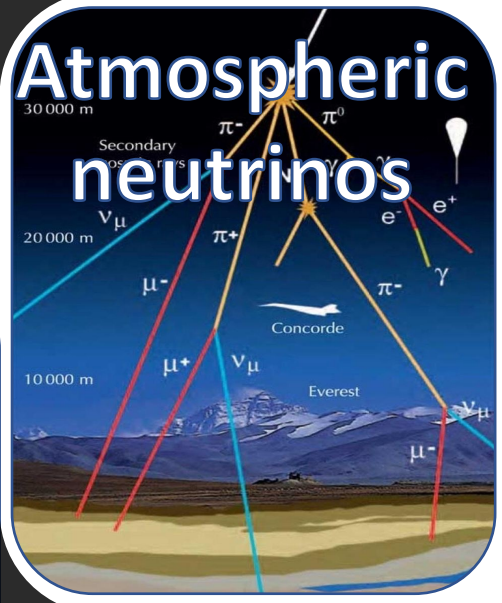


Accelerator neutrinos

Proton decay

Probe GUT

- **Observe CP violation for leptons at 5σ**
- **Precise measurement of δ_{CP} .**
- **High sensitivity to ν mass ordering.**

HyperK has an extensive physics program

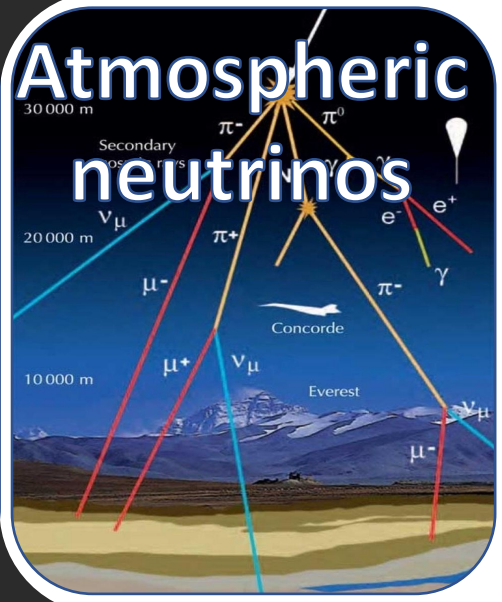
Solar neutrinos

- MSW effect in the sun
- NSI in the Sun

Supernova neutrinos

- Direct SNv :
- Relic SNv :

Atmospheric neutrinos



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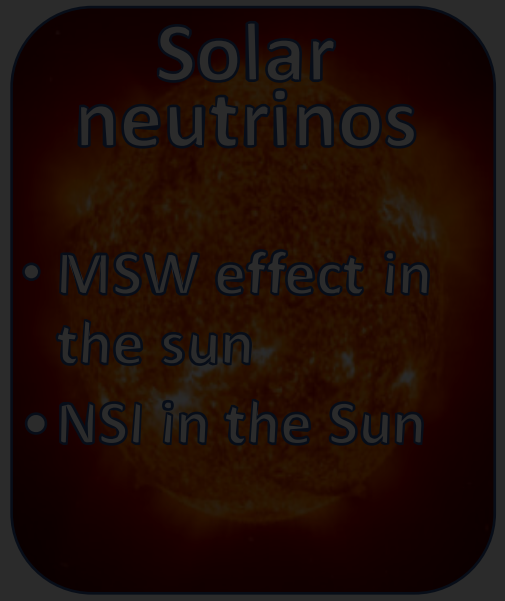

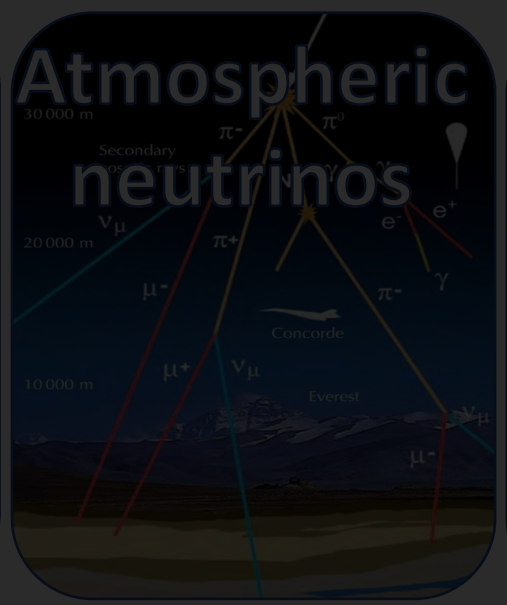

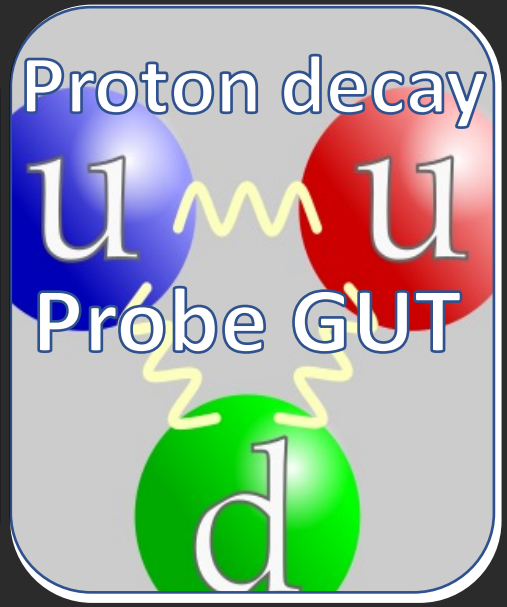

Large physics program ⇒ Strong requirements on electronics

HK = challenging measurements:
- **complex topologies: e.g. multiring samples**
- **large energy range: from SN to HE physics**
- **Michel-electron tagging**
- **neutron tagging**

HK = challenging systematics:
- **PMT response.**
- **Water transparency**
- **Direct vs indirect light**
- **Huge scale**

Strong requirements on electronics:
- **on charge measurements**
- **on timing measurements**
- **on hit rate and dead time**

Large physical program ⇒ Strong requirements on electronics

Physics constraint	Impact on electronics requirement
Detect synchronous (beam) & asynchronous (atm., solar, p-decay, SN) events	Self triggering for each channel
Detect close SN (e.g. Beltegeuse) w/ no event loss	Channel dead time < 1 µs
Detection threshold as low as possible (negligible noise compared to PMT one)	Charge threshold <= 1/6 p.e.
Excellent detection & no charge ↔ E bias from low (solar, SN) to high energy physics	Charge linearity < 1 % from 0 to 2500 pC (0 to 1250 p.e. for HK)
Excellent charge ↔ E resolution	Charge RMS <= 1%
Electronics < PMT time resolution (1.3 ns)	Electronics timing RMS < 0.3 ns at 1 p.e.
Low power consumption as under water	1 W/ channel

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Large physical program ⇒ Stron

The challenge was taken up

Impact on electronics requirement
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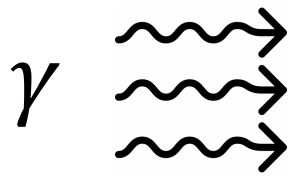
Charge RMS <= 1%
Electronics timing RMS < 0.3 ns at 1 p.e.
1 W/ channel

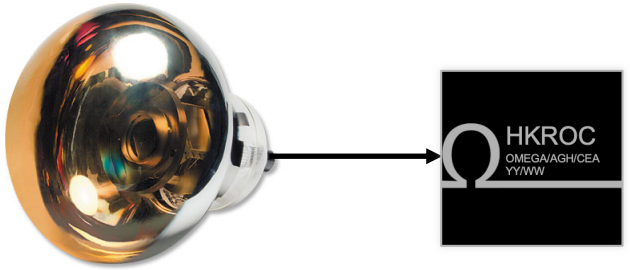
LLR, OMEGA and CEA present

Advanced ASIC chip for PMT readout

Part I: Introduction

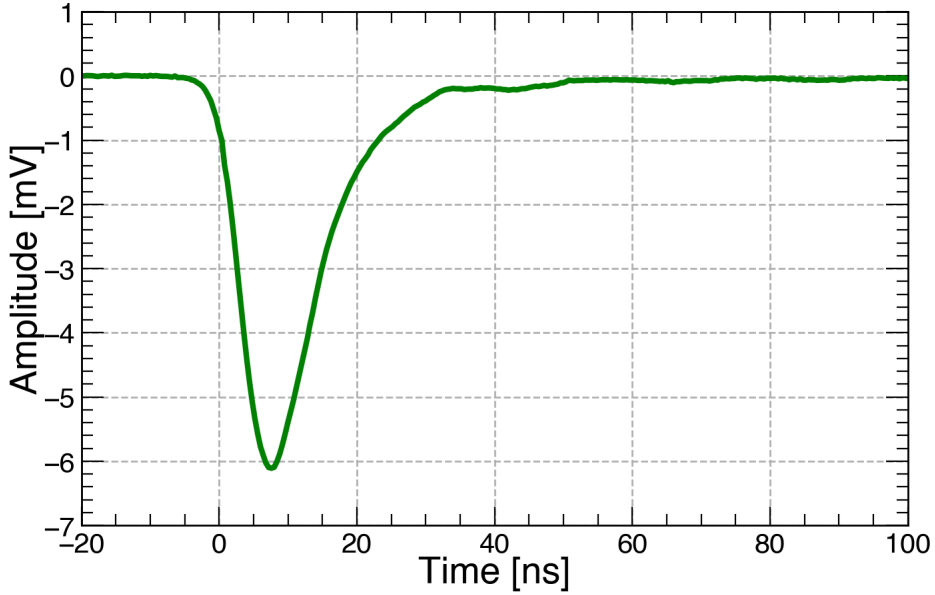
- **H**yper-**K**amiokande **R**ead **O**ut **C**hip - ASIC designed read out of the PMT of the future Hyper-Kamiokande experiment.



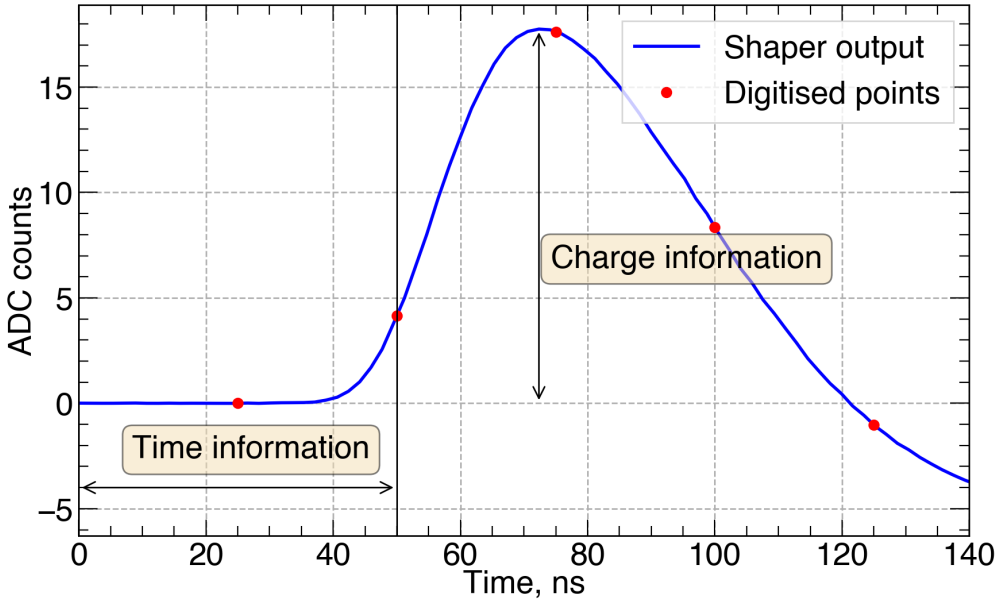


- The **HKROC** is a waveform **digitizer**: it reconstructs the full **shape of the charge-signal** waveform and provides extremely **precise timing measurement**.

PMT input signal of one photoelectron (p.e.)



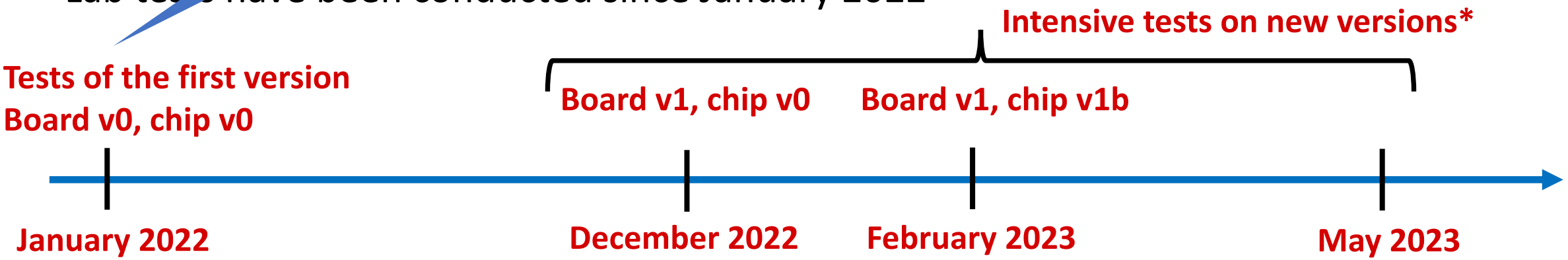
Digitisation output (red points)



We found significant cross-talk!
Well, let's do the new version
and find students to test it

History

- Derived from the **CROC** chip originally designed for the CMS High Granularity Calor.
- The first HK version was designed in 2021
- Lab tests have been conducted since January 2022



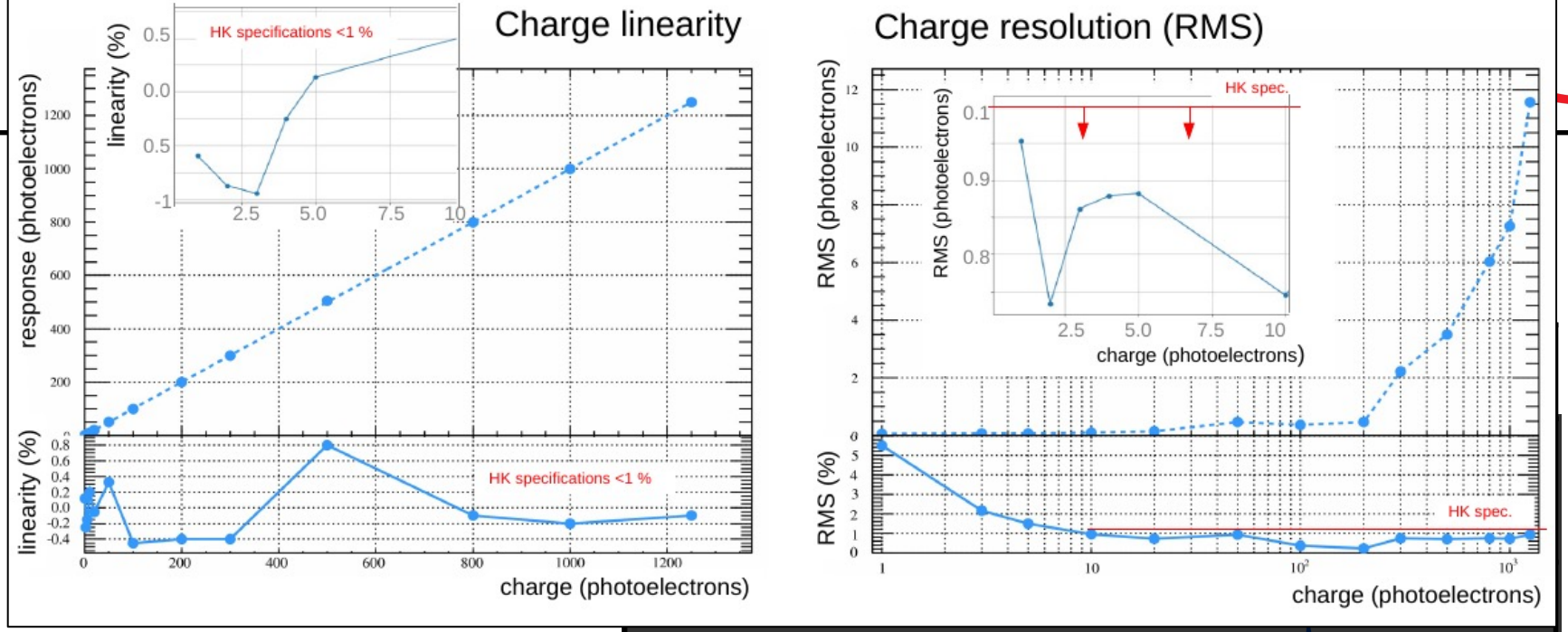
- In **December 2022** new version of mother board with **BGA-packaged HKROC** arrived (was designed to avoid closed cross-talk, see details later)
- In **February 2023** new version of chip **HKROC v1b** arrived (was designed to avoid diffuse cross-talk)

The results of our tests in the last part will be based on **v1b BGA-packaged** version

Part I: Introduction

Fully satisfied

HKROC
OMEGA/AGH/CEA
YY/WW



Key characteristics:

- Charge threshold: **1/6 p.e**.
- Charge **linearity**: **<1%**
- Dynamic range: **1-1250 p.e**.
- Charge **resolution**: **<1%**
- Power cons.: **< 1 W/channel**

Charge threshold <= 1/6 p.e.
Charge linearity < 1 % from 0 to 2500 pC (0 to 1250 p.e. for HK)
Charge RMS <= 1%
Electronics timing RMS < 0.3 ns at 1 p.e.
1 W/ channel

Fully satisfied

Time me

HKROC
OMEGA/AGH/CEA
YY/WW

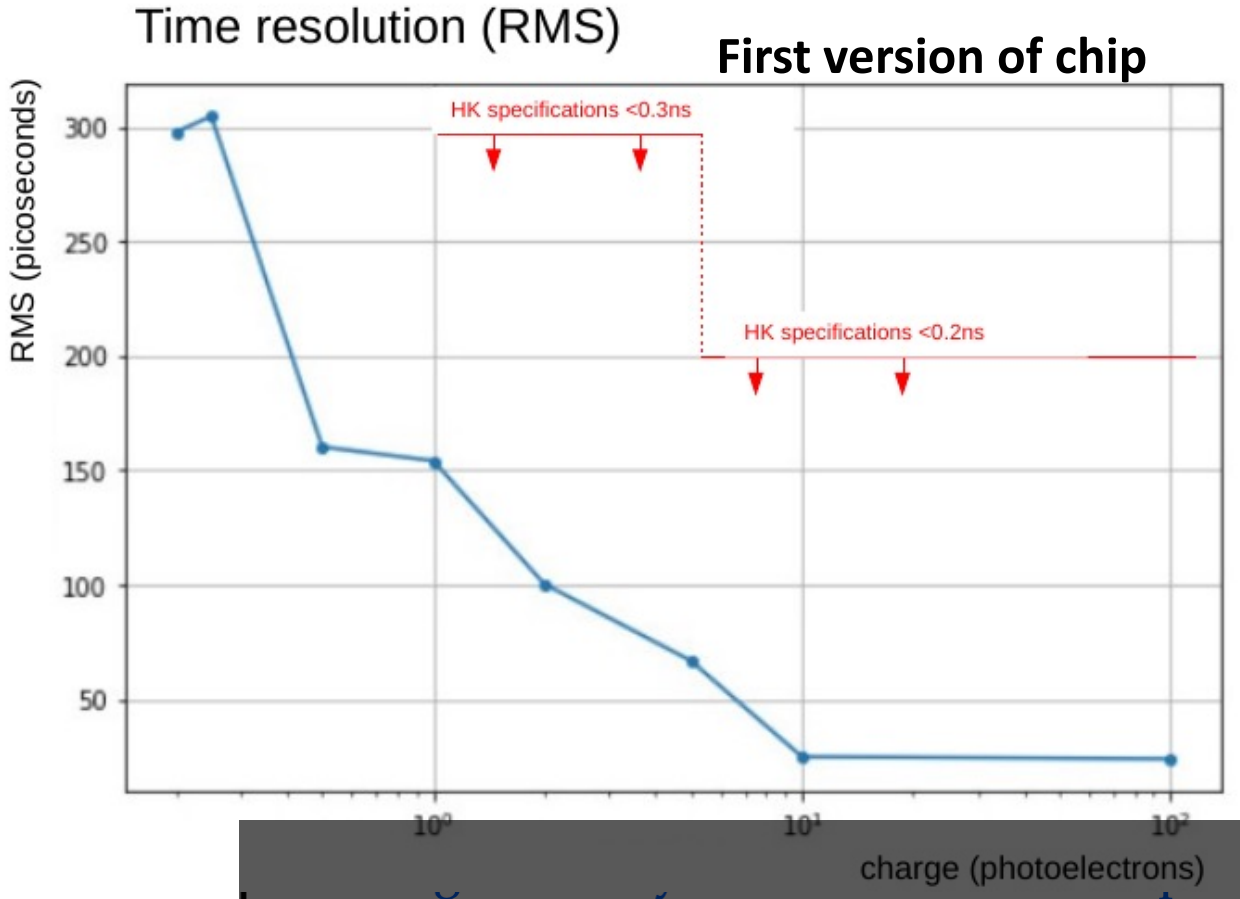
HKROC, good job!

Key characteristics:

- Self triggering for each channel
- Dead time: **30 ns**
- Time resolution: **25 – 150 ps**

Very precise timing characteristics
Even exceed the requirements

First version of chip



(0 to 1250 p.e. for HK)

Charge RMS <= 1%

Electronics timing RMS < 0.3 ns at 1 p.e.

1 W/ channel

Part II:
The HKROC ASIC

- General description
- Block scheme
- Operating principle

Part II: The HKROC ASIC

High gain channels

Medium gain channels

Low gain channels

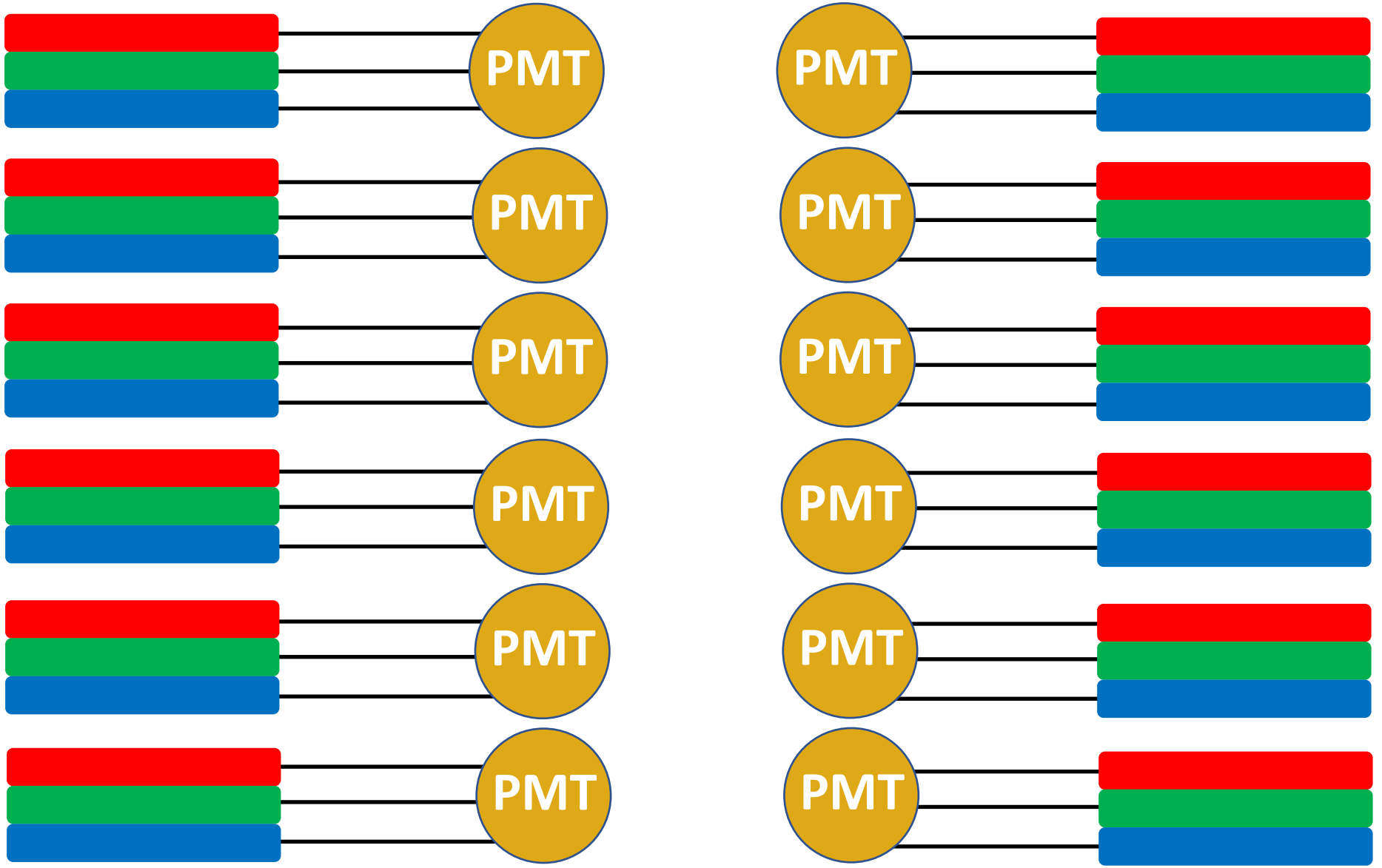
1 HKROC

II

36 channels

II

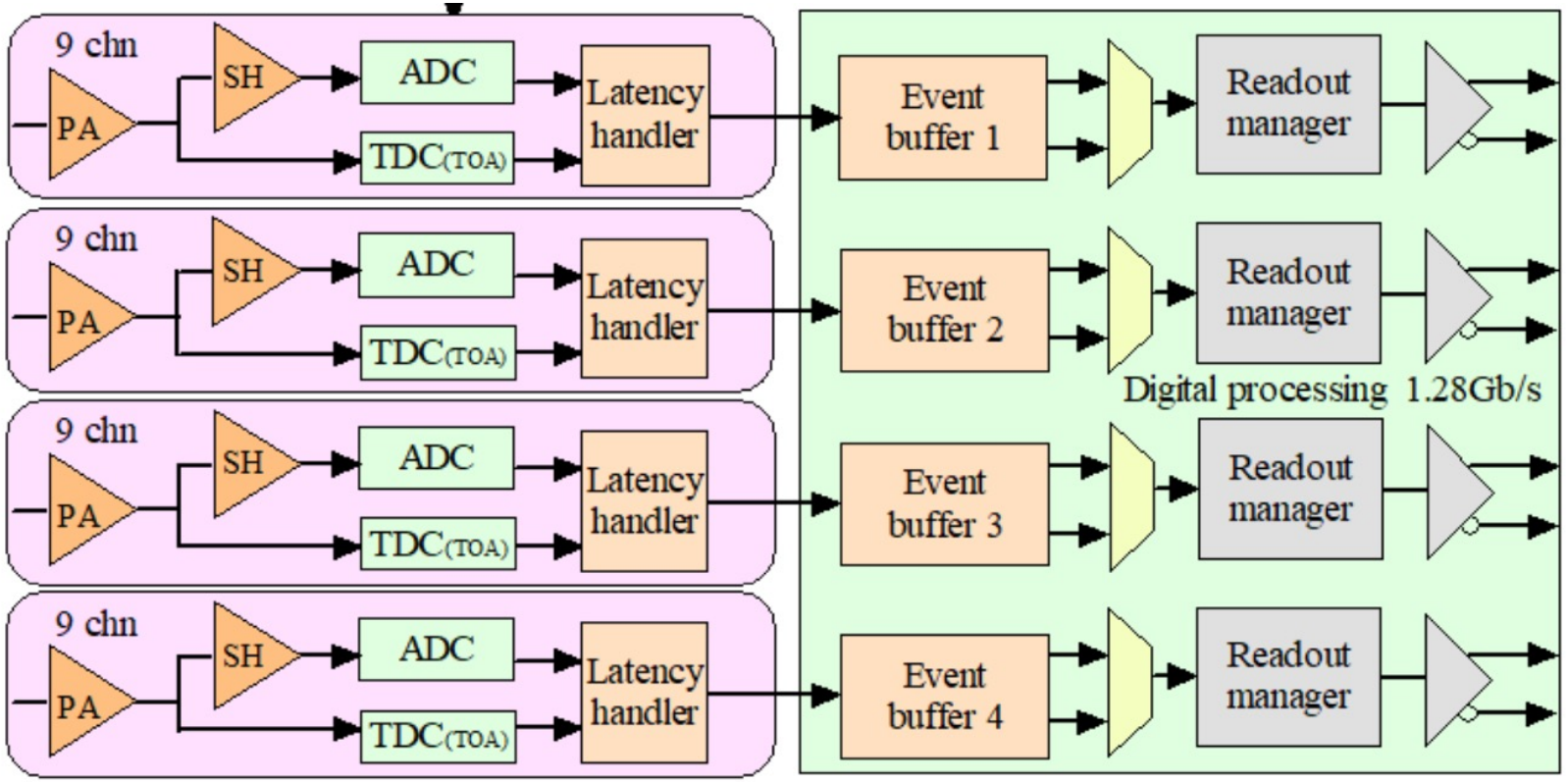
12 PMTs



Part II: The HKROC ASIC

Each channel includes converters for the charge and the time measurements:

- 10-bit 40 MHz Analog-to-Digital Converter (ADC)
- 10-bit Time-to-Digital Converter (TDC) (designed at CEA IRFU)



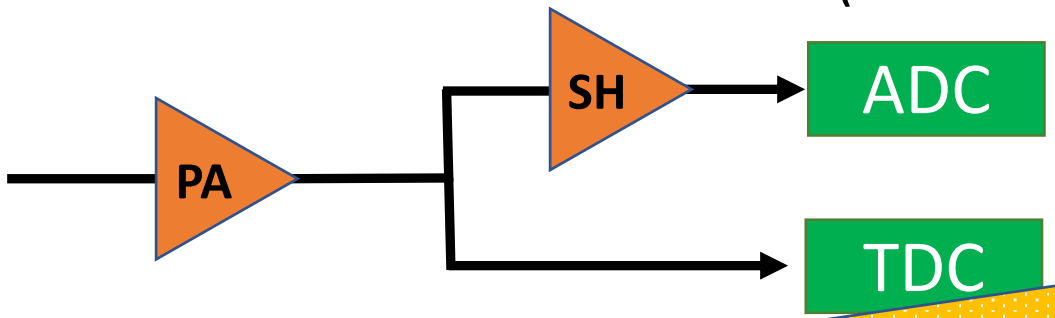
All the relevant data (charge and time) are stored into local memories (depth 32) and then read out through four high speed differential links sending data at 1.28 Gb/s.

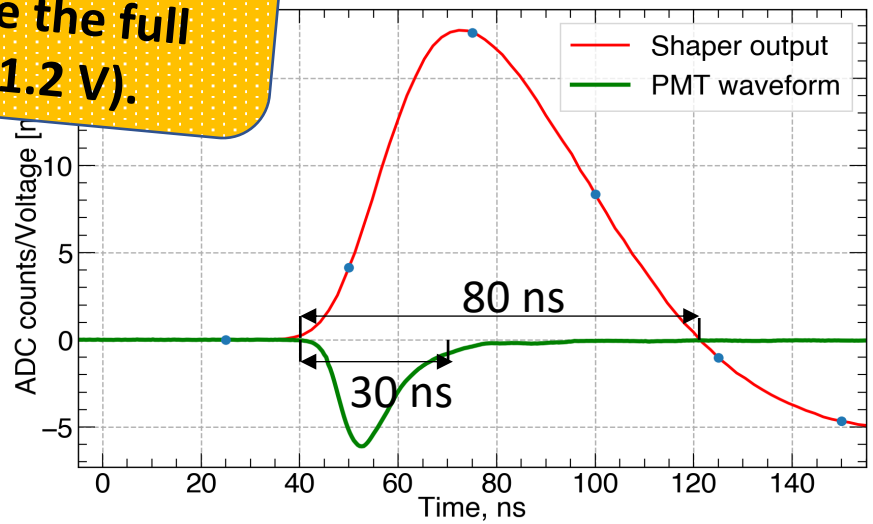
Shapes the PA output signal to allow the charge measurement, to optimize the signal-to-noise ratio and use the full available dynamic range (1.2 V).

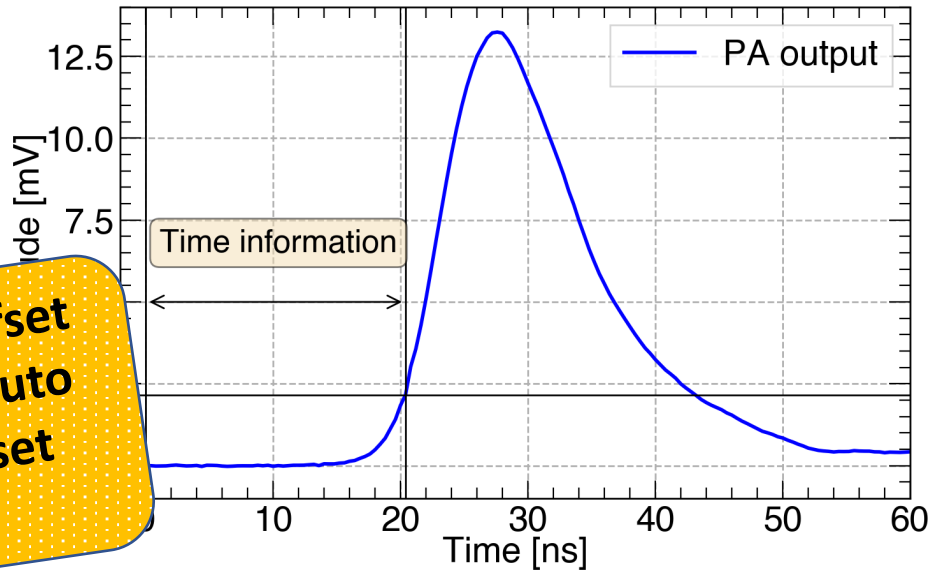
Operating principle

After preamplification signal follows two paths:

- A slow path with shapers connected to the ADC for charge measurement
- A fast path with a discriminator connected to the TDC for time measurement (dead time 30 ns)







The PA signal is sent to a low offset discriminator which allows to auto trigger on the signal above a set threshold.

Part III:
The results of the performed tests

- Calibration
- [illegible]
- [illegible]urements
- Cross-talk measurements
- Charge measurements

Follow Rudolph's presentation

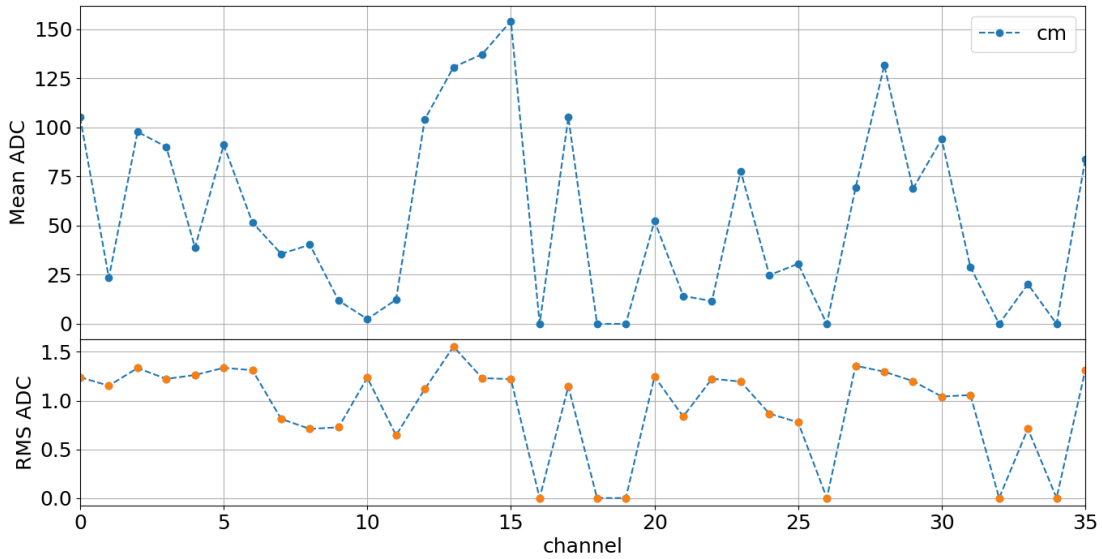
Calibration

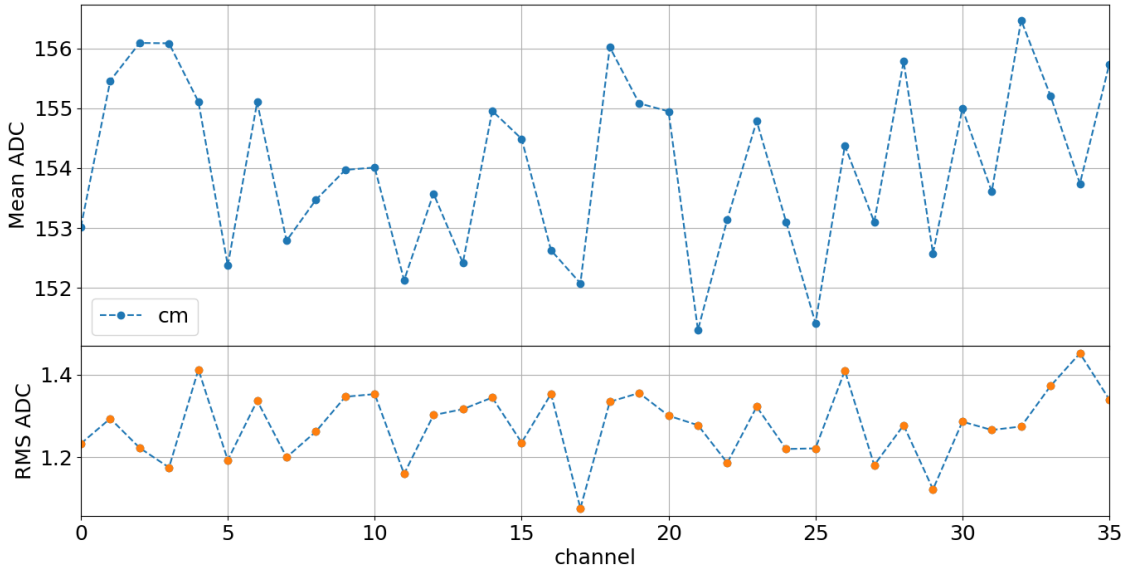
Step I: Stardartisation of DC level

Goal: the pedestal level should be uniform for all channel to have the same dynamic range.

For this purpose:

- ADC is measured is absence of injected charge to measure the pedestal.
- Using slow control parameters the pedestals are changed to be as uniform as possible

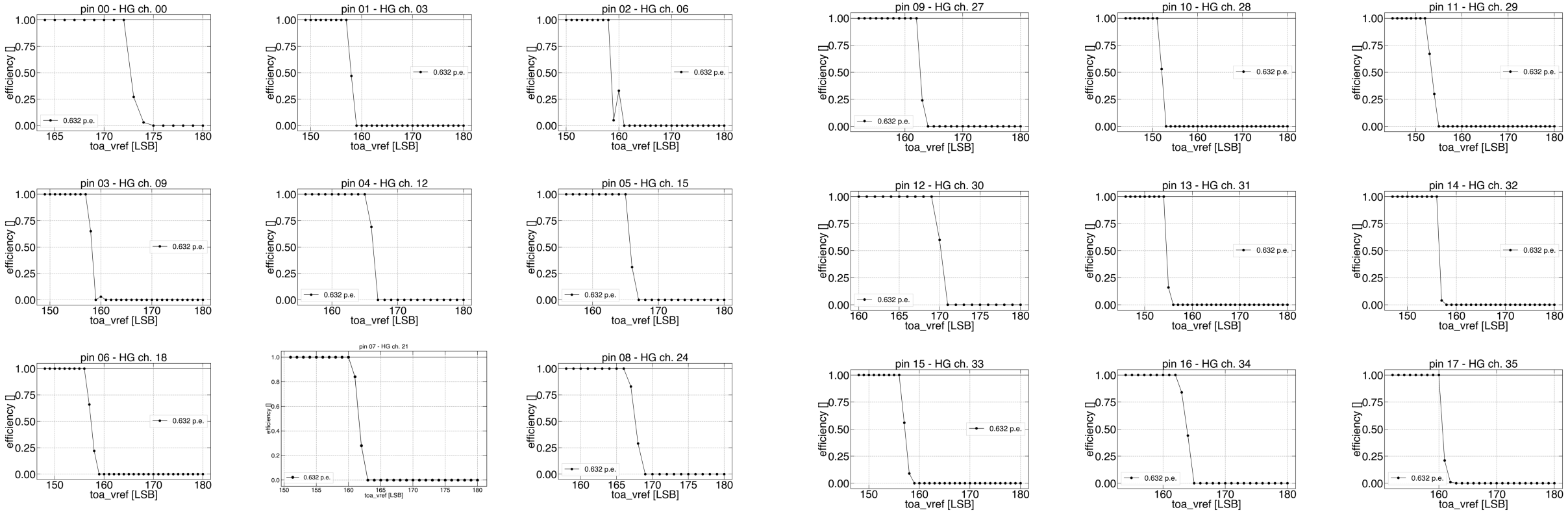




Calibration

Step II: Trigger threshold channel by channel

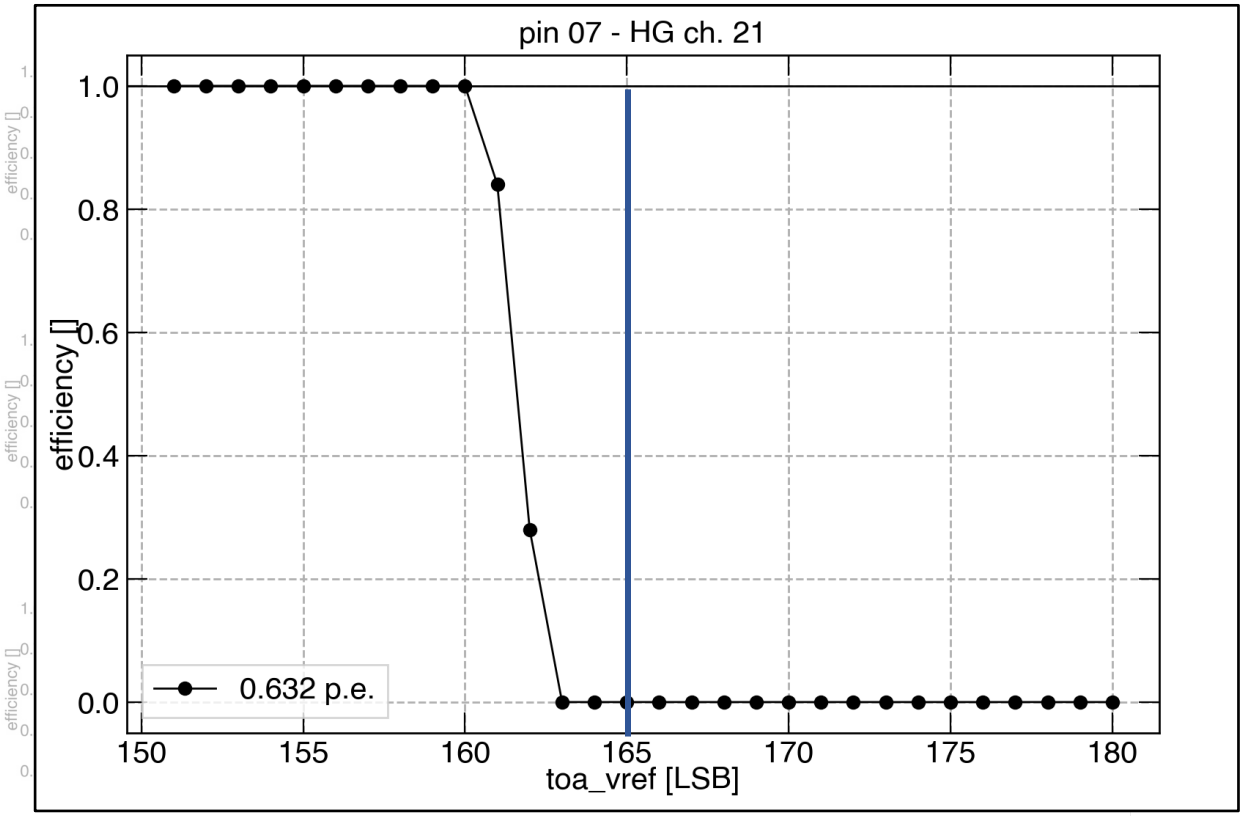
Goal: The level of triggering threshold for each should be a set at specific level (**HK requirement – 1/6 p.e**)

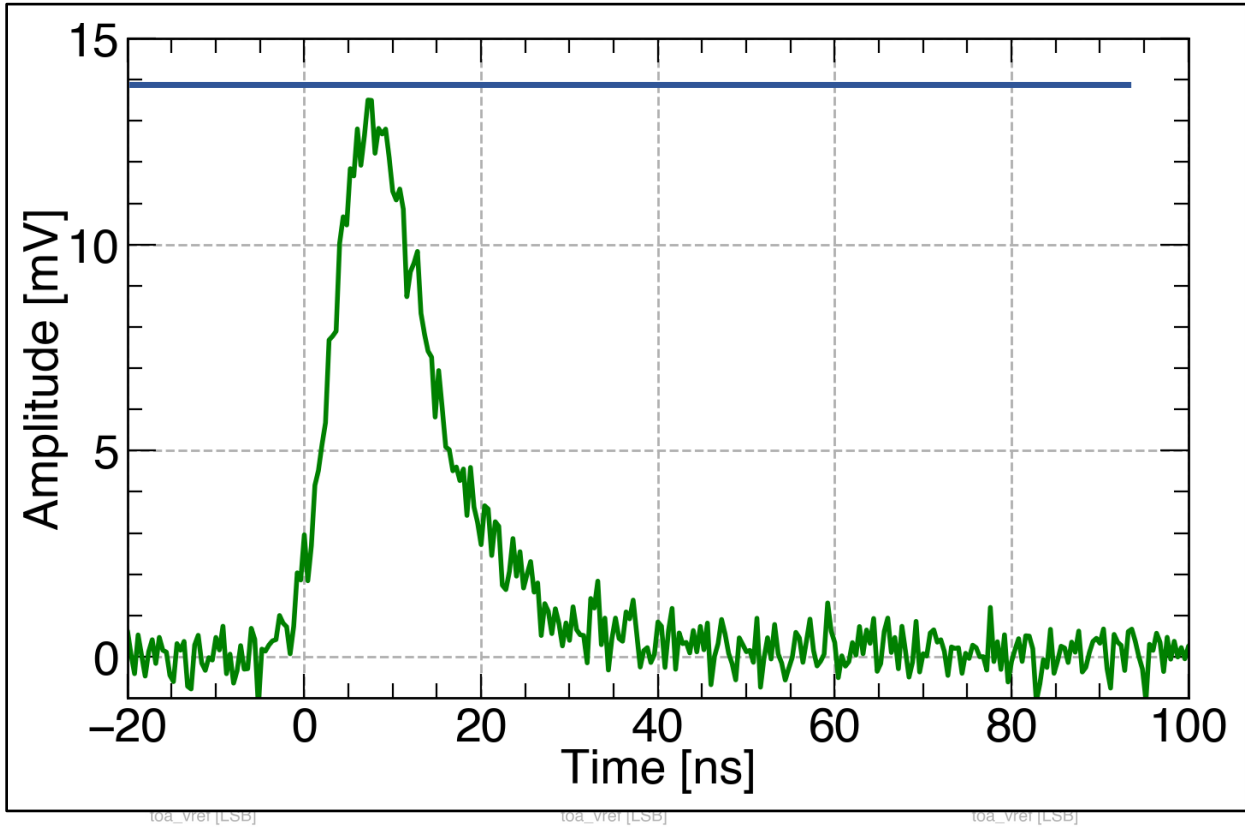


Calibration

Step II: Trigger threshold channel by channel

Firslty, we werform threshold scan channel by channel using a **global** slow control parameter





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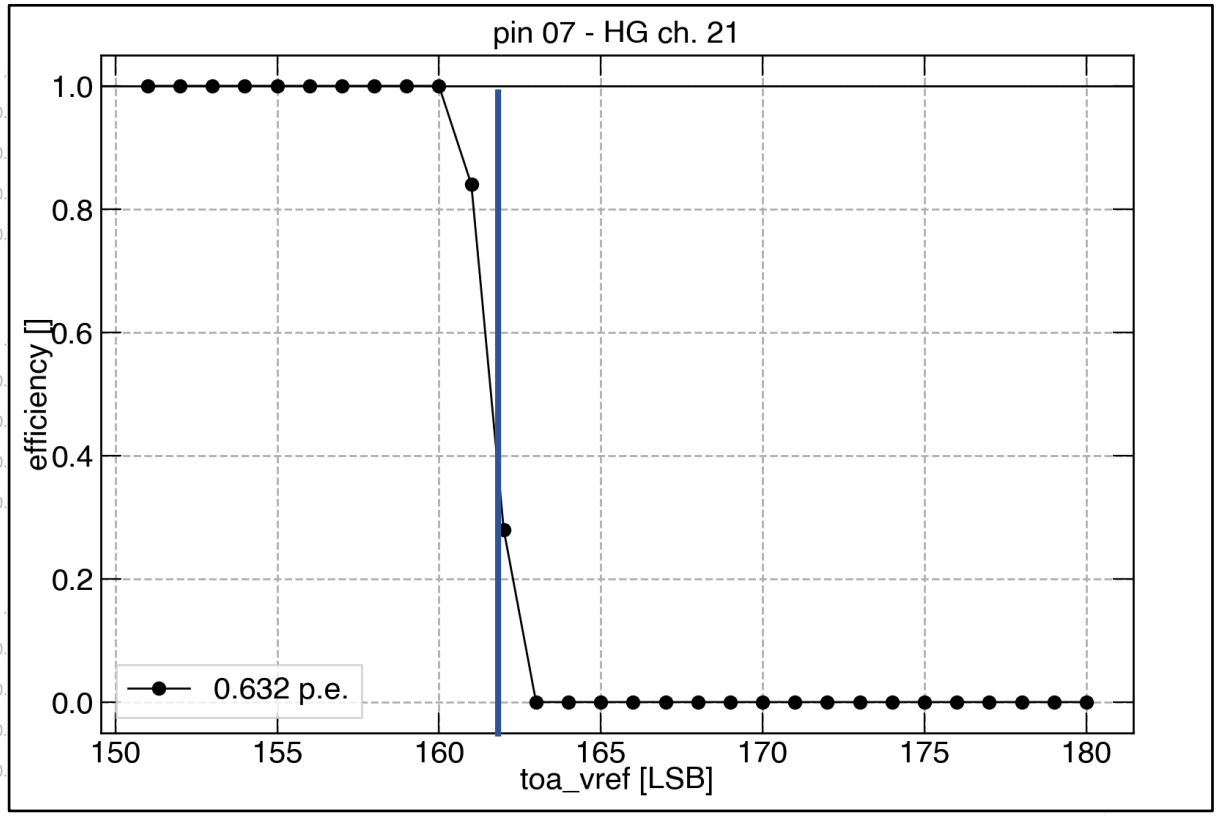

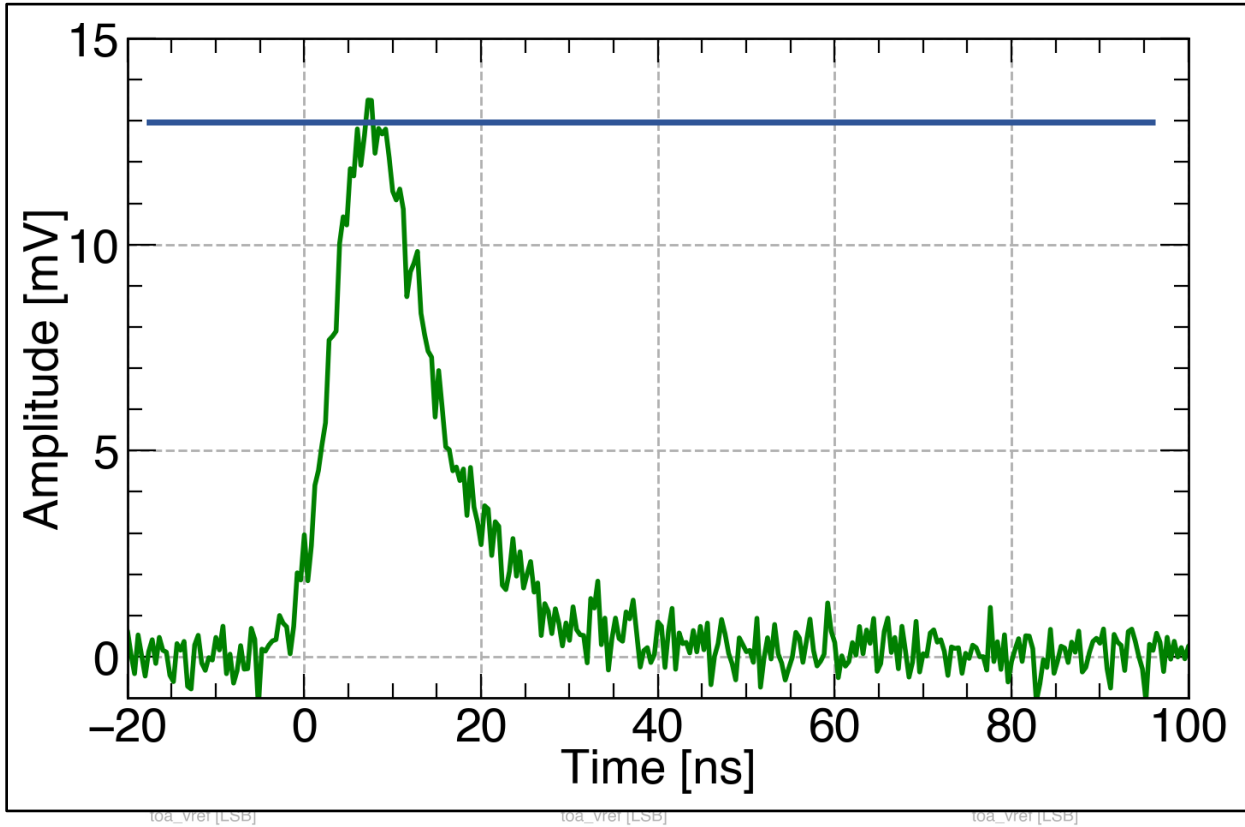

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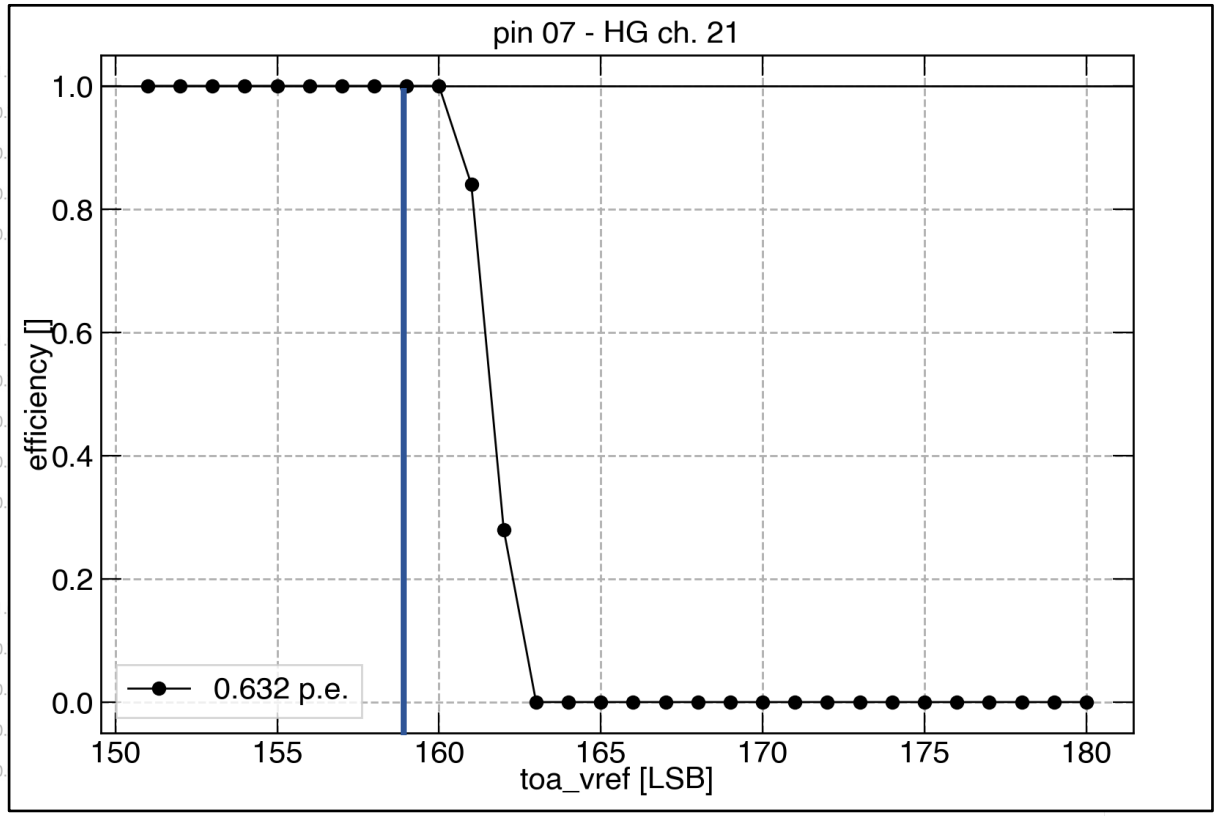
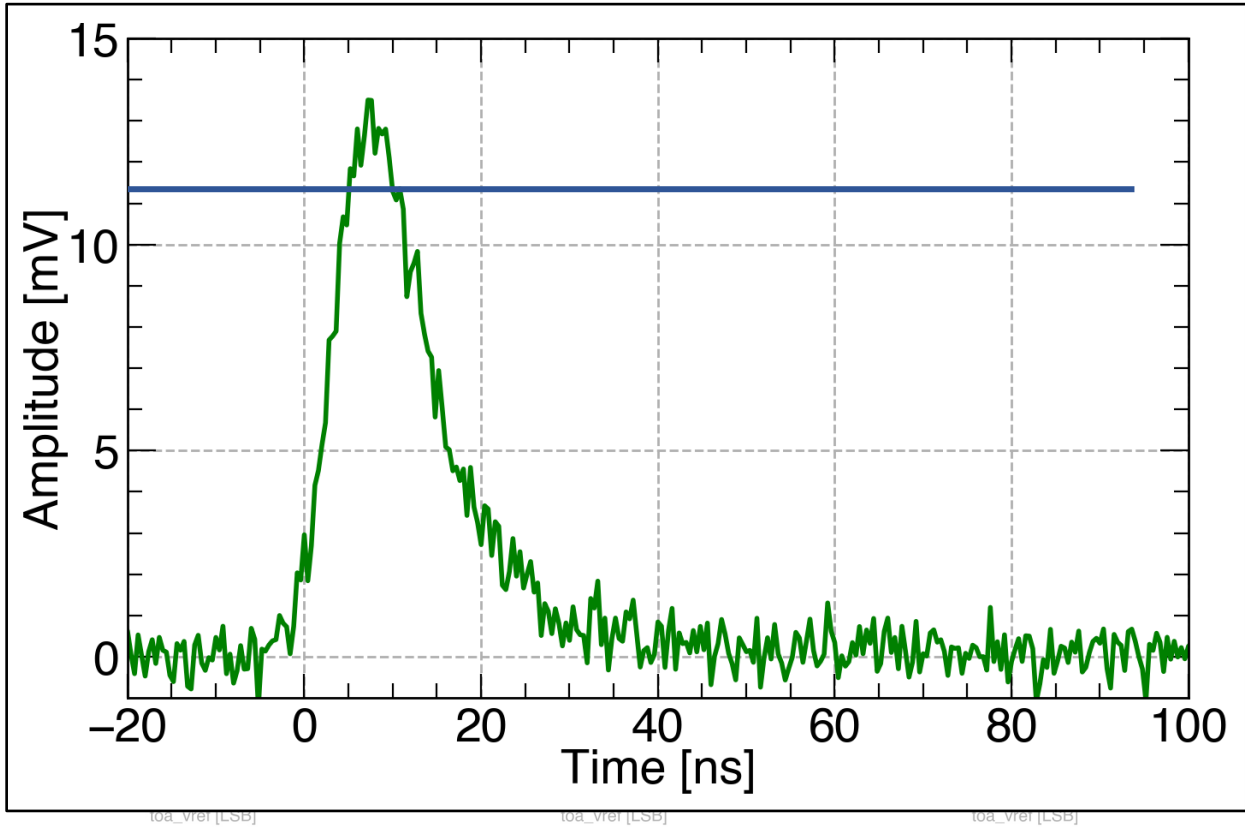
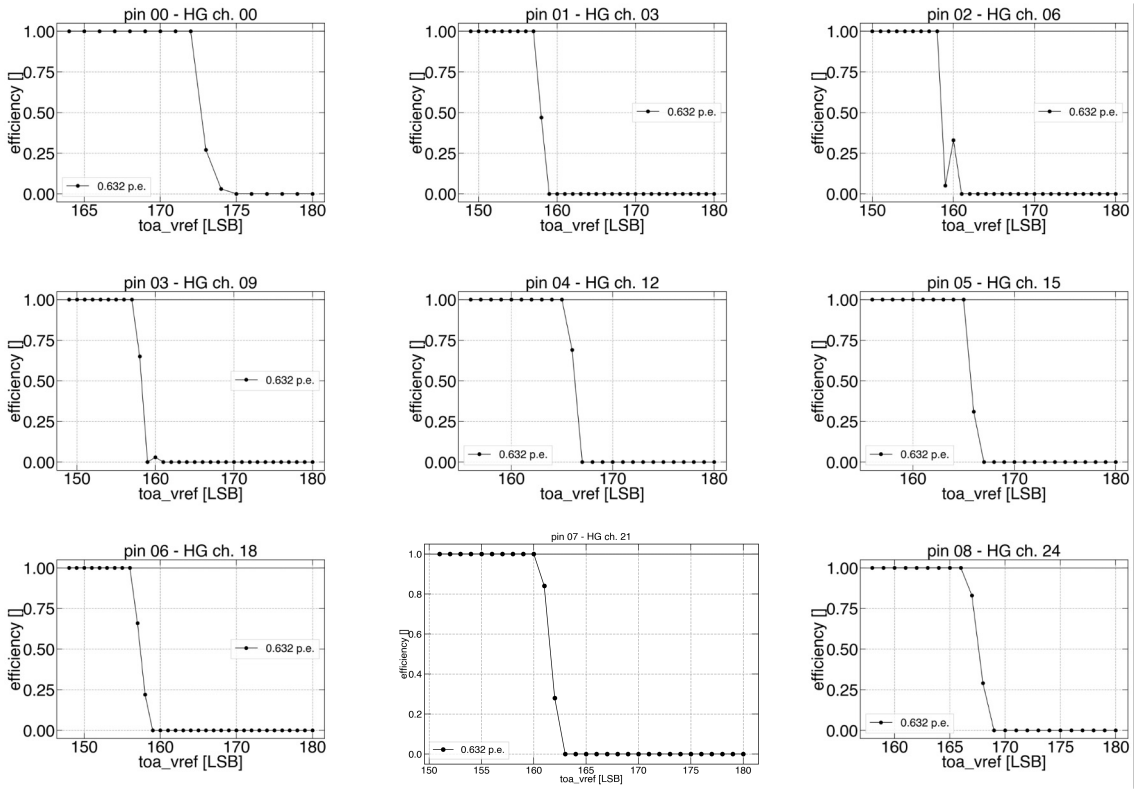


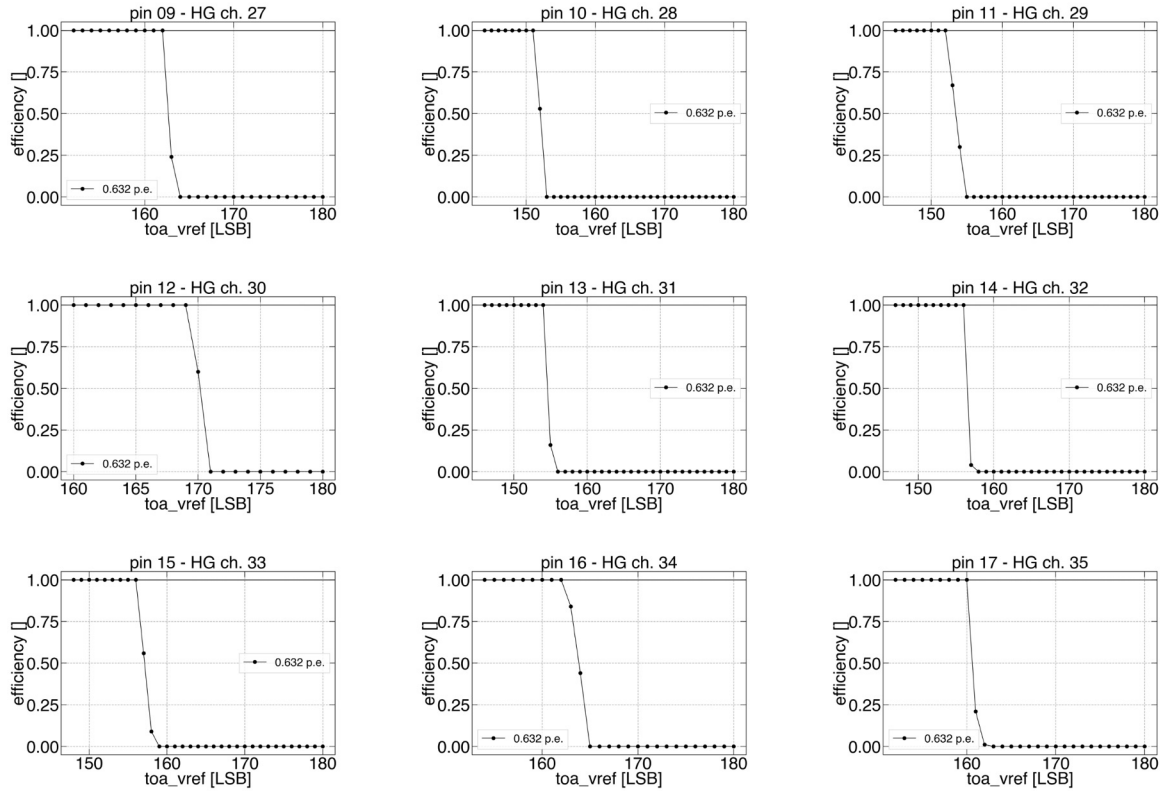


Calibration

Step II: Trigger threshold channel by channel

The global level is set after the scan

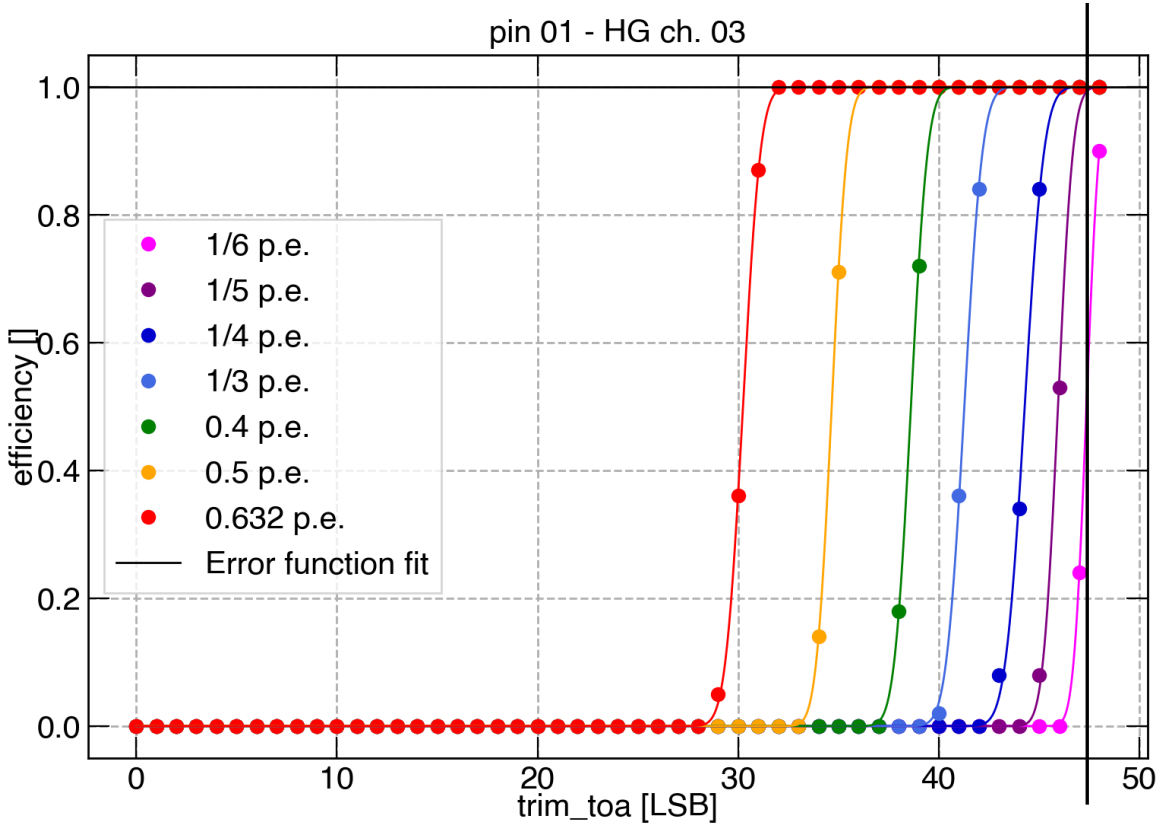




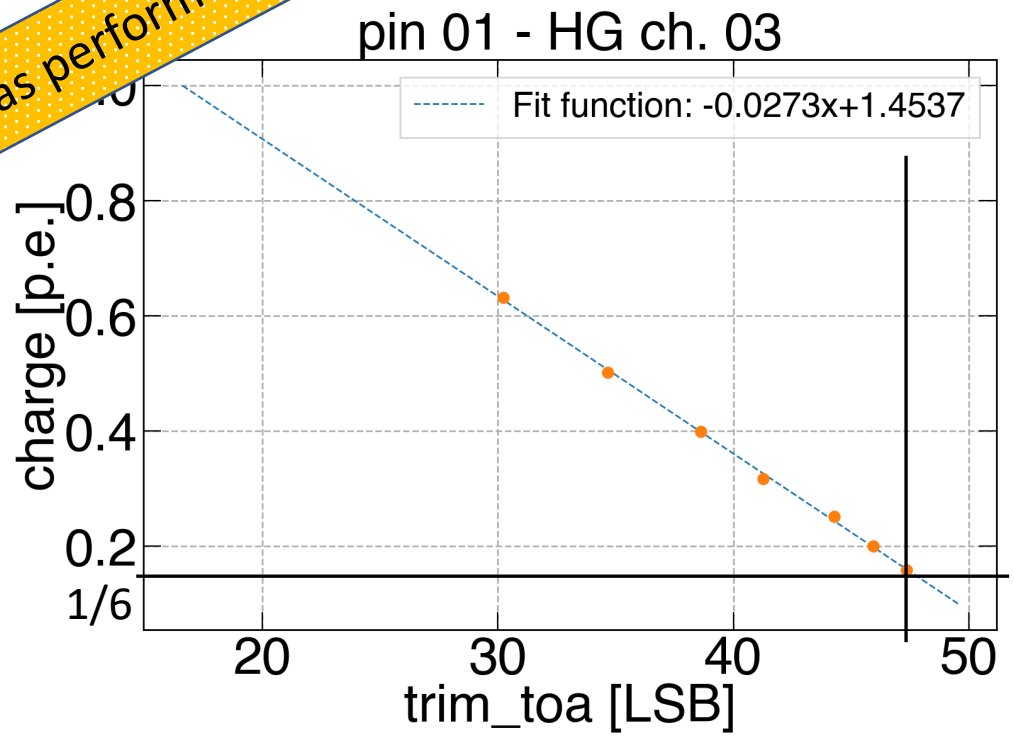
Calibration

Step II: Trigger threshold channel by channel

Secondly, we perform **fine threshold tuning** channel by channel for different
Performing fit with error function the conversion from threshold in bit charge units is done



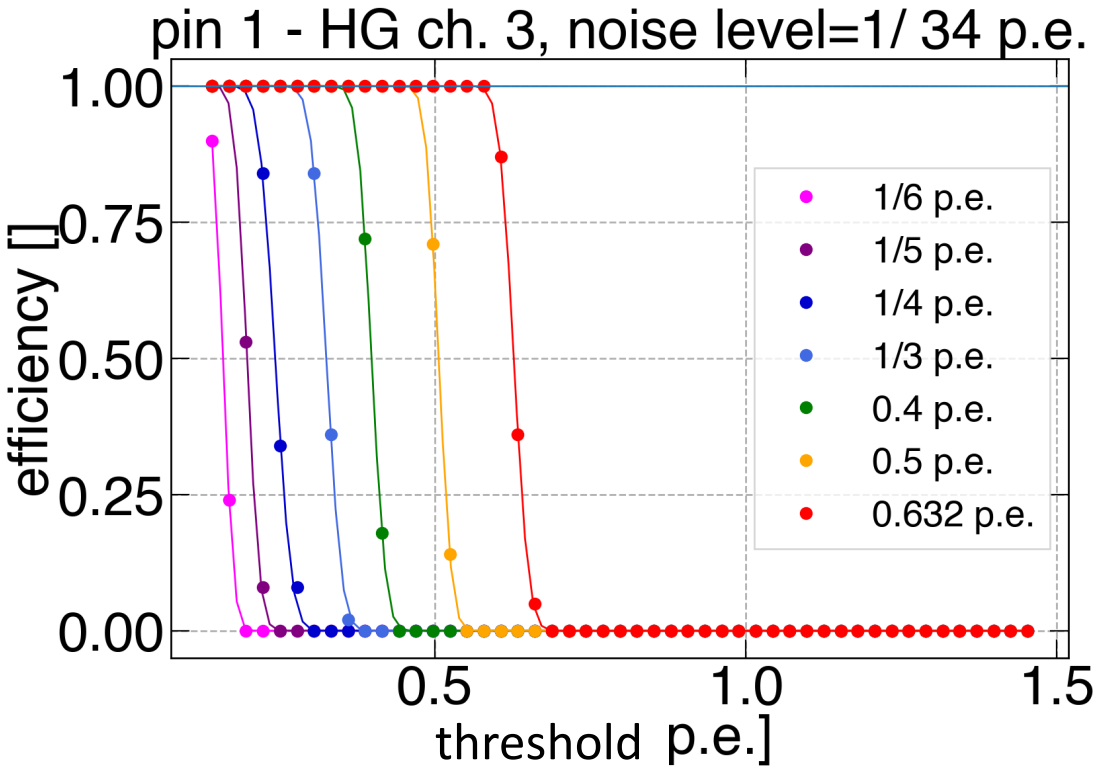
This was performed for every channel



The slow parameter corresponging to 1/6 p.e. is set

Noise level evaluation

Trigger efficiency



Fit function for efficiency plot:

$$f(x) = \frac{2}{\sqrt{\pi\sigma^2}} \int_0^x e^{-\frac{(t-x_0)^2}{2\sigma^2}} dt = \frac{2}{\sqrt{\pi}} \int_0^{\left(\frac{x-x_0}{\sigma}\right)} e^{-\frac{u^2}{2}} du = Erf\left(\frac{x-x_0}{\sigma}\right),$$

where

x – threshold level in charge units

x_0 –input charge

σ – noise

σ is extracted

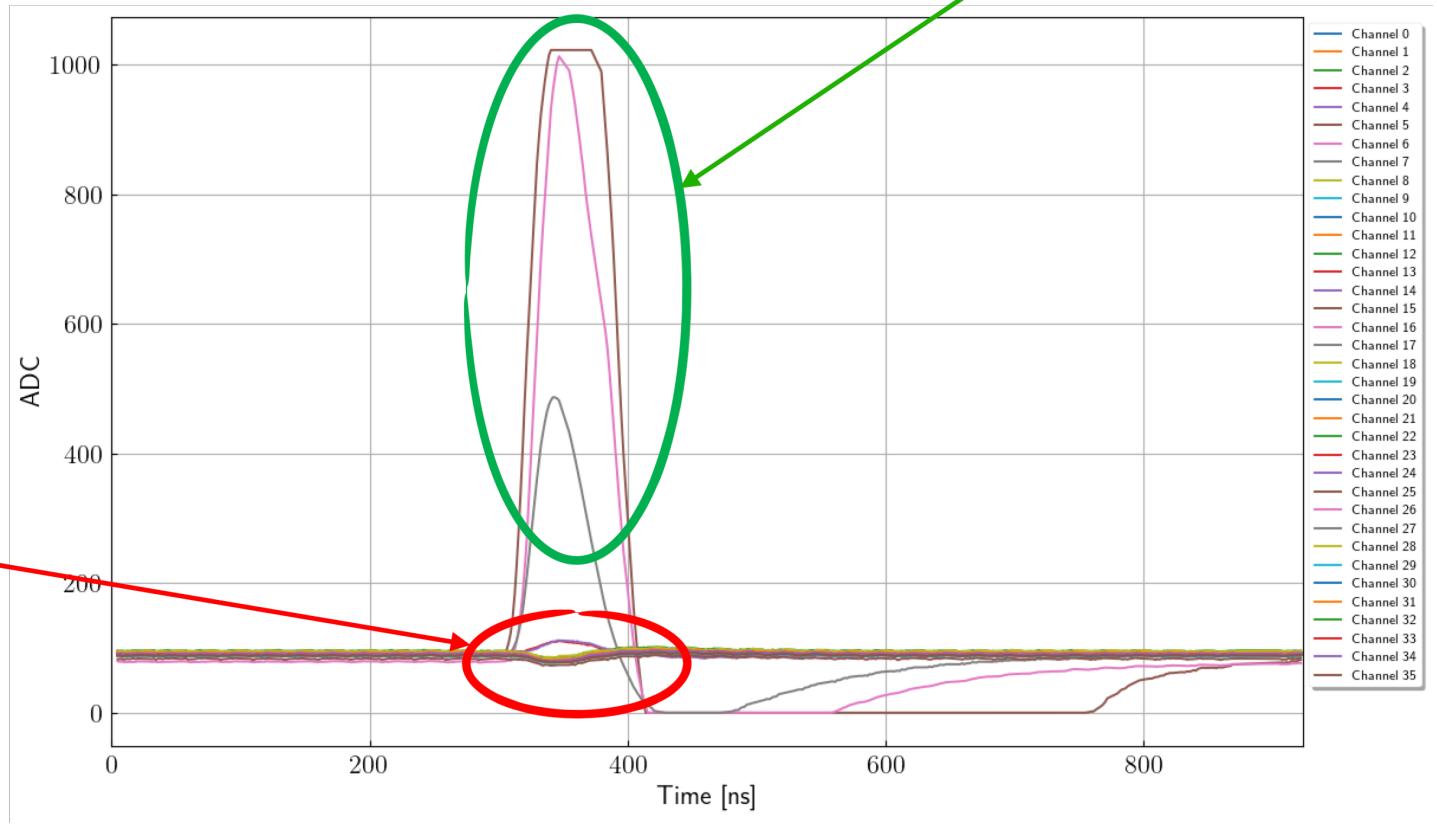
Noise level $< \frac{1}{22}$ p.e. for all channels

Cross-talk measurements

Measurement principle

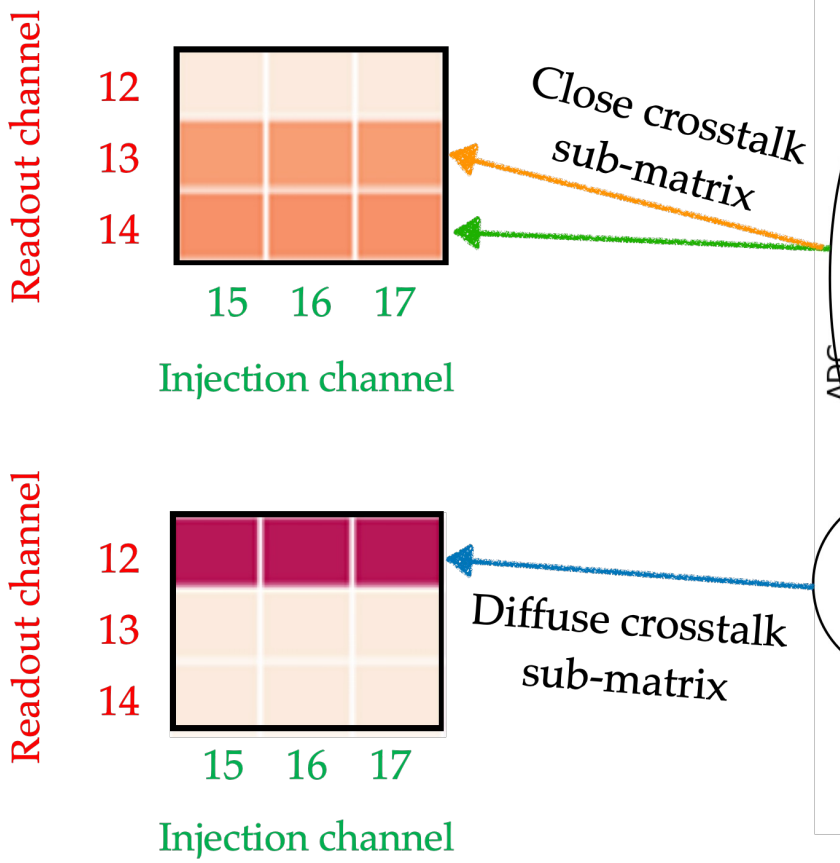
~ 800 p.e. input signal in the injection pin (HG, MG and LG channels)

Measure the output signal in the other channels

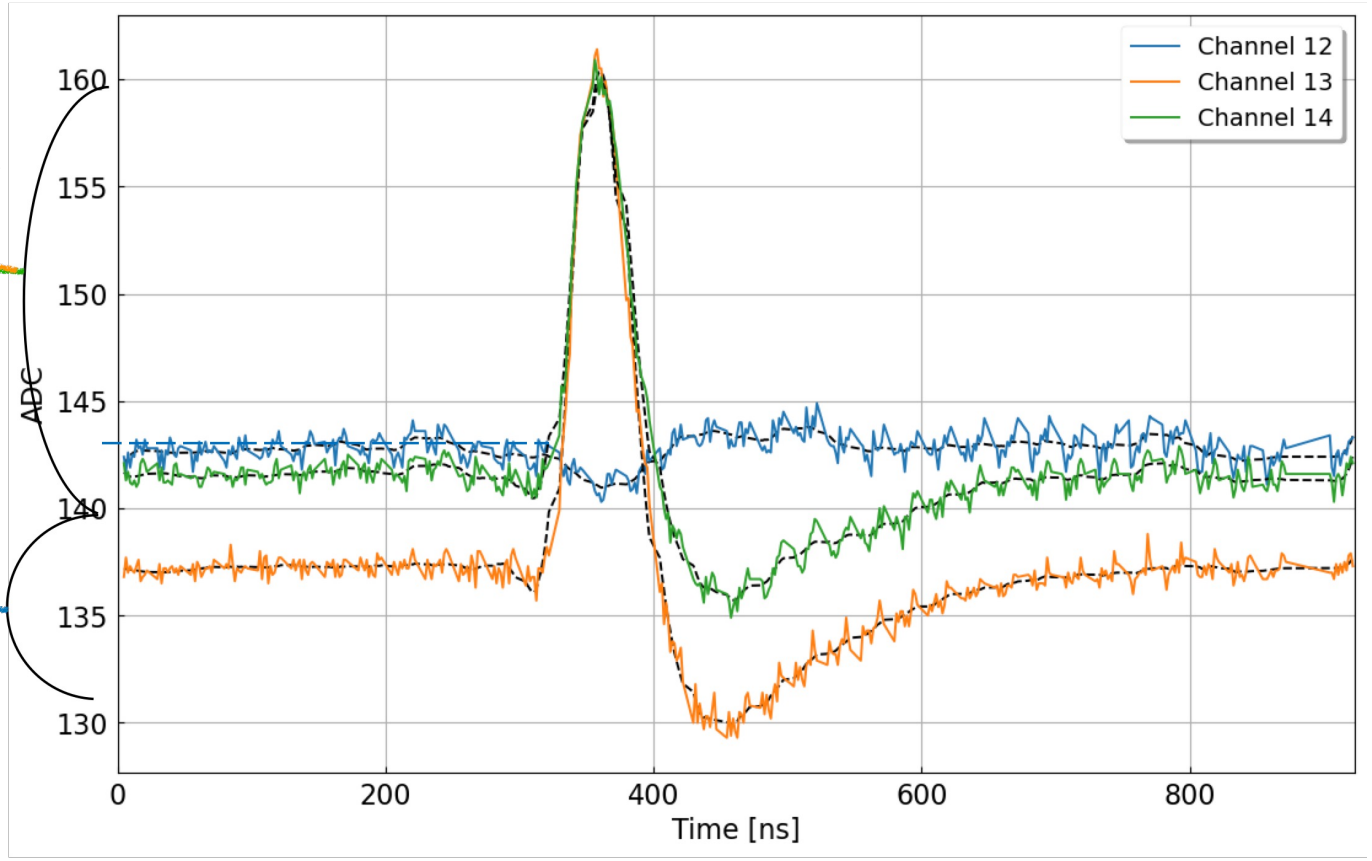


Part III: Test results

Injected channels: **15, 16, 17**
Readout channels: **12, 13, 14**

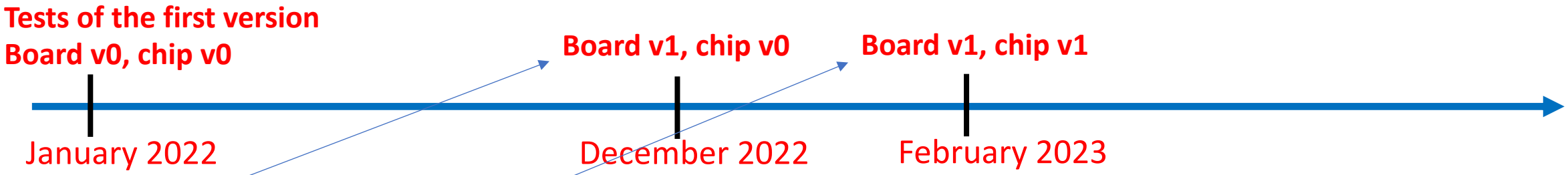


An example



Part III: Test results

Reminder



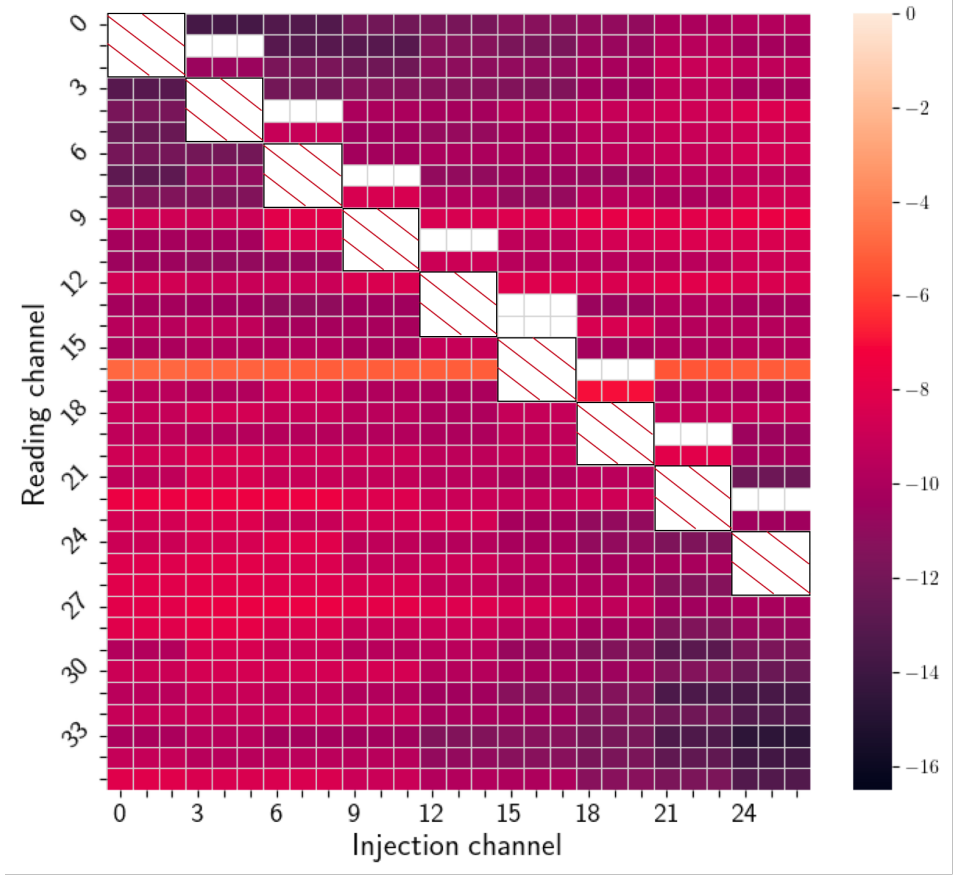
Second version of board (**board v2 BGA**) was designed mainly to reduce **close cross-talk** what was discovered for first version of board.

Second version of chip (**HKROC v1b**) was designed mainly to reduce **diffuse cross-talk** what was discovered for first version of chip.

Close cross-talk = cross-talk in neighboring channels of the injected channel
Diffuse cross-talk = cross-talk all channels

Diffuse cross-talk matrices – Board v2 (BGA)

Chip v0 [ADC units]

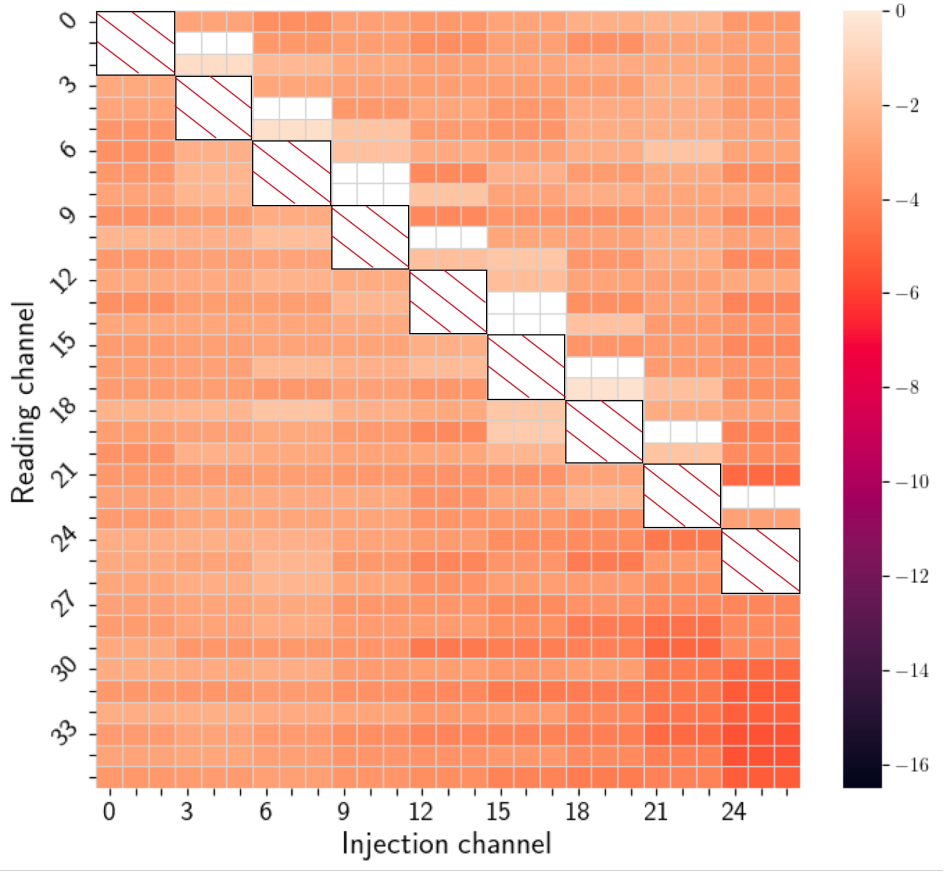


Comparison of different chips

Diffuse XT Reduction

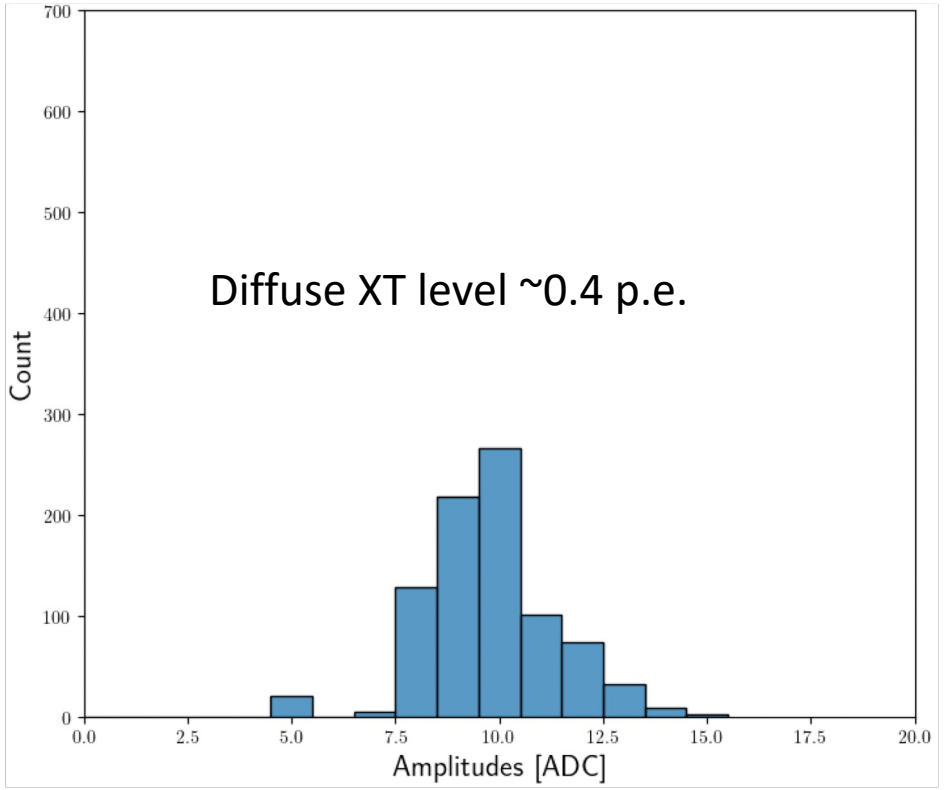
from v0 to v1b
(chip-to-chip)

Chip v1b [ADC units]



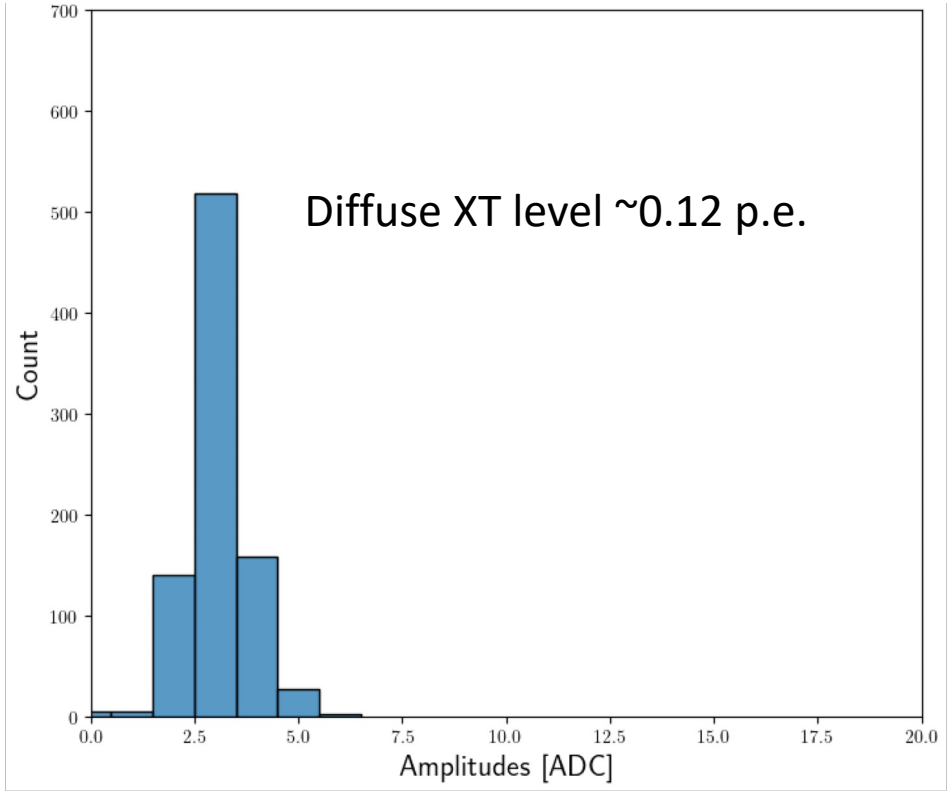
Indeed, diffuse XT came from the chip

Diffuse cross-talk distribution (taking amplitudes of diff. XT from all channels)



Diffuse XT Reduction

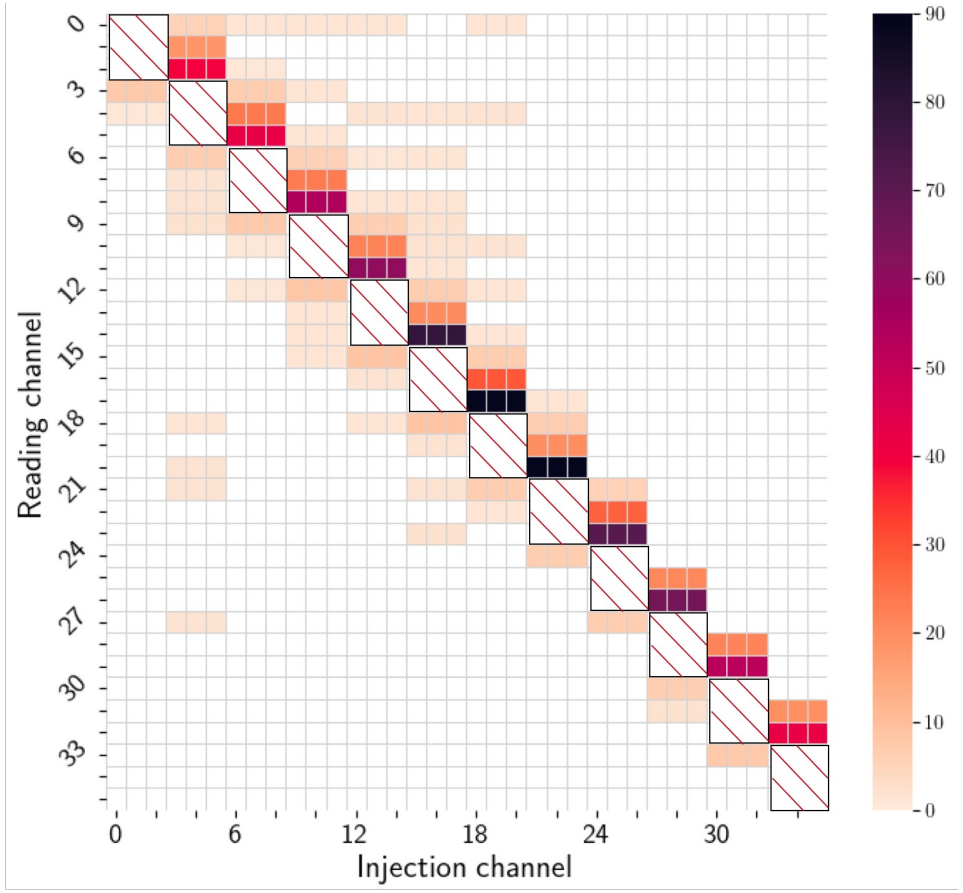
from v0 to v1b
(chip-to-chip)



From chip v0 to v1b: **Factor 3 of reduction** of diffuse XT
Diffuse cross-talk level: **0.12 p.e**.

Close cross-talk matrices – chip v1b

Board v1 (Mezzanine) [ADC units]



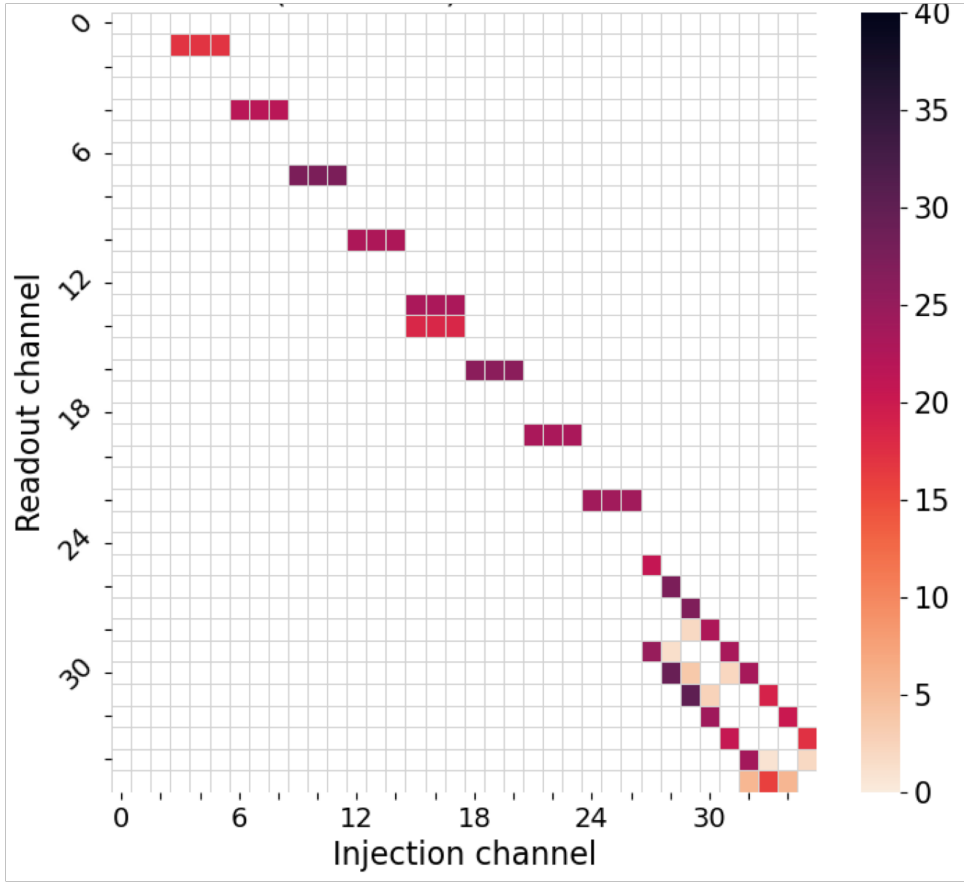
High Xtalk in previous Low Gain and Medium Gain channels

Comparison of different boards

Close XT Reduction

from v1 to v2 (board-to-board)

Board v2 (BGA) [ADC units]

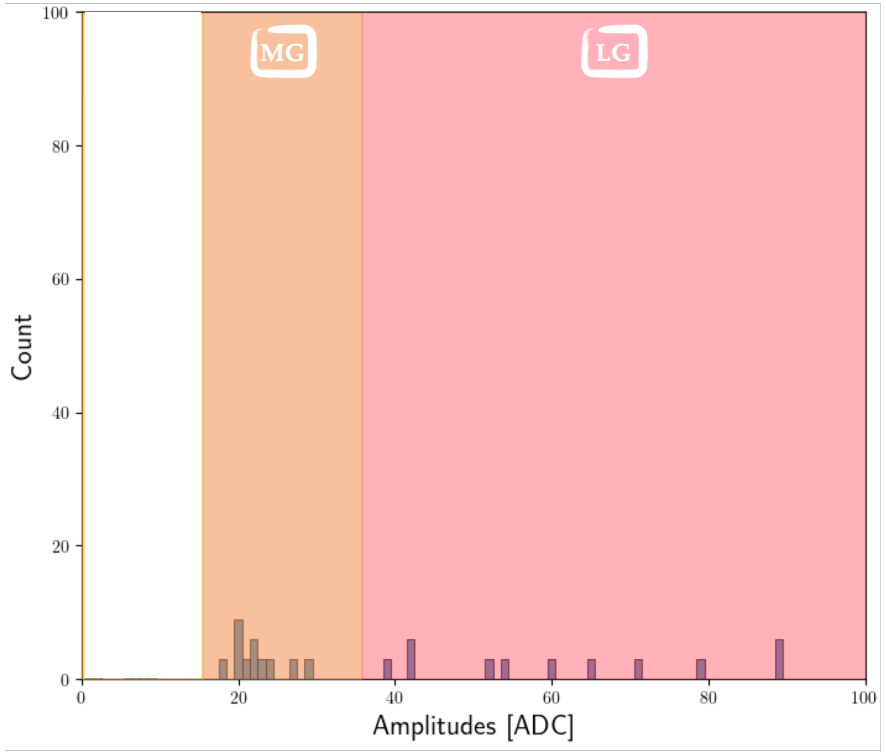


Xtalk only in Medium Gain channels

Part III: Test results

Close cross-talk distribution (taking amplitudes of diff. XT from all channels)

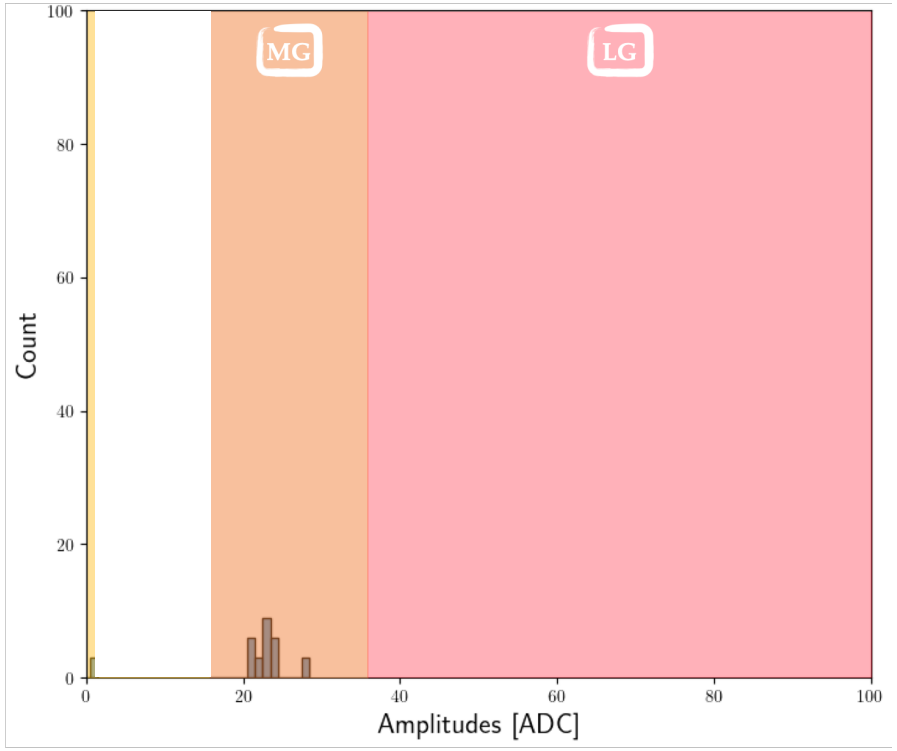
Board v1 (Mezzanine)



Close XT Reduction

on HG and LG ch.

Board v2 (BGA)



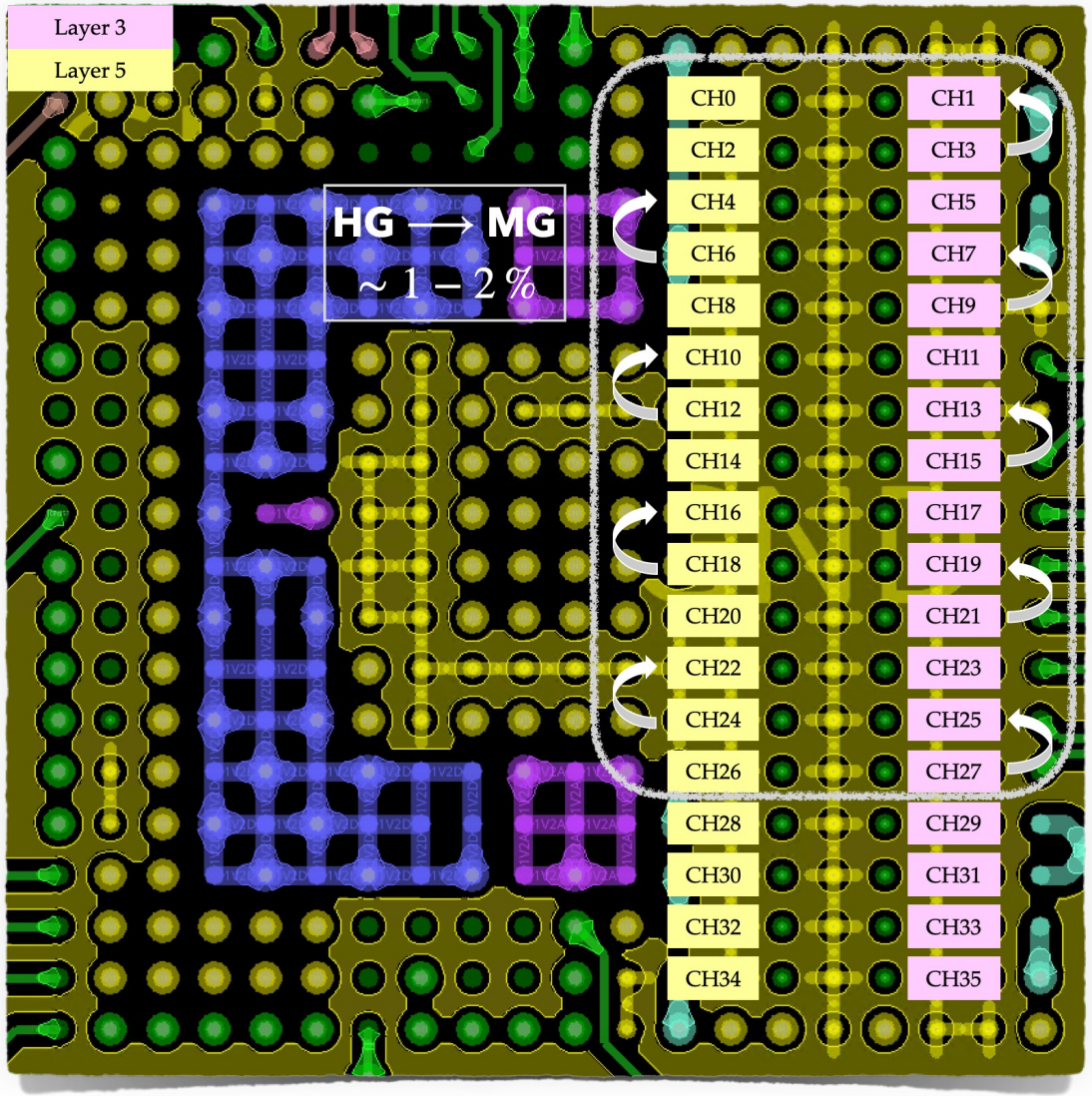
Conclusions:

Suppression of the close cross-talk : HG ch. ➡ HG + LG ch.
Survival 1-2 % close cross-talk: HG ch. ➡ MG ch.
Abnormal 5-6% close cross-talk HG ch. 15 ➡ LG ch. 14.

Part III: Test results

Why close cross-talk was reduced?

The BGA-packaged HKROC has been designed so its input lines are alternated on two different layers separated by a ground layer.



Conclusion of cross-talk measurements

Diffuse cross-talk:

From chip v0 to v1b: Factor 3 of reduction

Diffuse cross-talk level: 0.12 p.e.

Close cross-talk:

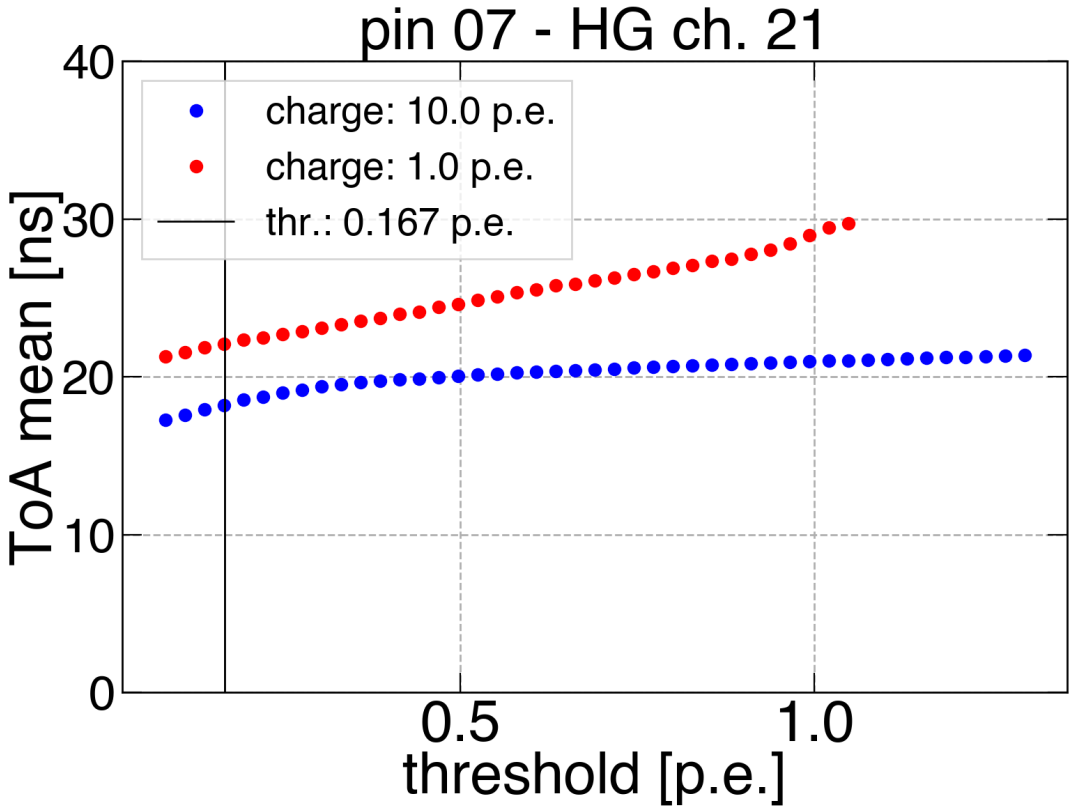
Suppression of the close cross-talk : HG ch. ➡ HG + LG ch.

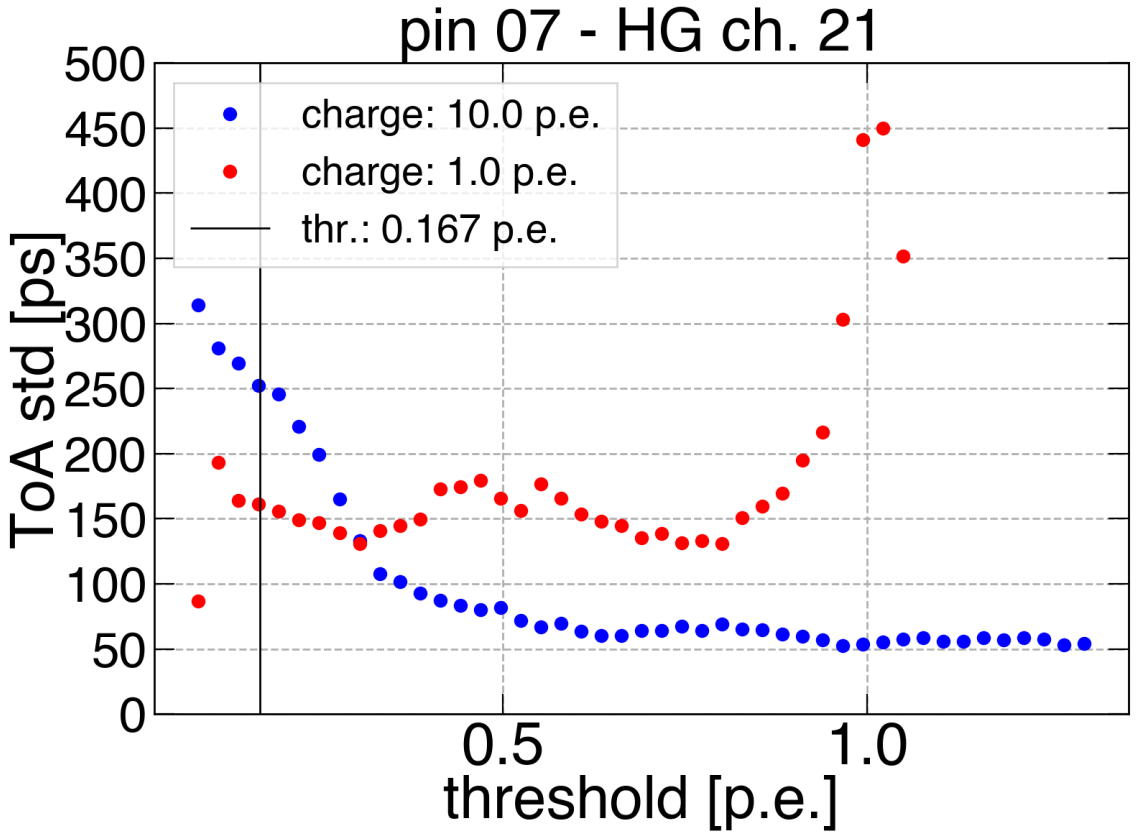
Survival 1-2 % close cross-talk: HG ch. ➡ MG ch.

Abnormal 5-6% close cross-talk HG ch. 15 ➡ LG ch. 14.

Time measurements

Example for channel 21

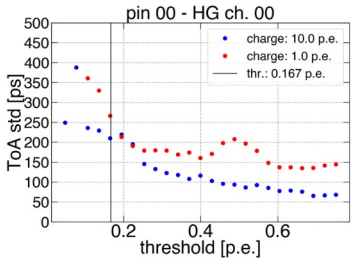


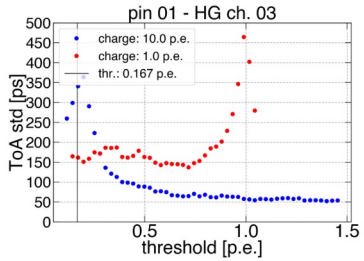


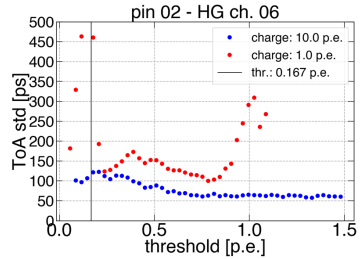
Time resolution: 150 p.s for 1 p.e
50 p.s for 10 p.e.

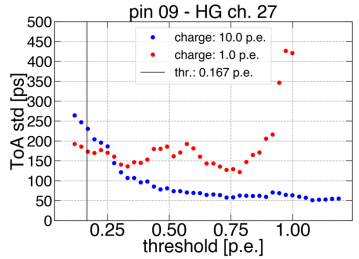
Part III: Test results

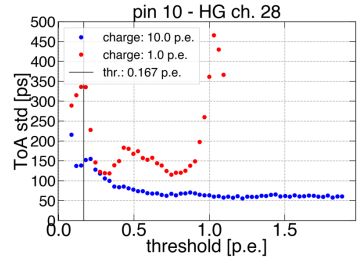
Time measurements

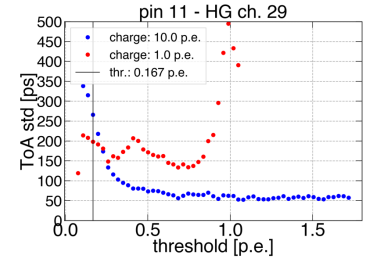


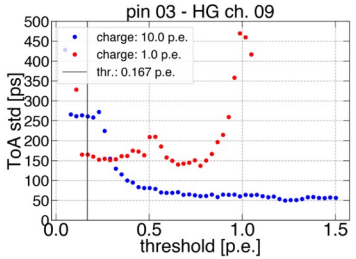


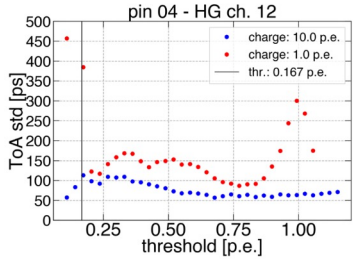


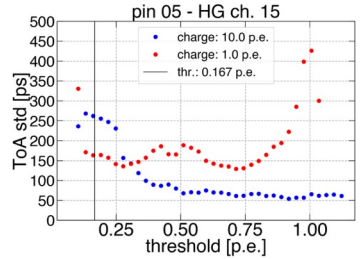


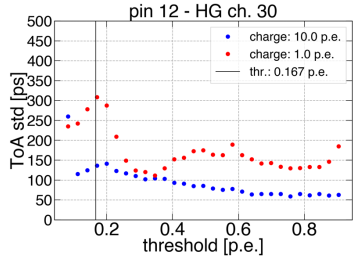


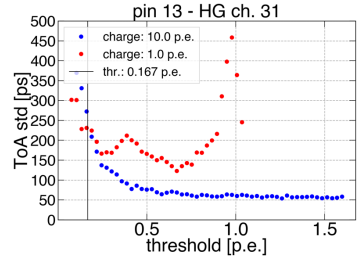


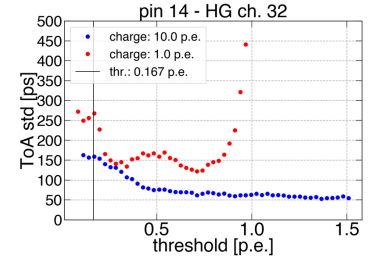


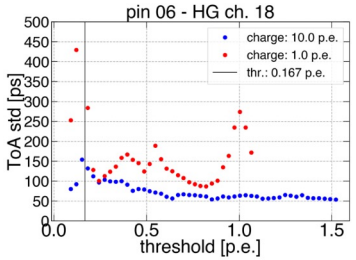


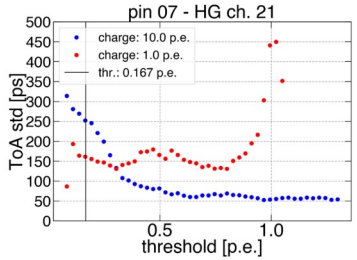


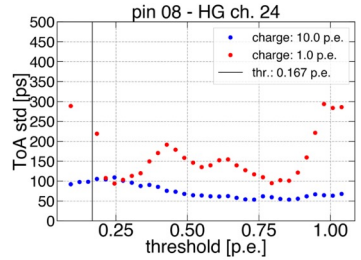


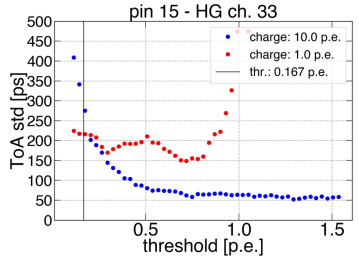


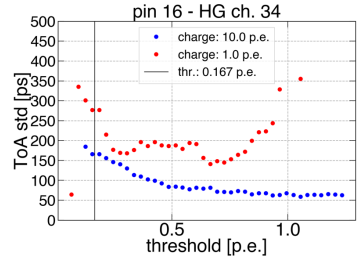


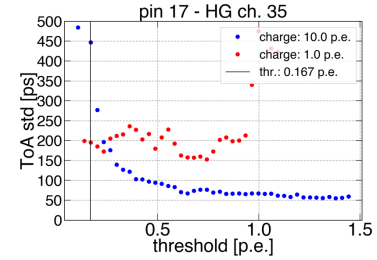






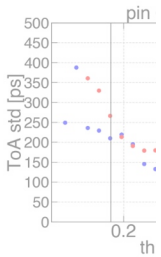


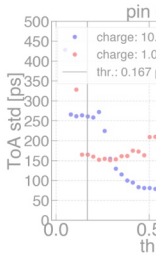


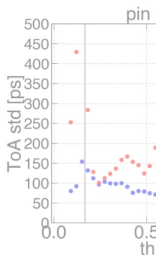


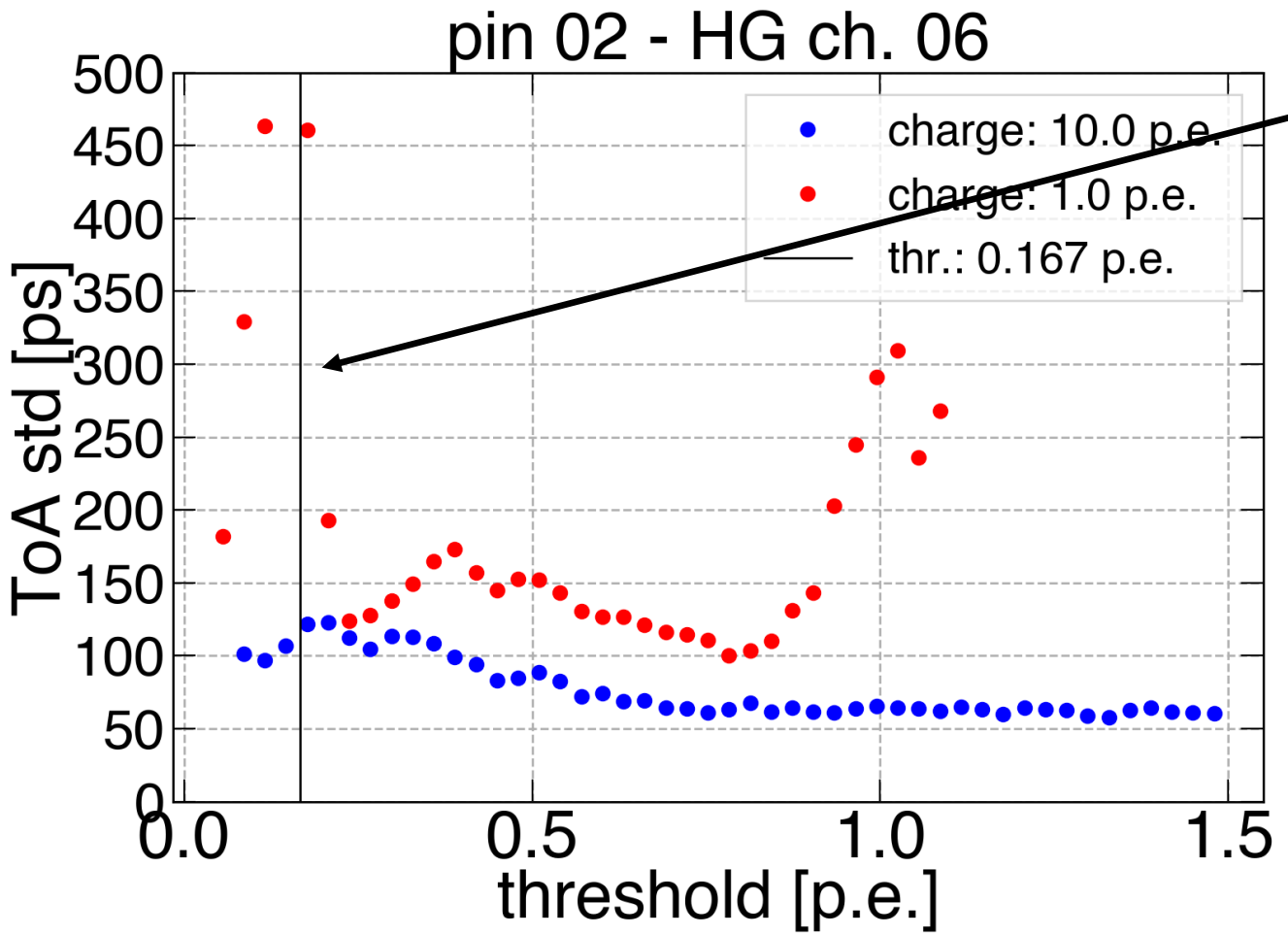
Part III: Test results

Time measurements







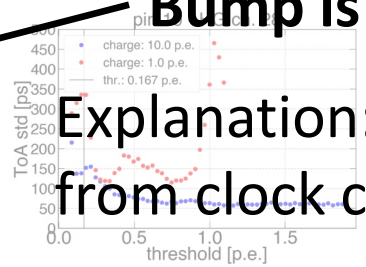


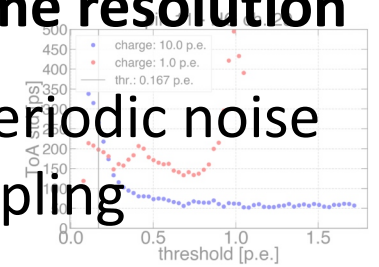
Bump is time resolution

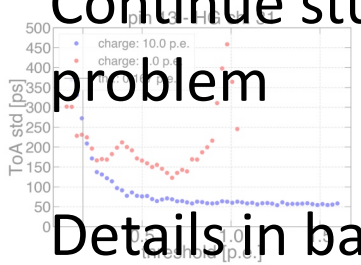
Explanation: periodic noise from clock coupling

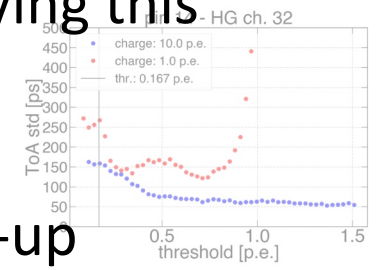
Continue studying this problem

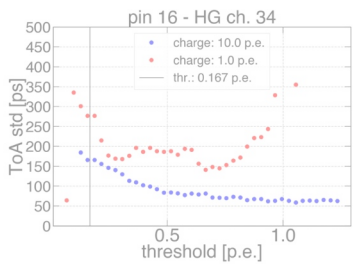
Details in back-up

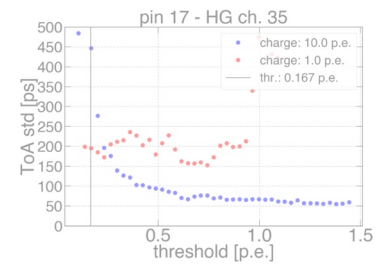












Part III:
The results of the performed tests

- Calibration
- Noise evaluation
- Time measurements
- Cross-talk measurements
- Charge measurements

Part III:
The results of the performed tests

Charge measurements

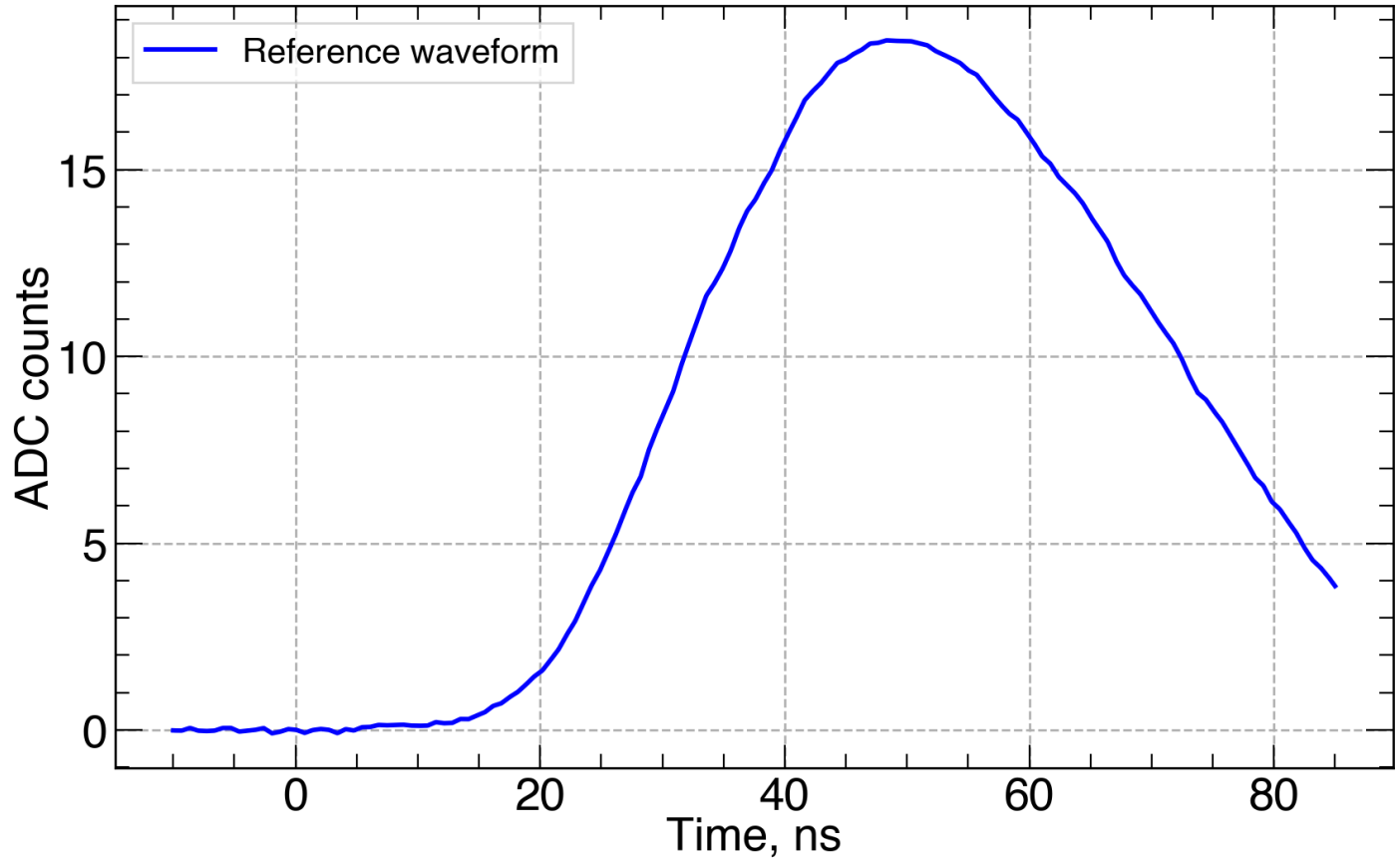
Benjamin Quilon: ”Be aware, it is the trickiest part of the analysis”
Rudolph and Denis: “Thanks for motivation!”

We are close to the end…

Algorithm for charge reconstruction

Step 1: Building the reference waveform

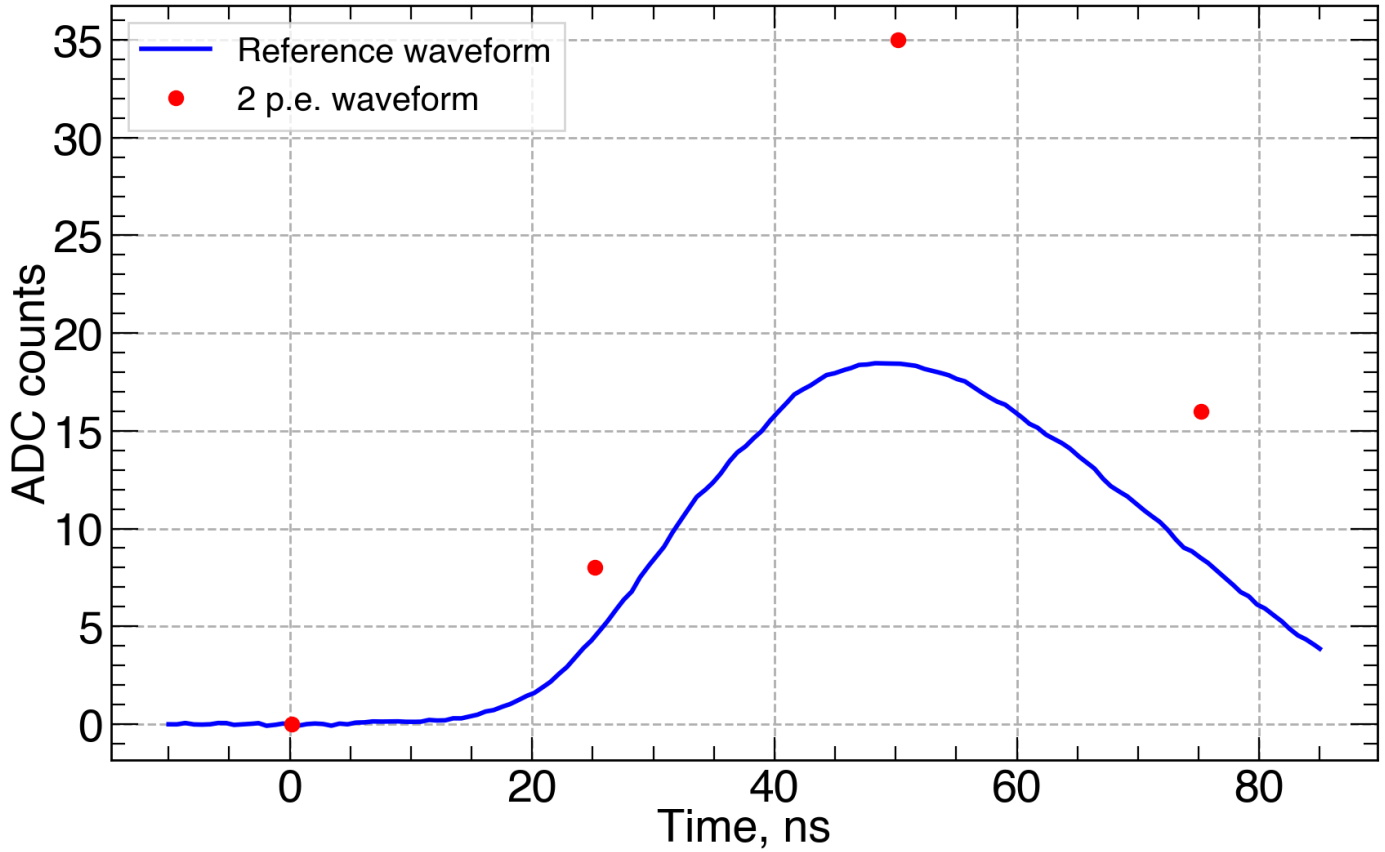
It can be waveform corresponding to 1 p.e., for instance



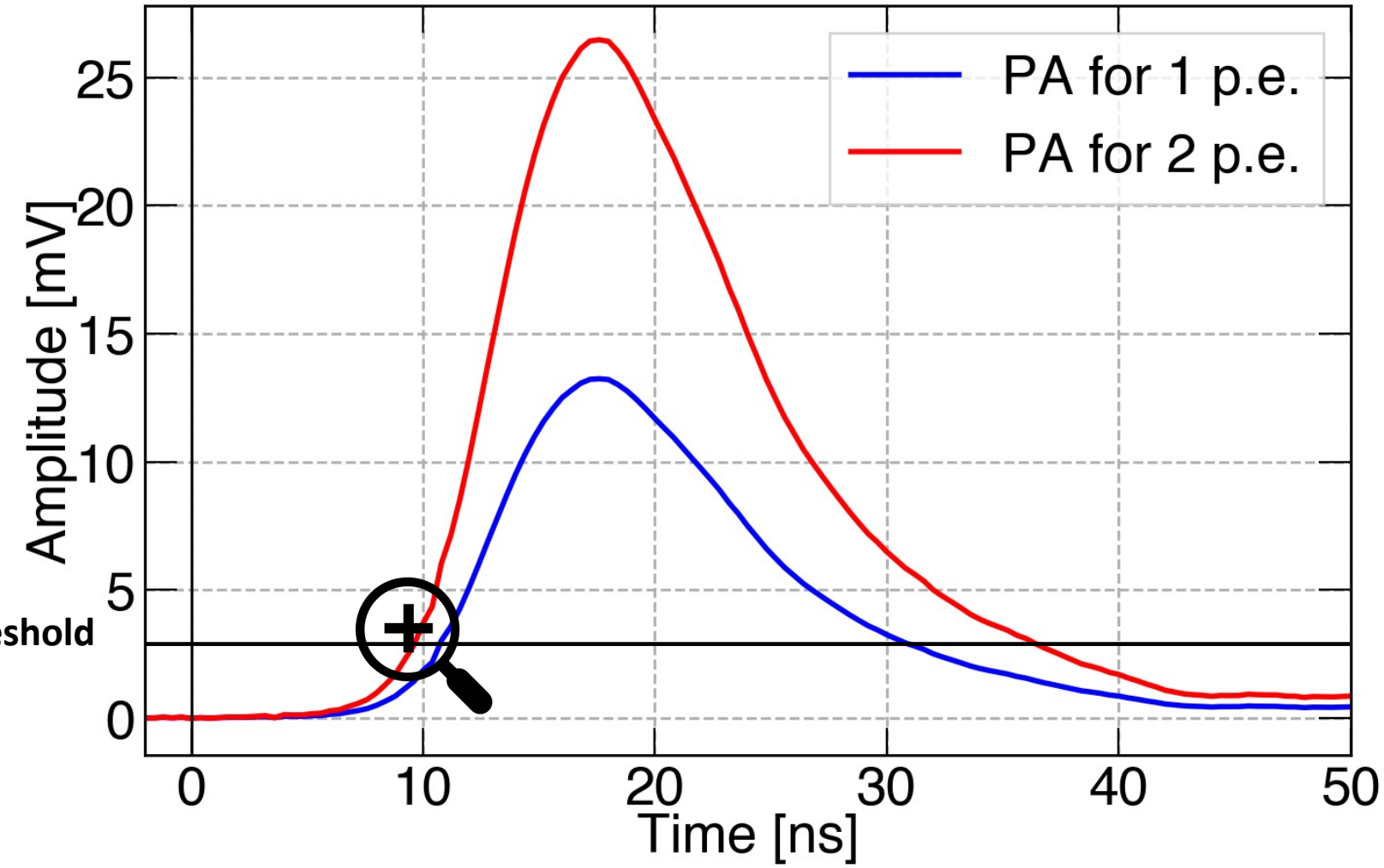
Algorithm for charge reconstruction

Step 2: Digitisation of the waveforms for other charges

For each waveform from 3 to 7 points can be digitised



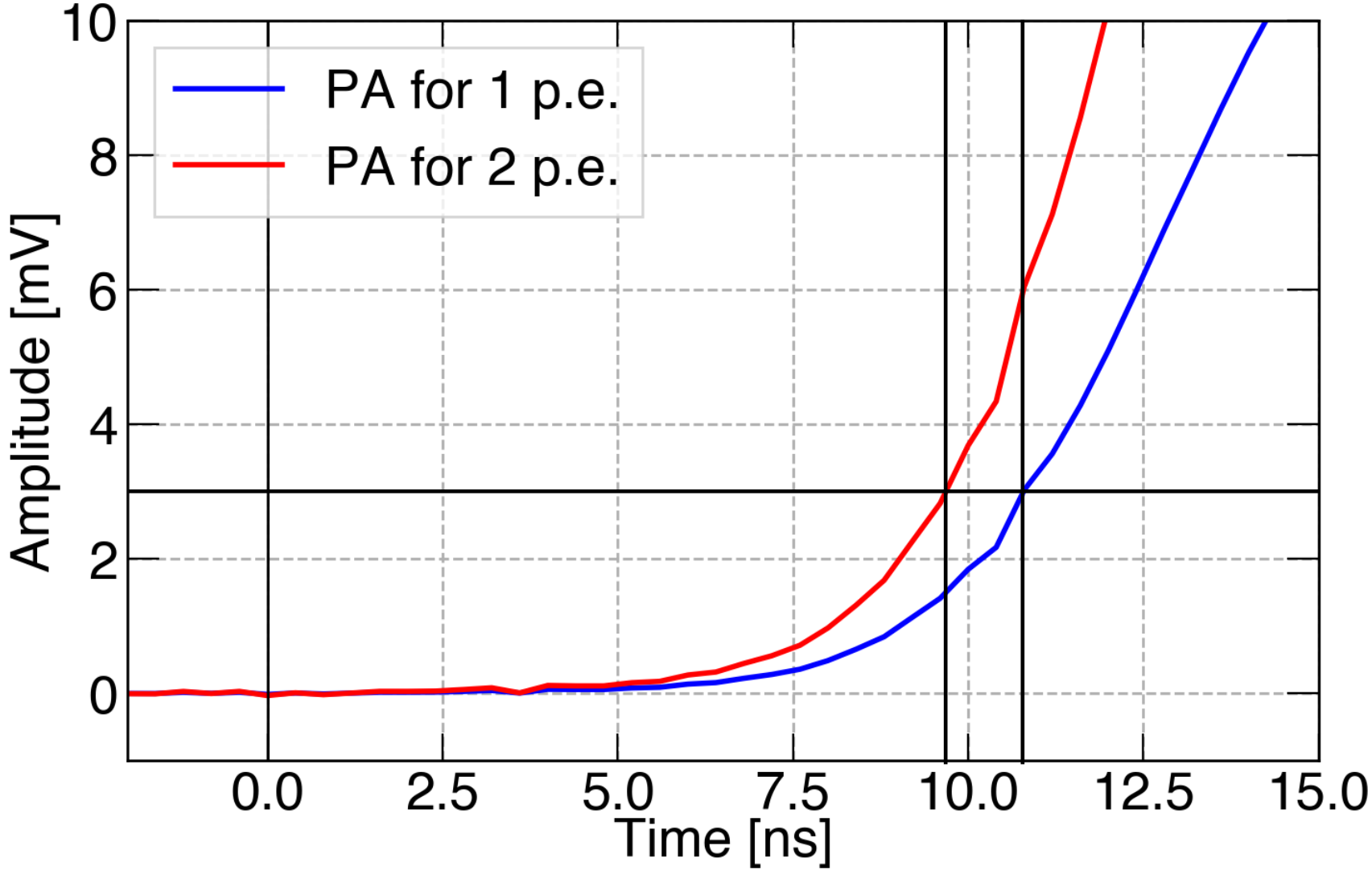
Step 3: Timewalk correction



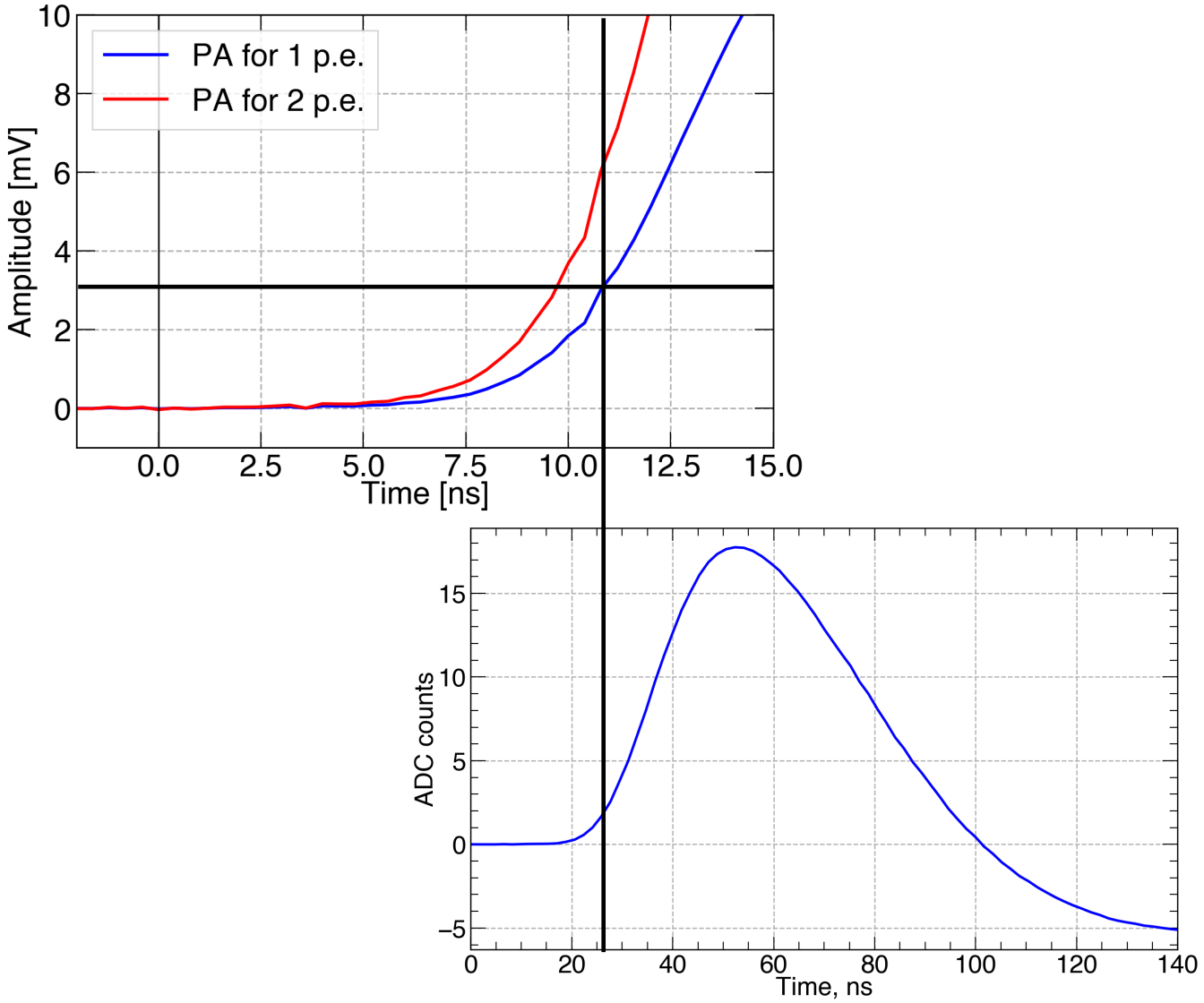
Trigger threshold

Step 3: Timewalk correction

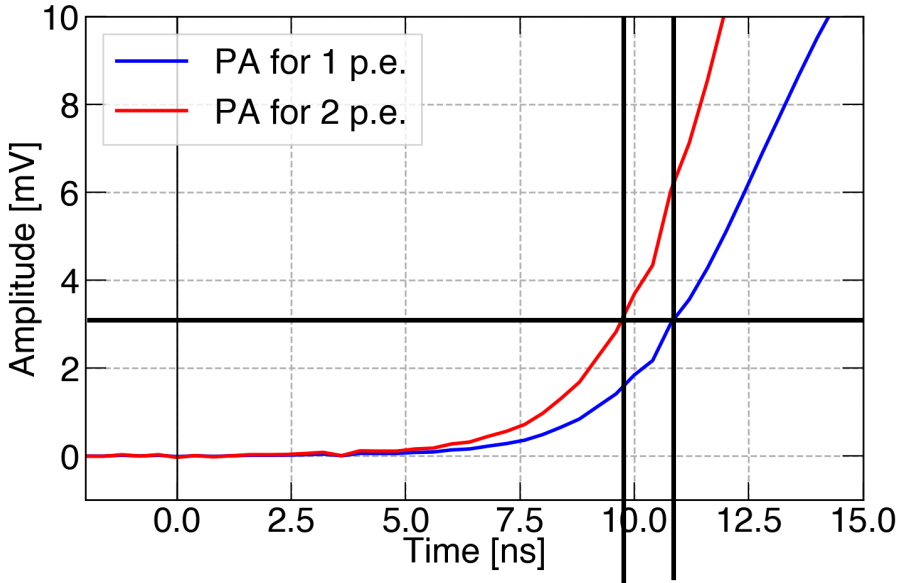
Trigger threshold

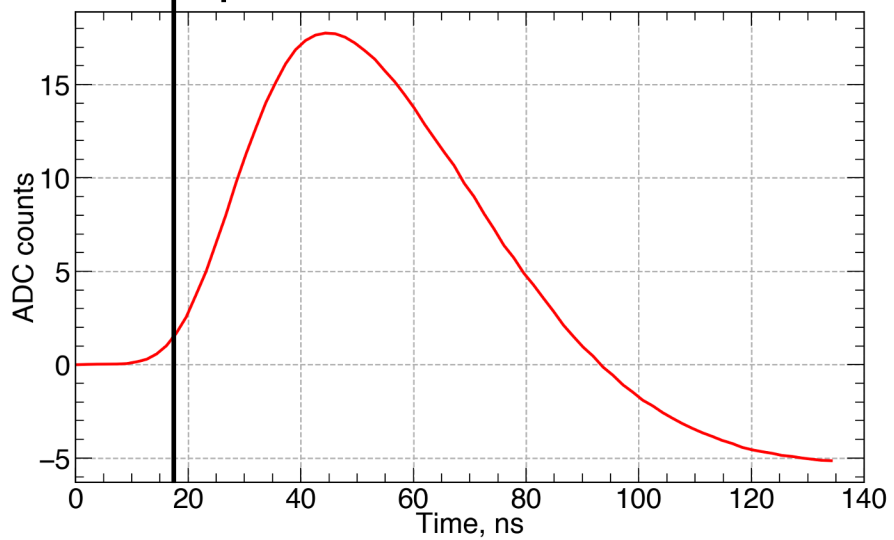


Step 3: Timewalk correction

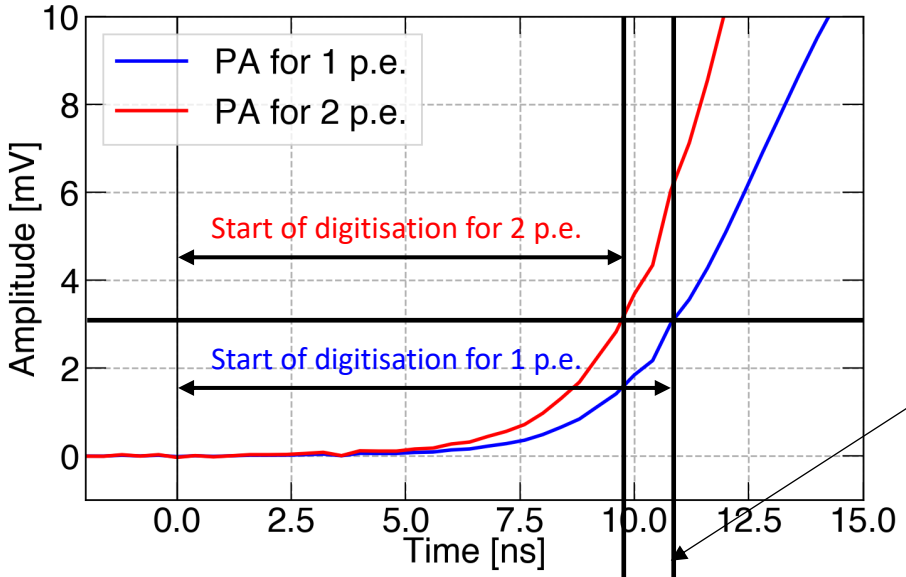


Step 3: Timewalk correction



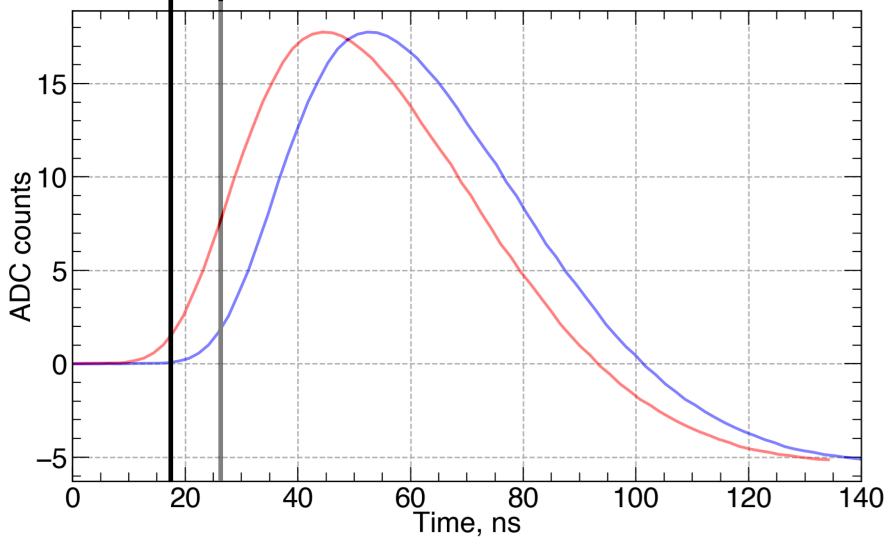


Step 3: Timewalk correction



Here the effect exaggerated for visuality.
The shift is of order 1 ns

Here reconstructed wv are normalised by 1 p.e.



Waveforms have different amplitudes

⬇

Waveforms have different trigger time

⬇

Start of digitisation start at different time moment

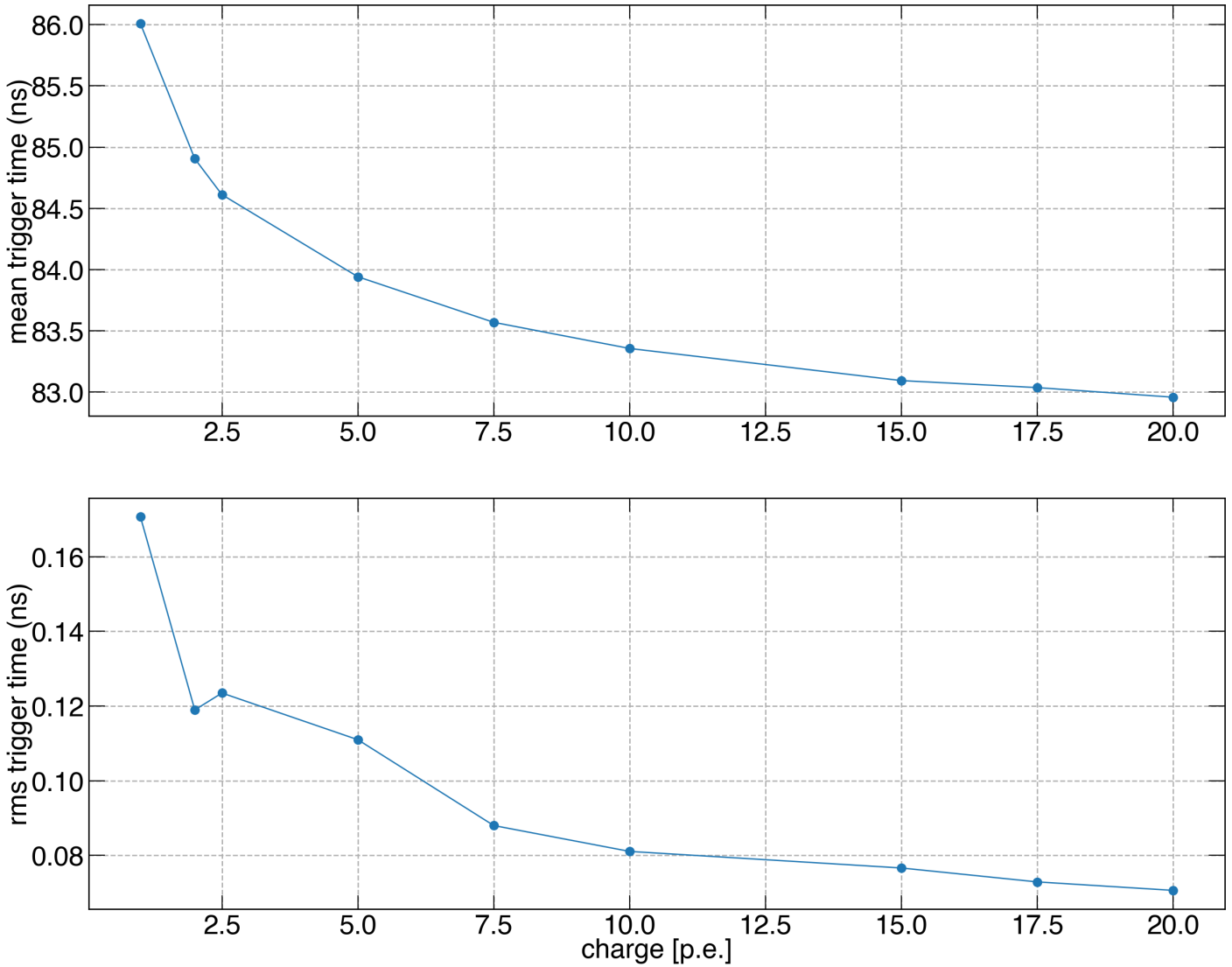
⬇

Reconstructed waveforms for different charges are shifted in time

Step 3: Timewalk correction

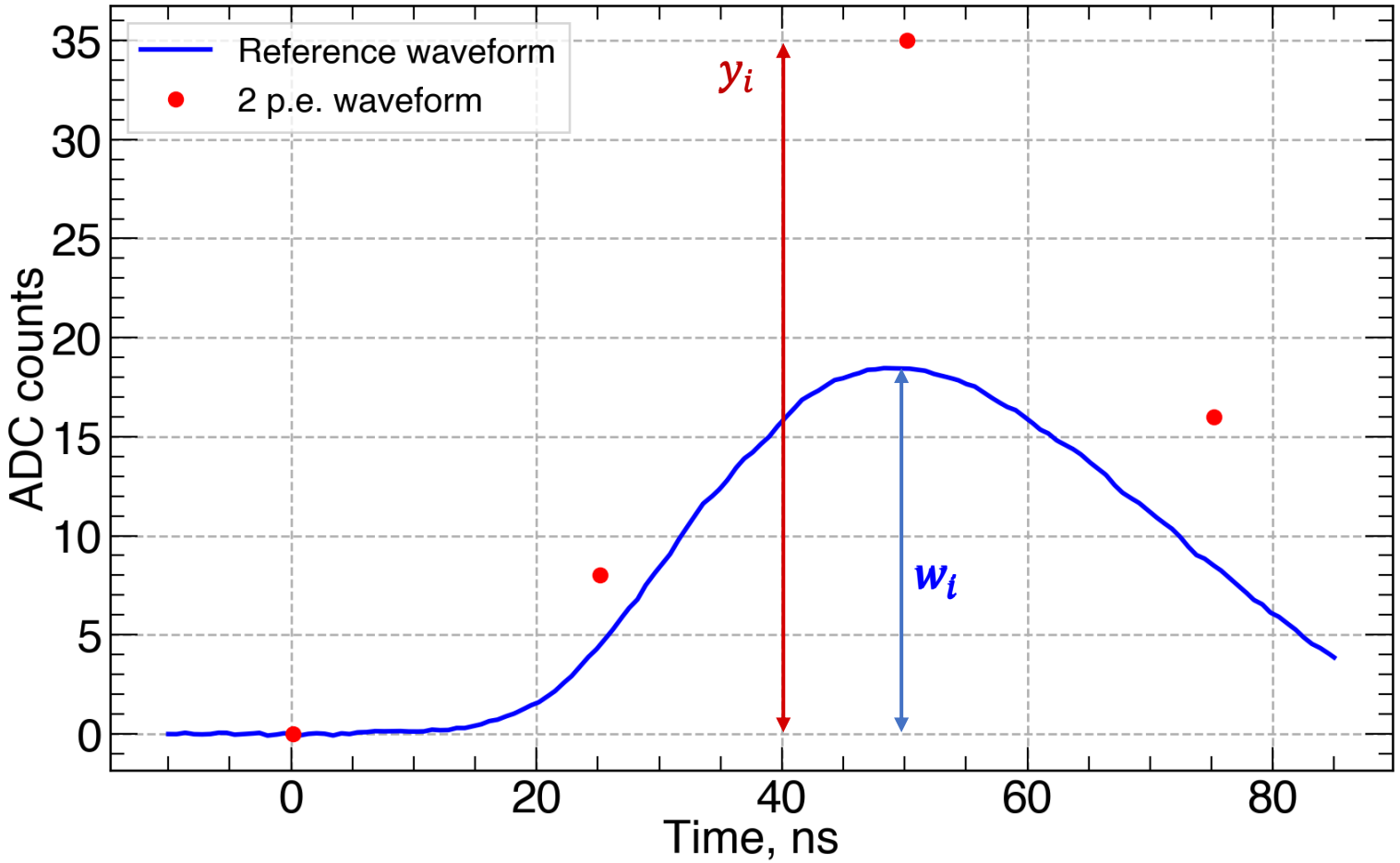
Example for channel 0

Trigger time dependence on ingected charge



Step 4: Charge inference from χ^2

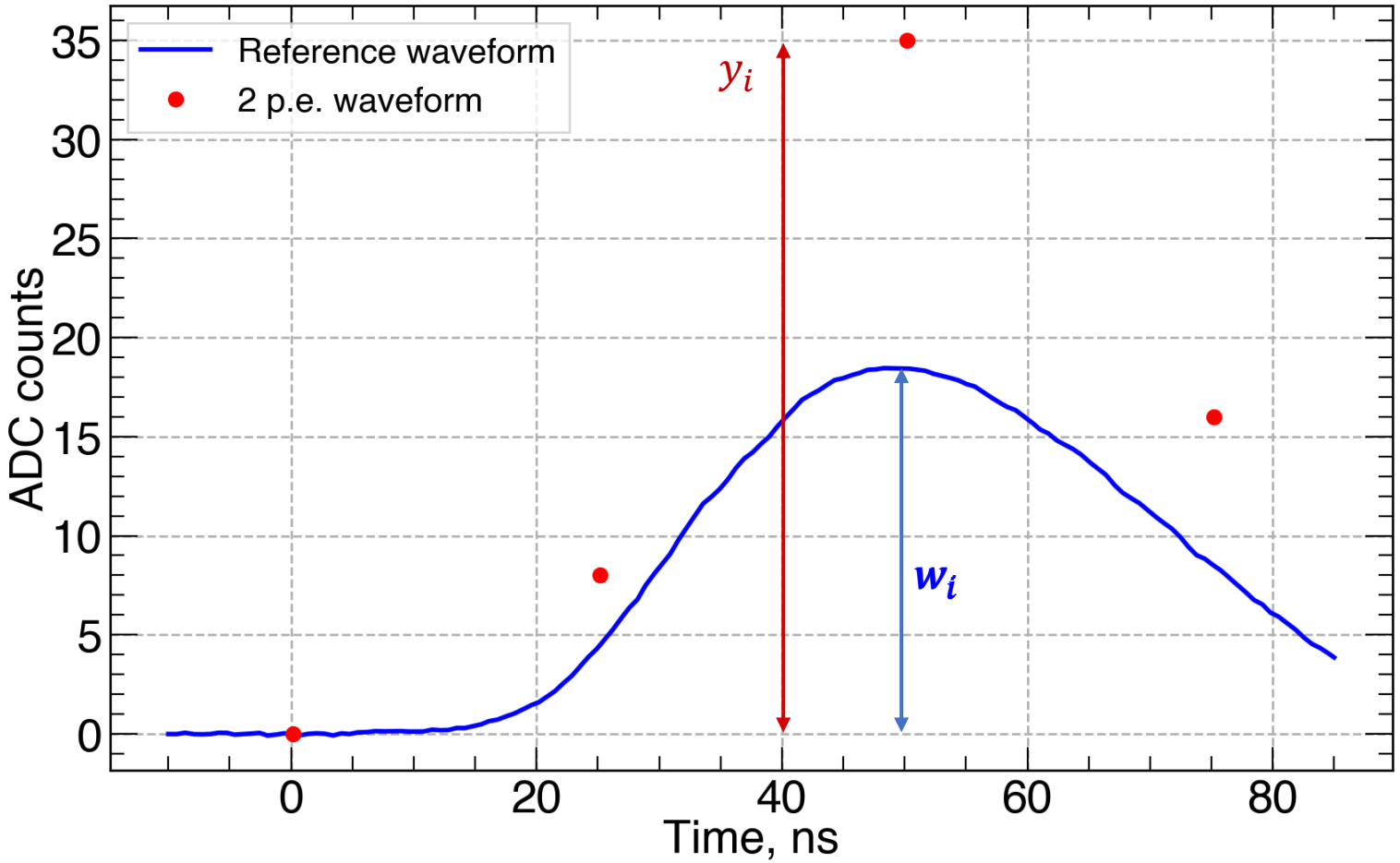
$\chi^2(q)$



Step 4: Charge inference from χ^2

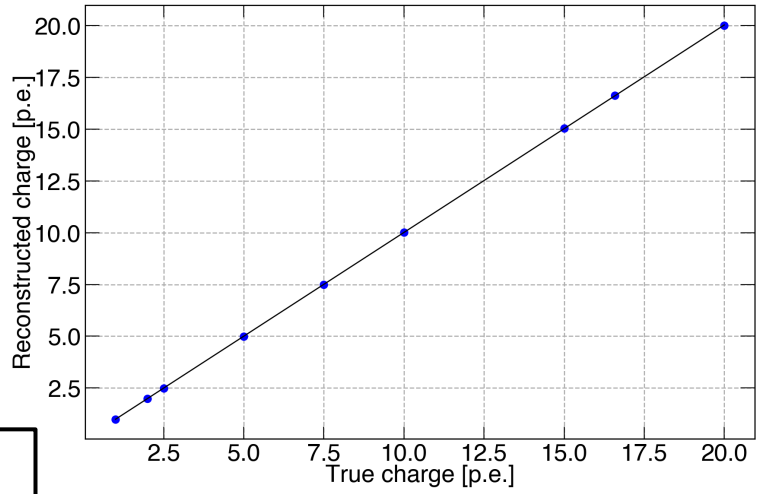
$$\chi^2(q) = \sum_{i=1}^{N} \left(\frac{y_i - q w_i}{\sigma_i} \right)^2$$

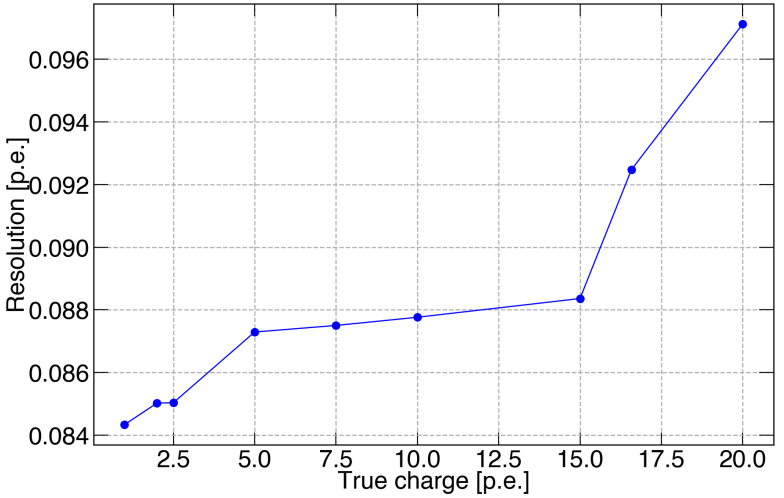
$$q = \frac{\sum_{i=1}^{N} \frac{y_i w_i}{\sigma_i^2}}{\sum_{i=1}^{N} \frac{w_i}{\sigma_i^2}}$$



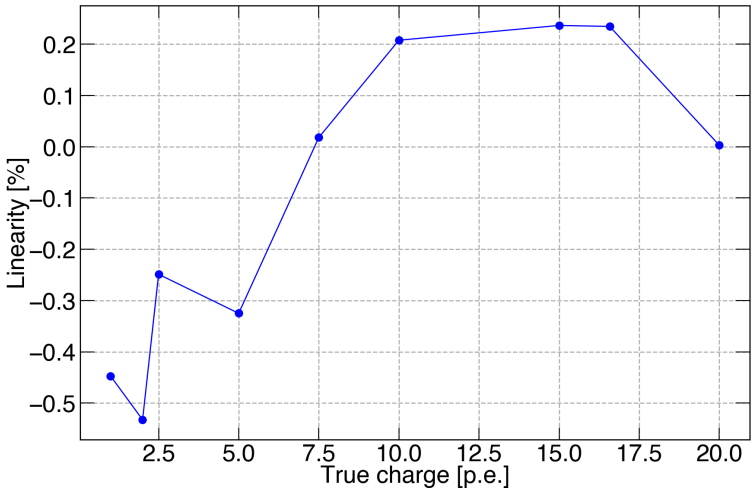
Results

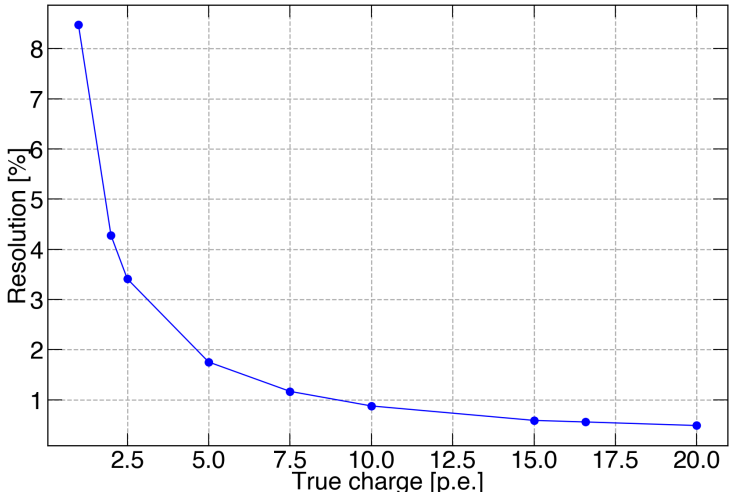
Example for channel 0





Linearity less then 1%



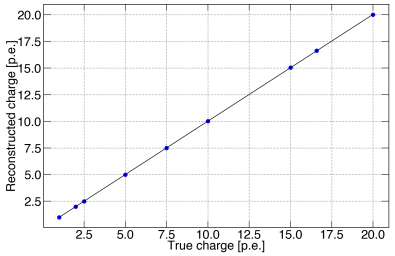


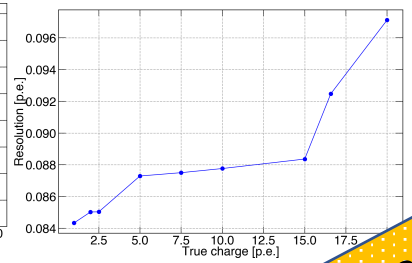
Resolution better then 0.1 p.e.

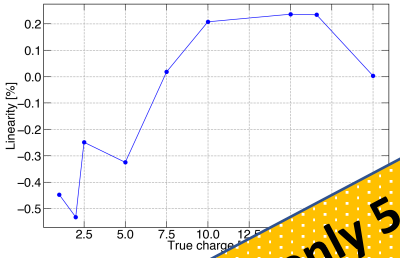
Part III: Test results

Results

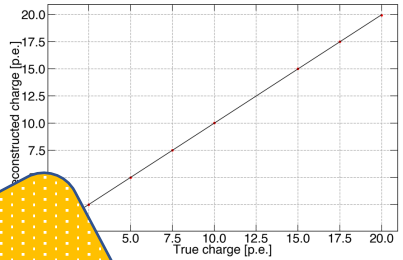
Channel 0

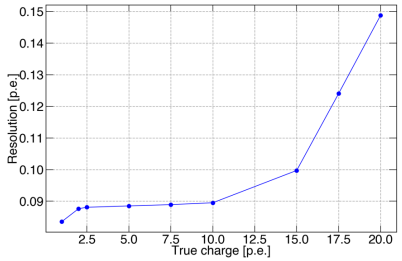


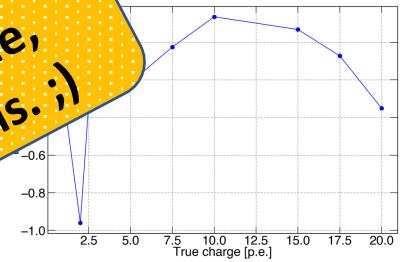


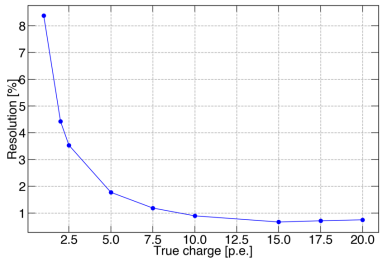


Channel 3

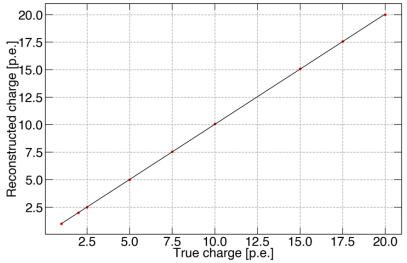


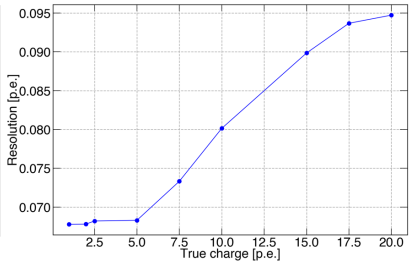


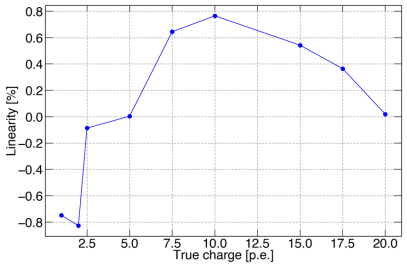


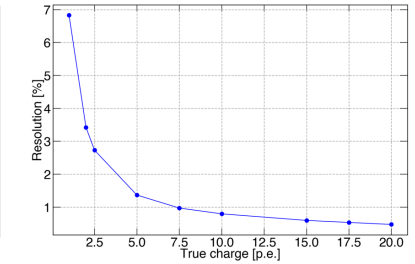


Channel 6



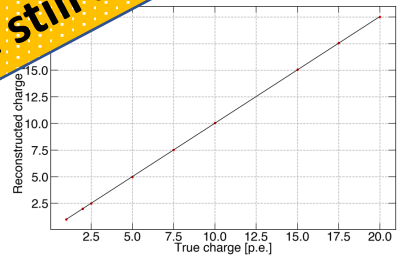


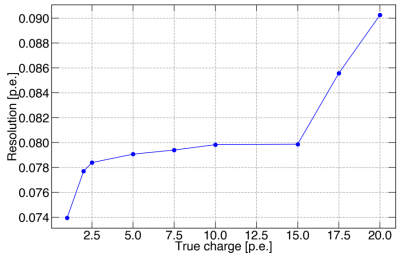


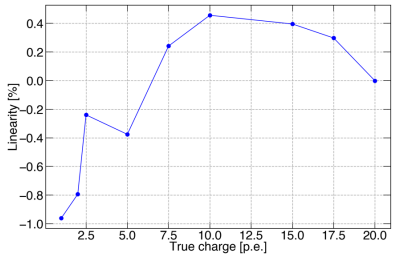


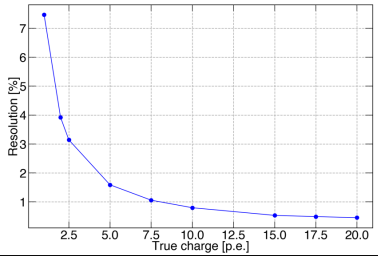
For now only 5 channels were tested for charge rec. If somebody has time, there are still 31 untested channels. ;)

Channel 21

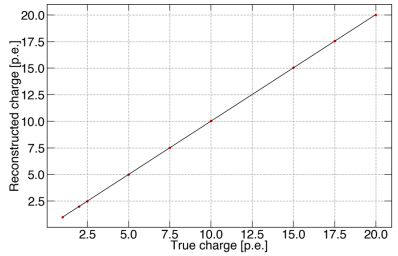


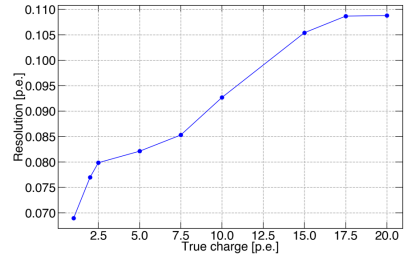


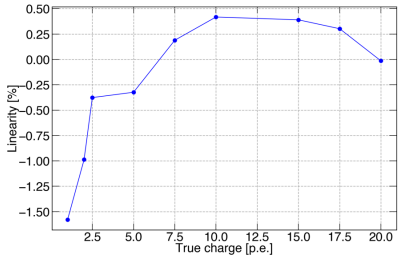


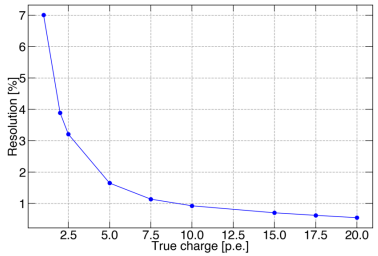


Channel 24









Plans

- Finish charge reconstruction for all channels
- Measure the effect of cross-talk on charge reconstruction
- Write a paper for last version of HKROC (summer 2023)


HKROC
OMEGA/AGH/CEA
YY/WW

The end

to be continued...

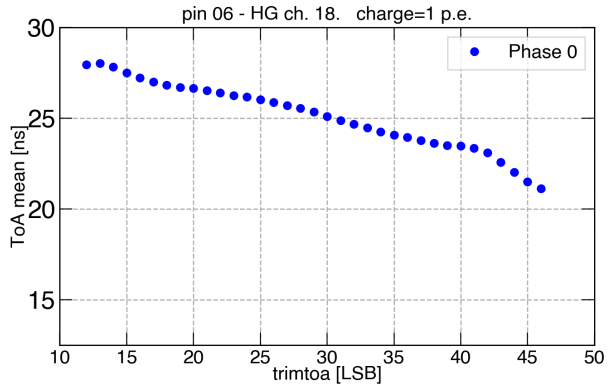
“Completely no pressure but finish the tests by the end May”

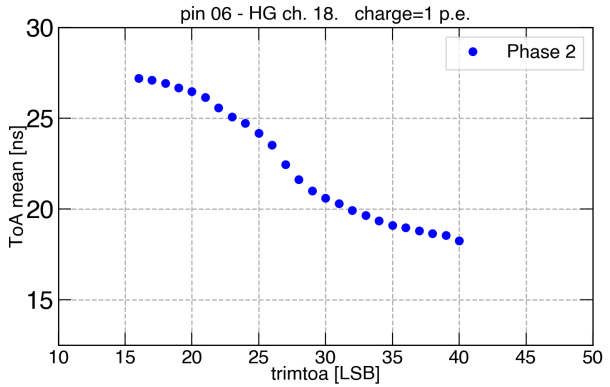
Benjamin

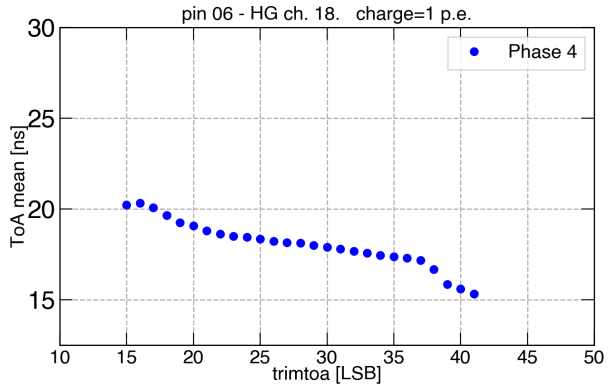
Part III: Test results

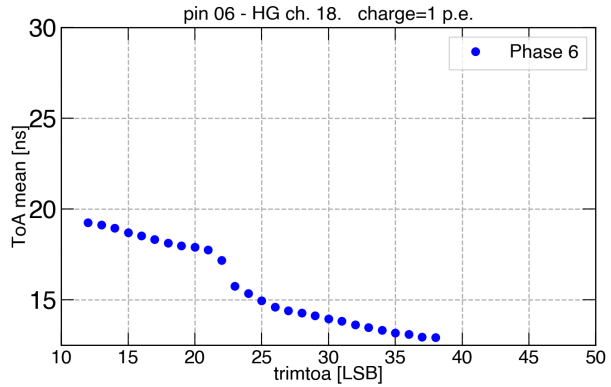
Time measurements

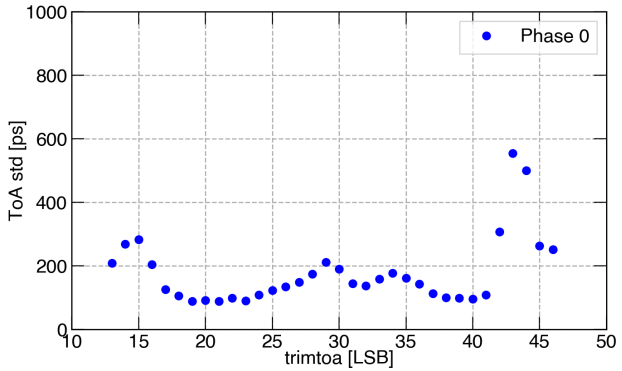
Bump noise depends on relative phase between internal clock and input signal

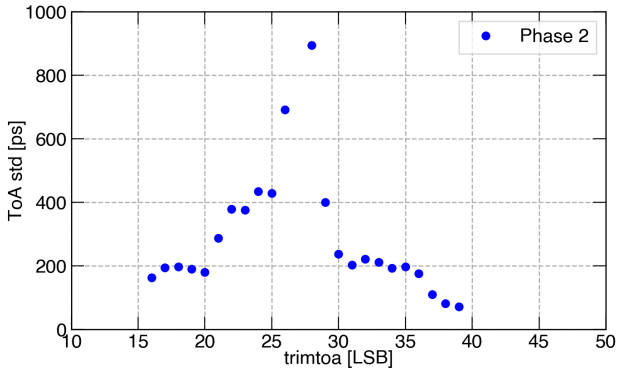


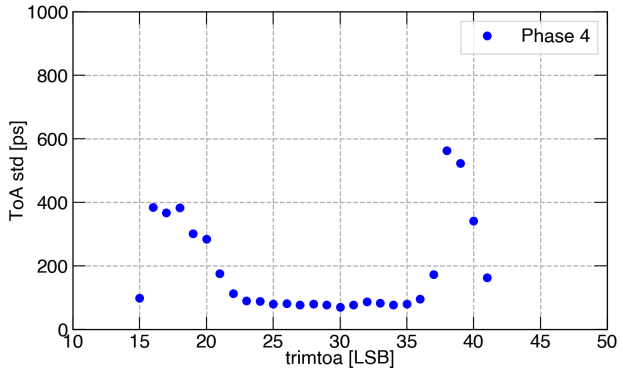


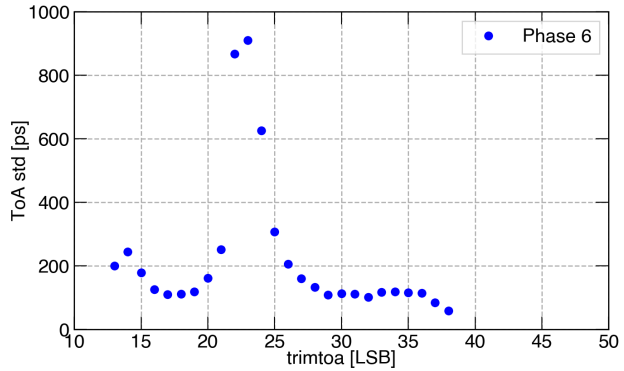








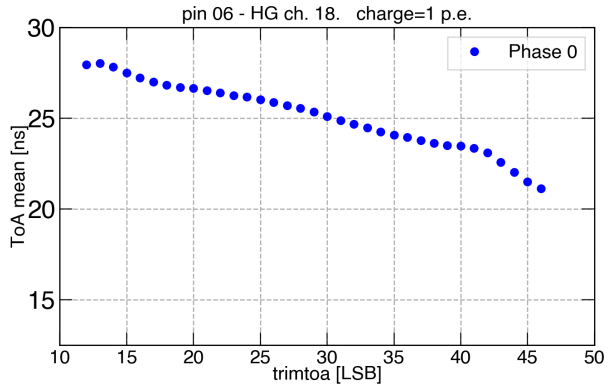


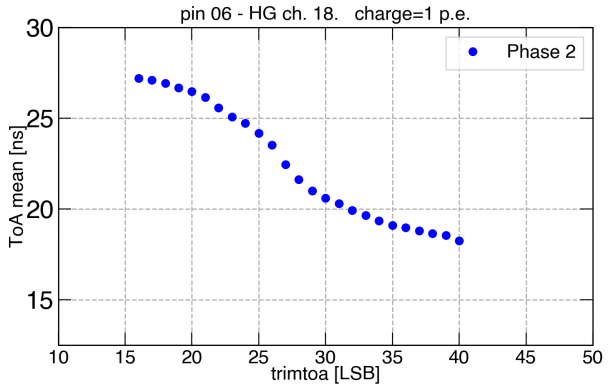


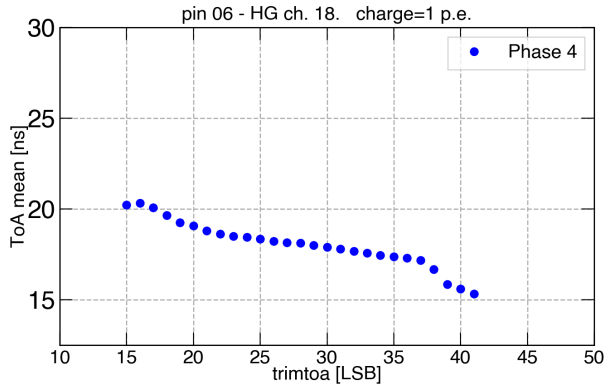
Part III: Test results

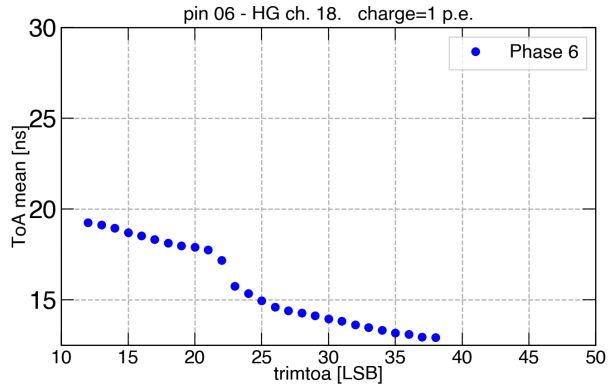
Time measurements

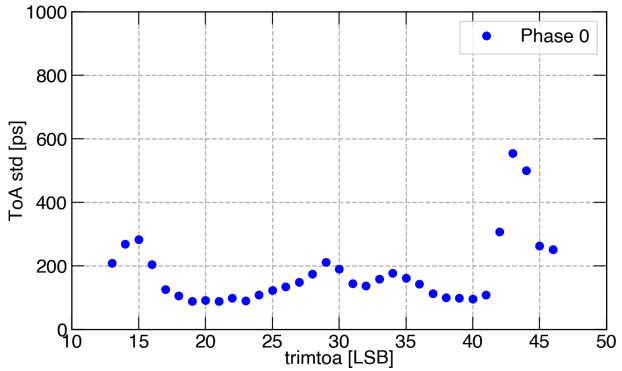
Bump noise depends on relative phase between internal clock and input signal

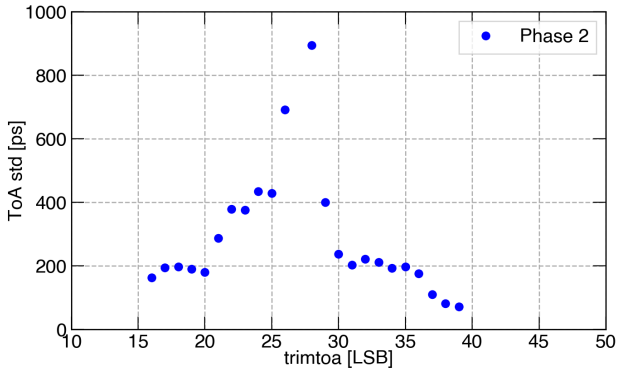


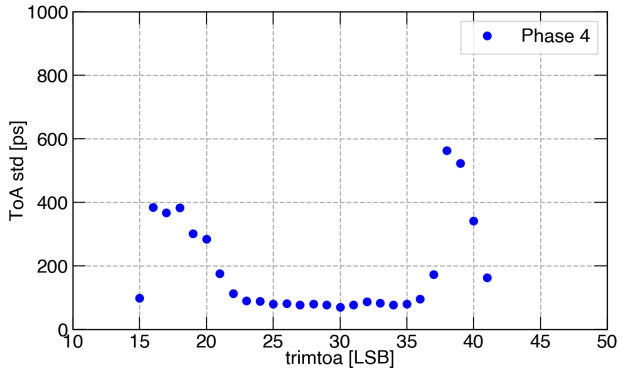


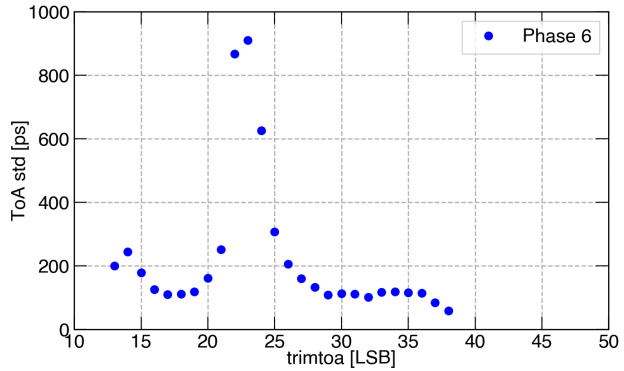










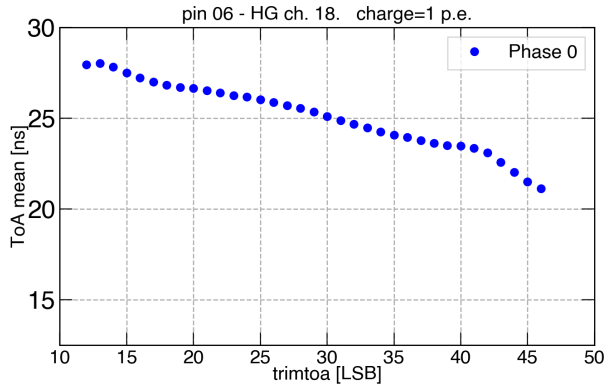


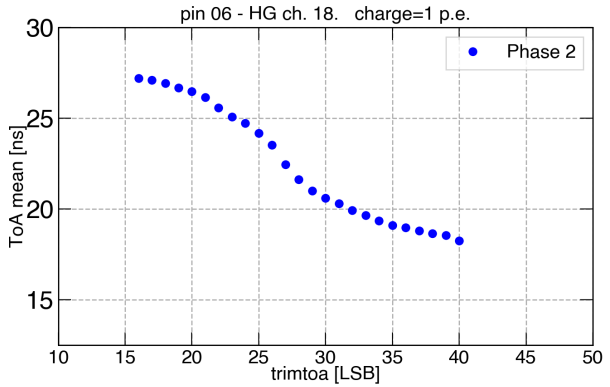
Part III: Test results

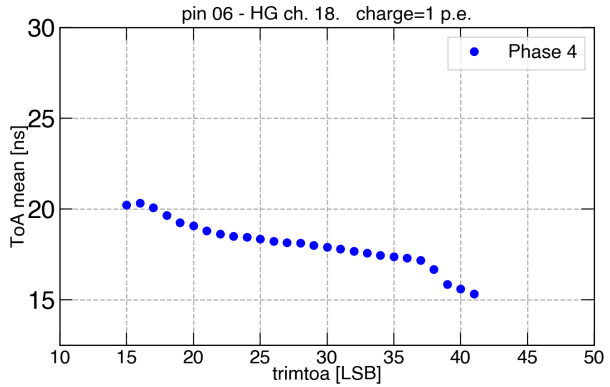
Time measurements

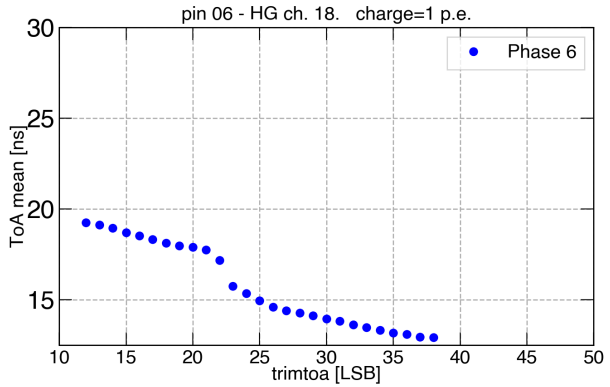
Bump noise depends on relative phase between internal clock and input signal

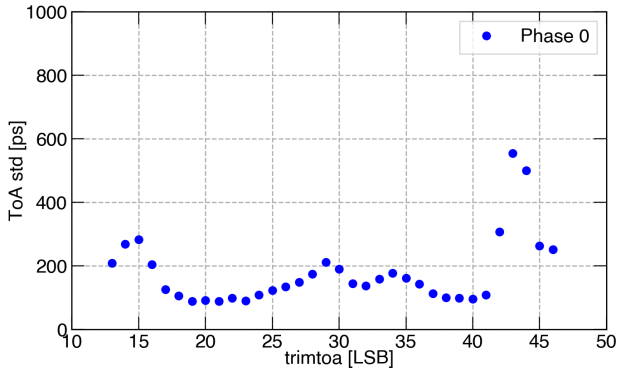
BACKUP

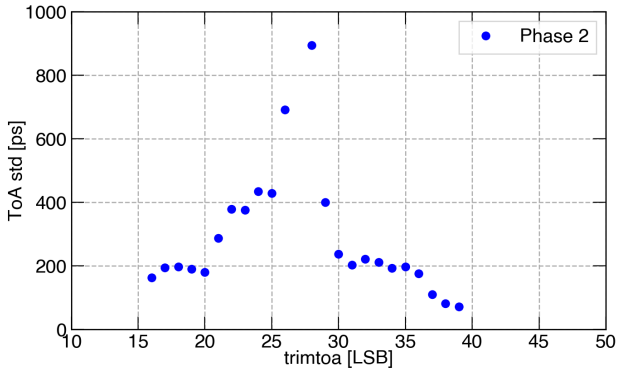


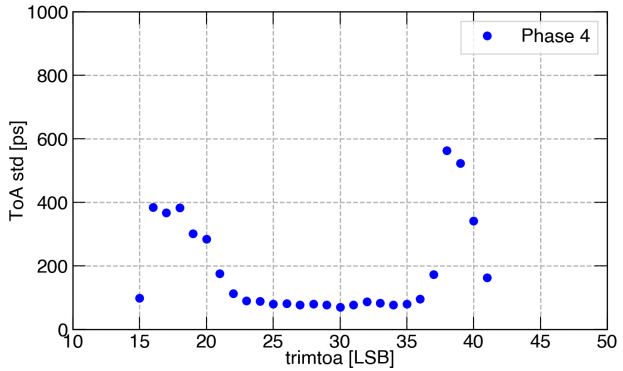


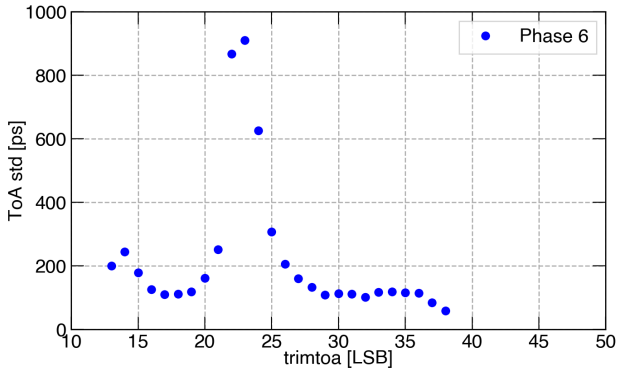






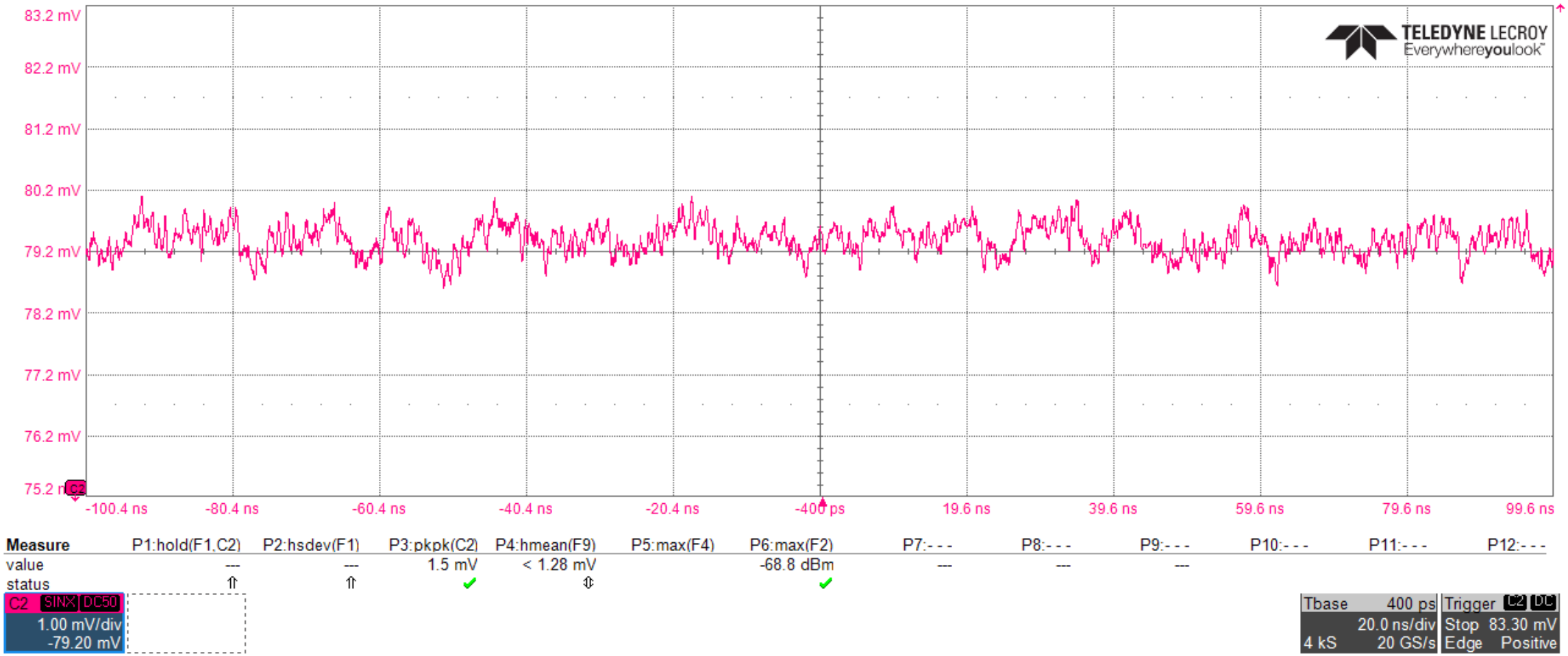




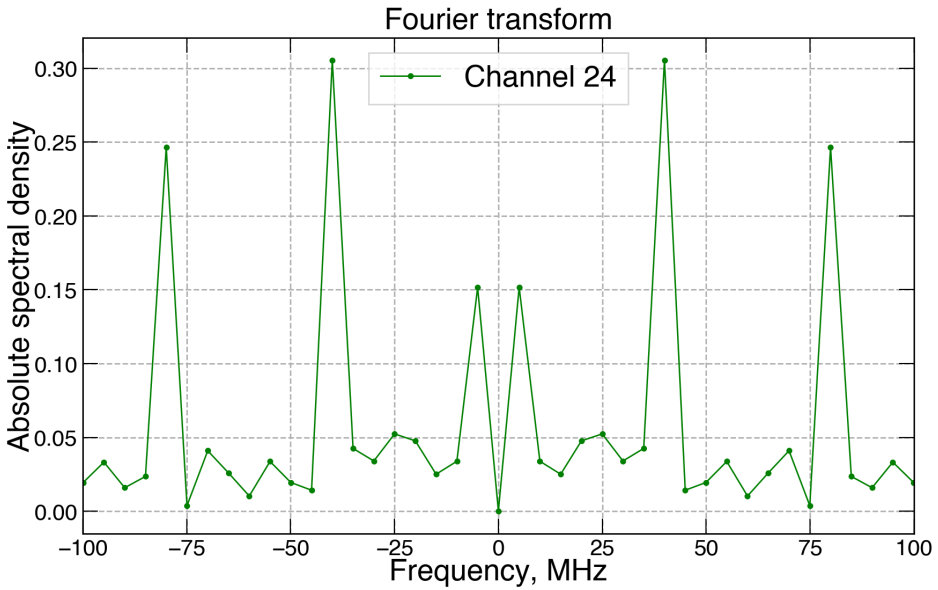


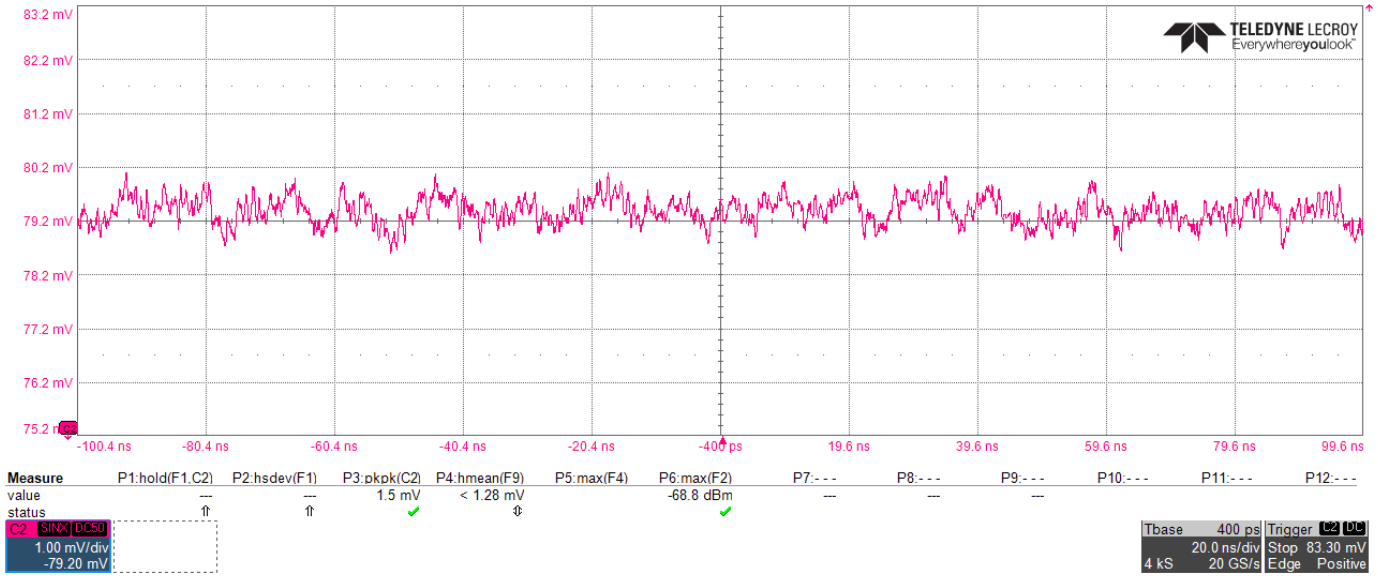
Part III: Test results

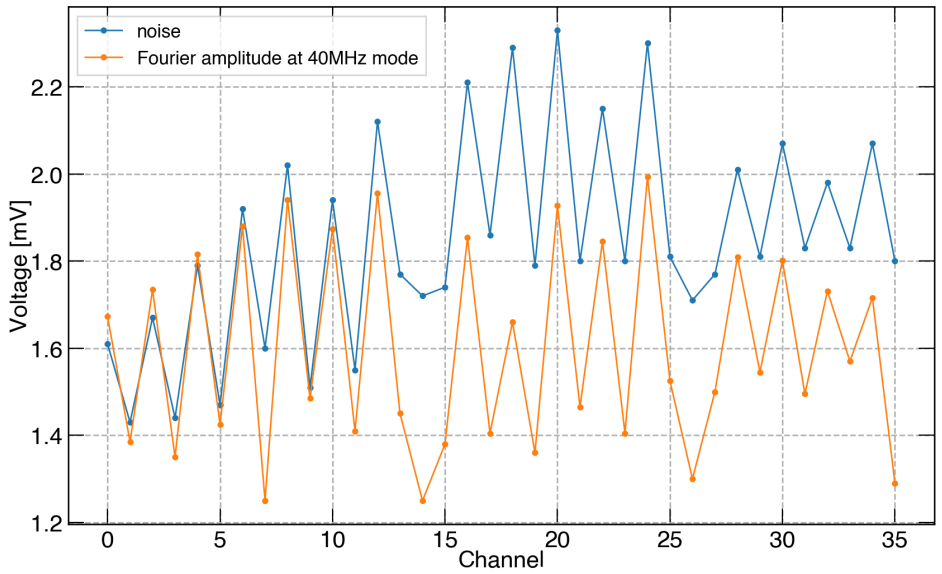
Time measurements



Part III: Test results







Backup

The HKROC ASIC is designed in TSMC 130 nm technology.

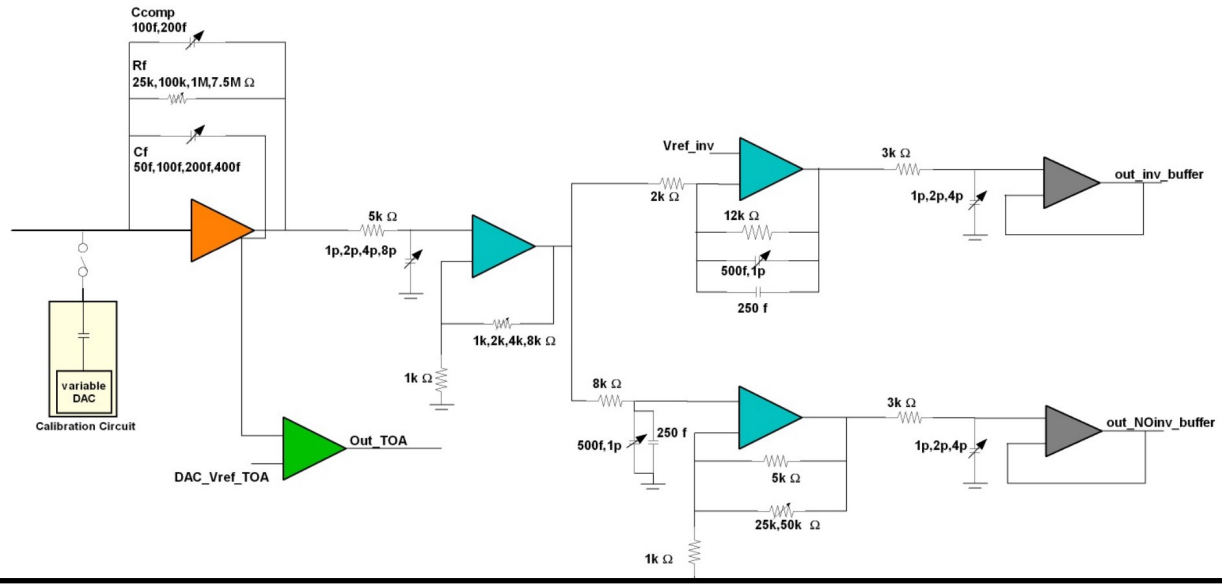
1. An analog front end part that allows the input signal amplification, the trigger detection and the signal shaping ;
2. A mixed part to provide the charge and time of arrival measurements
3. A digital part to manage all the system, the conversion and the read-out.

Backup

Analog part

1. PA - provides the first amplification of the PMT signal with the best noise performances. The preamplifier provides two outputs: an output connected to the TOA discriminator for the time of arrival measurements and a second output, through a buffer, connected to the shaper path to allow charge measurement.
2. The purpose of this slow path is to shape the PA output signal in order to allow the charge measurement, to optimize the signal-to-noise ratio and use the full available dynamic range (1 V).
3. The trigger path (green part in Fig. 2.1) is responsible for the trigger formation. The PA signal is sent to a low offset discriminator which allows to auto trigger on the signal above a set threshold. The threshold is set by a global 10b-DAC (tuneable by SC) and a local trimming 6b-DAC (tuneable by SC) to reduce the dispersion per channel. The trigger signal is sent to the TDC block for the measurement of the arrival time.

BACKUP



Backup

Mixed part

The HKROC contains a 10b SAR ADC, designed by AGH in Krakow.

The timing channel that generates the precise ToA (time of arrival) of the particle consists of a discriminator followed by a TDC circuit. The Charge Sensitive Amplifier (CSA or pre-amplifier) output voltage is compared to a reference voltage whose value is adjustable by slow-control and corresponds to the trigger threshold.

This innovative multichannel TDC architecture is chosen for its conversion speed > 40 MHz and its intrinsic resolution of 25 ps. Its low power consumption is also a key point in the HyperKamiokande environment.
Power consumption of less than 1W has been observed for 1 chip of 36 channels (12 PMT) including the interface cards (mezzanine, motherboard and KCU), so well inside the HyperKamioaknde specifications requiring <1 W per PMT channel.

BACKUP

Backup

FIFO

The ASIC has 4 DATA FIFOs that are standard circular FIFOs. Each FIFO has a depth of 32 sampling points whereas each word contains 32 bits. If a physics event is digitized with 3 sampling points, a FIFO has a depth for 10 to 11 consecutive events. As a reminder, each sampling point consists of 10 words (normal-mode) or 4 words (supernova-mode).

Normal mode

Data Header	SN	Dh	24b Timestamp			P	1
Data Header	Chn #0	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #1	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #2	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #3	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #4	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #5	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #6	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #7	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #8	Dh	H	10b TOA	10b ADC	P	1

Supernova-mode

Data Header	SN	Dh	24b Timestamp			P	1
Data Header	Chn #0	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #3	Dh	H	10b TOA	10b ADC	P	1
Data Header	Chn #6	Dh	H	10b TOA	10b ADC	P	1

BACKUP

Noise->Bump in resolution
A plot

Previous results

New results