ALICE ITS 3

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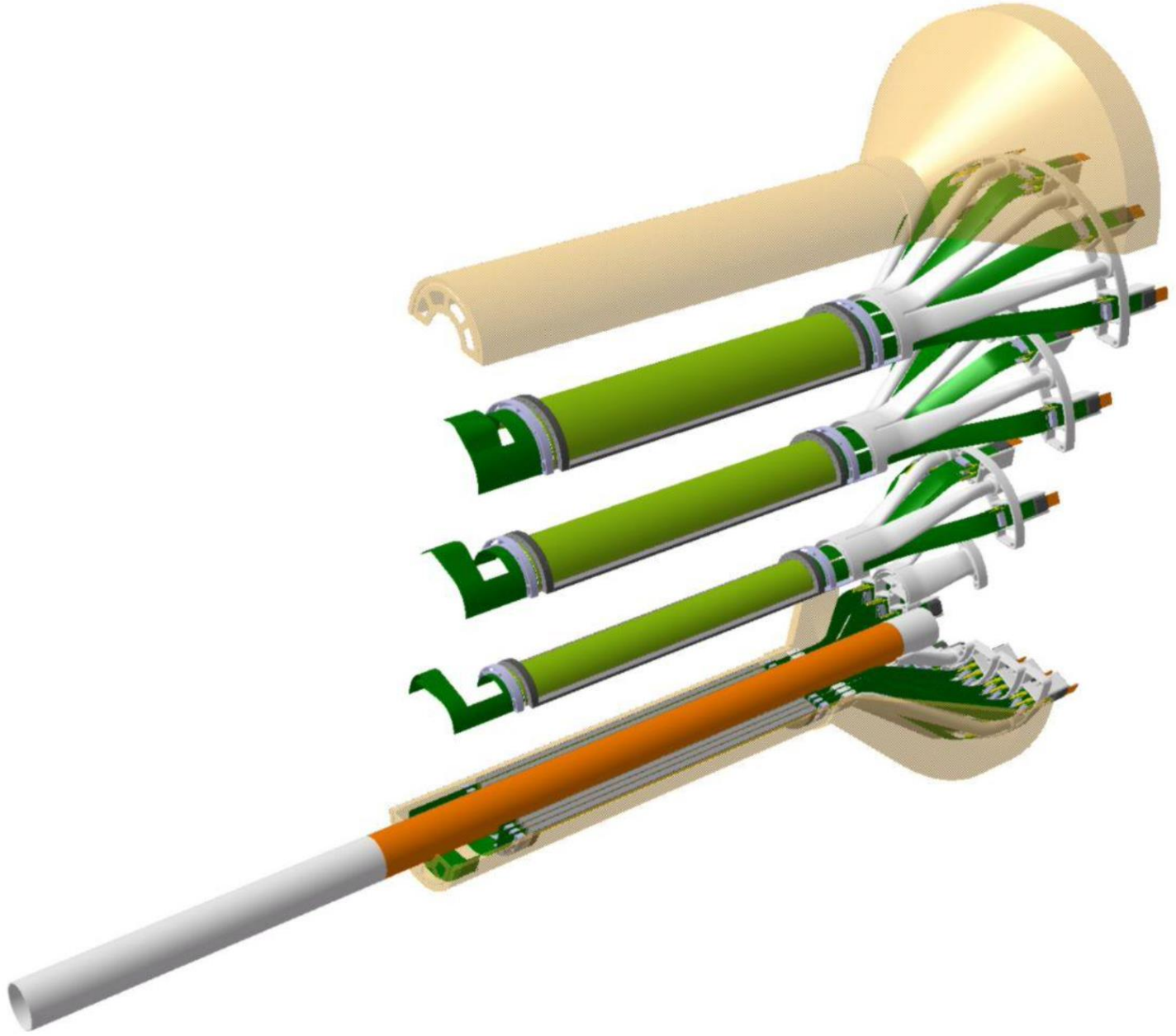
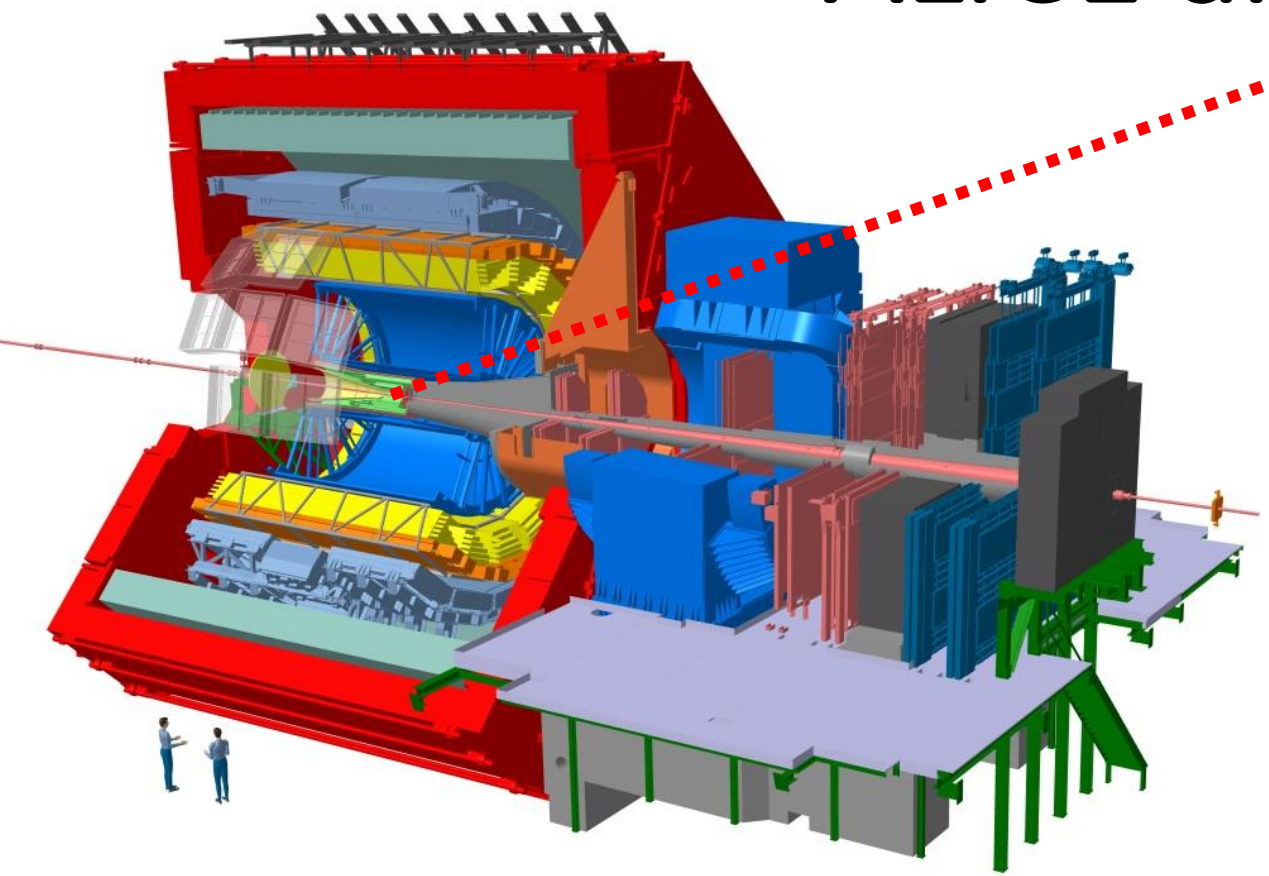
on behalf of ALICE collaboration



ALICE and ITS(s)



General purpose detector at LHC:

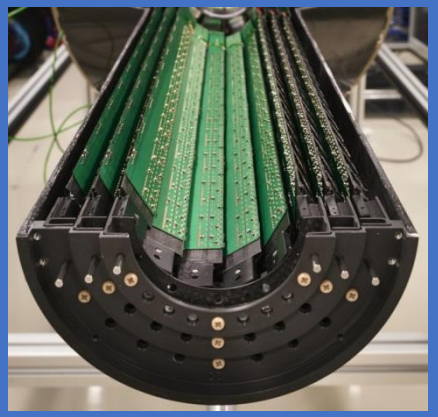
- Tracking (100 MeV/c – 100 GeV/c)
- Particle identification: π, K, p, e (0.1 – 50 GeV/c)

ITS 1 (LHC Run 1/2)

- Hybrid pixels
- Pixels: 50×425 μm^2
- C4F10 cooling
- ~ 1.1 % X_0

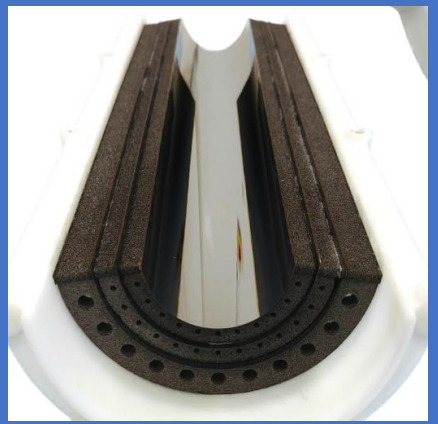
ITS 2 (LHC Run 3)

- MAPS
- Pixels: 27×29 μm^2
- Water cooling
- ~ 0.3 % X_0 (inner layers)



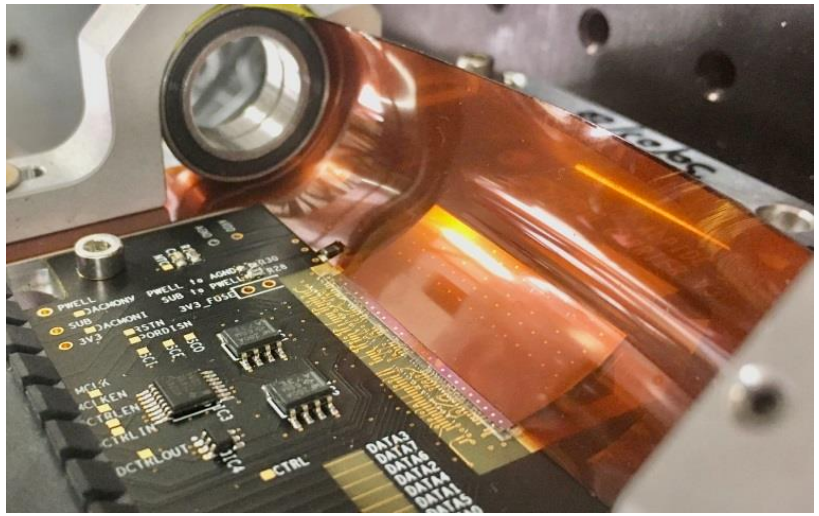
ITS 3 (LHC Run 4)

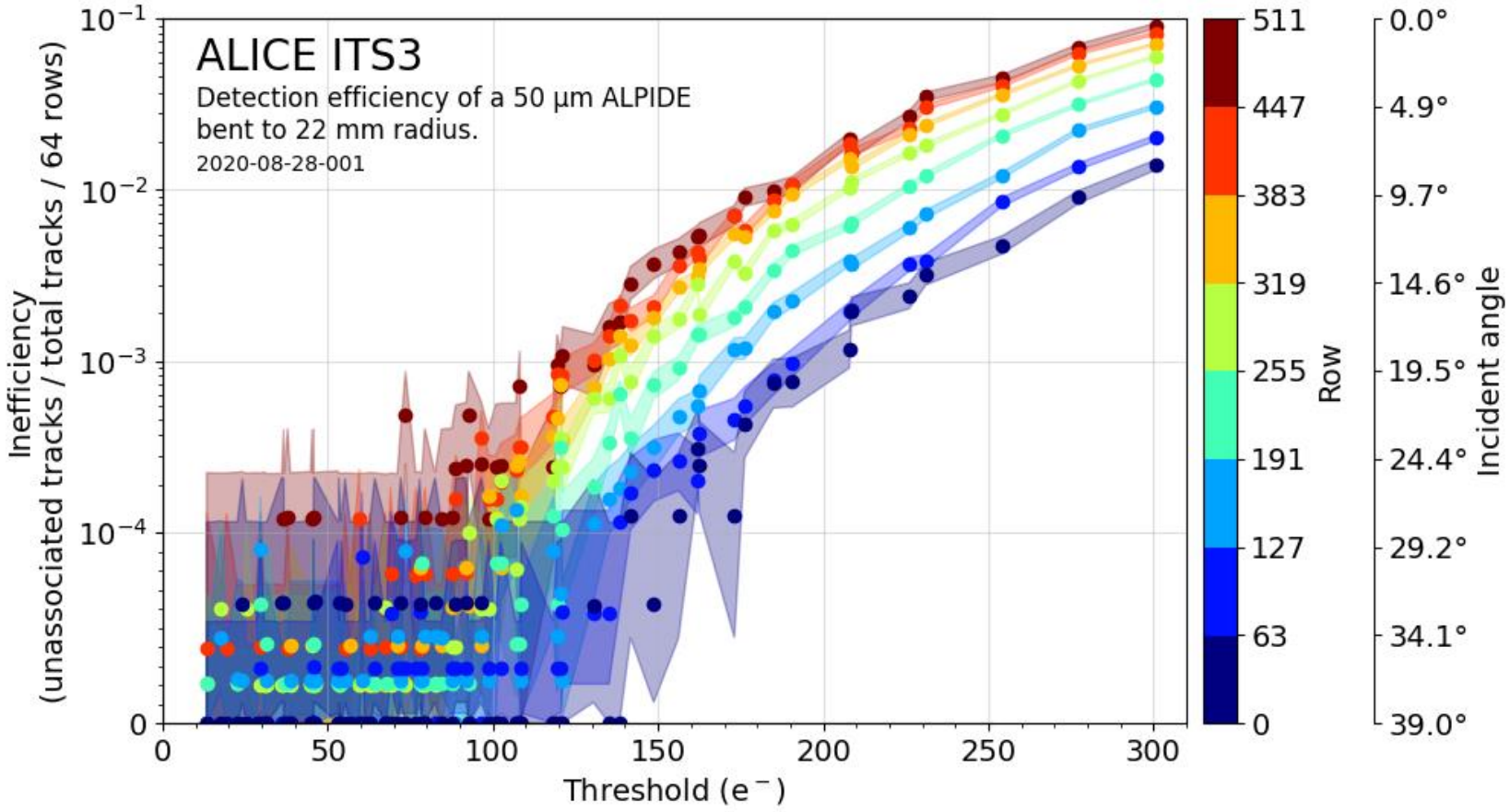
- Stitched MAPS
- Pixels: ~20×22.5 μm^2
- Air cooling
- ~ 0.05 % X_0 (inner layers)



Excellent performance for small bent sensors

In 2020 50 µm thick ALPIDE chip bent to 22 mm along columns showed excellent efficiency in the beam test

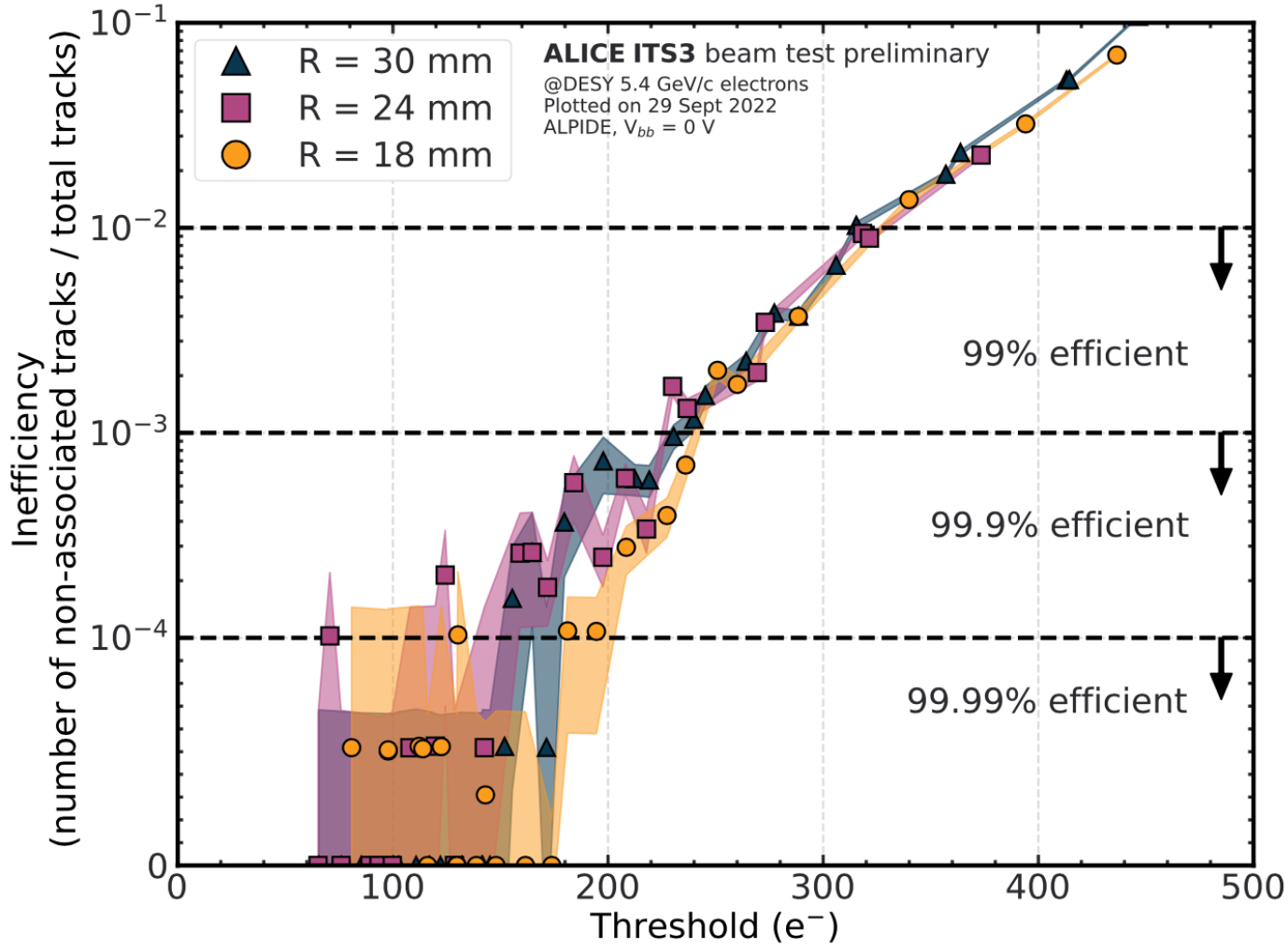




https://doi.org/10.1016/j.nima.2021.166280

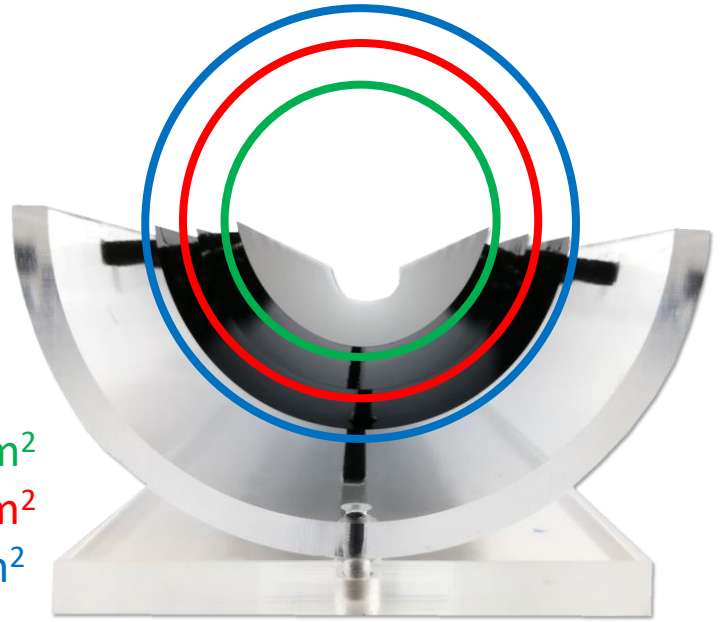
Excellent performance for small bent sensors

In 2021 *µITS3* – assembly of 3 ALPIDE sensors bent to ITS3 radii (18, 24, 30 mm) along rows – tested and also showed excellent detection efficiency not depending on the radius

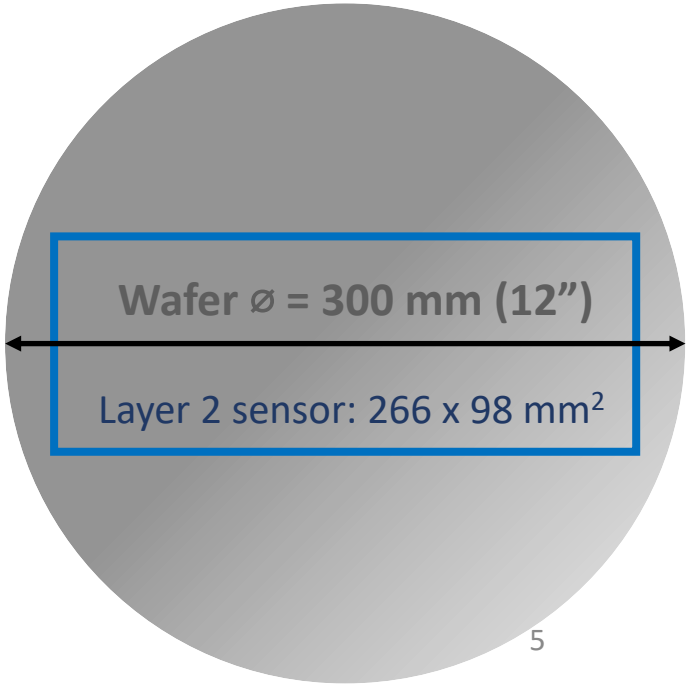


ITS3 requires large sensors → New CMOS process is needed

- ITS3 sensors size up to ~27×9 cm^2
- Can only be produced via stitching on 12-inch wafers
- Available from Tower Partners Semiconductor Co. TPSCo in 65 nm
  - Continuation of TJ 180 nm used in ITS2
  - Custom process modifications for full depletion ported from TJ180
  - Lower power consumption
  - Potentially better radiation hardness



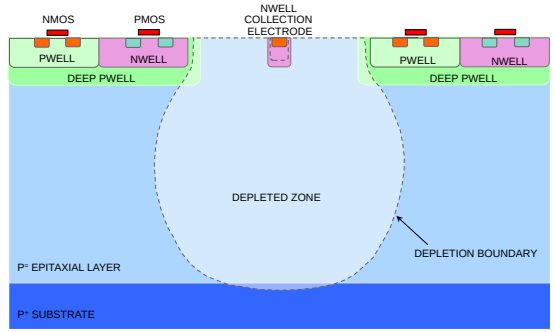
2 x 266×59 mm^2
2 x 266×79 mm^2
2x 266×98 mm^2



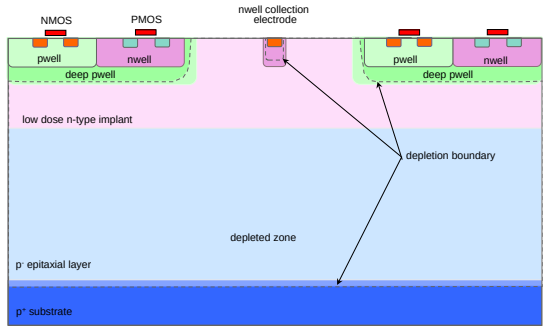
MLR1: first TPSCo 65 nm submission for technology validation

- Submitted Dec 2020 -> Delivered July 2021
- Three main goals:
  - Learn technological features
  - Characterize charge collection
  - Validate radiation hardness
- Large variety of small chips (1.5×1.5 mm^2)
  - Analogue and digital blocks
  - 3 pixel matrices: APTS, CE65 and DPTS
- Standard process + 2 modified for better depletion:
  - “Modified” – low dose n-type blanket
  - “Modified with gap” – same as above with gaps on pixel edge

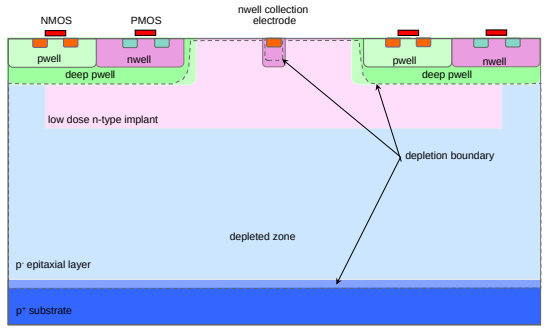
Standard



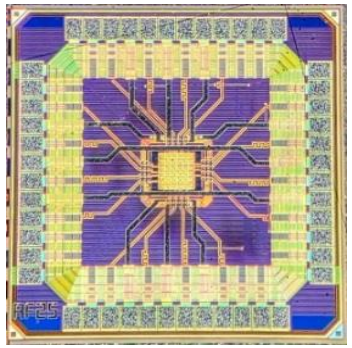
Modified



Modified with gap

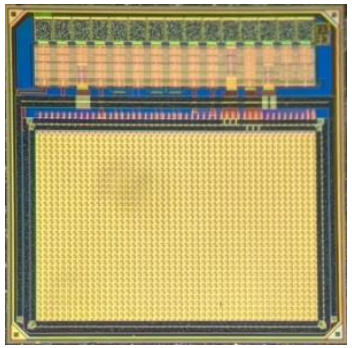


Pixel chips: APTS, CE65, DPTS



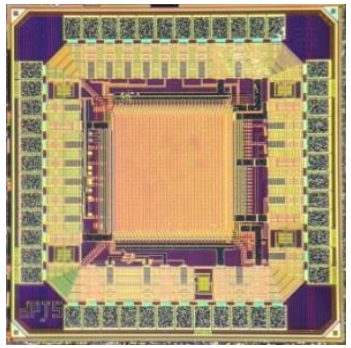
APTS
(Analogue Pixel Test Structure)

- 6×6 pixel matrix
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  - Source follower (APTS-SF)
  - Very fast OpAmp (APTS-OA)
- AC/DC coupling
- 4 pitches: 10, 15, 20, 25 µm
- 3 process variations



CE65
(Circuit Exploratoire 65 nm)

- 2 matrix sizes
  - 64×32 with 15 µm pitch
  - 48×32 matrix with 25 µm pitch
- Rolling shutter readout (50 µs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - **Standard process 15 µm pitch**
  - Modified process 15 µm pitch
  - **Modified process with gaps 15 µm pitch**
  - Standard process 25 µm pitch

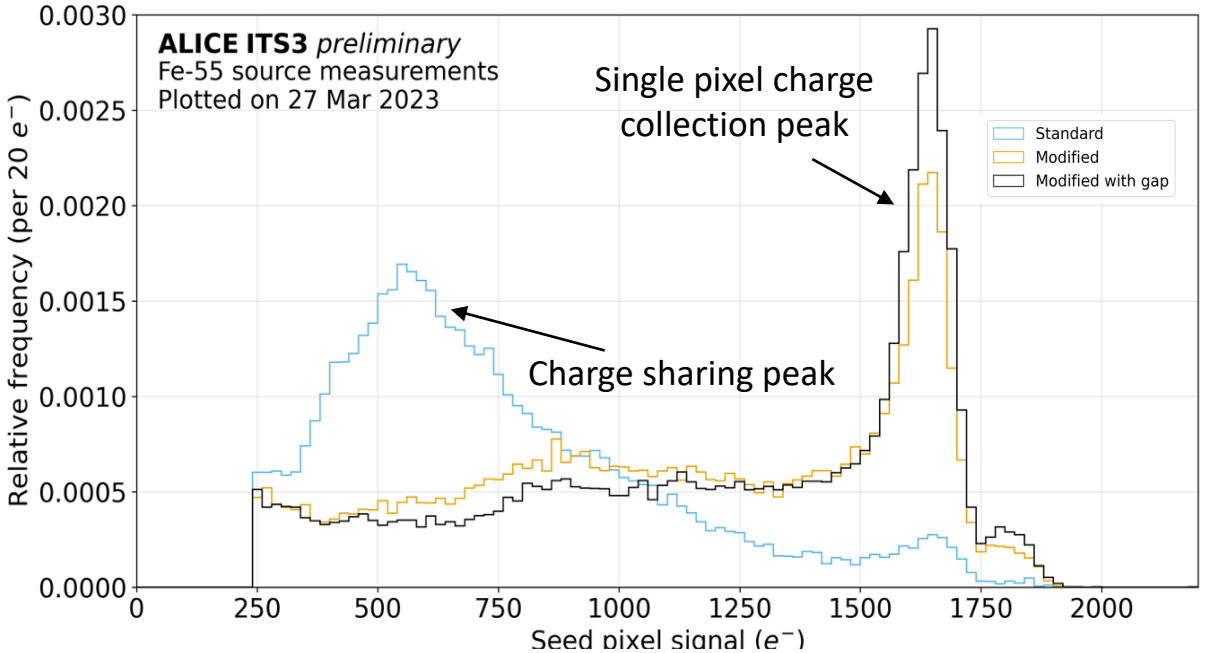


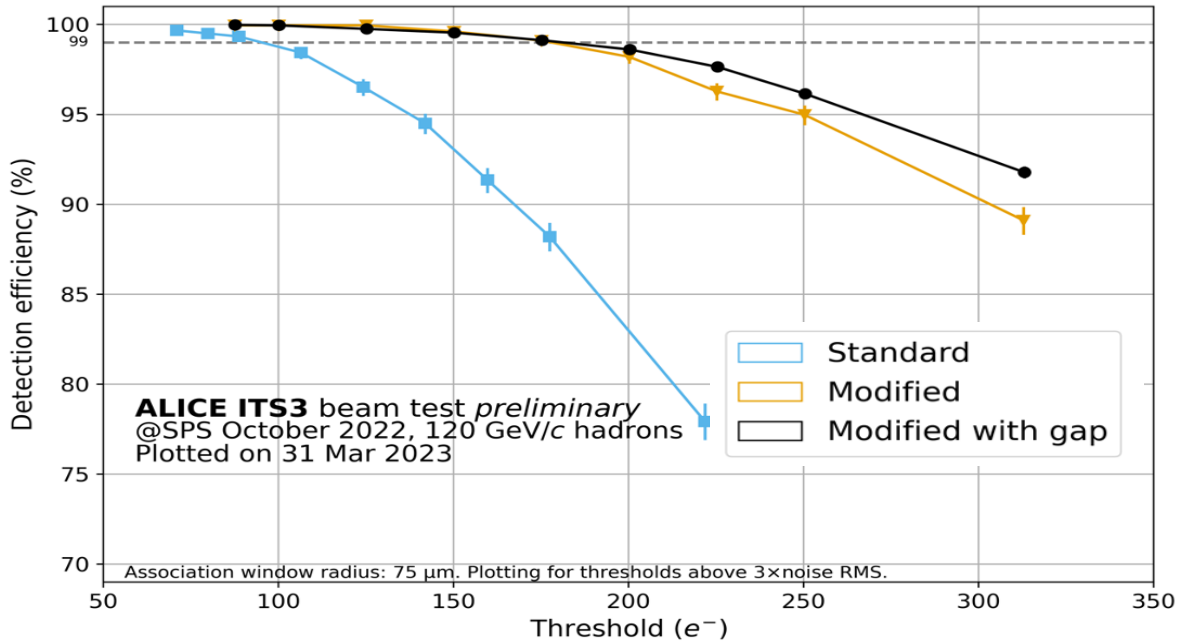
DPTS
(Digital Pixel Test Structure)

- 32×32 pixel matrix
- Asynchronous digital readout
- Time-over-Threshold information
- Pitch: 15×15 µm^2
- Only “modified with gap” process modification

Characterization results: effect of modified process

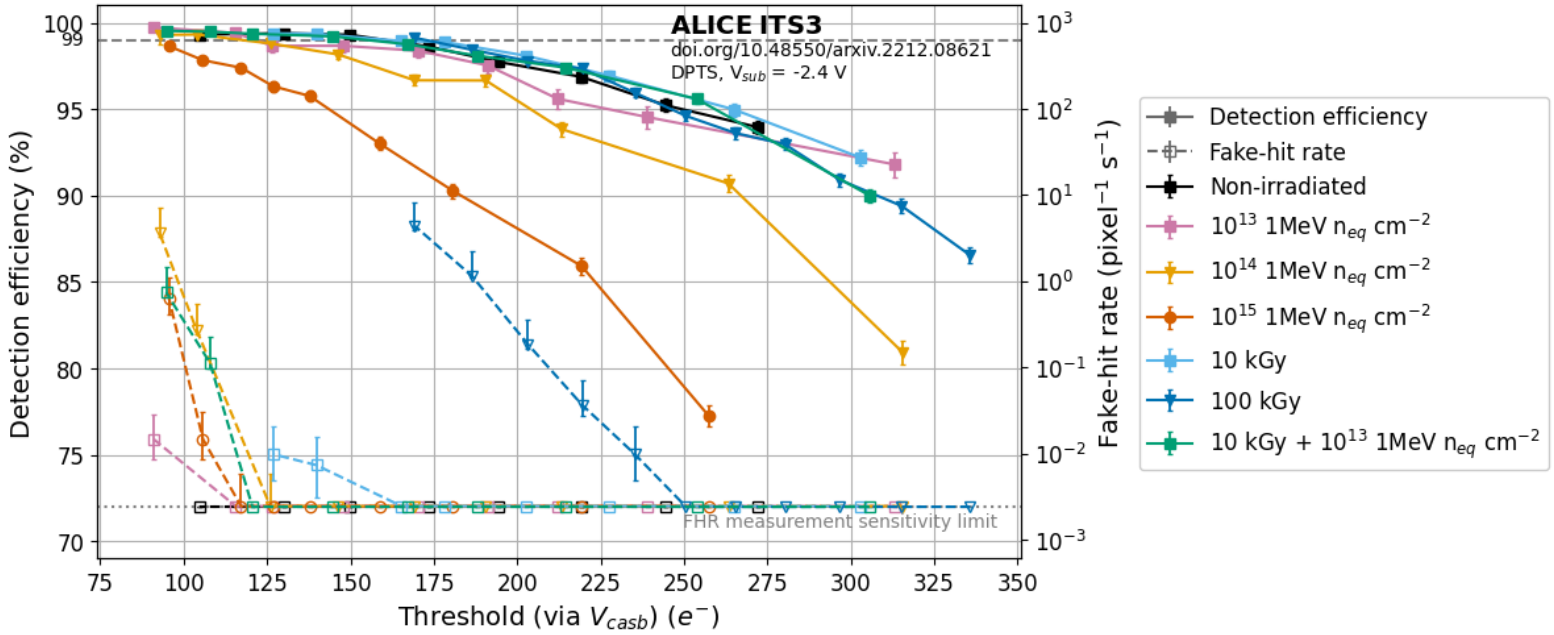
- Process modifications make almost all the charge to be collected by seed pixel due to full depletion of epi-layer
- This effect greatly extends working range with excellent detection efficiency





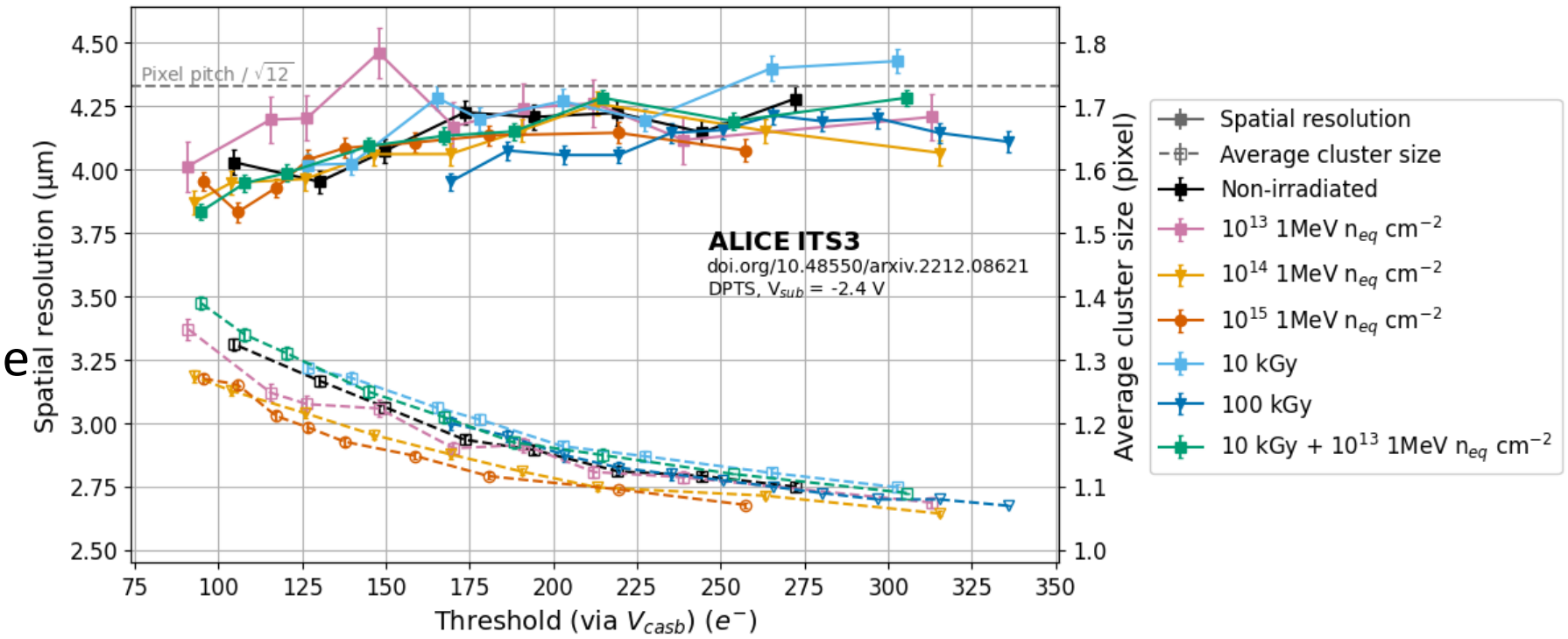
Detection efficiency and FHR vs. irradiation

- Detection efficiency decreases with NIEL dose
- FHR increases with TID dose
- **Perfect performance at ITS3 combined level of 10 kGy + 10^{13} n_{eq} /cm²**



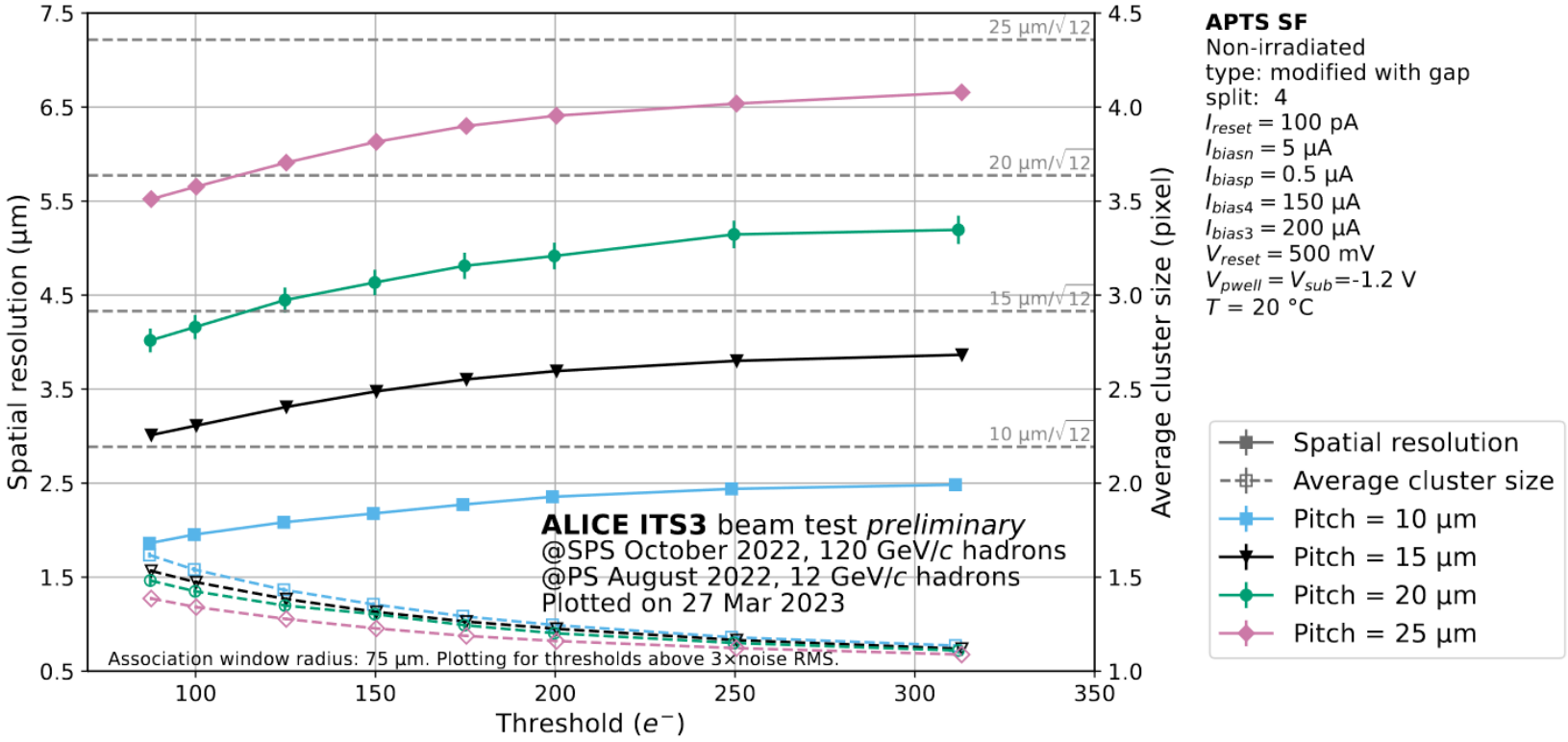
Spatial resolution and cluster size vs. irradiation

- Spatial resolution isn't affected by irradiation
- Cluster size slightly increases with NIEL irradiation
- Resolution is compatible with mostly single pixel clusters and digital readout

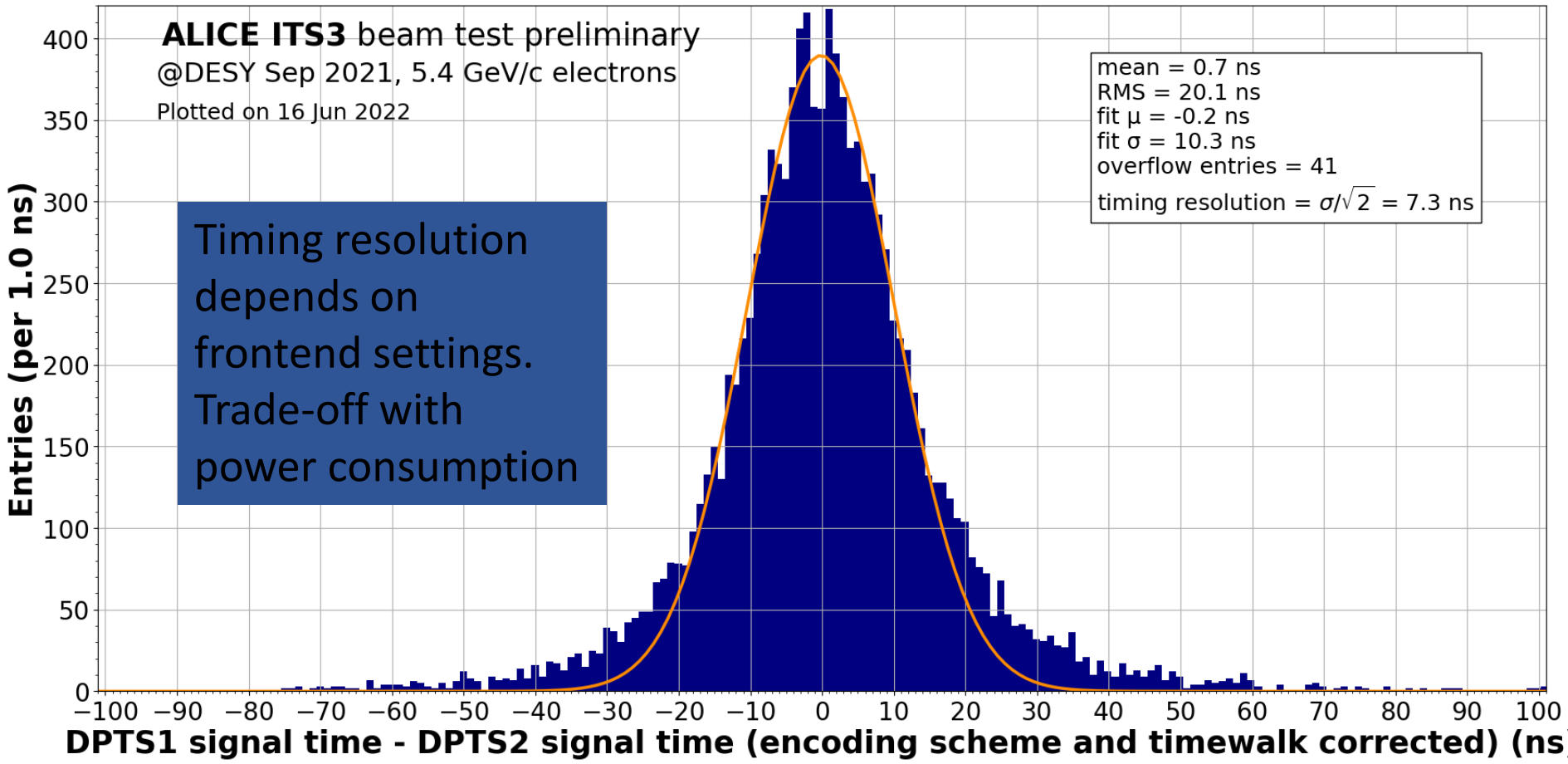


Spatial resolution and cluster size vs. pitch

- Weak dependence of cluster size on pixel pitch
- **Spatial resolution of about 5 µm for expected pitch value of 22 µm**



DPTS: Temporal resolution ~7 ns

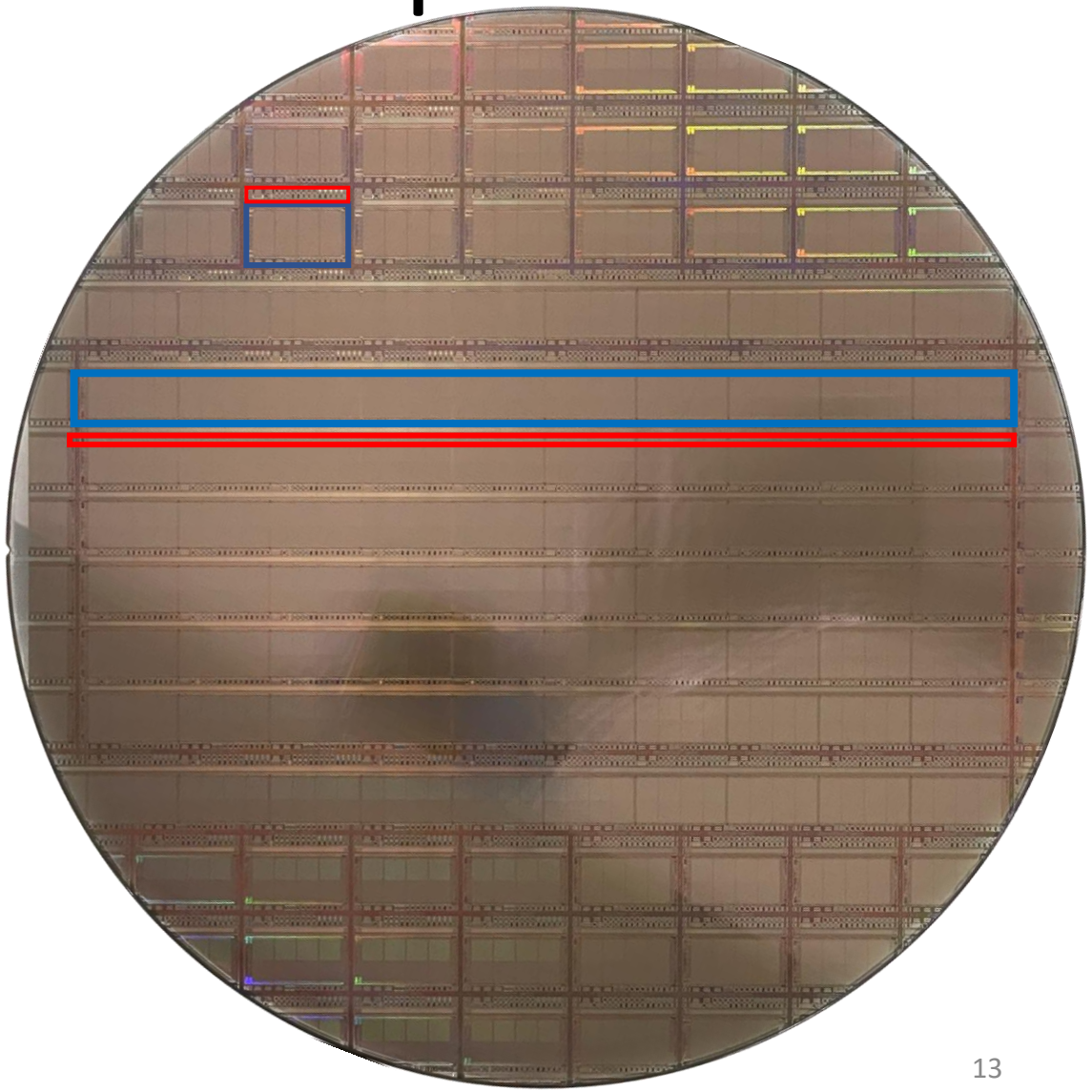


DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$
$V_{pwell} = V_{sub} = -1.2V$

DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 280\,mV$
$V_{pwell} = V_{sub} = -1.2V$

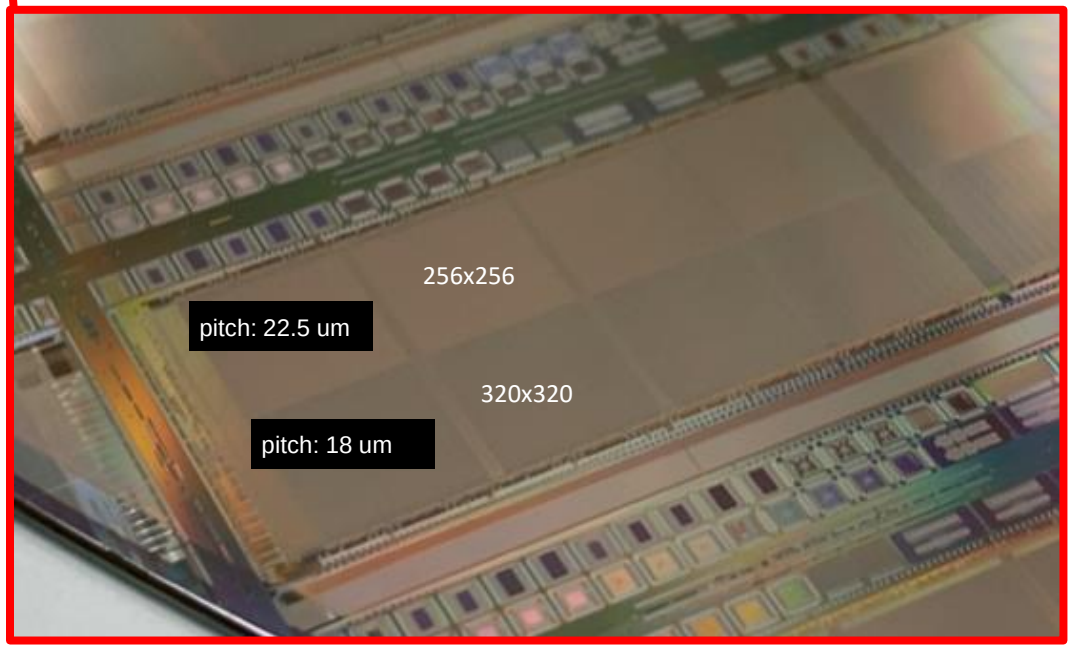
ER1: First submission of stitched chips

- Submitted Dec 2022
- Received May 2023
- Two types of stitched chips:
  - MOSS (259×14 mm^2)
  - MOST (259×2.5 mm^2)
- 1/10 versions of MOSS(T)
  - Baby-MOSS
  - Baby-MOST
- Multiple small chips (1.5×1.5 mm^2)



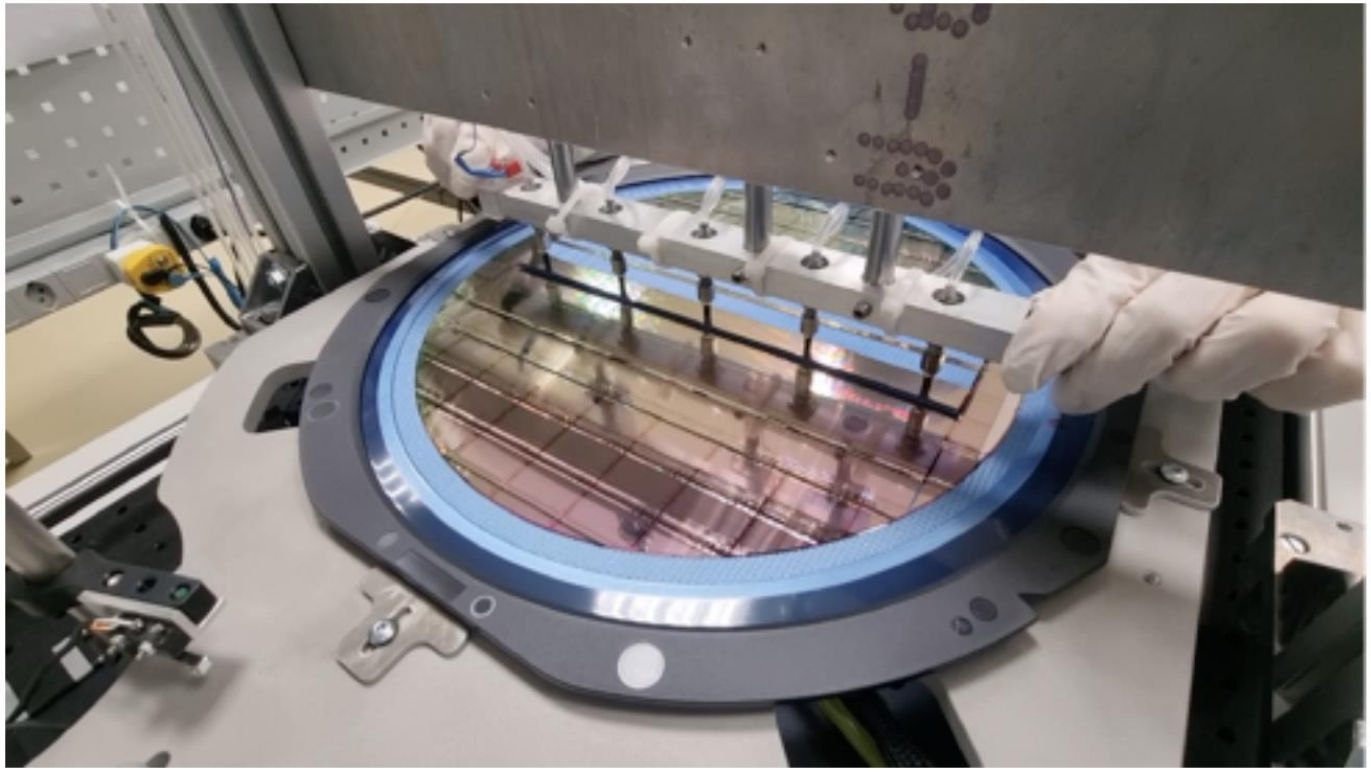
MOSS - MOnolithic Stitched Sensor

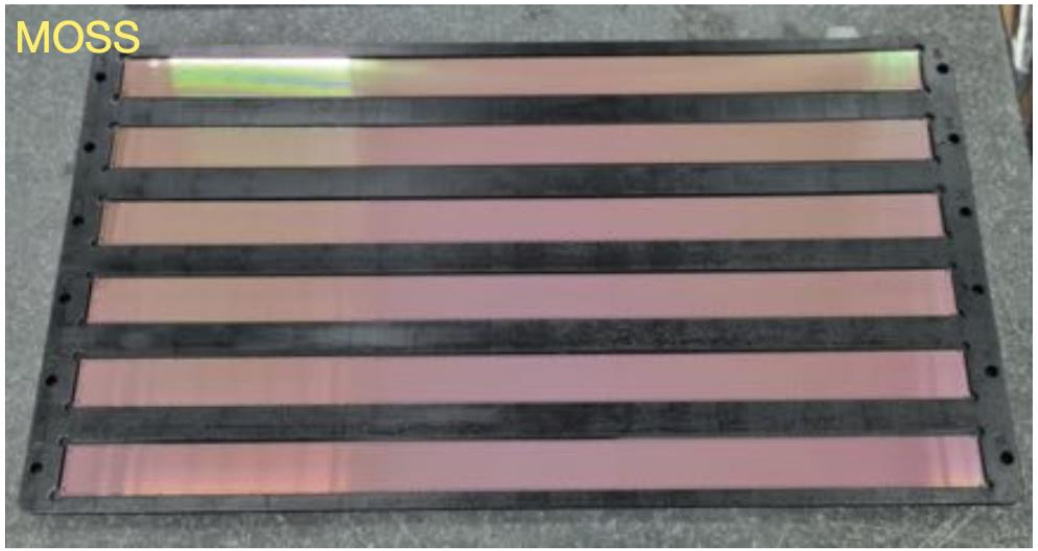
6.72 megapixel

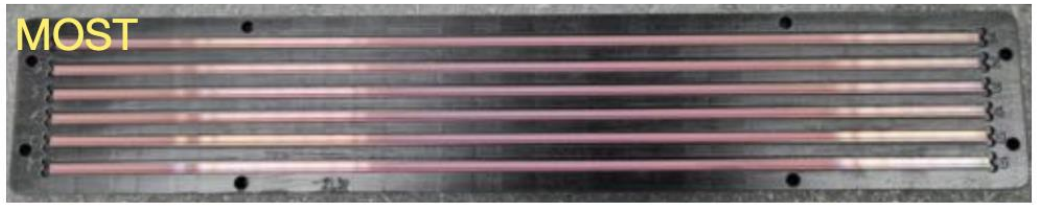


- **10 Repeated Sensor Units** (**RSUs**) per sensor
  - Independent power supply, control & readout
  - **2 half-units** (**HUs**) per RSU
    - Power segmentation domains
    - **Top (22.5 um pitch):**
      - Conservative layout
      - 7 mW/cm^2 (analog FE)
    - **Bottom (18 um pixel pitch):**
      - Compact layout
      - 11 mW/cm^2 (analog FE)
    - **4 regions** in each half-unit

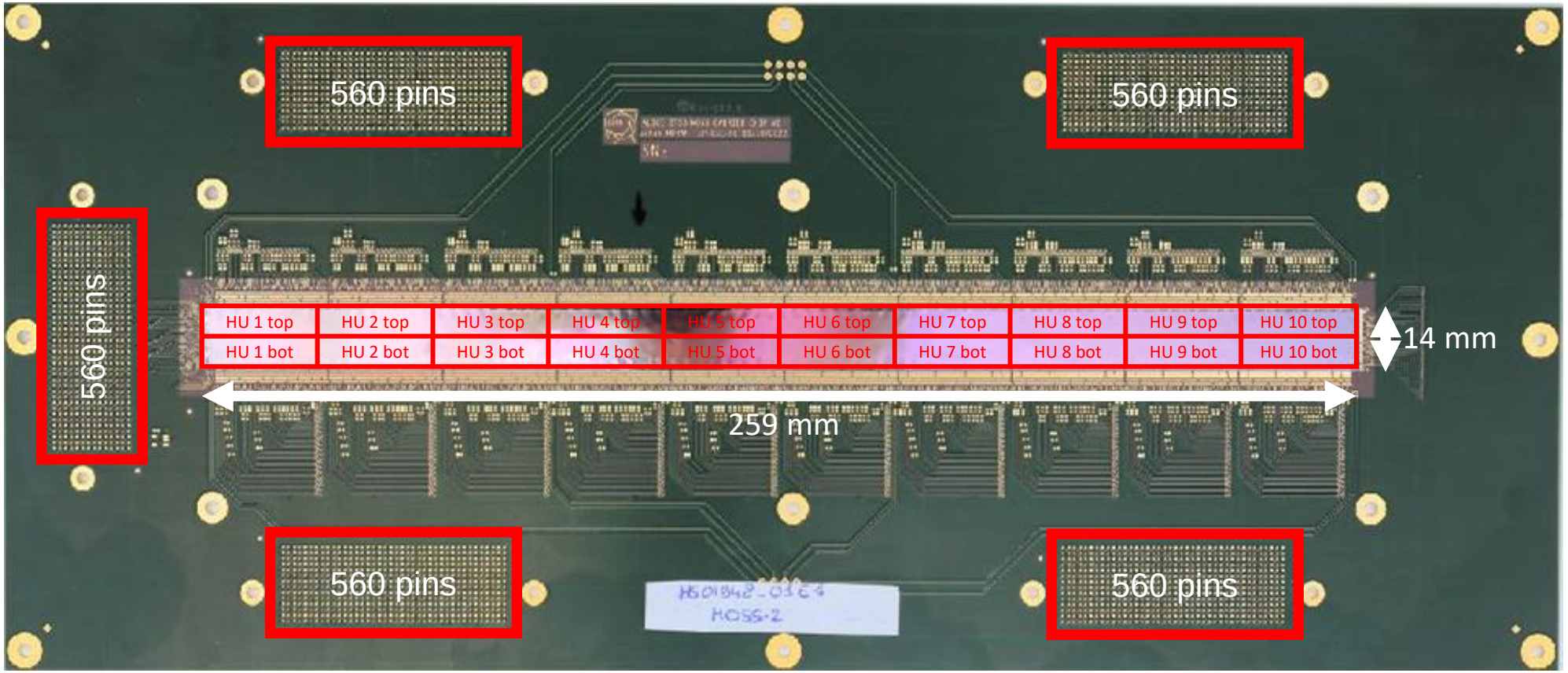
Challenging handling of stitched chips







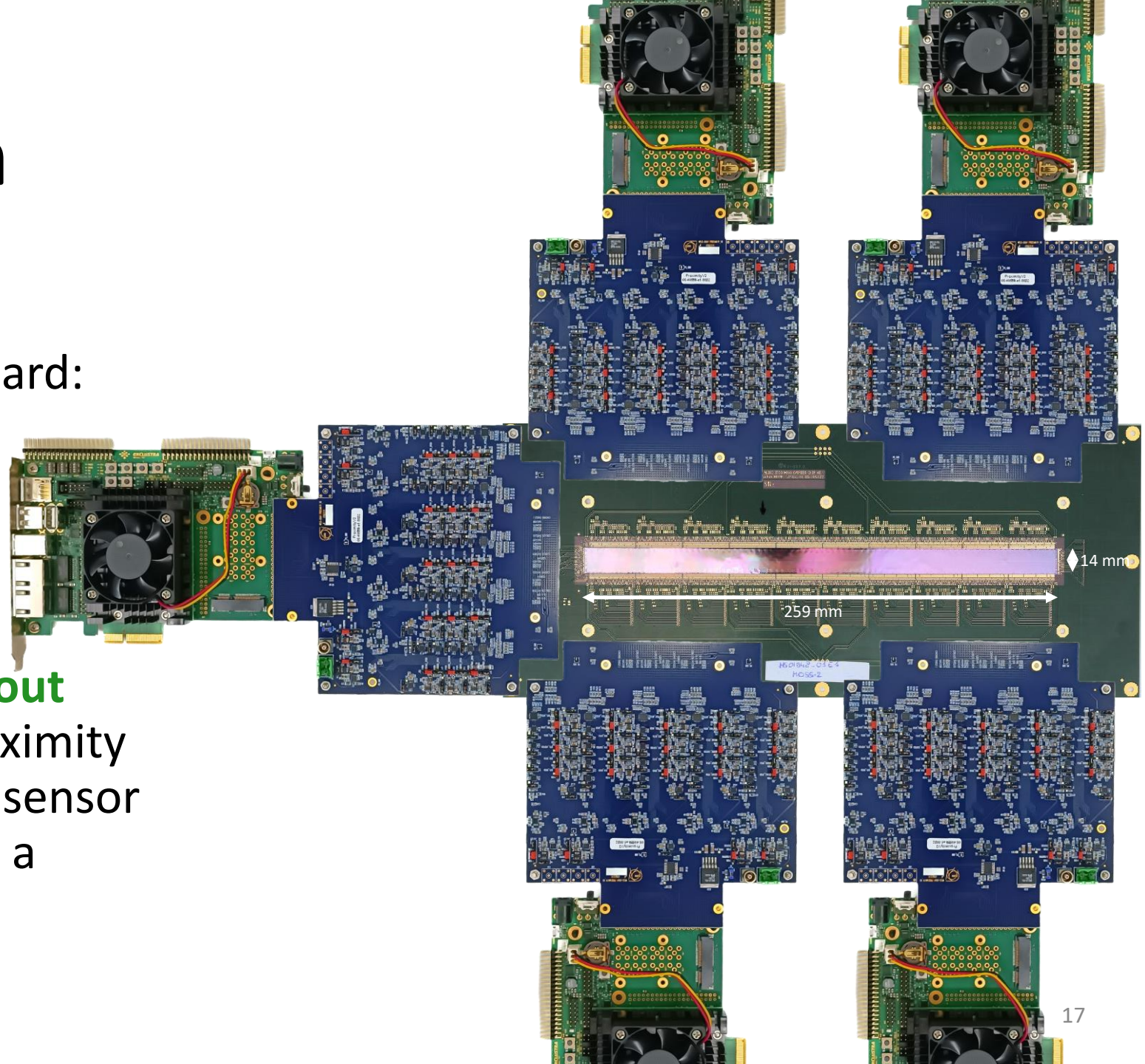
MOSS on the carrier card



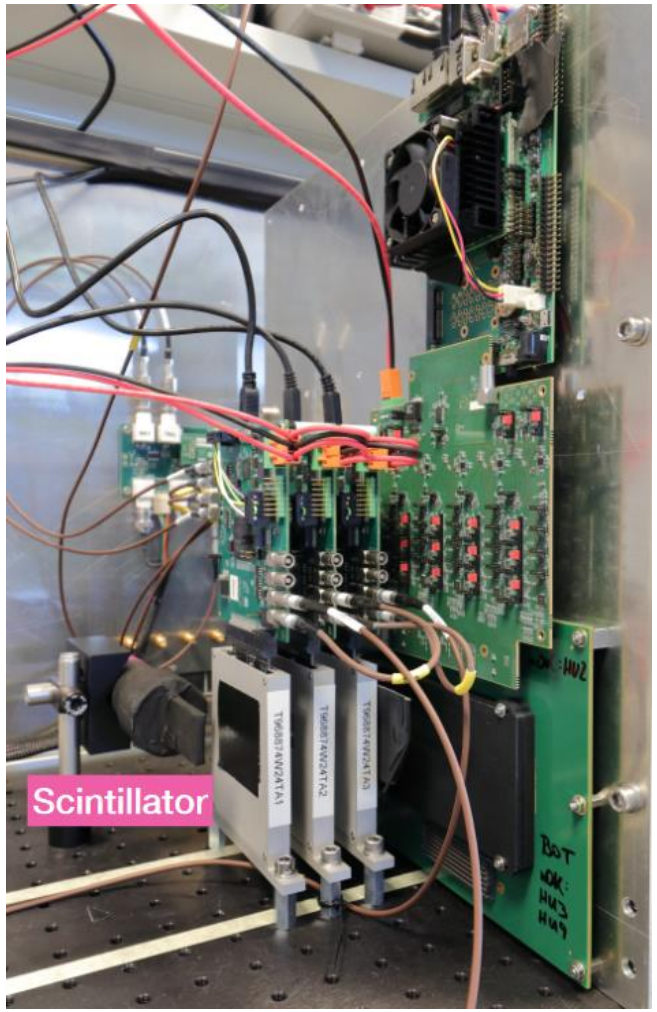
MOSS test system

Three different types of board:

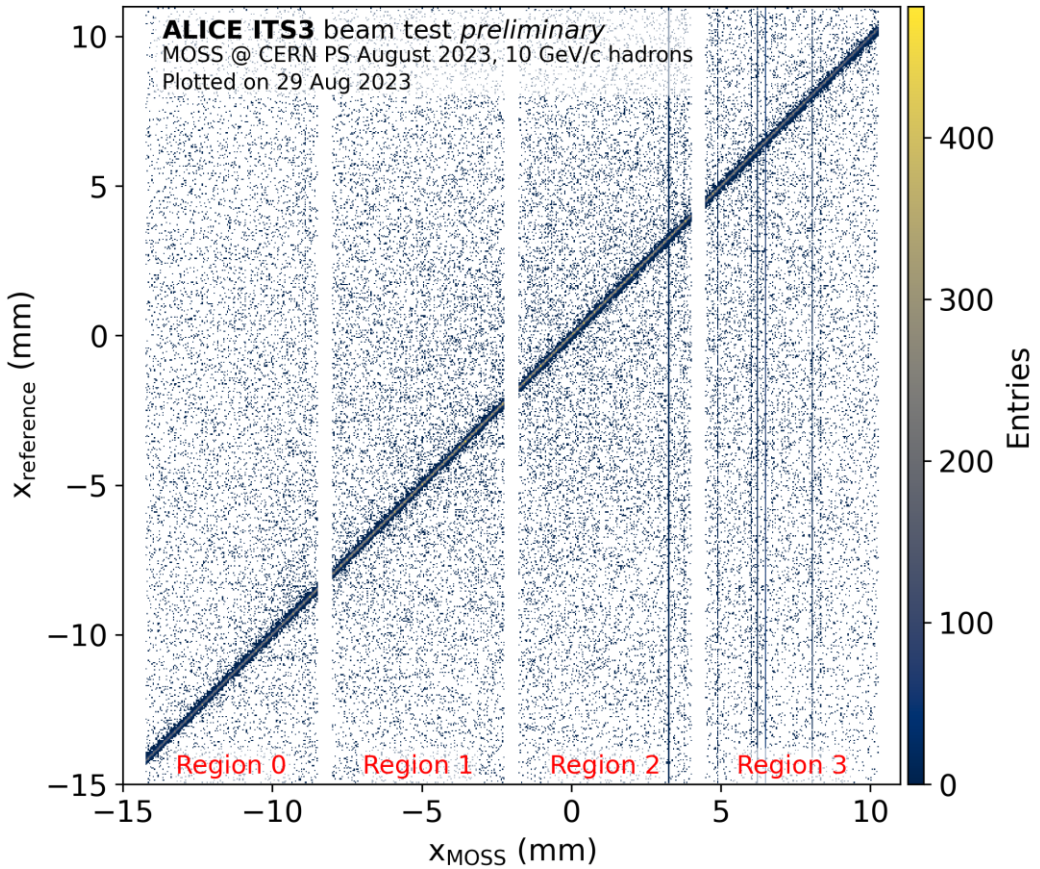
- **Carrier card**
- **5x proximity cards**
  - 1 card x 4 quadrants
  - 1 top/bottom halves
- **5x automation and readout modules** to steer the proximity boards and interface the sensor control and readout with a computer

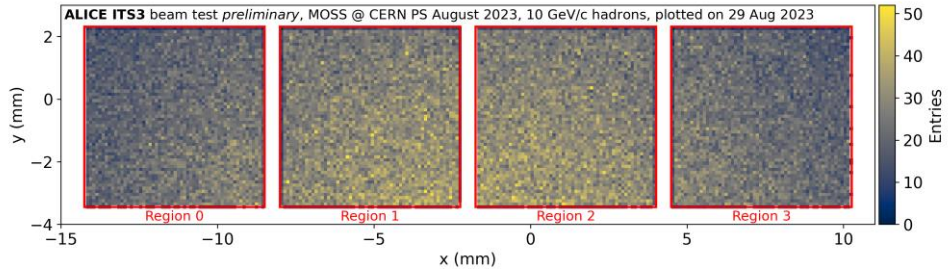


MOSS – first test results



- 16 MOSS bonded and being tested
- Collecting data on the yield
- First chips tested with the beam





Summary and outlook

- Bending of MAPS down to 18 mm doesn’t affect their performance
- TPSCo 65 nm CMOS process is validated for ITS3:
  - Spatial resolution: ~ 5 µm
  - Radiation hardness: 10 kGy + 10^{13} n_{eq} /cm^2
- First stitched prototypes work and being tested
- ER2 submission in preparation: final full scale sensor prototype
- TDR to be presented to LHCC in November 2023


ALICE