VTX detector for the Belle II Experiment

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INTENSITY frontier GDR-InF

Outline

01 Belle II Experiment

02 Vertex detector VXD

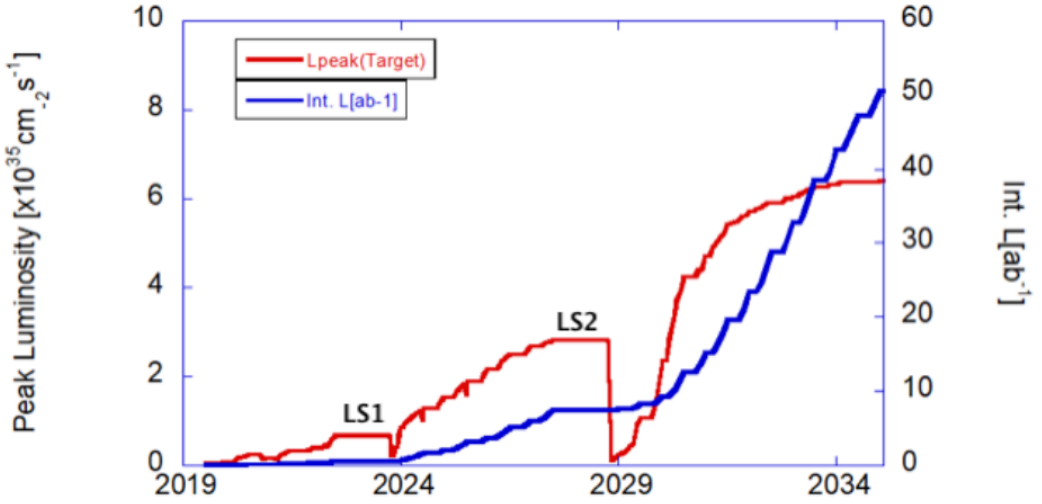
03 VTX concept

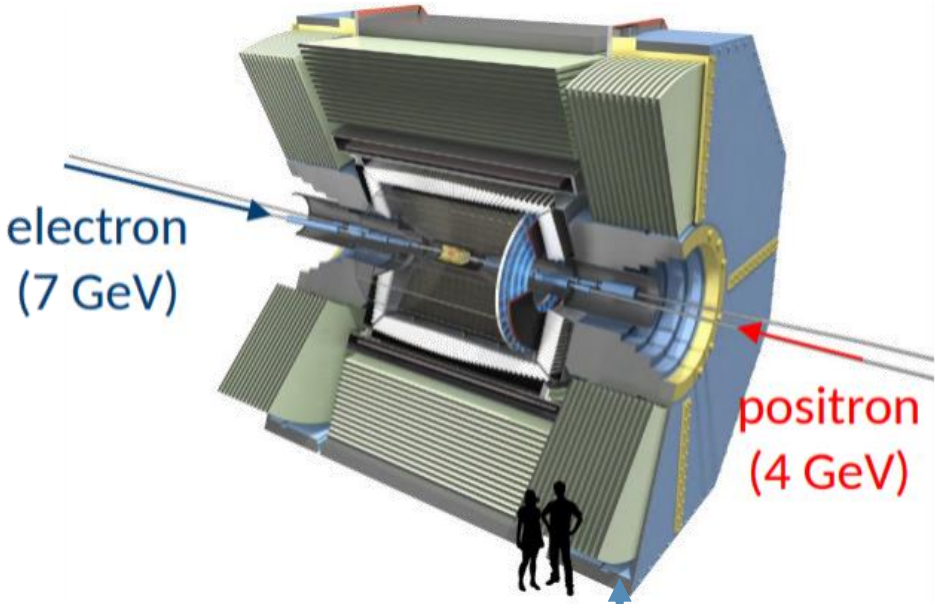
04 Tower Jazz-Monopix 2 chip

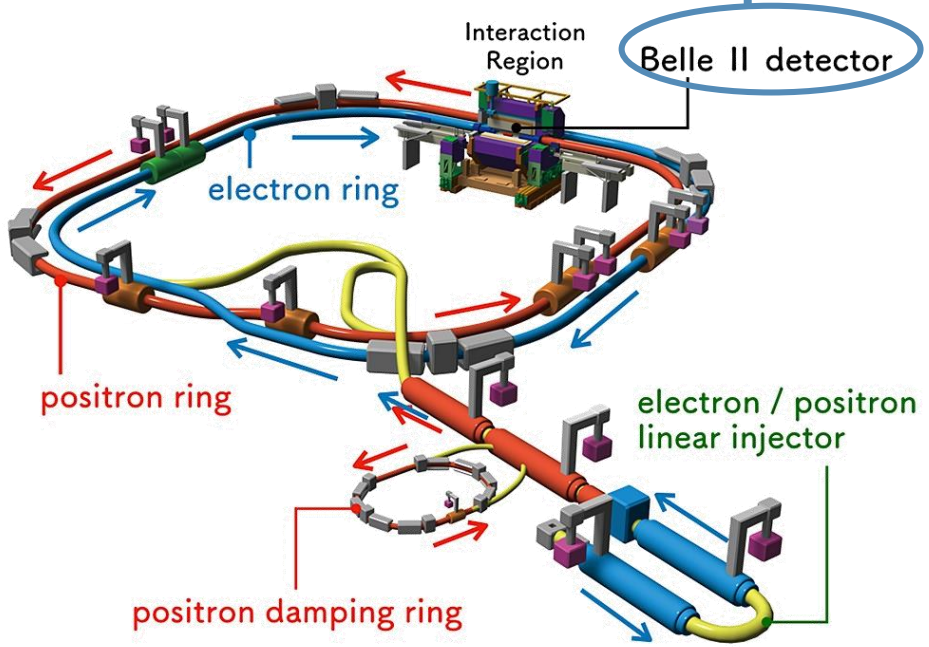
05 OBELIX sensor : Optimized BELLE2 pIXel sensor

Belle II Experiment

- Located at the SuperKEK-B collider in Tsukuba,Japan
- Asymmetric e^+- e^- collider at 4 / 7 GeV and √s = 10.58 GeV
- Target integrated luminosity of **50 ab^{-1}**
- Target instantaneous luminosity of **$6x10^{35}$ cm^{-2} s^{-1}**
- A long shutdown (LS2) is foreseen around year 2027

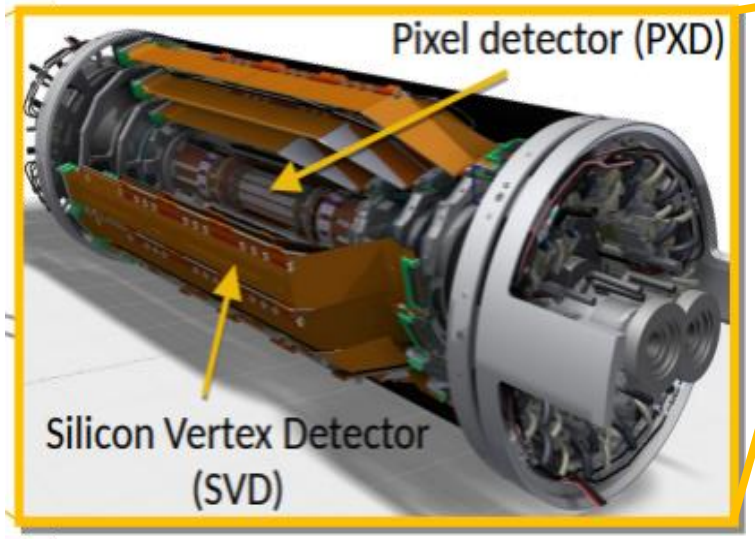


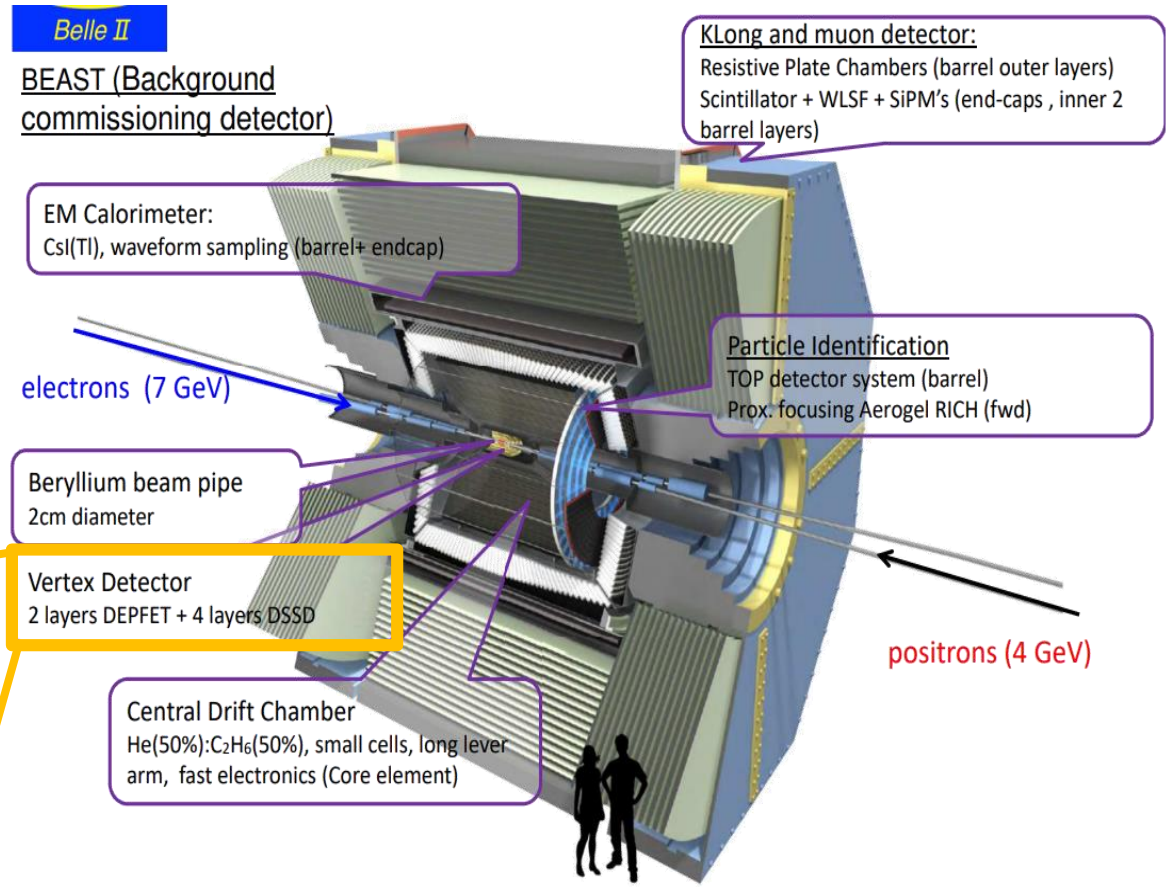




Current vertex detector VXD

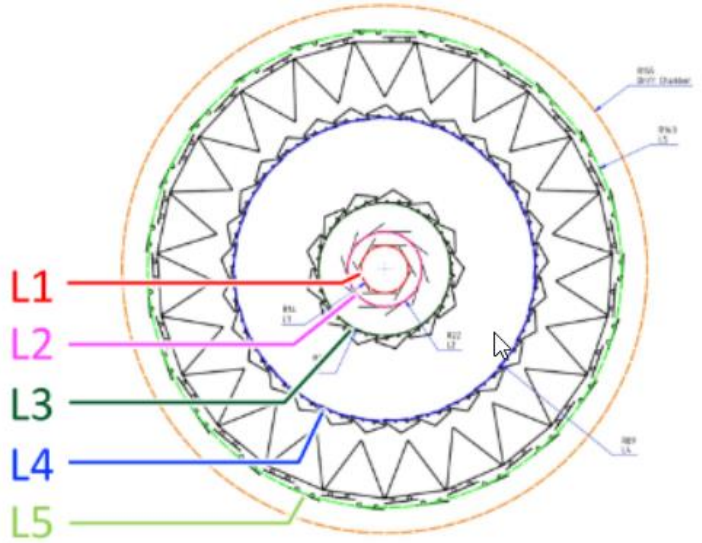
- The main tracker device is the central drift chamber (CDC), which is complemented by a vertex detector (VXD).
- Its main task is the precise estimation of decay vertices in addition to very low momentum track finding.
- Two different technologies compose the VXD :
  - Two layers of DEPFET pixels (PXD)
  - Four layers of double sided silicon strip sensors (SVD)

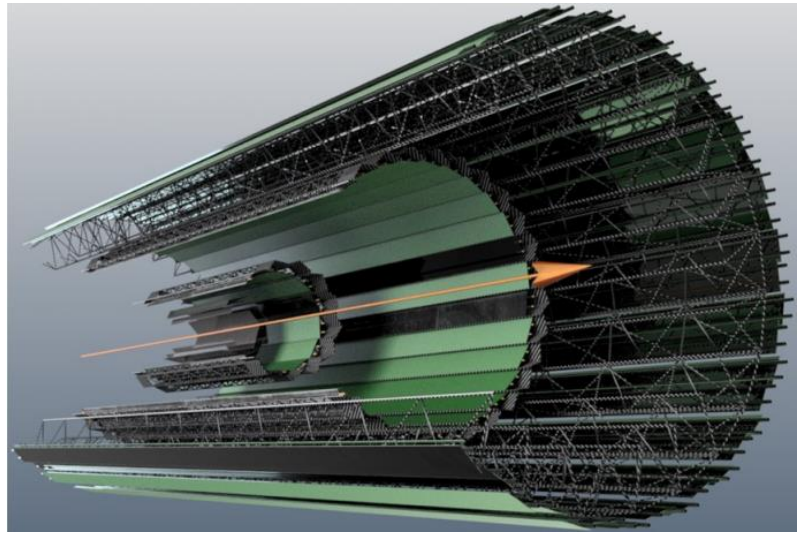




VTX upgrade concept

- The VTX Upgrade Concept scheduled for 2027/2028
- A new fully pixelated CMOS detector to replace the VXD ➡ **VTX**
- Reduced material budget ~ 2.5%X0 instead of 3.8%X0 (sum of all layers)
- Improved tracking resolution
- Increase space-time granularity
- 5 straight layers :
  - L1 and L2 (iVTX)
  - L3 to L5 (oVTX)
- Identical chips on all layers: **O**ptimized **BEL**le II p**IX**el sensor
- **D**epleted **M**onolithic **A**ctive **P**ixel Sensors (**D**MAPS) process





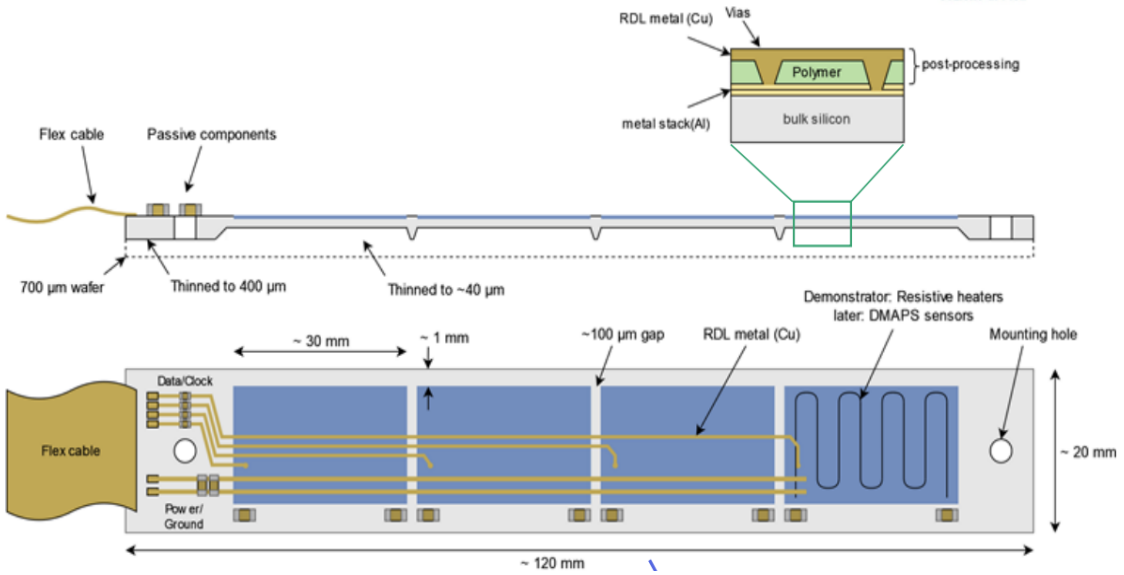
VTX upgrade requirements

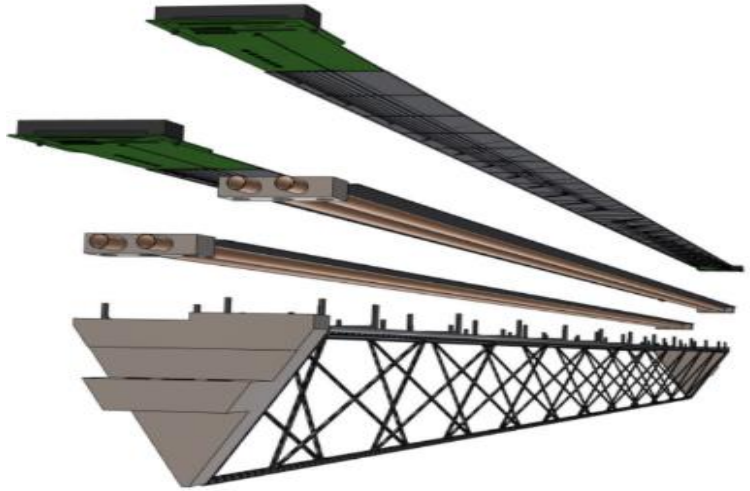
- Fast sensor integration time : 25 to 100 ns
- High granularity (pixel pitch in the range 30-40 µm²)
- Low material budget ~ **2.5%X0** (sum of all layers)
- Hit rate: about 120 MHz/cm²
- TID : about 10 Mrad / year
- NIEL : about 5x10¹³ n_{eq} /cm²/year
- Limited power dissipation (maximum allowed of 200 mW/cm²)
- Same sensor type for all layers

VTX detector mechanics

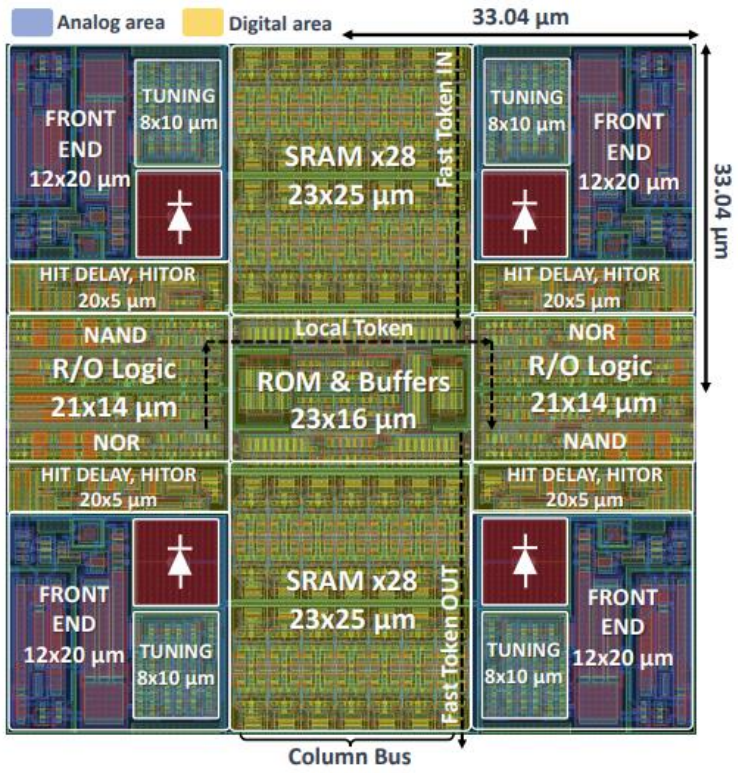
- L1 and L2 (iVTX):
  - Radii at 14, 22 mm
  - All silicon ladders
  - Air cooling (constrains power)
  - ~ 0.1%X0 for L1 &L2

- L3 to L5 (oVTX):
  - Radii at 39, 90, 140 mm
  - Carbon fiber support frame
  - Cold plate with water cooling
  - ~ 0.4 %X0 for L3
  - ~ 0.8%X0 for L4 & L5

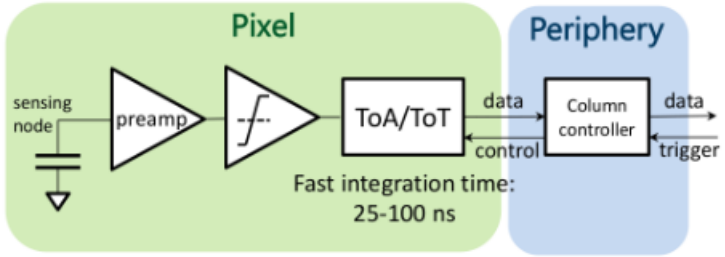




Tower Jazz-Monopix 2 chip



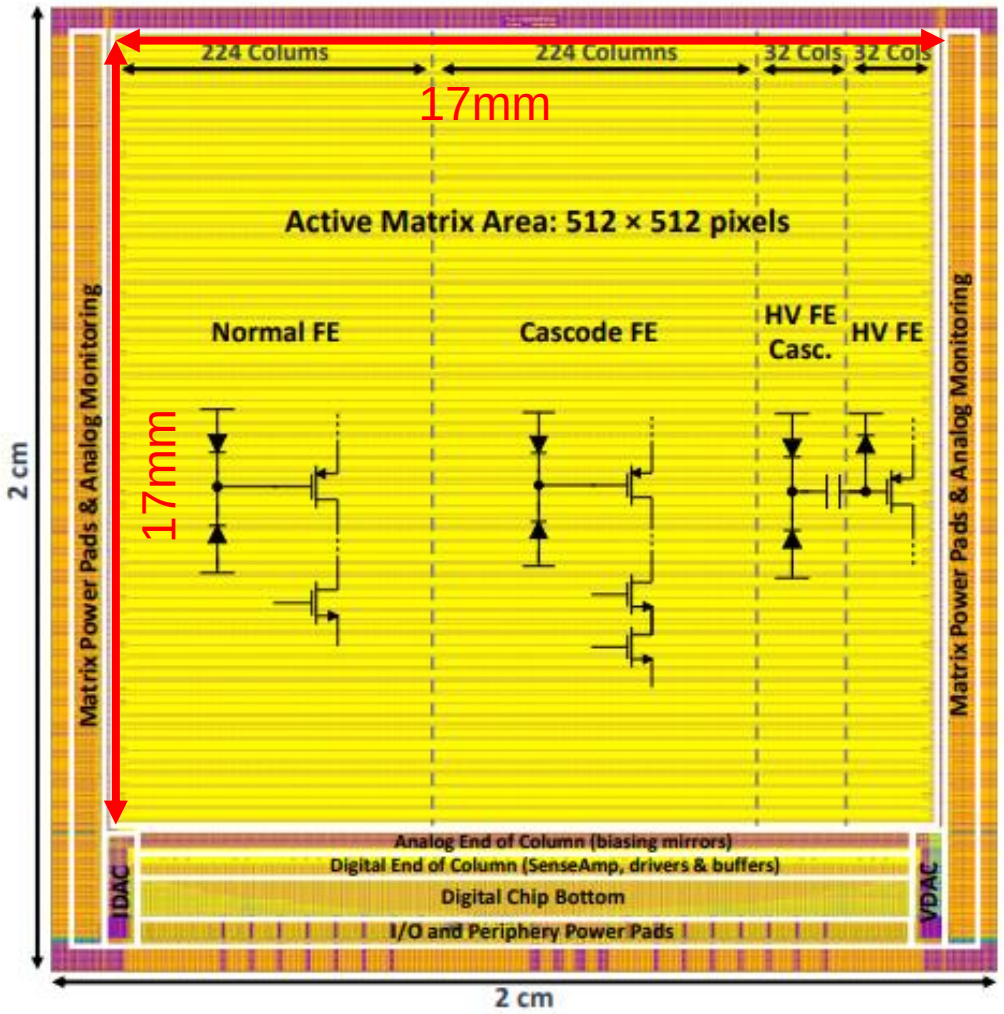
TJ-Monopix readout scheme



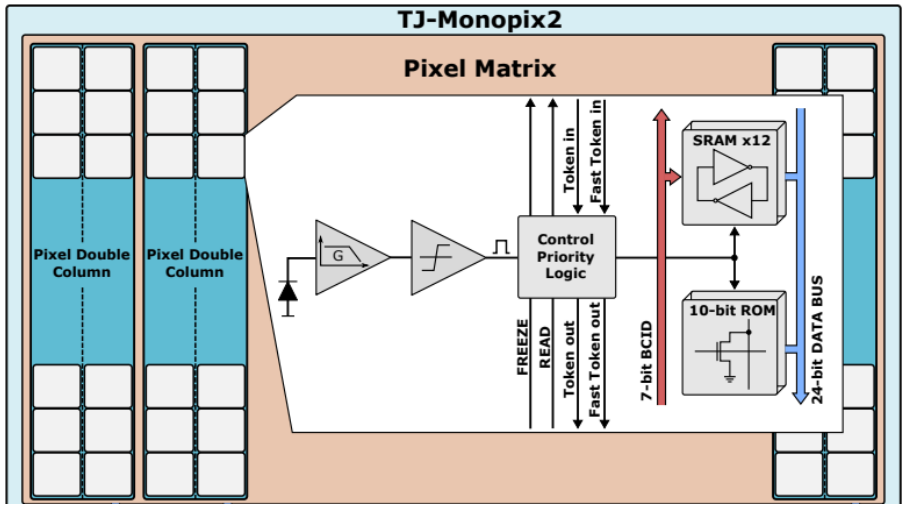
- Developed for ATLAS experiment (2020)
  - FE derived from ALPIDE
  - Column-drain R/O architecture
- DMAPS Tower Jazz 180 nm process
- 2 × 2 cm² chip : 512 × 512 pixels
- Pixel pitch: 33.04 × 33.04 µm²
- Expected from design:
  - ~ 100 e− min. threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - MIP ~ 2500e−

Base-line option for OBELIX

Pixel Matrix: TJ-Monopix 2



Kostas Moustakas thesis (https://cds.cern.ch/record/2782279?ln=fr)

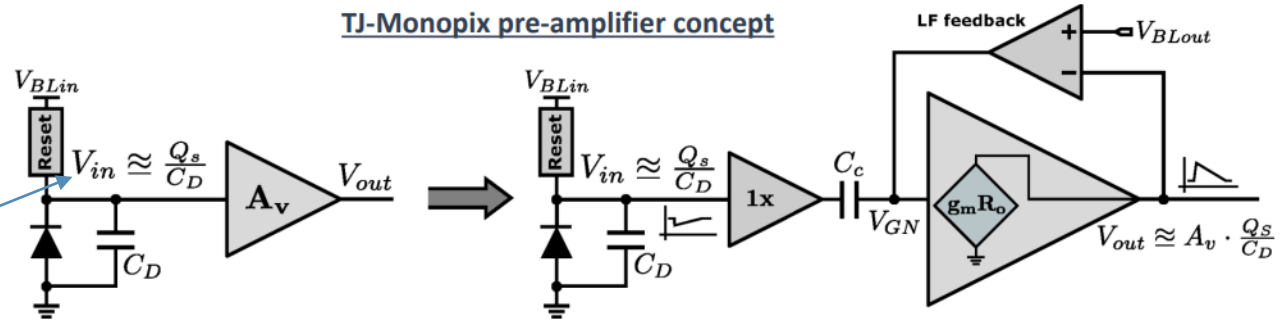


- 17mmx17mm active area
- Four pixel Front-End (FE) flavors with differences in pre-amplifier, sensor coupling and biasing
- Two columns for Analog Monitoring
- Full custom in-pixel digital

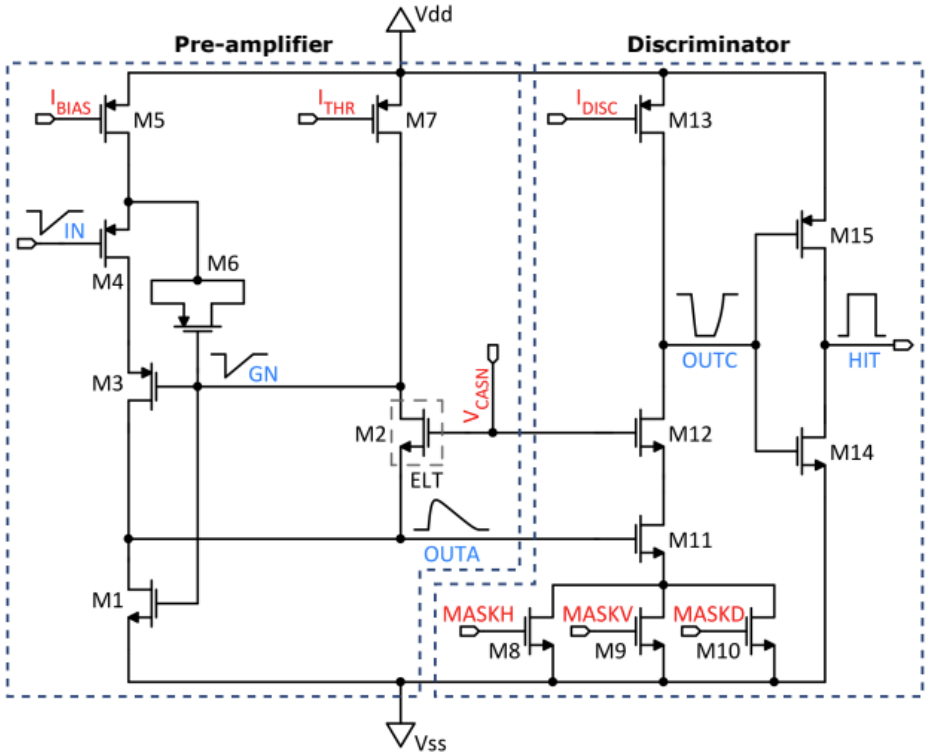
Pixel Matrix: Analog Front End

Very low input capacitance → High input voltage

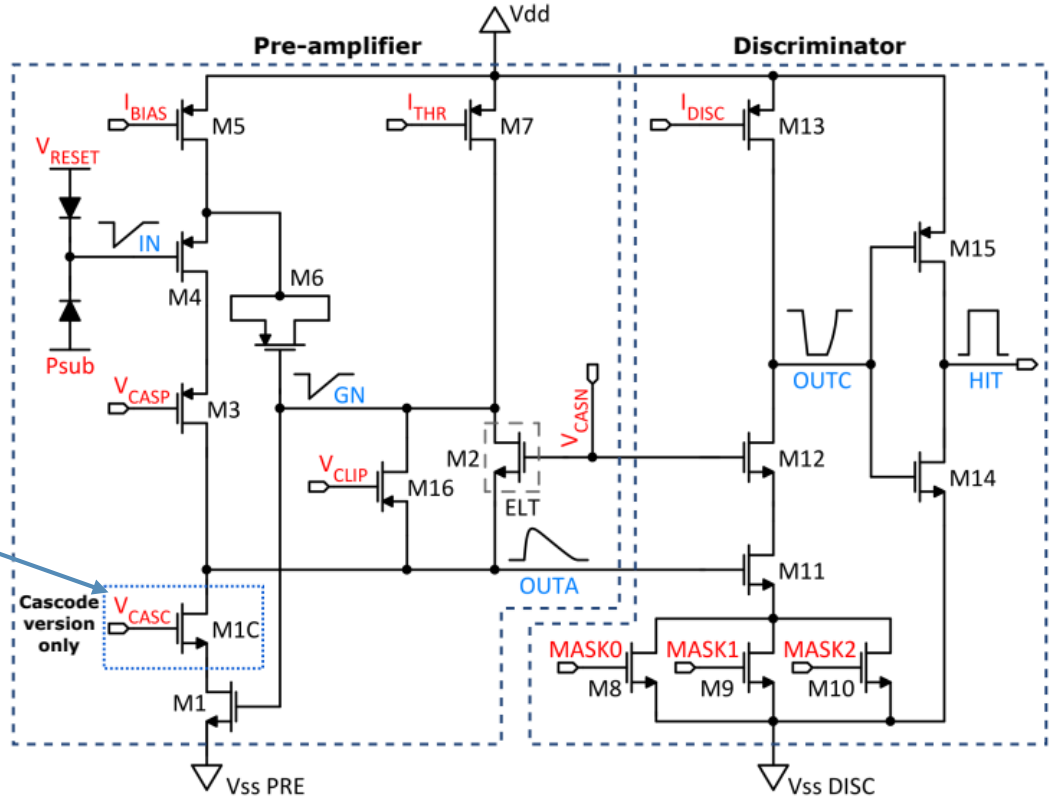
TJ-Monopix pre-amplifier concept



Voltage amplifier



Cascode architecture → High gain



Normal Front End Design

Cascode Front End Design

Pixel Matrix: Analog Front End simulation

Objective : Reduction of the TJ-MONOPIX2 front-end (FE) preamplifier's power consumption

Normal FE pixel preamplifier	Improved normal (FE) pixel preamplifier	Cascode FE pixel preamplifier	Improved cascode (FE_casc) pixel preamplifier
Ibias = 500 nA	**Ibias= 300 nA**	Ibias = 500 nA	**Ibias= 300 nA**
Power consumption = 1µW	**Power consumption = 650nW**	**Power consumption = 1µW**	**Power consumption =650nW**
Peaking Time = 107,48 ns	**Peaking Time = 129,46 ns**	Peaking Time = 132,85 ns	**Peaking Time = 182,34 ns**
Gain = 1,74 mV/e-	Gain = 1,53 mV/e-	**Gain = 3,35 mV/e-**	**Gain = 2,81 mV/e-**
SNR = 39,1	**SNR = 39,13**	SNR = 56	**SNR = 57,33**
ENC = 2,55 e- rms	ENC= 2,55 e- rms	ENC = 1,78 e- rms	ENC = 1,74 e- rms

→ The power consumption can be reduced by 35%

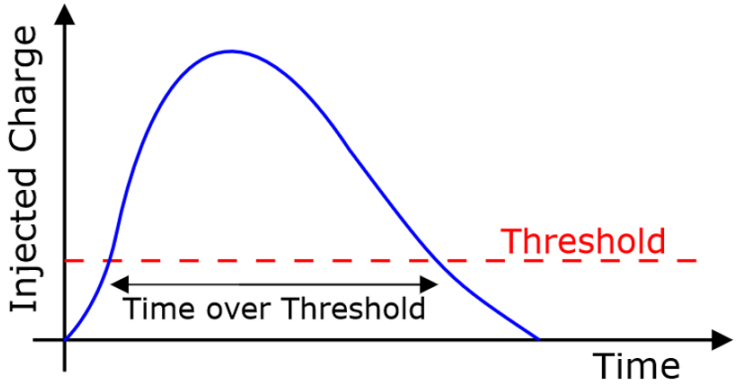
Pixel Matrix: Analog Front End simulation

- On going : study of reducing the main biasing current in order to have low power dissipation
  - Lowering the main biasing current from 500 nA to 300 nA leads to a lowering of the power dissipation by 35% (for both Normal FE and cascode FE).
  - However by reducing the current Ibias , we have small variation on peaking time
  - The gain of the preamplifier is also reduced but it can be improved by varying the feedback current Ithr while keeping a signal-to-noise ration (SNR) as high as possible.

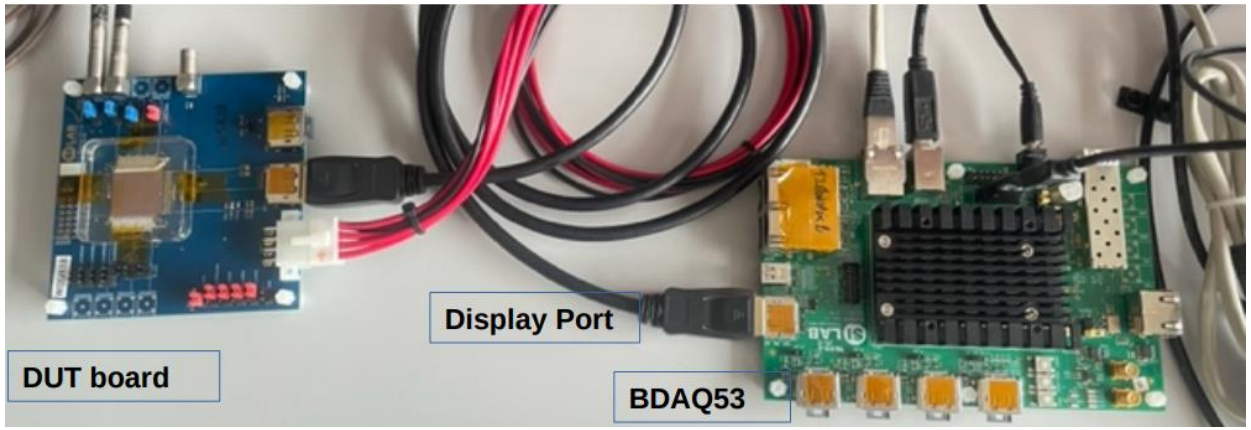
The cascode Front End flavor is chosen for OBELIX

TJ-Monopix 2 testing

- Characterization on-going
  - Threshold (lowest value, dispersion)
  - Noise testing
  - ToT (Time Over Threshold) calibration



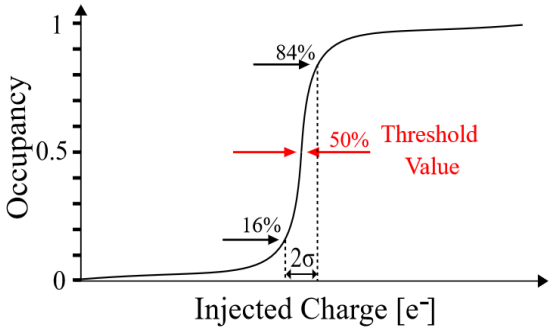
- Setup composed by BDAQ53 board and DUT board through a display port
  - Use a external power supplies for the main powers
  - Software is based python3.8, use ananconda as environement, Basil3.2.0 as low level and TJMonopix2 software available on Silab Git repository

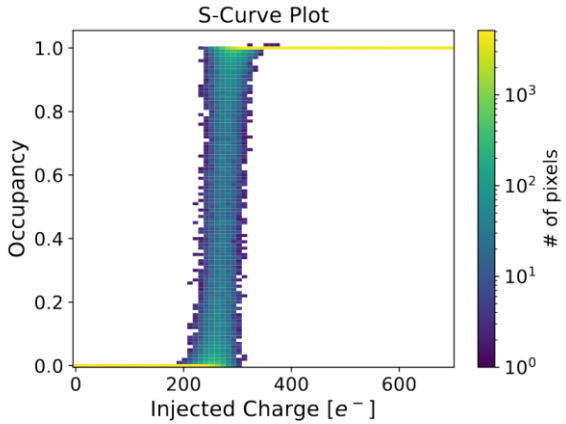


Banc de test de TJ-Monopix2

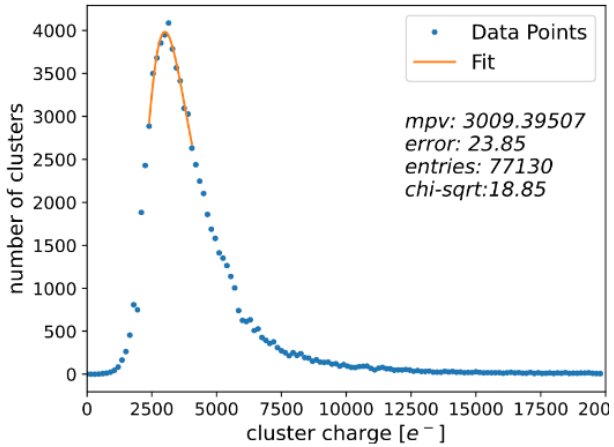
TJ-Monopix 2 testing

- Tests done in in Bonn, Pisa, HEPHY, CPPM, Gottingen
- The internal injection test :
  - A deliberate amount of known charge is introduced into the pre-amplifier of the system
  - The output generated is then quantified using the Time Over Threshold
- S-curve tests to determine threshold : as the injected charge, at which a 50% occupancy is reached
- The noise level can be determined from the slope of the S-curve





- Beam testing performed at DESY in Jun 2022 (4 GeV e-)
- Unirradiated chips
  - Preliminary settings used
  - Very high thresholds ~ 550 e–
  - Hit efficiency: 99.54 +- 0.04 %
  - Cluster position residuals: 9.15 um



- New test beam in July 2023:
  - Lower threshold settings
  - Angle scan
  - Efficiency for irradiated chip $10^{14} - 10^{15}$ n_{eq} /cm²
  - Data analysis ongoing

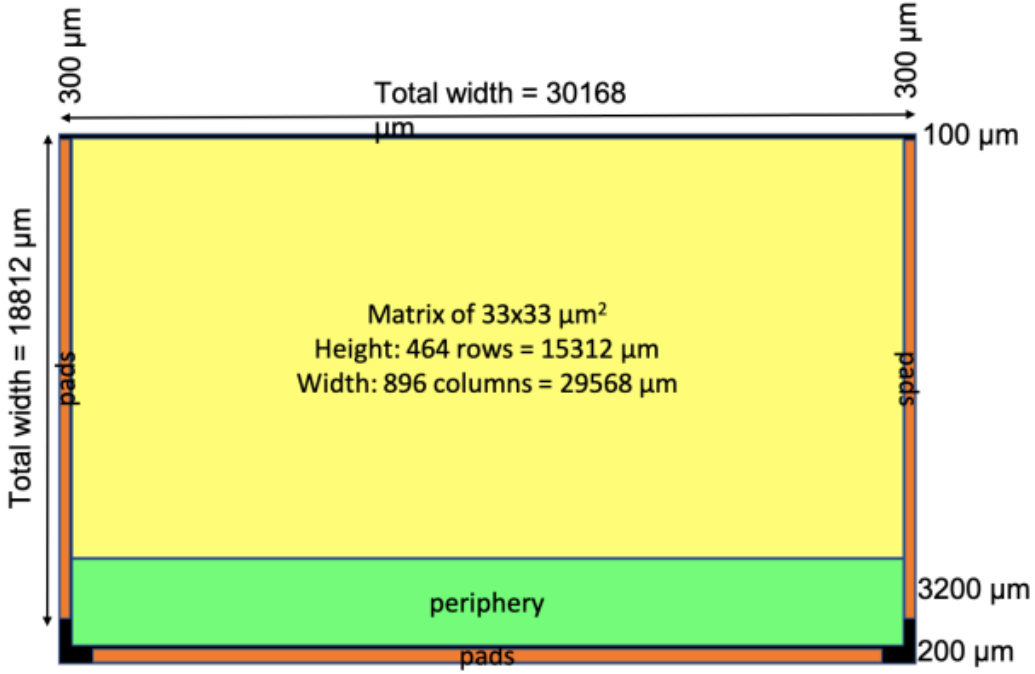
OBELIX sensor

- The OBELIX sensor is under development
- Derived from the existing TJ Monopix2 chip
- Matrix size: 464x896 pixels
- Timestamp resolution: ~50ns
- Power consomption < 1.5 W
- Up to 10µs trigger latency
- Technology : Tower-Jazz 180 nm

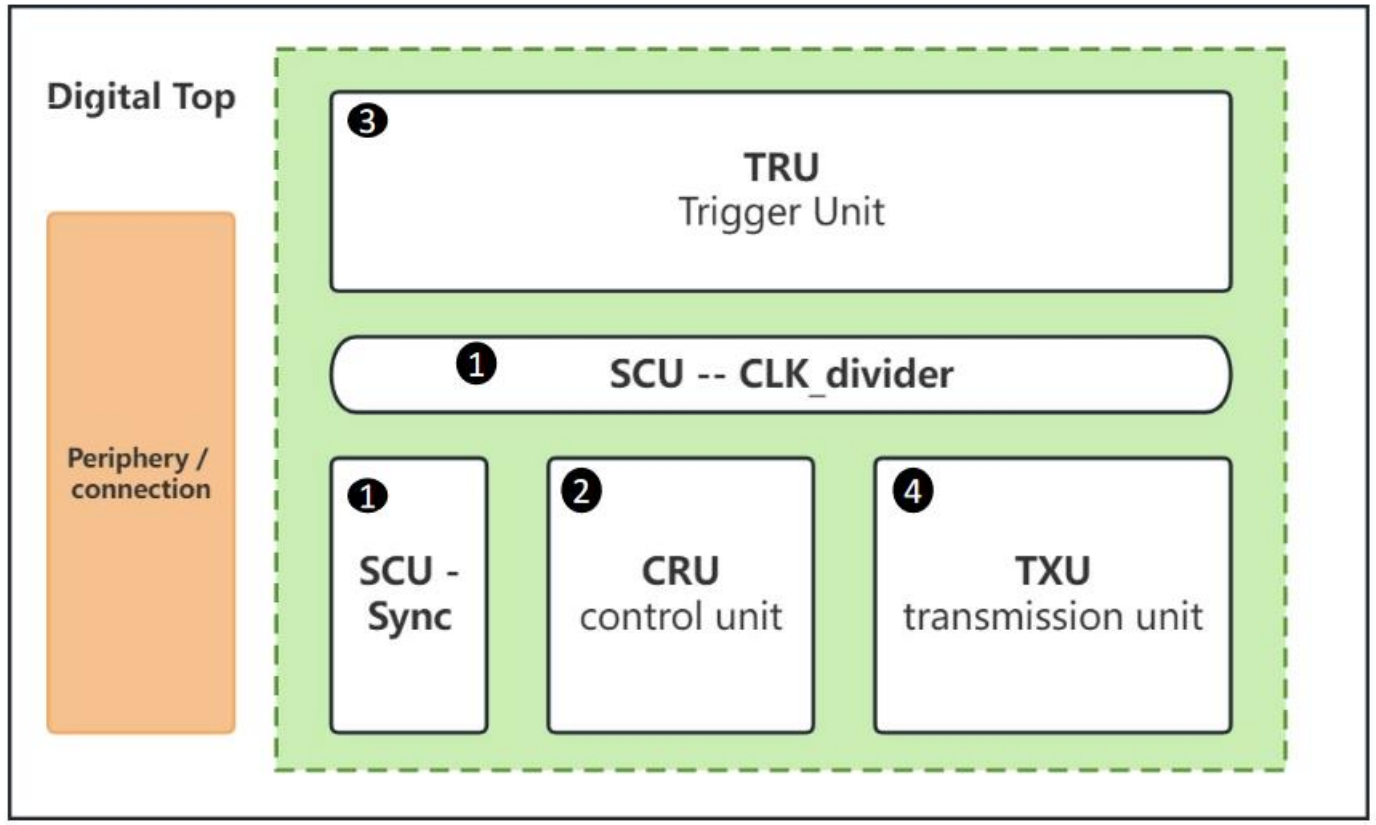
Pixel matrix
- Copied from TJ-Monopix2
- Radiation tolerance granted
- Possible power optimisation

Power pads
- Power regulators added
- Simplified system integration

Periphery
- Main clk-in : 160MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 320 MHz average bandwidth
- RD53 control/readout protocol



OBELIX : Digital Blocks



- Module division : 4 main parts

❶SCU – sync & clk divider: clock divider, Rx_data SIPO synchronization

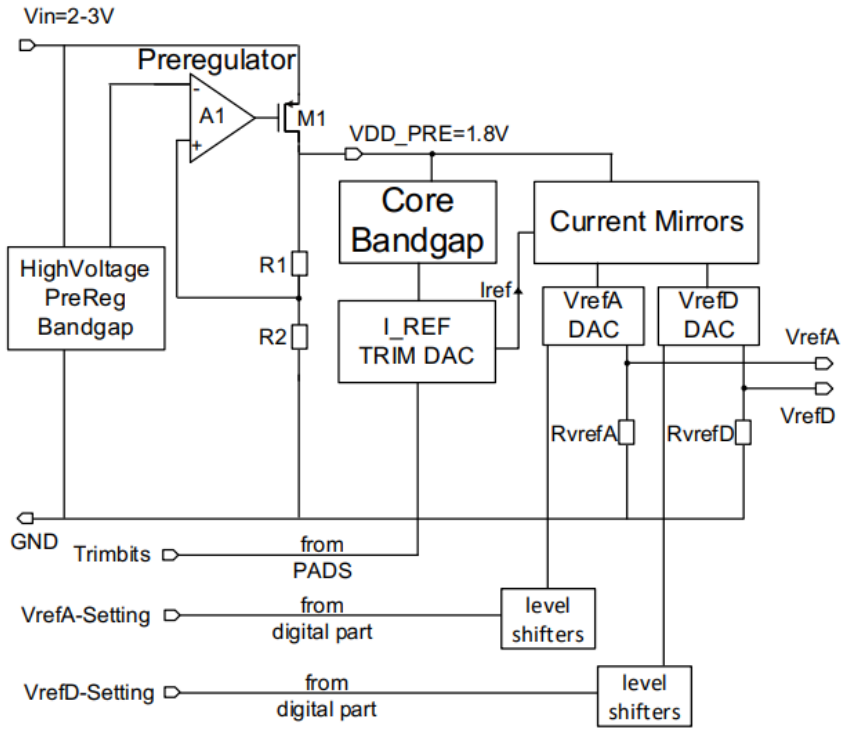
❷CRU – Control Unit: Implementation RD53B interface, main functions: command decoder, global register configuration

❸TRU – Trigger Unit: Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output

❹ TXU – TX Unit: generate output data and sequential output, main functions: data framing, serializer

OBELIX Power Management

- Long linear ladders: voltage drop across ladder
- Narrow LDOs (Low Dropout) on both sides of the chip
- Input voltage 2 to 3 V
- LDO allows to compensate the voltage drop
- LDOs cause some dead area, but TJ-Monopix2 matrix requires power from the sides
- Aspect ratio of regulators as high as possible to keep dead area small



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Conclusion and outlook

- The upgrade to Depleted CMOS MAPS technology offers a promising path for enhancing the SuperKEK-B vertex detector
- The OBELIX chip is based on the analog part of TJ-Monopix2
- The careful characterization of the TJ-Monopix2 sensor matrix is crucial for the VTX Upgrade proposal
- Possibility to reduce the biasing current of the Front End in order to have less power consumption
- The OBELIX design is in development, with the aim of submitting it at the end of the year
- The VTX collaboration will contribute to a conceptual design report (CDR) for the Belle II upgrade by end 2023 and continue to work on testing and developing the system

Thank you

Backup slides

Depleted Monolithic Active Pixel Sensors

- Sensor and readout electronics on single wafer
- DMAPS combines the compactness of **CMOS sensor** with the performance of **hybrid planar silicon sensors** by :
  - using high-voltage compliant CMOS processes
  - using an isolated deep well that collects charge and includes both analogue and digital circuits : monolithic pixel

- Large signal and fast charge collection
- Sensors can be thinned to 50 µm without signal loss
- Sensors can operate in a high rate environment (< 25 ns)
- Good radiation tolerance