# Le(s) Tracker(s) de l'expérience CMS

**Gaëlle Boudoul (IP2I Lyon/ AICP)**

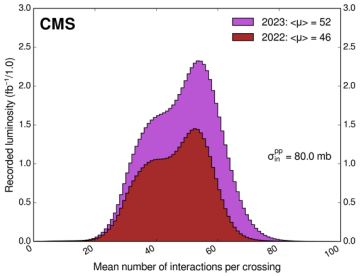
**Intensity Frontier (GDR-InF)**

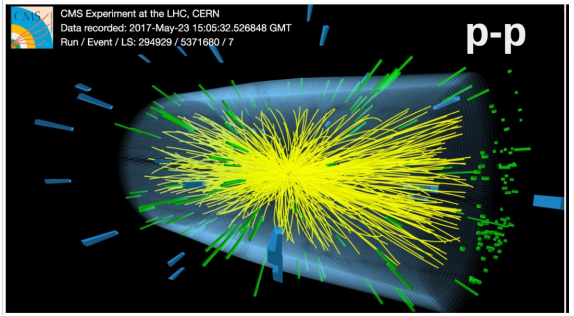
**20 Septembre 2023**

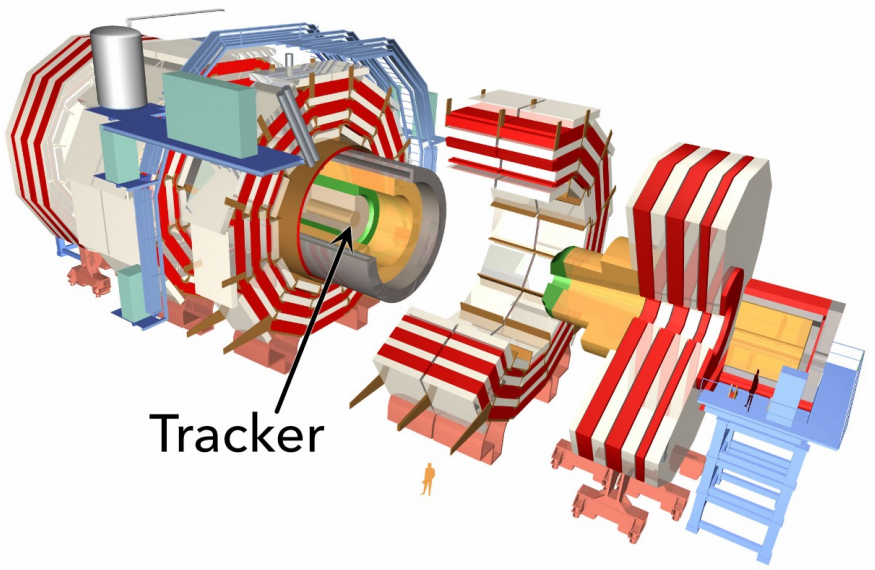
# CMS Tracker

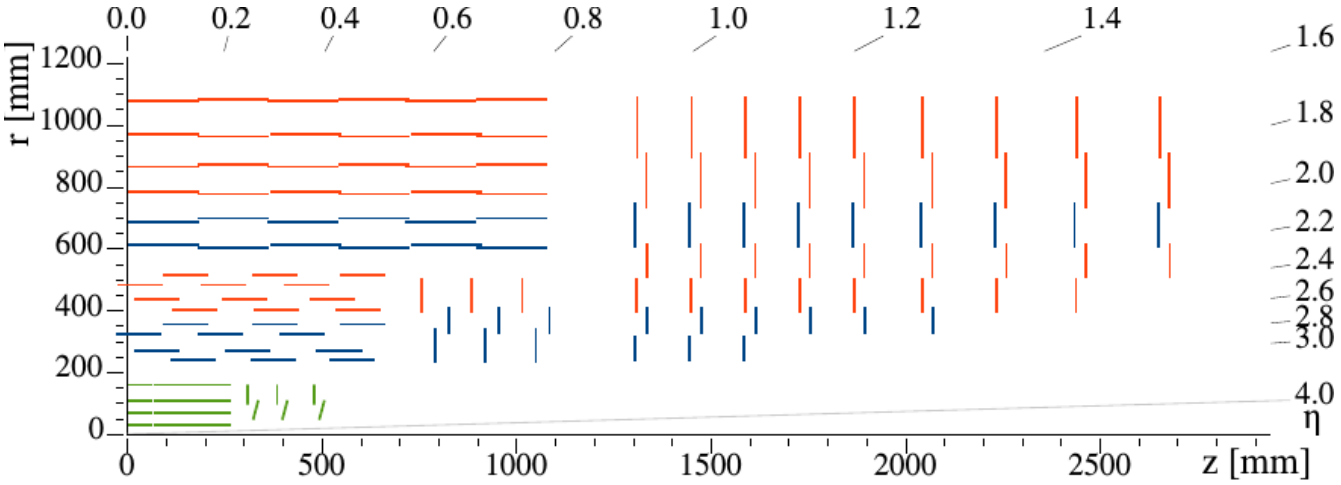
CMS magnet : 3.8T uniform in the tracker volume

typically 30 charged particles within the tracker acceptance per p-p collisions (pile up 50 60 -ish…) → 0(1000) tracks



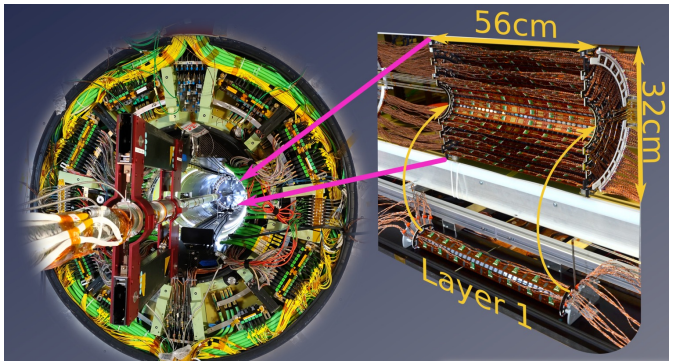




Innter tracker (pixels) - 124 Million pixels

Silicon strips tracker
cooling system (C6F14) will extract the 60 kW power that the front-end electronics dissipate
15 148 individual silicon detection modules comprising 9.3 million readout strips.
200m$^2$ silicium

# The CMS pixel detector in a nutshell

- Closest subdetector to collisions point
- Main upgrade in 2017 (so called phase-1)
  - detector replaced during the winter shutdown (2016-2017)
- Composed of
  - 4-layer Bpix
  - 2x3 disks Fpix
- 124 M readout channels
- 40 MHz triggered readout
- 1184 pixel modules in Bpix
- 672 pixel modules in Fpix



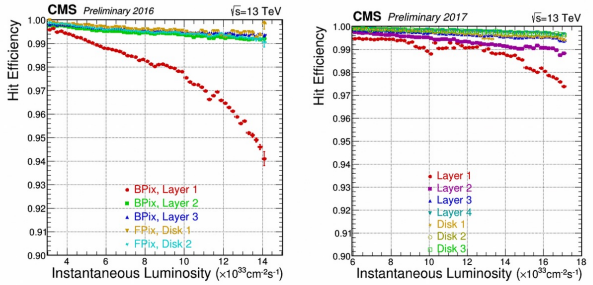
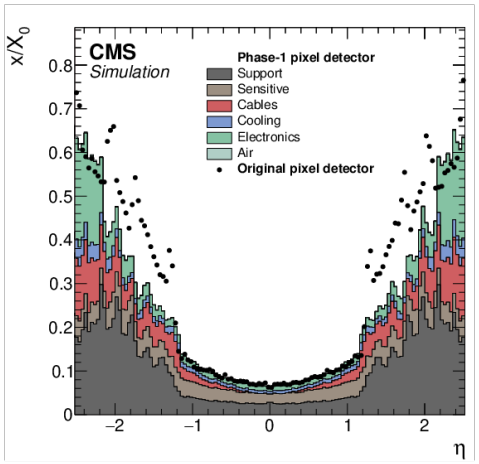
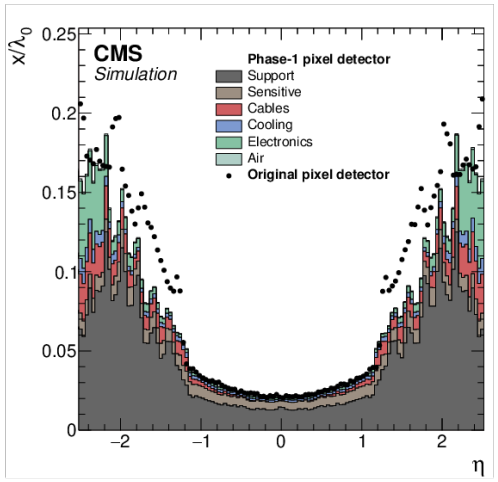
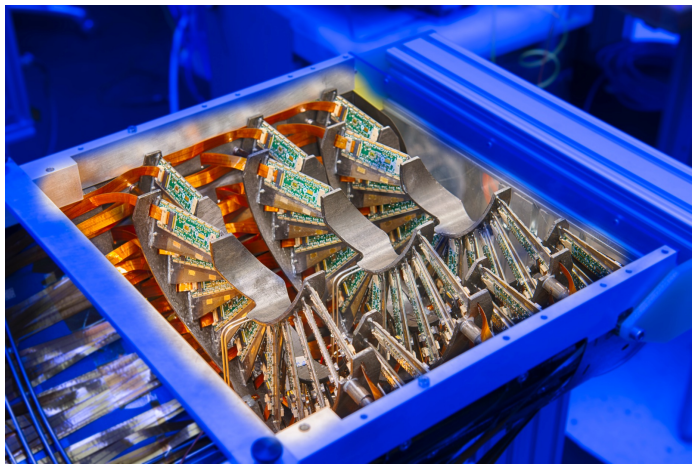



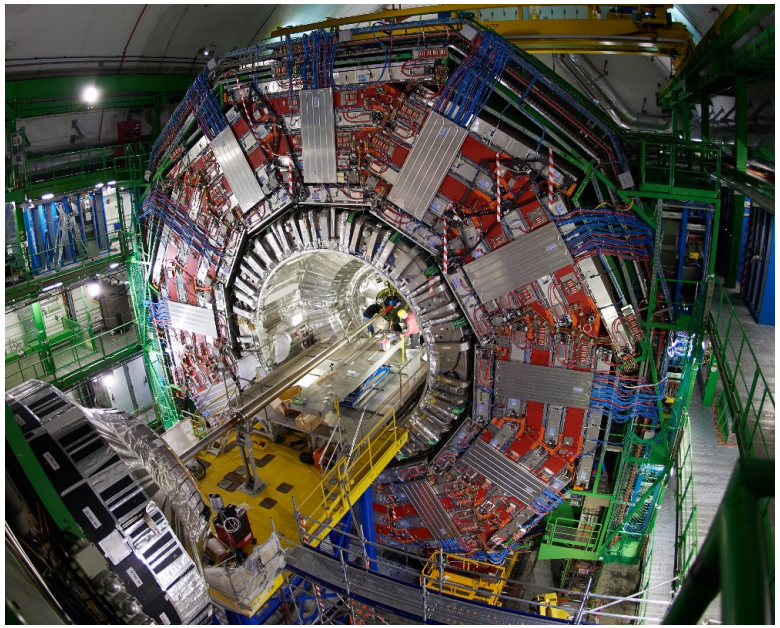

**Figure 2. Hit Efficiency as a function of instantaneous luminosity for different layers of the pixel detector. (from CMS Public result).**
**Left: for the original Pixel Detector. Right: for the upgrade Phase-1 Detector (from CMS public result).**

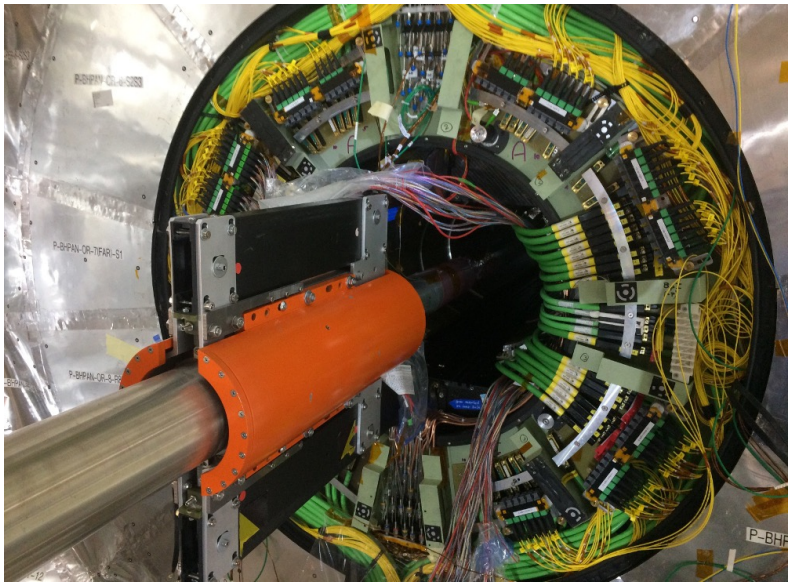


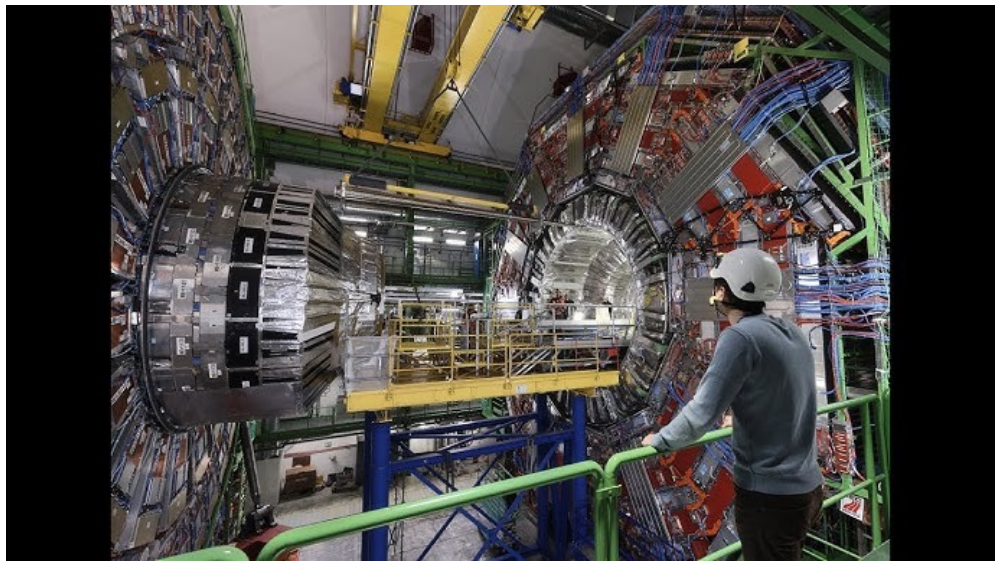



# Installation

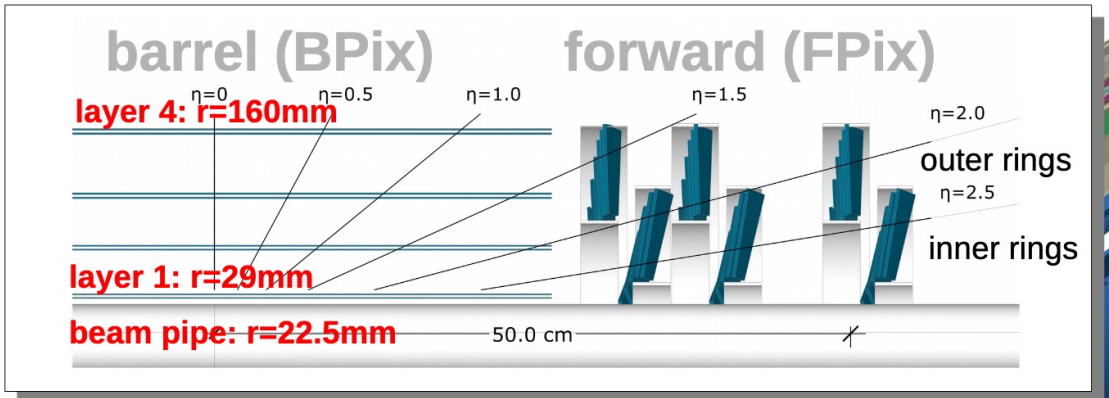


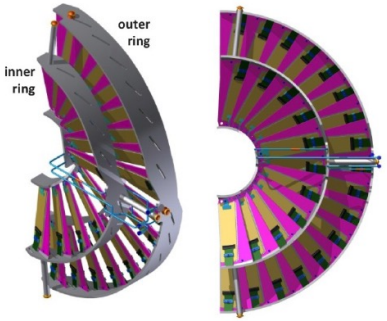




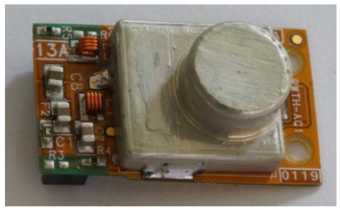
# CMS Phase-1 Pixel Detector

- **4-hit coverage** up to |η|<2.5
- first pixel layer **very close to IP**
- fourth pixel layer connecting better to strip detector
- **turbine-like module arrangement** in **forward disks**
  (inner rings tilted for optimal radial and azimuthal resolution)



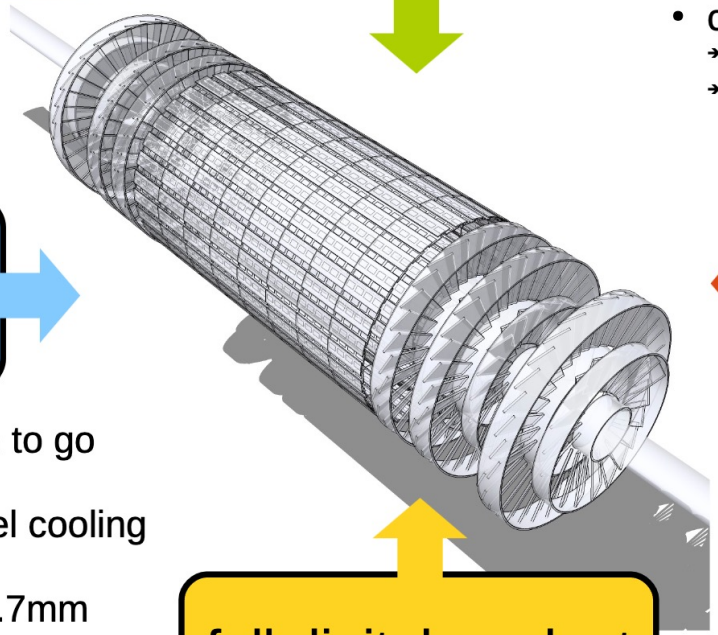



# CMS Phase-1 Pixel Detector – Key Technologies



## DCDC powering

- 1.9 times more channels
- same power cables
- DC-DC conversion near the detector 9-11.4V to 2.4V/3.0V
- core: FEAST 2 ASIC from CERN
  - magnetic field tolerant: 4T
  - radiation hard: >200 Mrad (Si), 5e14 $n_{eq}/cm^2$

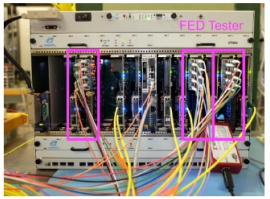


## $CO_2$ cooling

- -22°C, option to go lower
- stainless steel cooling loops:
  - diameter 1.7mm
  - wall thickness 50µm
- very lightweight

## full digital readout

## µTCA DAQ

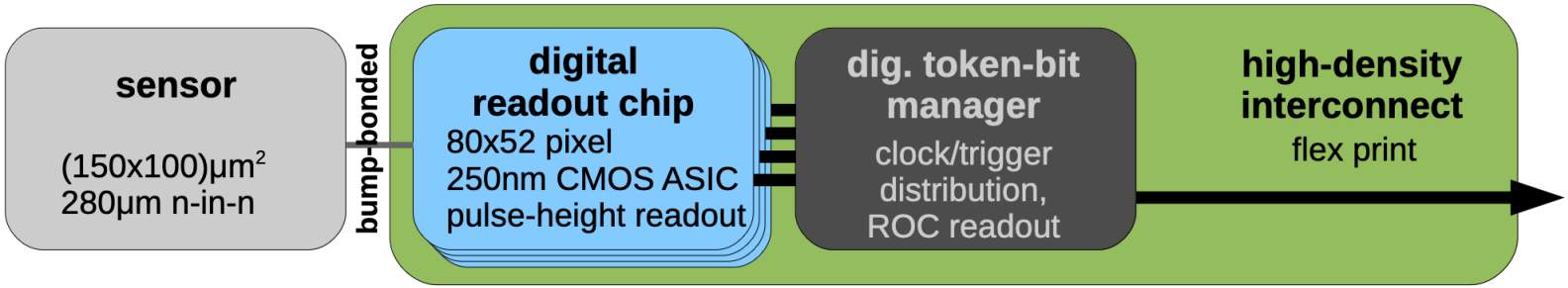



- 108 **FrontEndDrivers** (FED)
- 16+3 **FrontEndController** (FEC)
- all based on **generic AMC card** (FC7) built around Kintech 7 FPGA and 4GB DDR3 RAM
- different flavors realized with **FPGA mezzanine cards** and **firmware**

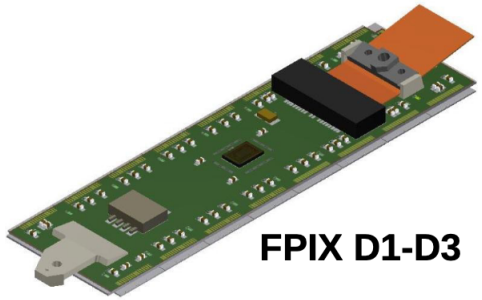
**The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade**

The cooling system has been designed to cope with a total power of 15kW (marging)

# CMS Phase-1 Pixel Detector – Modules

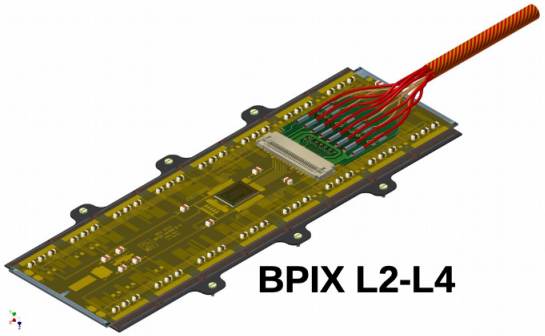



**3 flavors of modules**



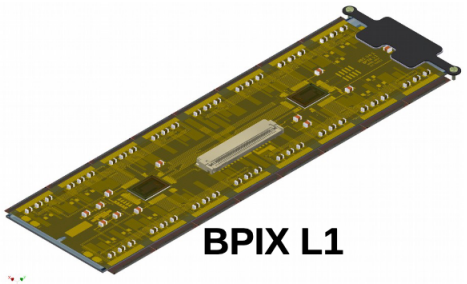
**FPIX D1-D3**

- 672 modules
- 40-100 MHz/cm²
- **PSI46dig** (column drain)
- 50 Mrad (Si)
- 672 fibers



**BPIX L2-L4**

- 1088 modules
- 40-120 MHz/cm²
- **PSI46dig** (column drain)
- 50 Mrad (Si)
- 1312 fibers



**BPIX L1**

- 96 modules
- 580 MHz/cm²
- **PROC600** (dynamic cluster colmn drain)
- 480 Mrad (Si)
- 384 fibers

- Layer 1 is designated to withstand a particle rate of 600MHz.cm-2

# Hit rate/ Fluence / Dose

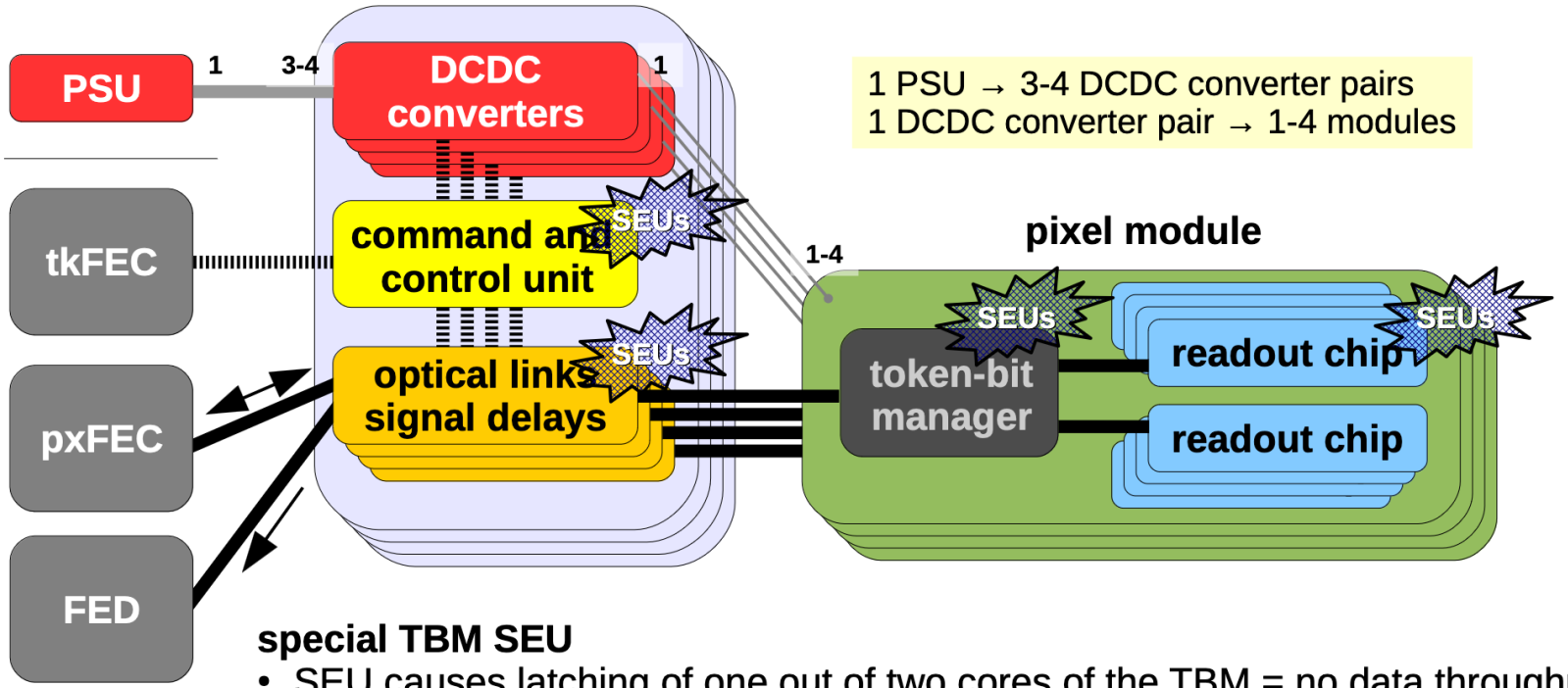
**Table 2**. Expected hit rate, fluence, and radiation dose for the BPIX layers and FPIX rings [7]. The hit rate corresponds to an instantaneous luminosity of $2.0\times10^{34}$ cm$^{-2}$ s$^{-1}$ [4]. The fluence and radiation dose are shown for integrated luminosities of 300 fb$^{-1}$ for BPIX L1 and 500 fb$^{-1}$ for the other BPIX layers and FPIX disks.

| | Pixel hit rate [MHz/cm$^2$] | Fluence [$10^{15}$ n$_{eq}$/cm$^2$] | Dose [Mrad] |
|---|---|---|---|
| BPIX L1 | 580 | 2.2 | 100 |
| BPIX L2 | 120 | 0.9 | 47 |
| BPIX L3 | 58 | 0.4 | 22 |
| BPIX L4 | 32 | 0.3 | 13 |
| FPIX inner rings | 56–260 | 0.4–2.0 | 21–106 |
| FPIX outer rings | 30–75 | 0.3–0.5 | 13–28 |

# Single Event Upsets

**status in 2017/2018**

- single event upset expected in high radiation environment
- SEUs observed in many components in 2017/2018
- normal procedure: download configuration parameters to the front-end regularly



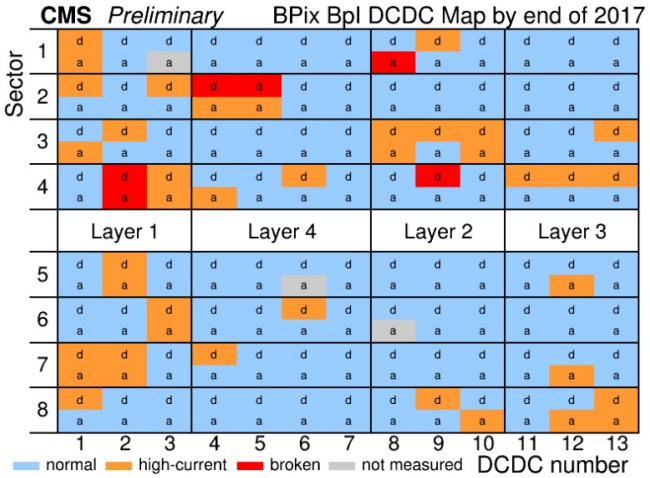

**special TBM SEU**

- SEU causes latching of one out of two cores of the TBM = no data throughput
- reprogramming the TBM does **not** resolve the problem
- only powercycle recovers the TBM core and thus the ROCs behind
- in 2017: command and control unit used to disable/enable DCDC converter

# The DCDC Story

**timeline**

- October 5th 2017: first DCDC converter stopped working
- extrapolation of failure rate to 2018: no sufficient tracking by mid 2018
- extraction of the detector and replacement of ALL converters with similar version, but bigger fuse (allowing to operate the converters at a lower input voltage = higher input current)

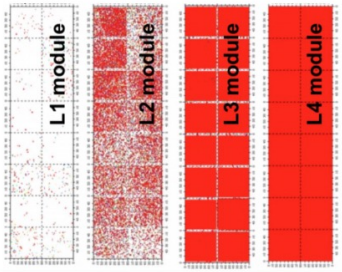



**characterization of extracted converters**

- I-V characterization of all extracted converters:
  - 65 not switching anymore
  - 333 higher currents in disabled state
  - rest (~1800) behaves normally

**damage on modules**

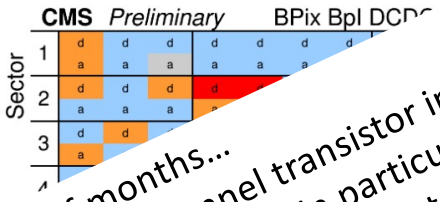
- sensor leakage currents cannot be drained efficiently if ROC is not powered
- damage on the pre-amplifier if HV on/ LV off
- damage proportional to time and sensor leakage current
- 6 (accessible) out of 8 damaged modules in L1 replaced



# The DCDC Story

**timeline**

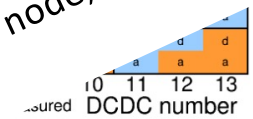
- October 5th 2017: first DCDC converter stopped wo
- extrapolation of failure rate to 2018: no suffici
- extraction of the detector and replacem
  bigger fuse (allowing to operate th
  higher input current)




After a couple of months...
One high-voltage n-channel transistor in the circuit has however not been protected for all functional sequences, in particular the leakage current can flow when the converter is disabled (which is done via a dedicated pin of the FEAST2.1 circuit). This current is amplified and integrated on a capacitor, originating a large voltage transient in a critical node of the circuit. Since this transient can approach the input voltage (up to 12V), largely exceeding the 3.3V specified for most of the devices connected to the node, this over-voltage can eventually lead to irreversible damage to the circuit.

**converters**
all extracted

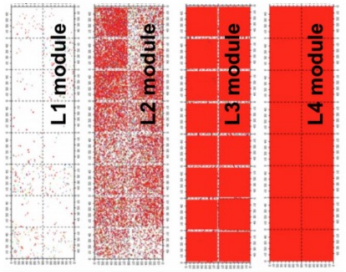
itching anymore
nigher currents in disabled state
rest (~1800) behaves normally




**odules**

leakage currents cannot be drained efficiently if ROC
not powered

- damage on the pre-amplifier if HV on/ LV off
- damage proportional to time and sensor leakage current
- 6 (accessible) out of 8 damaged modules in L1 replaced



# The DCDC Story

**after months of investigation**

- chip designers of the FEAST chip found a way to reproduce the breaking symptoms
- once a feedback loop was established, breaking mechanism could be identified quickly

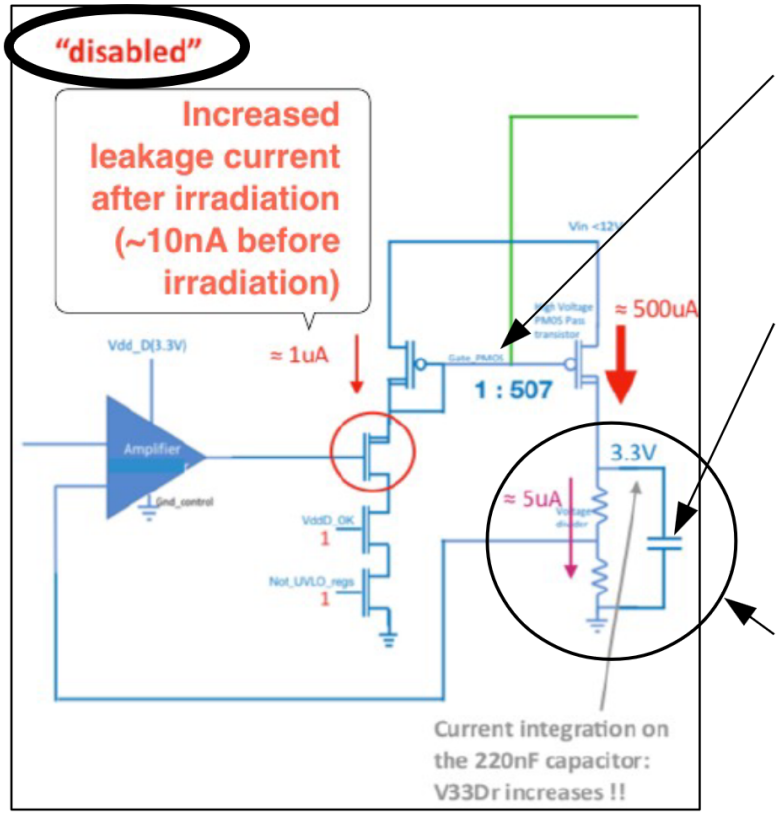



figure by Federico Faccio

amplifying current mirror

capacitor charging up in the disabled state causing voltage spikes well beyond 3.3V

part providing current to the drivers of the power transistors

**two possible results**

- high leakage current forms new ohmic path to ground (→ high current)
- converter breaks irreversibly (→ broken)

**consequences for operation**

- lower input voltage helps
- stop disabling the output
- what about latched TBM cores? → enable/disable output of the power supply (not DCDC)

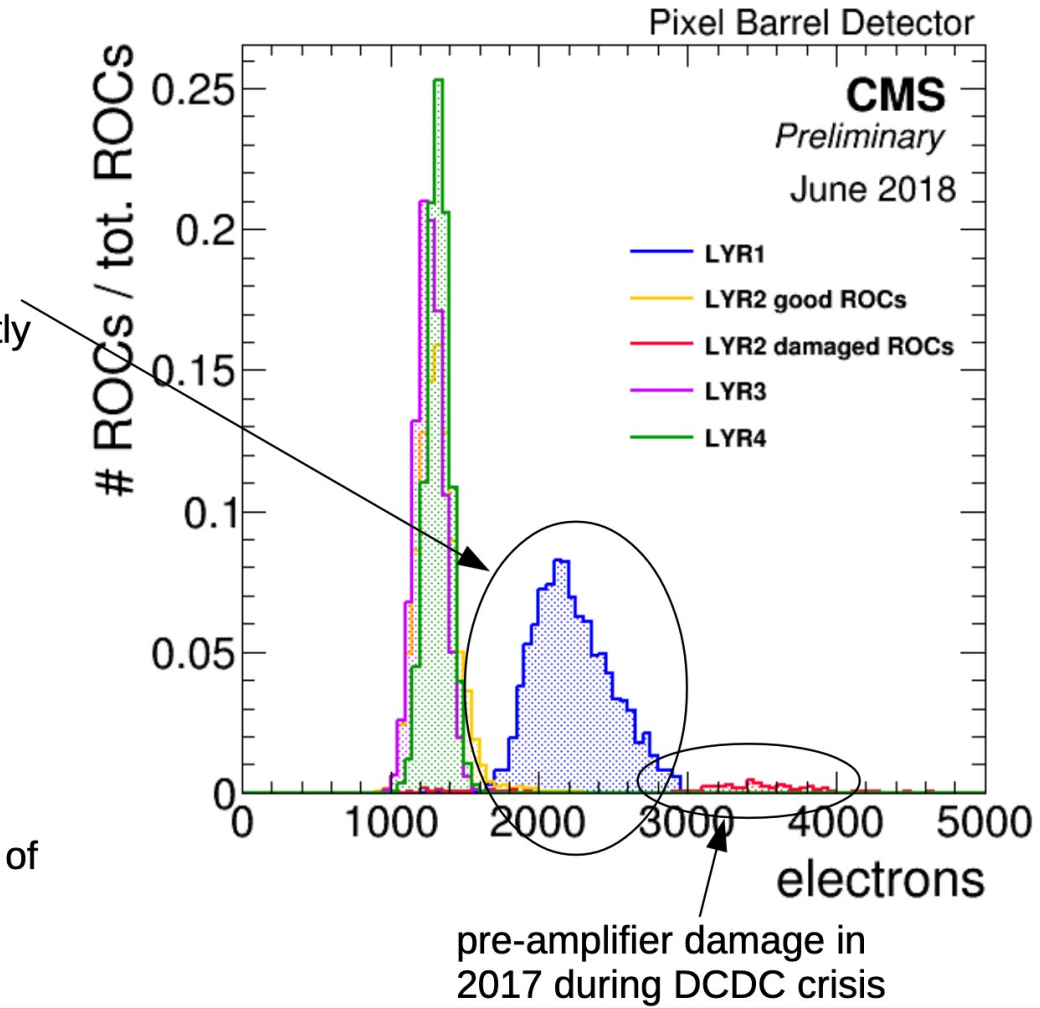
**no DCDC converter broke in 2018!**

# Layer-1 Readout Chip Crosstalk

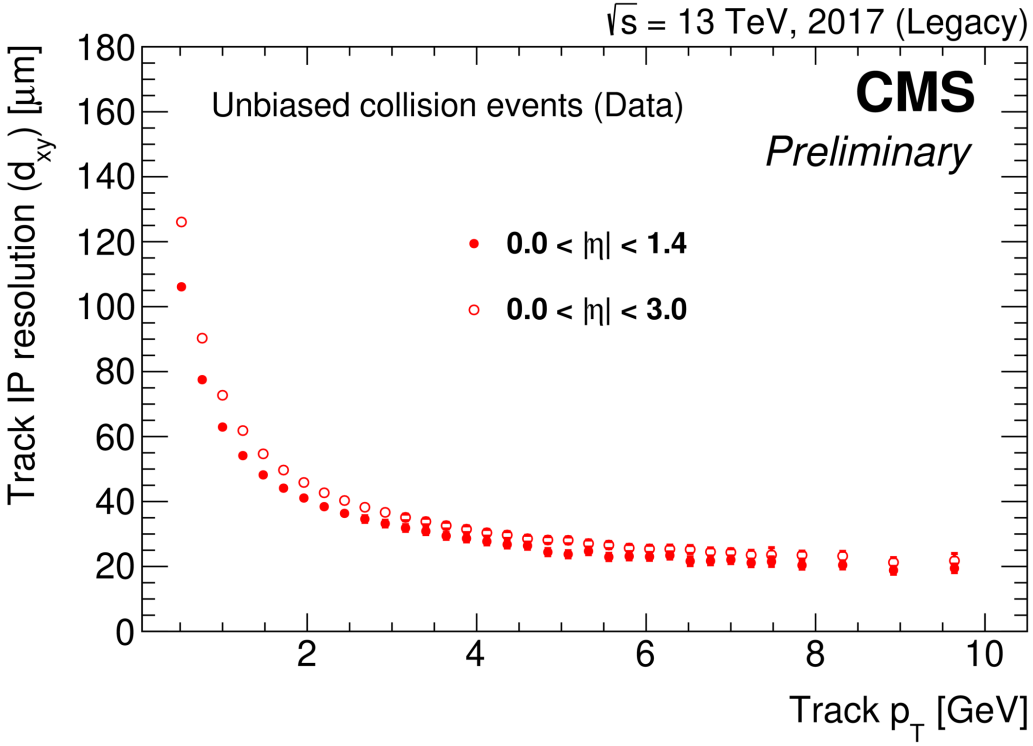
**observation**
- extra hits appear correlated with real hits
- effect is highly rate dependent

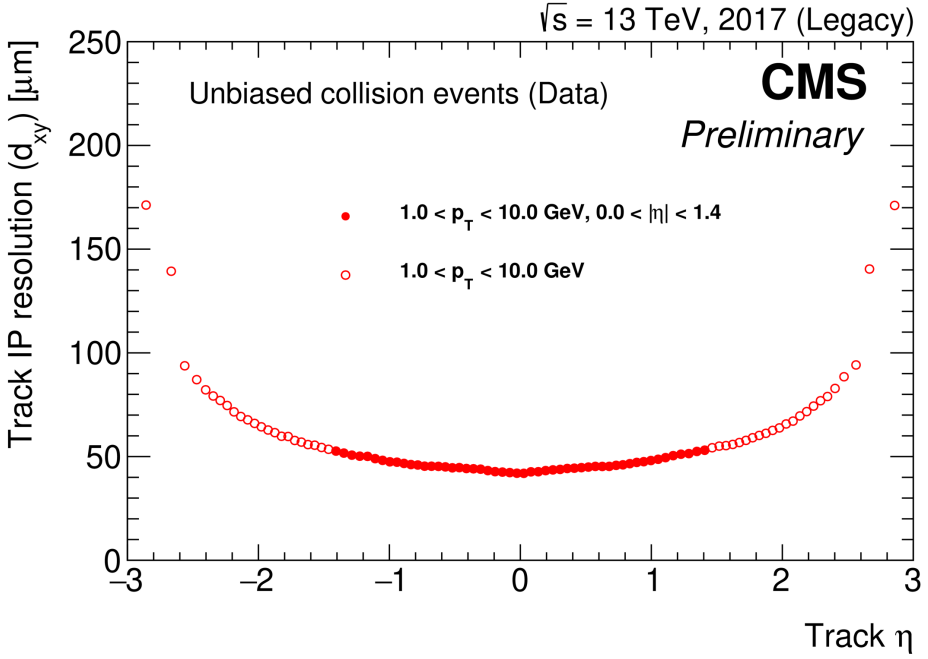
**consequences for operation**
- ➔ artificially higher thresholds in order to operate the chip efficiently with beam

**mitigation**
- two main sources of the problem identified
  - ➔ dominant contribution can be mitigated by optimized programming sequence
  - ➔ better shielding in the ROC design will further improve the situation
- will be addressed in new version of PROC600



# Tracking IP resolution

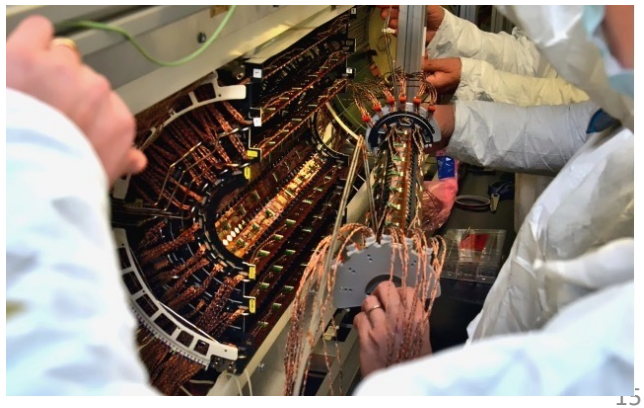


# From Run2 to Run3..

- Phase-1 pixel detector deployed in LHC Run 2 (2017 - 2018)
  - About 120 fb-1 data taken
  - Most radiation damage on layer 1 modules (closest to collisions)
  - Layer 1 HV ramped from 150 V to 450 V
- **During the LHC Long Shutdown 2 (2018-2021), the CMS Barrel Pixel detector was disassembled and its innermost layer was fully replaced.**
- New layer 1 needed for Run 3
  - More than twice as much data expected to be taken in Run 3
  - Fluence in L1 would exceed operational limits
- Design improvements in laver 1
  - New layer 1 HV can be ramped upto 800 V
  - Fixed data sync. loss issues in ROC
  - Lower thresholds through better electrical shielding in ROC
- Protection against single-event upsets in Token Bit Manager

- Refurbishments during LS2
  - BPix extracted from the CMS detector
    - Stored in a cold box
  - New layer 1 was built (started in 2020) and assembled at PSI
- Extraction of old layer 1 from Bpix
  - Replacing single layer 2 modules
  - Reassembling Bpix
  - New DCDC converters
  - Repair of faulty connections



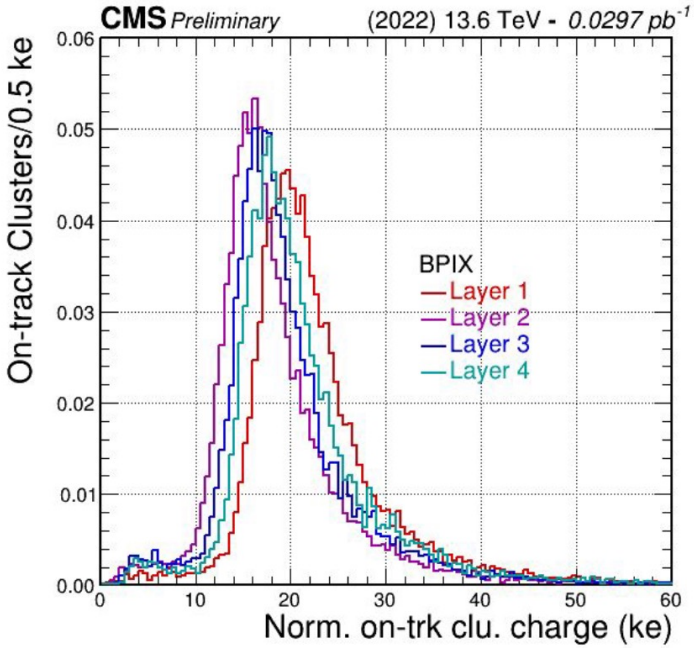
# New Pixel Layer 1: design improvements

- From “CMS Phase-1 pixel detector refurbishment during LS2 and readiness towards the LHC Run 3”
  - Lars O. S. Noehte and on behalf of the Tracker Group of the CMS collaboration 2022 JINST 17 C09017
  - https://iopscience.iop.org/article/10.1088/1748-0221/17/09/C09017/pdf

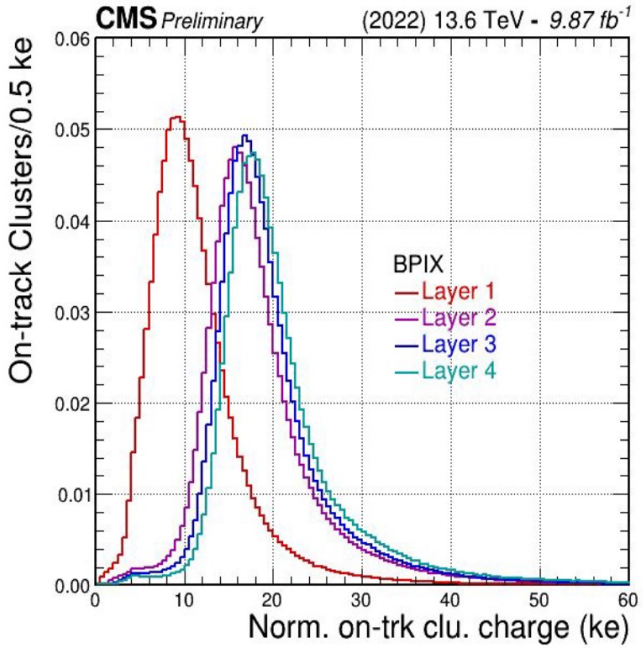
- The improved ROCs have better shielding of the calibration pulse injection circuit leading to reduced pixel cross-talk and noise.
- Moreover, they have an improved time-stamp buffer logic, which in the past caused timing errors and thus loss of data synchronization.
  - The old TBM suffered from a vulnerability for a specific single event upset (SEU) which required a power cycle of the TBM to recover.
  - The new TBM is guarded against this SEU phenomena.
- In addition, L1 is equipped with new high voltage cables with better insulation.
  - With the new cables and upgraded power supplies, the reverse bias voltage can be ramped up to over 800 V, compared to 450 V in Run 2.

# Cluster Properties Barrel Pixels

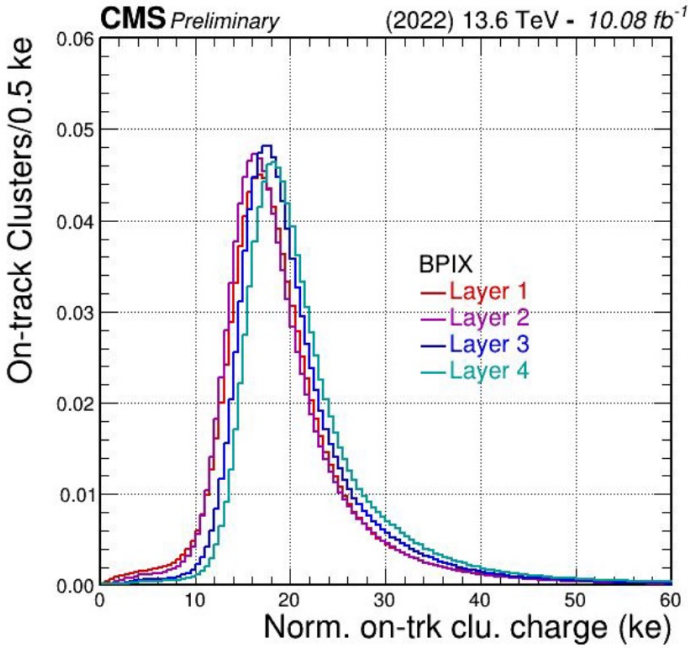
- Cluster Charge normalized by incidence angle
  - Clusters are required to be attached to tracks with $p_T$>1.0 GeV.
  - The distributions of the normalized on-track cluster charge (Norm. on-trk. clu. charge) for each barrel pixel (BPIX) layer differ because of loss of charge collection efficiency caused by radiation damage.
    - During the long LHC shutdown Layer 1 was replaced and thus started with no radiation damage (left) resulting in highest cluster charges.
    - Radiation damage introduced the charge efficiency loss for Layer 1 (middle) which is recovered by raising the bias voltage (right)
    - L1 bias voltages are set to 150V in left and middle plots and 300V in the right plot




150V

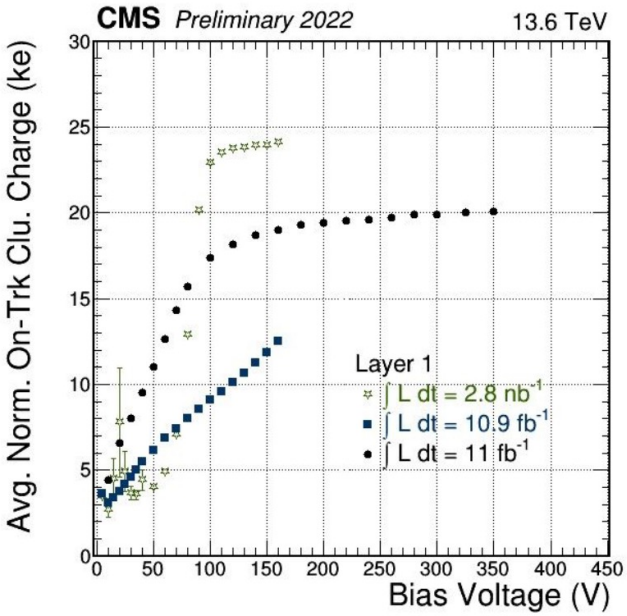


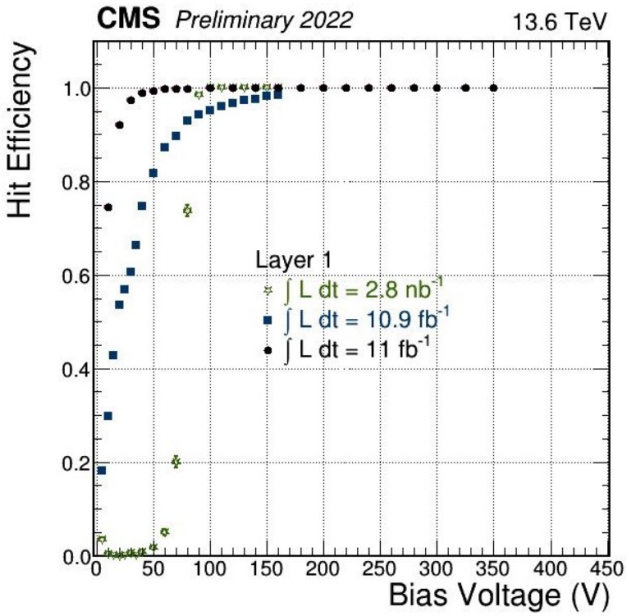

150V




300V

# HV Bias scan Layer 1

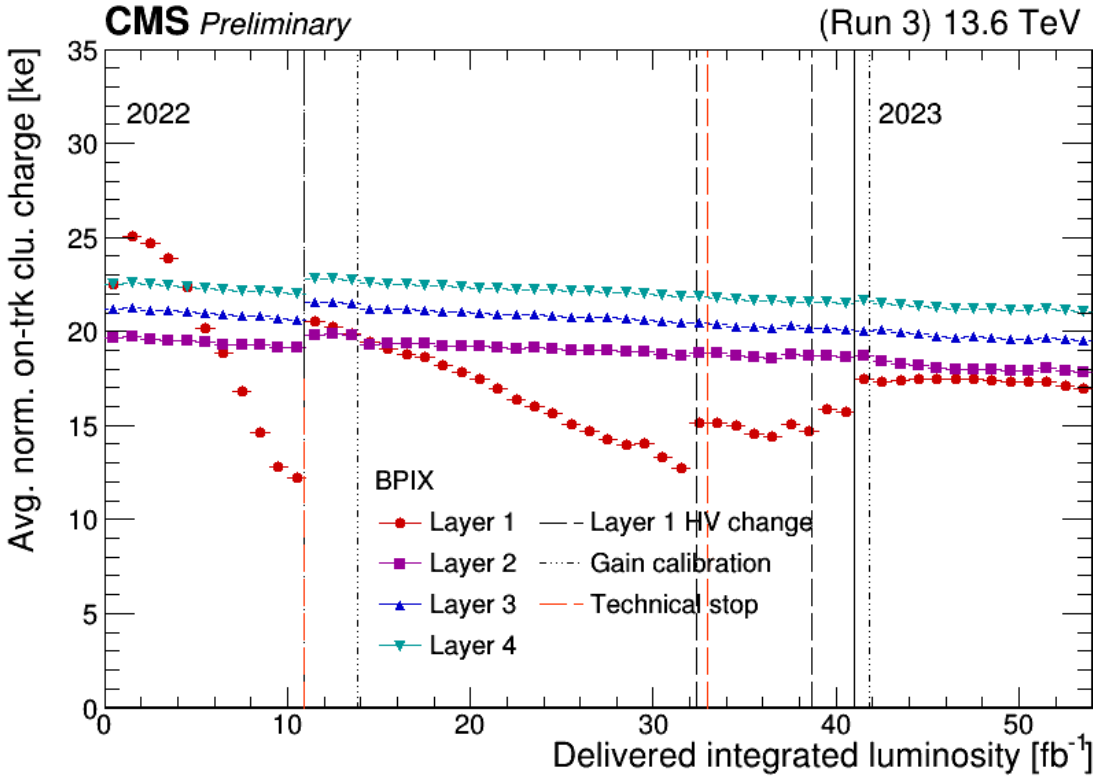


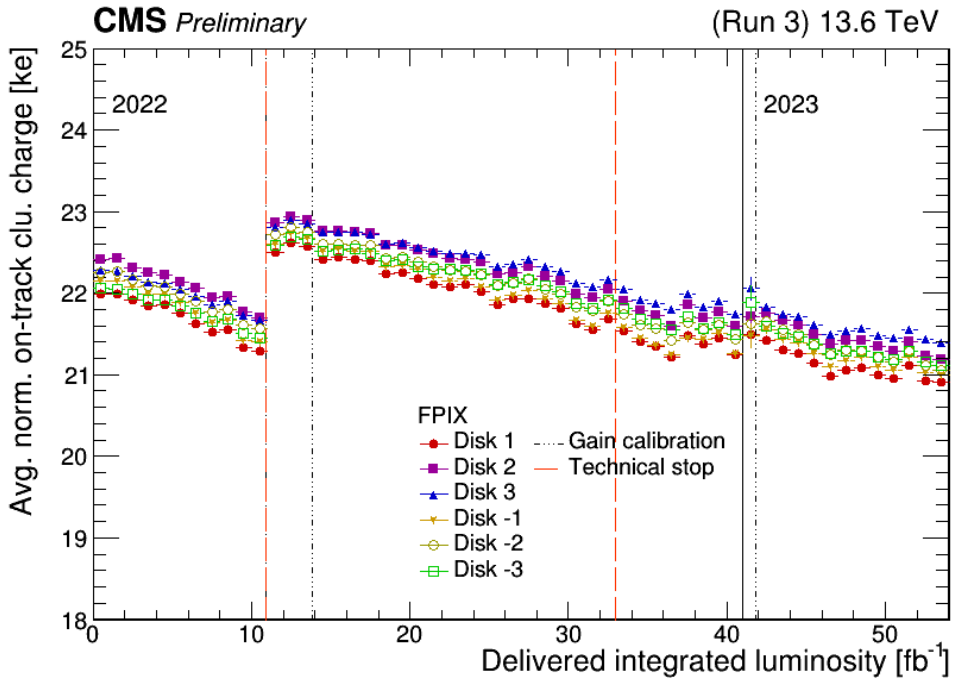




Three mini bias voltage scans performed in 2022 are shown at the integrated luminosity of 2.8 $nb^{-1}$ , 10.9 $fb^{-1}$ and 11 $fb^{-1}$

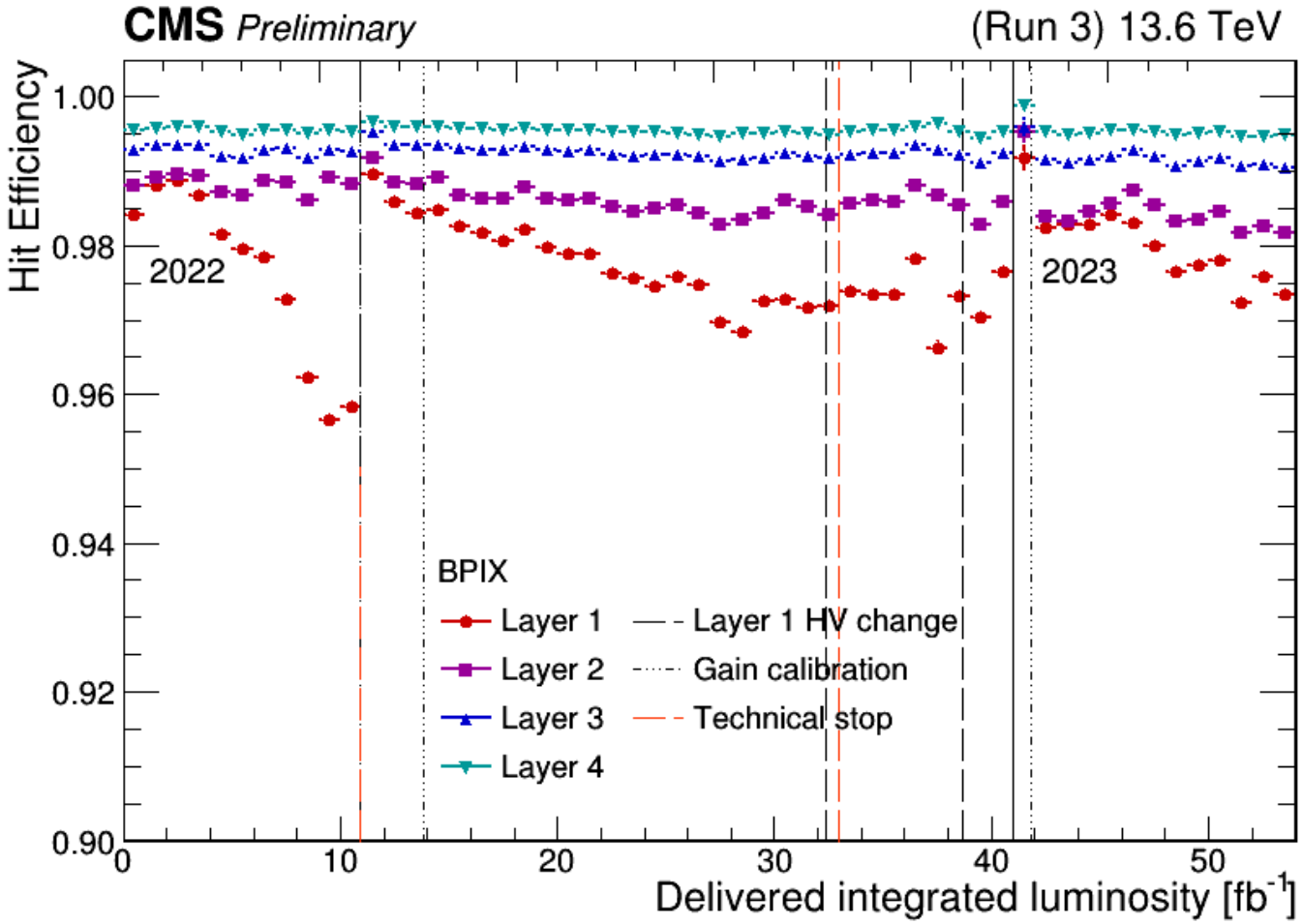
- The effect of radiation damage is visible in the shift of the plateau in different scans.
- The complex evolution of the hit efficiencies with irradiation is understood to come from multiple effects some of which are the inversion of the charge carrier type in the silicon sensor and the annealing during the periods with no data-taking.
- Between the last two scans there was a ~4 week period without data-taking; detector was annealed which had a beneficial effect for charge collection efficiency visible in the last scan.
- Operation voltage in Layer 1 at the startup was 150 V. After the second scan, it was increased to 300 V.

# Cluster charge evolution

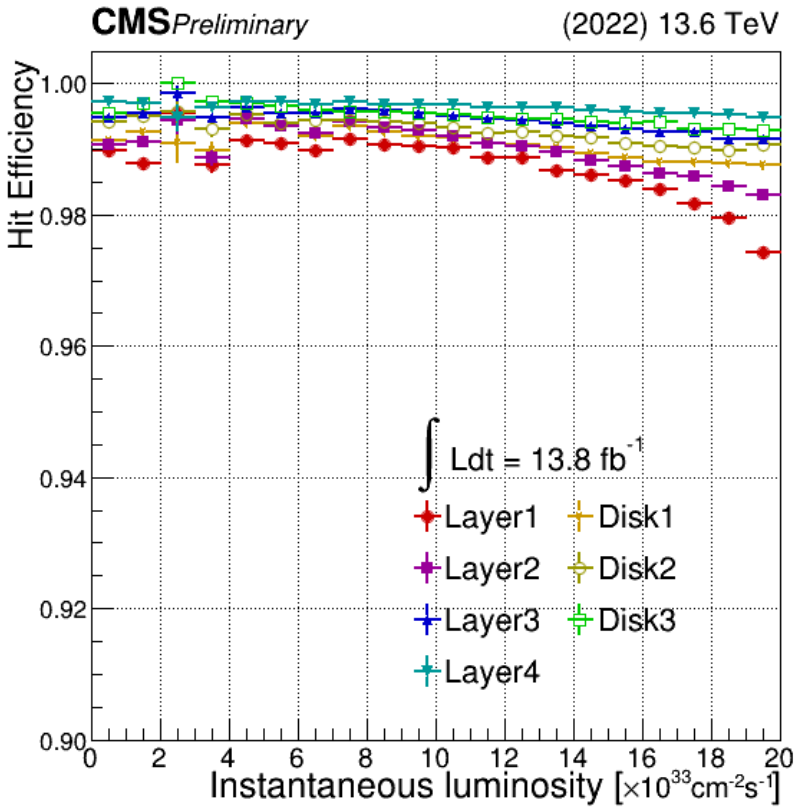


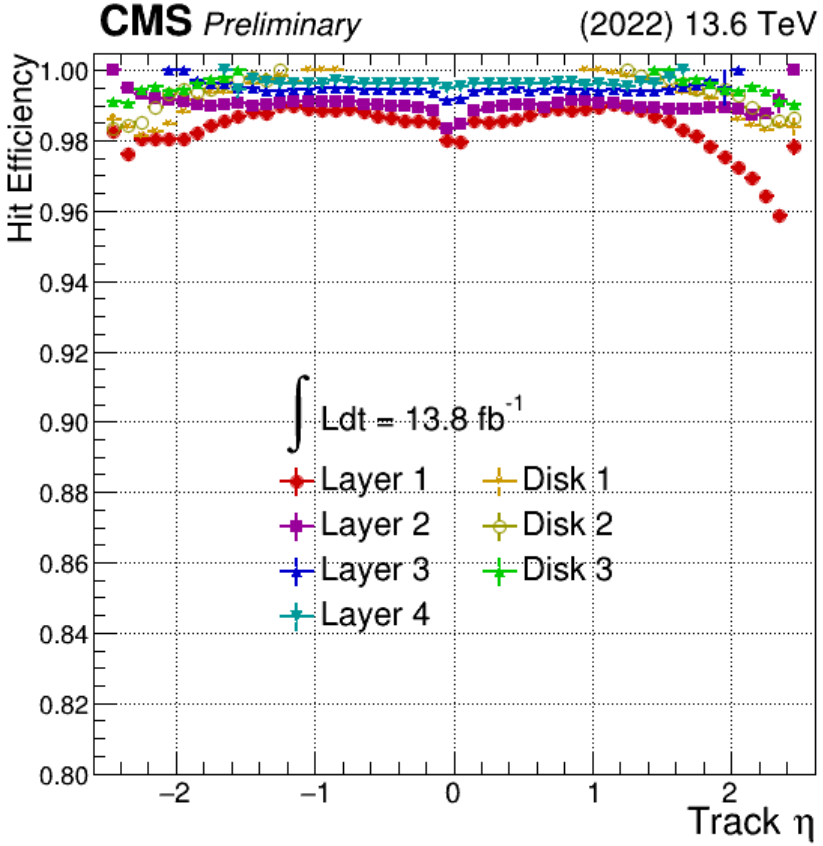



# Hit efficiency



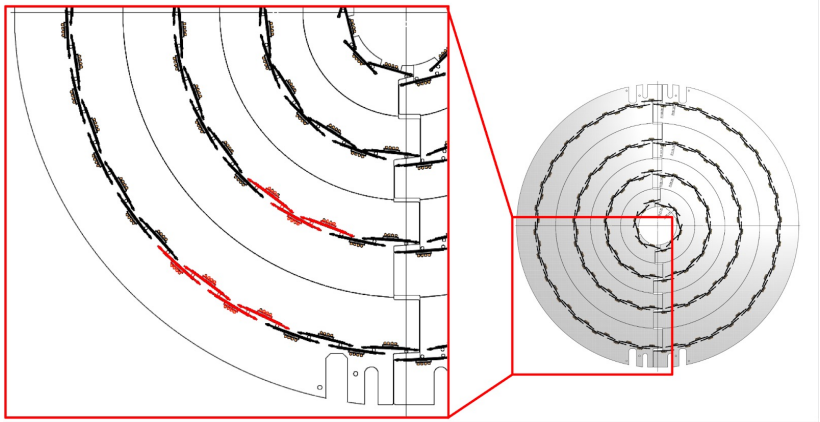
# Hit efficiency

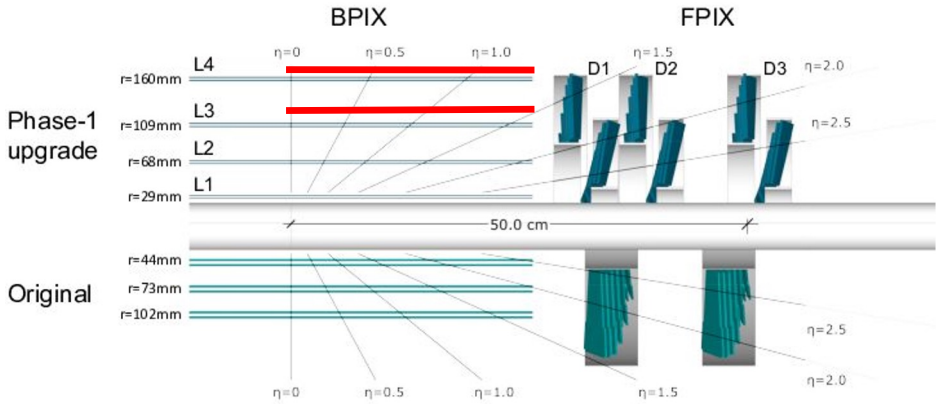


# Pixel 2023: Layer 3 and 4…

- After the Technical stop in early July 2023, we observed issues with BPIX layer 3-4
  - QPLL issue in BmI SEC7 Layers 3 and 4, since 19 June 2023
- An access & CMS opening is needed to possibly repair it
  - To be assessed, discussed… (risky operation, close to the beampipe..)





# References


- The bible :
  - **The CMS Phase-1 Pixel Detector Upgrade**
  - https://doi.org/10.48550/arXiv.2012.14304
- Lars O. S. Noehte and on behalf of the Tracker Group of the CMS collaboration 2022 JINST 17 C09017
  - https://iopscience.iop.org/article/10.1088/1748-0221/17/09/C09017/pdf
- **Operational experience of the Phase-1 CMS pixel detector**
  - **https://doi.org/10.1016/j.nima.2019.03.073**

- DCDC converter saga:
  - https://espace.cern.ch/project-DCDC-new/_layouts/15/start.aspx#/Reports
    - A short executive summary with the most relevant consequences for the users
    - A summary of all the measurements performed in the period January-September 2018 and how they led to unravel the mechanism at the origin of the problem
    - A detailed report of the two irradiation tests performed at the CERN IRRAD facility, where it was eventually possible to reproduce the same damage mechanism observed in the CMS pixel system