R&D for pixel detectors in the future hadron colliders

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GDR intensity frontier

Retour d'expérience et futurs projets

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CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
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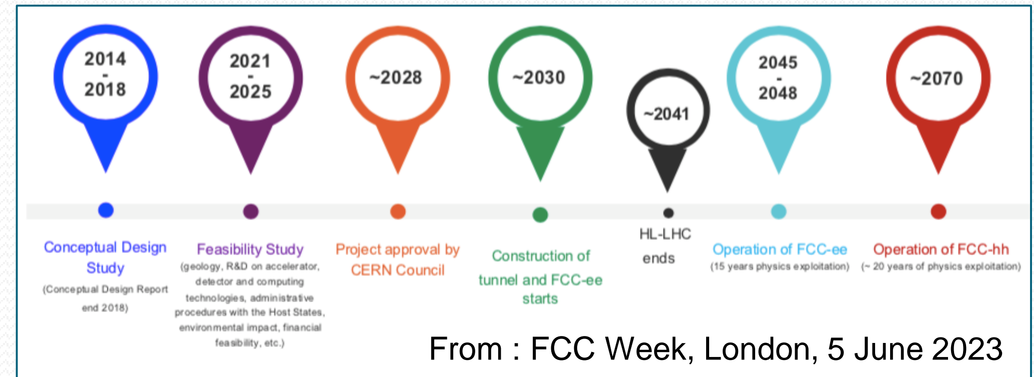
Outline

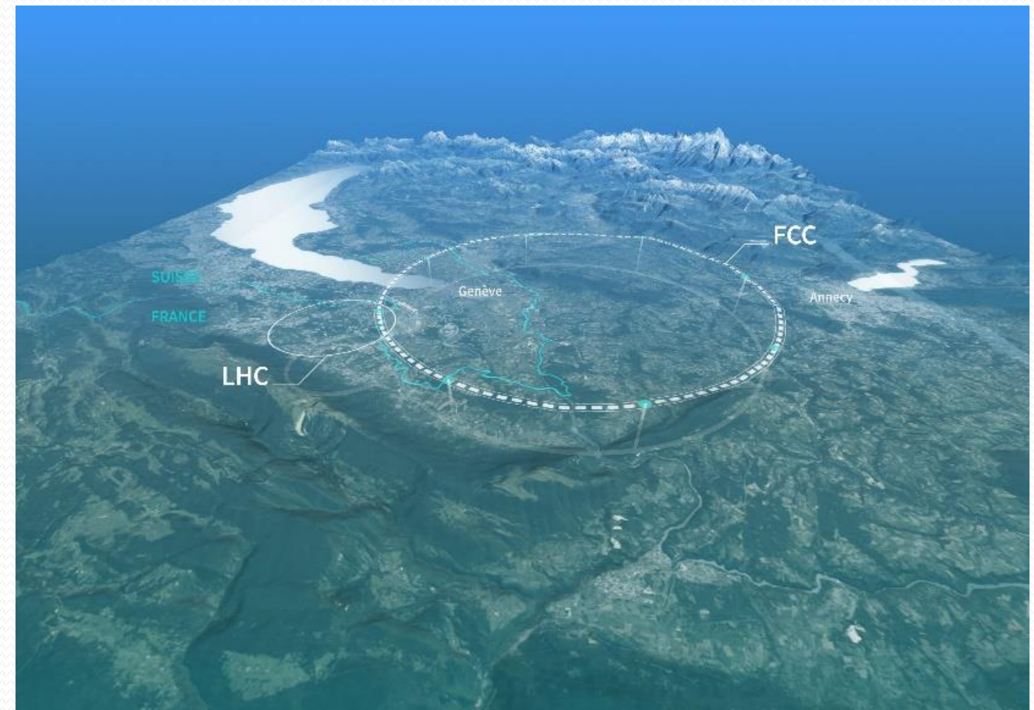
- Introduction: FCC timeline
- Requirements for future trackers
- Pixel front-end time resolution
- Technology used in current CERN experiments
- Technologies under consideration
- CPPM activities
- Conclusion

Introduction

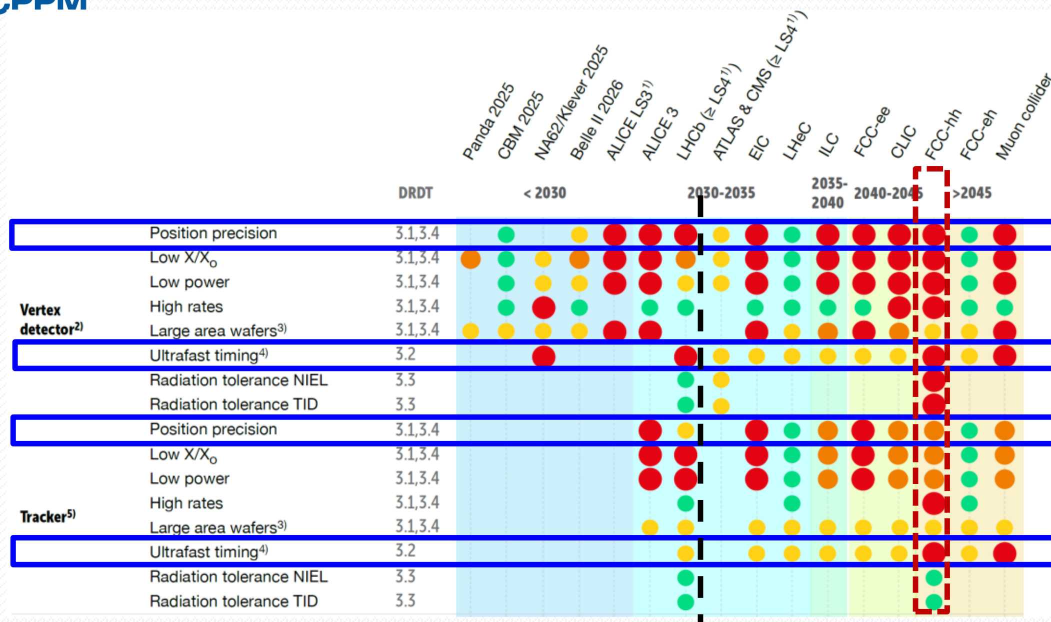
- **Realistic schedule** takes into account the past experience in building colliders at CERN
- The future collider at CERN cannot start physics operation before ~ 2045 but construction will proceed in parallel to the HL-LHC operation
- The operation of the **FCC-hh is planned for 2070**
- It is obviously not possible to define now the technology of the **pixel detectors** for the FCC-hh
  - This technology **does not yet exist**
- Which "long-term R&D" **is essential now** to enable the technical design of experiments in 30 years ?

Realistic schedule





Pixel detectors requirements in the future experiments



- **Future Circular Collider tracker (FCC-hh)**
- Efficient reconstruction of charged particle tracks in an environment of **high pileup density** (1000 pileup)
  - **Position: 7.5 - 9.5 µm, Time resolution = 5 ps**
  - **Radiation levels: 40 Grad and 1×10^{18} neq/cm2**
    - 40 times more intense than the HL-LHC.
  - **Huge data rates**
    - Hit rate of 30 GHz/cm² (HL-LHC ×10)
    - Need of 50-100 Gbps data links (low power, low material)
  - **A big challenge in sensor and ASIC design**

Intermediate steps :

- **The ATLAS and CMS tracker upgrades**
  - The two innermost pixel layers will need to be replaced after 5 years
  - The pixel **time resolution of 50 ps** is needed to boost the ATLAS performance
- **Electron Ion Collider (EIC)**
  - New accelerator to be built at Brookhaven National Laboratory will **start operating In 2031**
  - 4D detectors based on AC-LGADs are envisioned to provide timing capability
  - **Time resolution of 30 ps** is required
  - **Spatial resolutions of 15 µm** to 150 µm depending on the location.
- **Electron colliders**
  - Linear colliders (ILC, CLIC) and Circular colliders (FCC-ee)
  - **High precision** is required for physics measurements
  - **Pixel size** in the vertex detector < 25 µm x 25 µm
  - **Time resolution at the ns level** is required
  - Potential applications of **precision timing at the ps** level under investigation

Time resolution of the pixel FE

σ_{jitter}

- Due to the noise of the electronic front-end including the sensor
  - The jitter is proportional to the rise time (~1/BW) and inversely proportional to the S/N ratio.

$\sigma_{timewalk}$

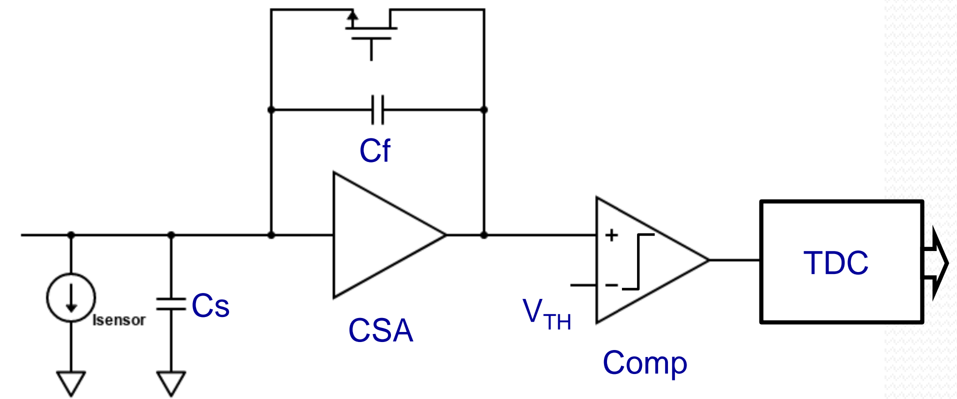
- Related to the variation of the deposited charge event-by-event
  - Variation of the time of arrival (TOA)
  - Correct the time of arrival (TOA) with a calibration based on the time over the threshold (TOT)

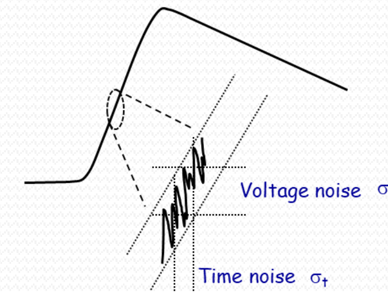
σ_{Landau}

- Due to the Landau distribution of the deposited charge
  - The **spatial variation along the path** and charges from different depths are collected at different times.
  - The effect is **small** for **thinner sensor, Absent** in **3D detectors** but **not negligible** in **LGAD** sensors

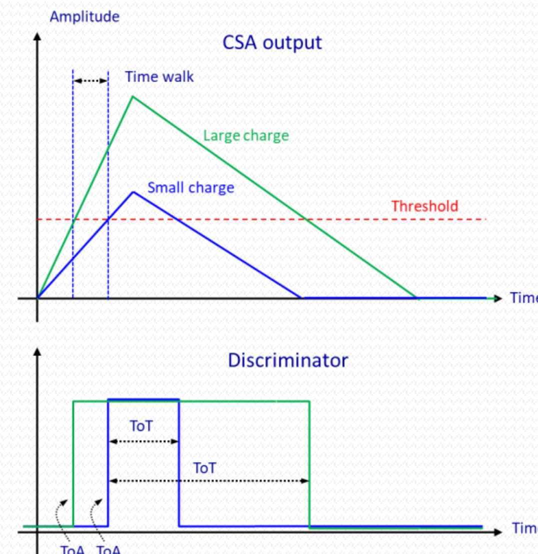
σ_{TDC}

- Due to the Time to Digital Converter (TDC) binning

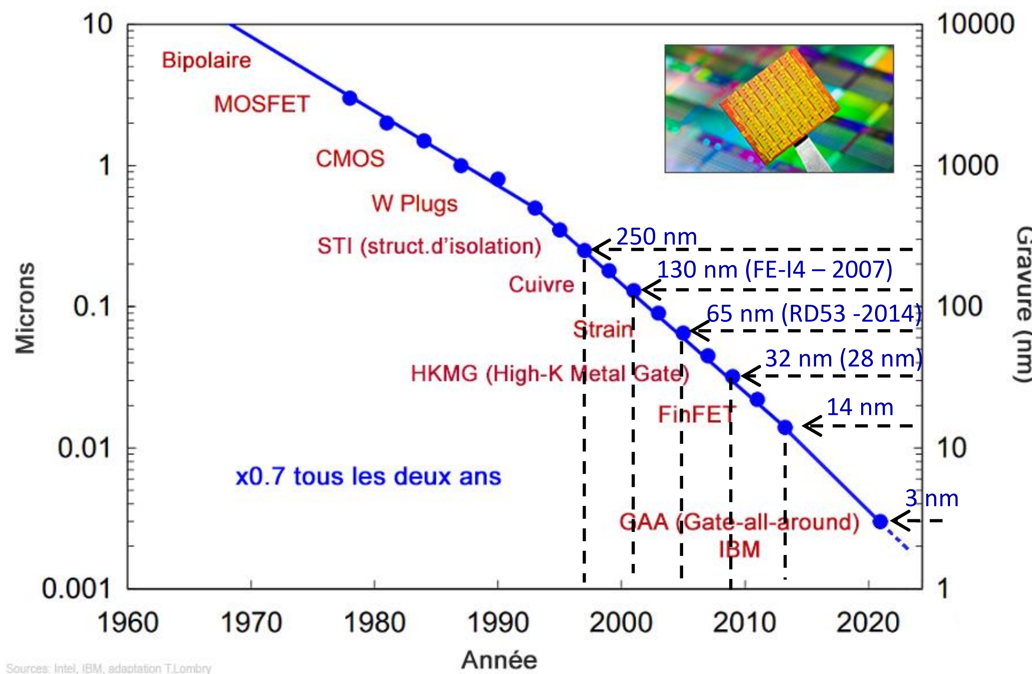




$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$



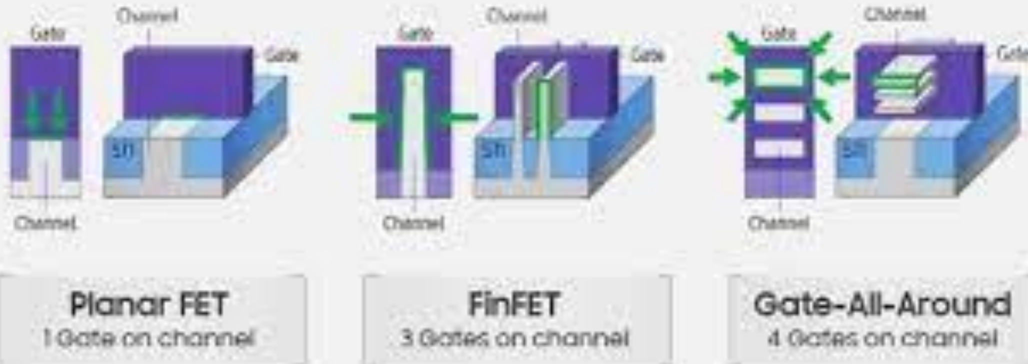
Technology used in current CERN experiments

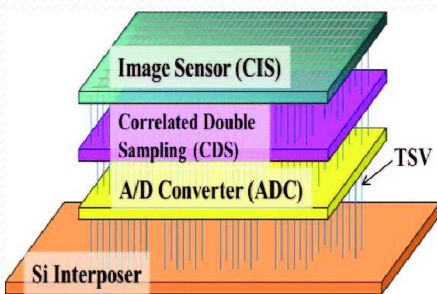


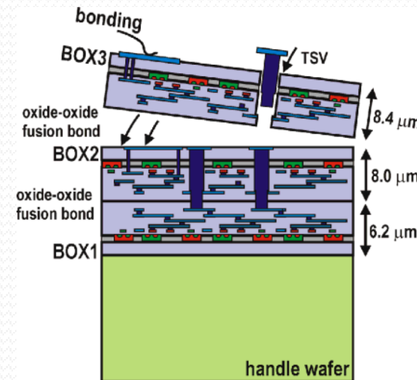
- The CERN community is lagging behind in the use of the new processes
  - Accessibility and cost
- ➢ Risk of technology aging and foundry can abandon the node

- Most of the designs for CERN experiments are based on 65 nm and 130nm CMOS
  - Technologies are already fifteen-twenty years old
- The 28nm CMOS process is considered as the next node for highly integrated chips such as pixel readout chips
- The requirements of electron and heavy-ion colliders seem to be mostly within reach of **technologies from HL-LHC**
- Within the **next 20 years**, it is certainly possible that we will have access to the most advanced CMOS nodes available today

Technologies under consideration







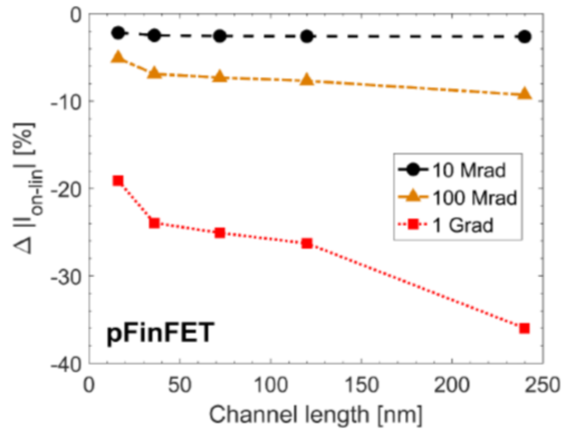
- For ASICs, the microelectronics industry has reached nanoscale CMOS nodes (< 3nm), based on new transistor structures (FinFETs and GAA)
- High-performance CMOS image sensors are based on stacked active layers to reduce pixel pitch and increase functionality
- 3D integration of a readout chip with a silicon photonics device may open way to high-rate data transmission (≥ 100 Gb/s)
- Beyond CMOS :
  - Carbon nanotubes and graphene have generated much interest: not yet clear if they will be a replacement for Si CMOS
- CMOS nodes **below 28nm need to be qualified**
  - Potential use in future applications requiring extreme miniaturization, High speed, and low power

Tolerance to high TID of nanoscale CMOS

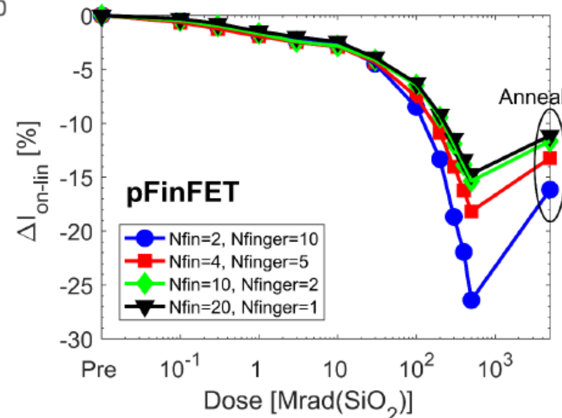
- 16 nm Si FinFETs have the best TID tolerance
- 16 nm pFinFET : Short channel devices shows better TID tolerance
- In general, pMOS have the worst TID tolerance
- No existence of bad annealing for modes ≤ 28 nm

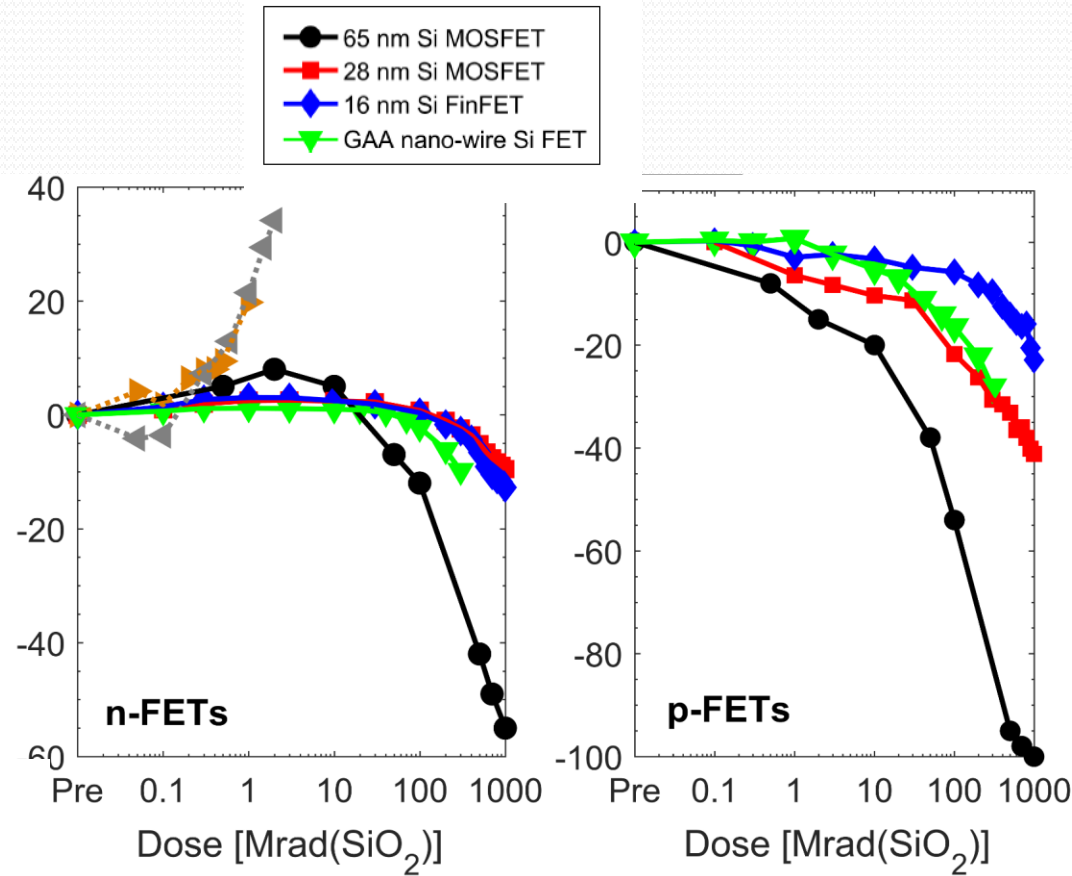
Stefano Bonaldo presentation: CERN DRDT7.4 - 2023, March 15th

Channel length effect



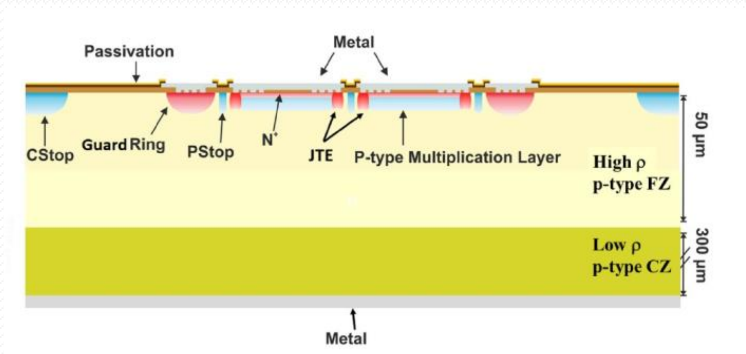
Annealing effect



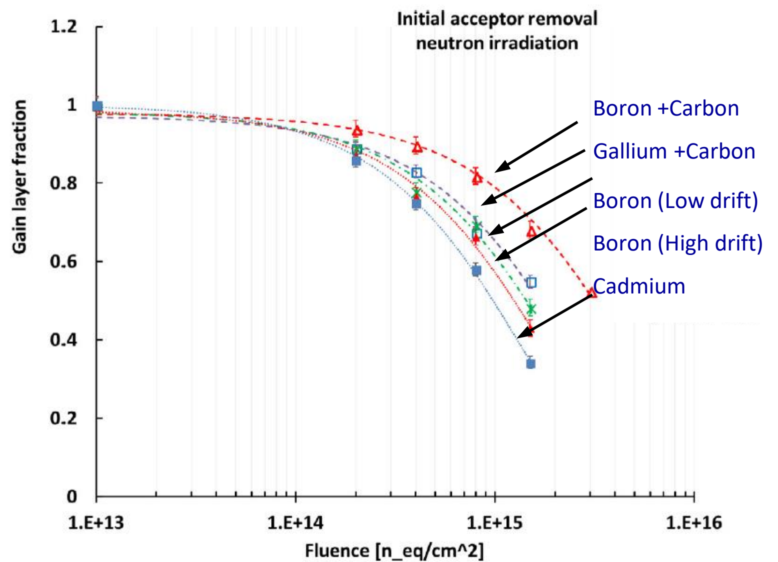


Timing sensors for high radiation levels

LGAD sensors



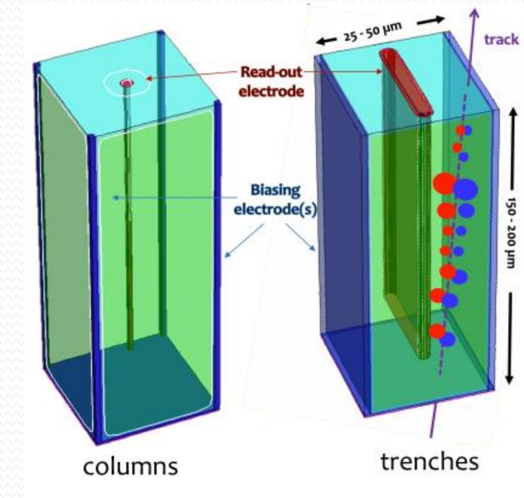
- LGAD sensors under irradiation → Modification of the gain implant profile
- Not adapted for fluence > 2-3 × 10^{15} neq/cm²



Fraction of gain still active versus neutron irradiation

M. Ferrero et. Al : Nuclear Inst. and Methods in Physics Research, A 919 (2019) 16–26

3D sensors



Doug Berry:FERMILAB-CONF-22-284-PPD1

- Developed and tested within the TimeSPOT project
- Pixels of 55 µm pitch
- No performance loss up to fluences of 2.5 × 10^{16} neq/cm²

CPPM activities

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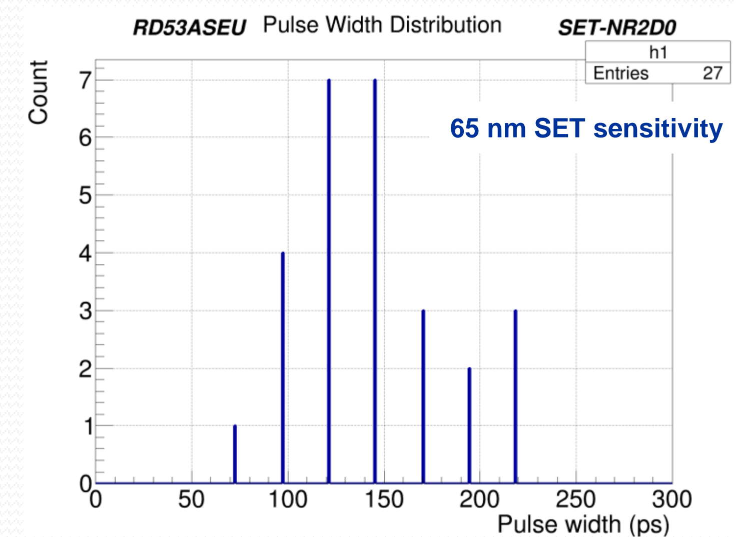
R&D CPPM projects

- Transverse project : DÉPHY : DÉveloppements Pixels HYbrides et monolithiques radio-tolérants» → Master Project IN2P3 that replaced the DICE project
- AIDAinnova Project (28nm + HVCMOS) accepted, started 2021
- CERN-DRD projects :
  - 4D and 5D techniques (WG 7.3) → High-precision timing
  - Extreme environments (WG 7.4) →Radiation hardness of advanced CMOS nodes
- RD53 collaboration started to be interested in 28 nm for the design of the pixel RO chip to be used for the replacement of the 2 internal ITK layers

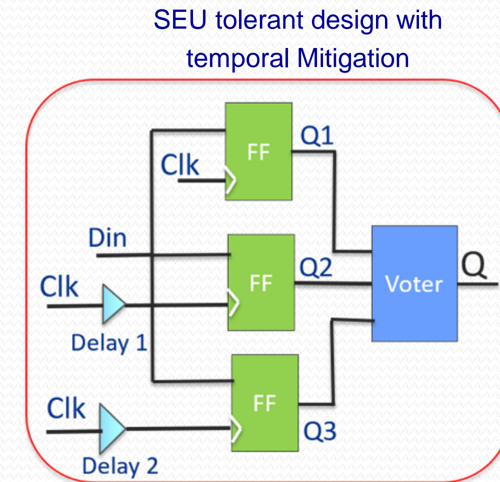
- **R&D axis around hybrid pixels** (25µm× 25µm) with the **28nm node** and Focuses on :
  - The **radiation tolerance** of the technology
  - **Time measurement** with a resolution better than **50ps**
- **Mini@sic of 2 mm x 1 mm** submitted December 24-2022
- Different structures implemented :
  - SET Testing structures
  - Ring oscillators for the TID tolerance test
  - Small pixel matrix: Fast charge amplifier
  - Devices for TID tolerance test

SEE/SET Testing

- The SEE mitigation is a major challenge for the next generation of pixel chips because of the luminosity increase
- SET propagation through combinatorial logic and generate SEU in memories, FIFO and state machines
- SET sensitivity increases with process advance and with speed
- SET test structures implemented in the prototype chip will allow characterizing the 28nm CMOS process for SET tolerance
- **Objectives :**
  - Measure the **SET cross-section**
  - Measure the SET pulse width with a **good resolution < 20 ps**
  - Measure the effect of **the std cell size**
- Allows for example to define the delay to be imposed for the triplication with time mitigation



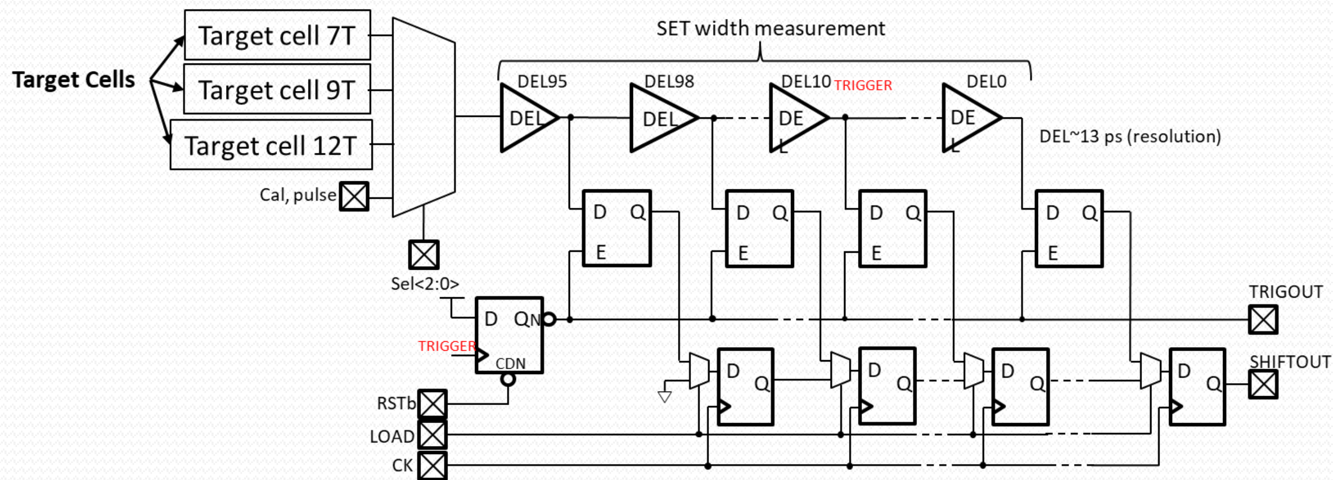
SEU tolerant design with temporal Mitigation

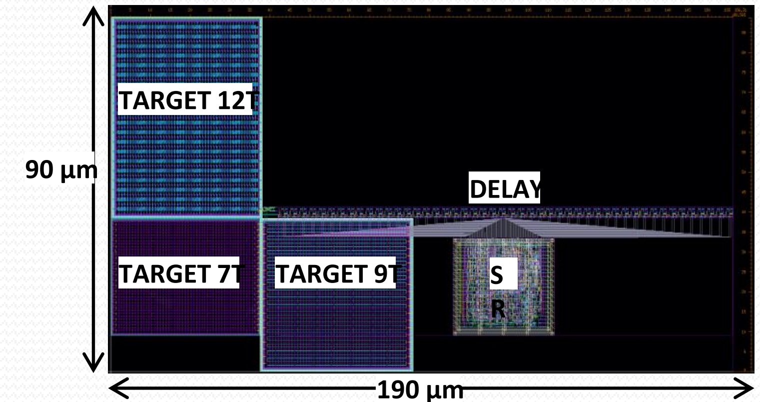


SET Bloc design

Designer : Denis Fougeron

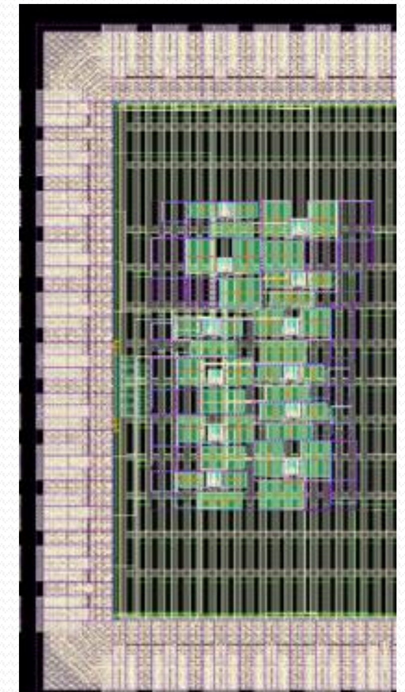
SET sub-bloc synoptic





Layout example for INVD4 cell

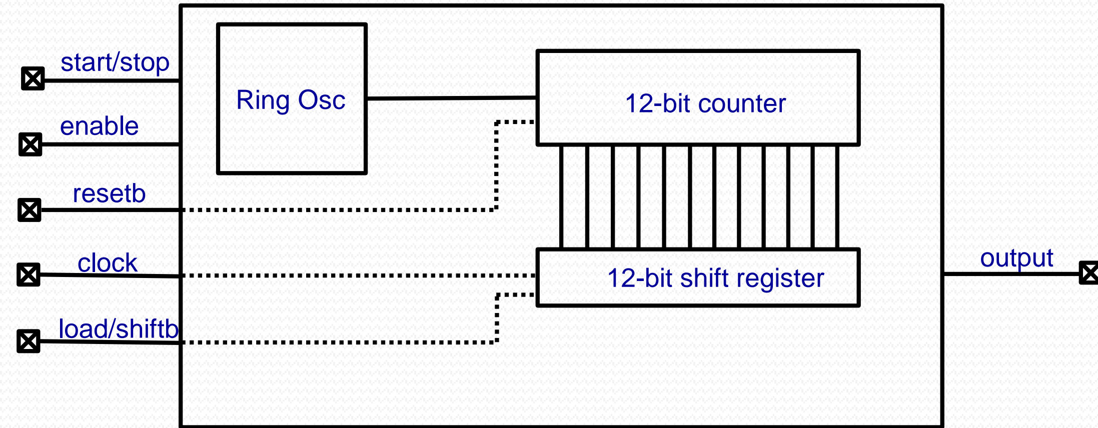
- Each sub-bloc contains
  - 3 target cells made up of thousands of basic cells + 1 calibration input
  - Circuit for SET width measurement 96 delay cells (13ps/cell) -> from a few ps to 1 ns
  - Shift register to send the data to the output when a trigger signal occurs
- 31 SET sub blocs
  - 24 uses SVT target cells (7T, 9T, 12T) -> **Effect of the cell size**
  - 7 uses LVT or HVT target cells -> Effect of **the device options**
- The whole bloc contains 6 inputs / 13 outputs
- In addition to SET testing, this constitutes a **sub-block of the TDC required in the pixel front end**



Ring Oscillator Design

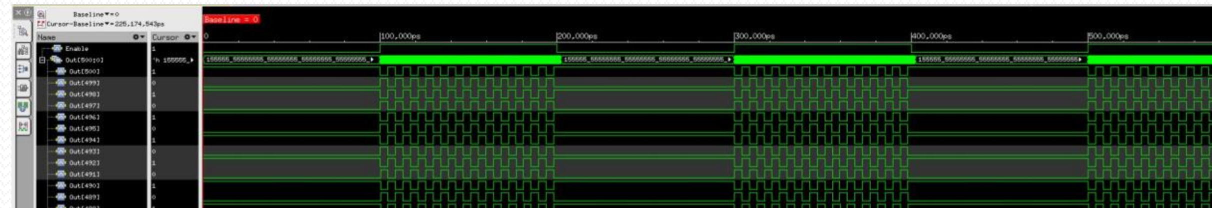
Designer : Eva Joly

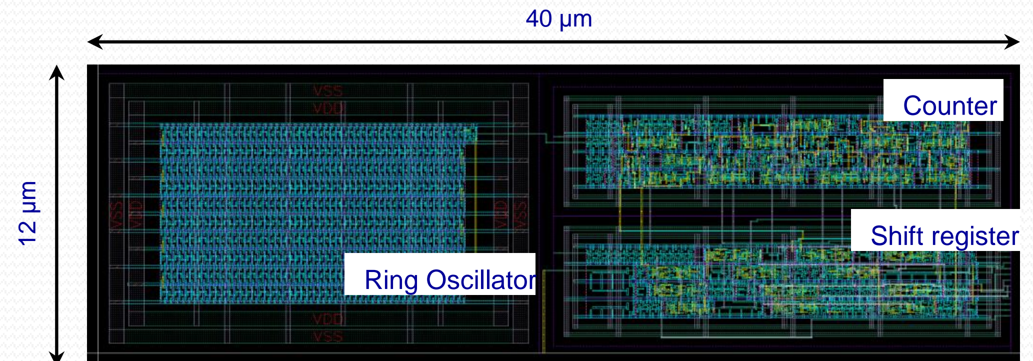
- Study the **effect of TID** on the performances of **digital standard cells**
  - **Timing** of combinatorial cells
  - **Leakage** currents and static power
- 96 ROsc sub-bloc
  - Cell size (7T, 9T,12T) -> **cell size** effects
  - Driving (D0, D2, D4) -> **cell driving** effects
  - SVT, LVT, HVT -> **device threshold** effects
- Design based on the **digital flow**



ROsc sub-bloc synoptic

Basic cells	Frequency (MHz)
INVD0	154
INVD2	222
NAND0	118
NAND2	143
NOR0	111
NOR2	139





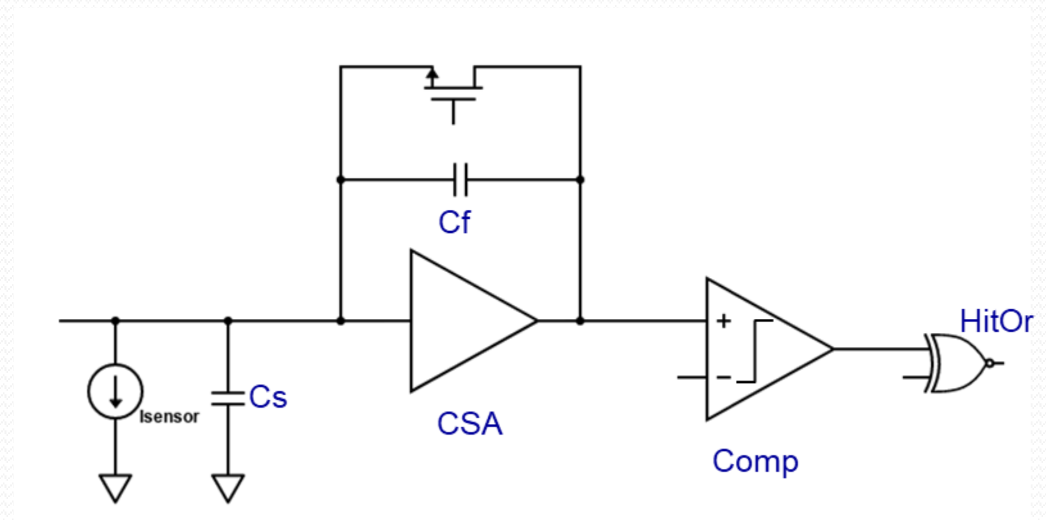
Simulation

Manual layout

Synthesis

Fast amplifier design

- Study the limits to **time resolution** in the analog front- end designed with the **28 nm CMOS** process
- Effects of the Current bias, power supply, Bandwidth, Noise …
- Design and test a **pixel array of 36 × 12 cells** where only the analog part is considered and implemented



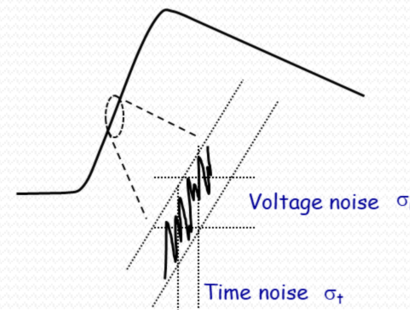
Analog FE pixel design

- The time resolution of a detector:

$$\sigma^2_{total} = \sigma^2_{jitter} + \sigma^2_{timewalk} + \sigma^2_{Landau} + \sigma^2_{TDC}$$

Minimizing the front-end jitter corresponds to :

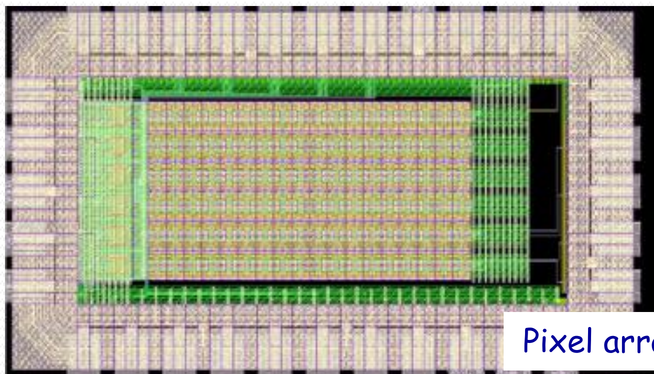
- Low RMS noise of the charge amplifier (CSA)
- High output voltage
- Small rise time → High bandwidth



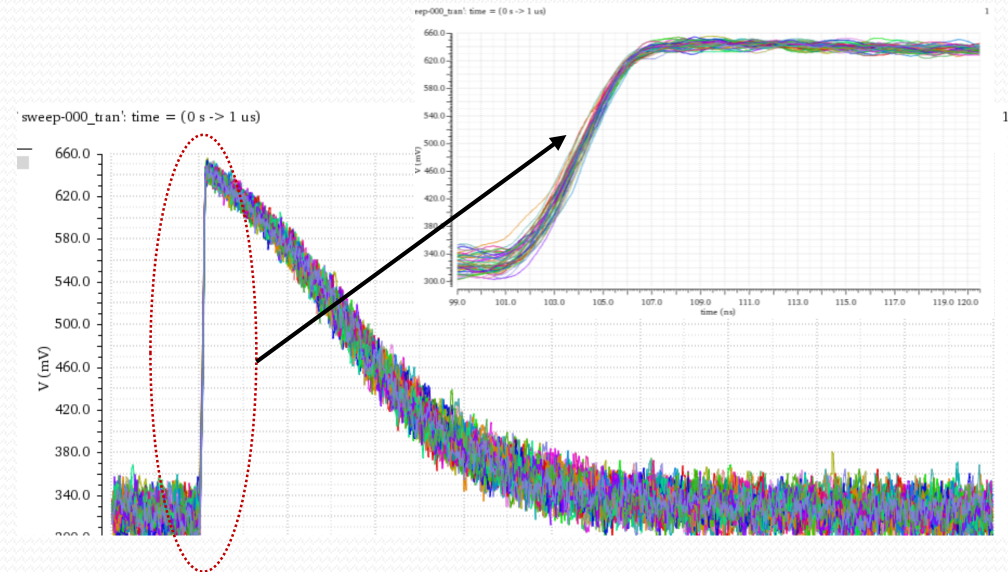
$$\sigma_{jitter} = \frac{\sigma_{noise}}{dV/dt} = \frac{t_r}{\left(\frac{S}{N}\right)}$$

Analog FE pixel prototype

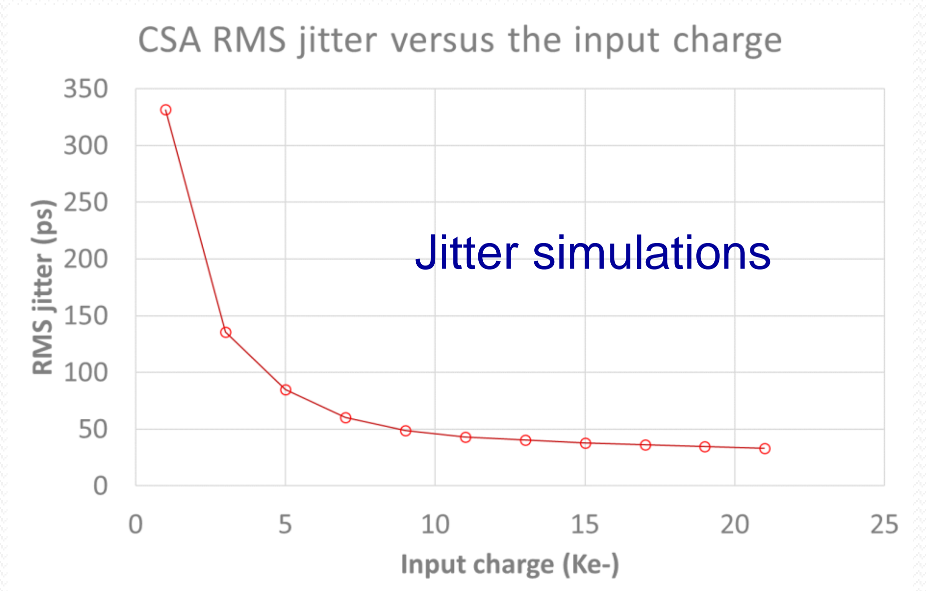
- For each pixel :
  - The charge amplifier current bias can be set in the range of 2µA-20µA
  - MOM capacitance connected to each preamplifier input -> test for different input capacitance values
- Large bandwidth buffers (> 1GHz) implemented and connected for a few pixels for direct jitter measurement
- Simulations for I_{CSA} = 5 µA
  - dV/dt = 100 mV/ns
  - RMS noise = 97 e- RMS for Cin = 100fF
  - Jitter < 100 ps RMS for input charge > 4 ke-
  - Jitter < 40 ps RMS for charge > 10 ke-
- Each pixel contains : CSA + Discriminator + 6 bit DAC
  - Size : 20 µm × 12 µm



Pixel array of 36 × 12 pixels

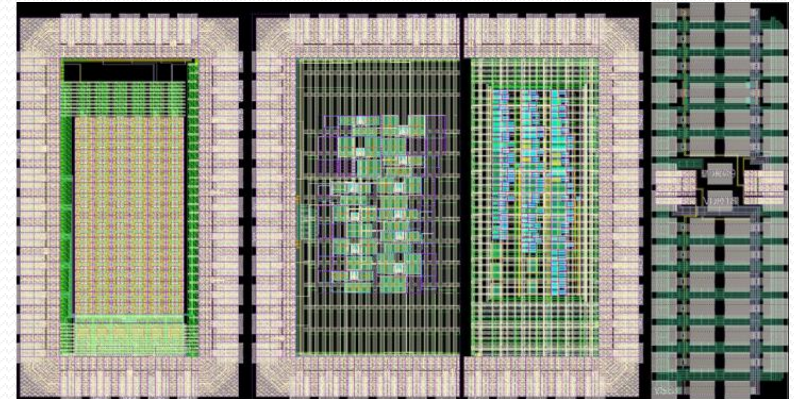


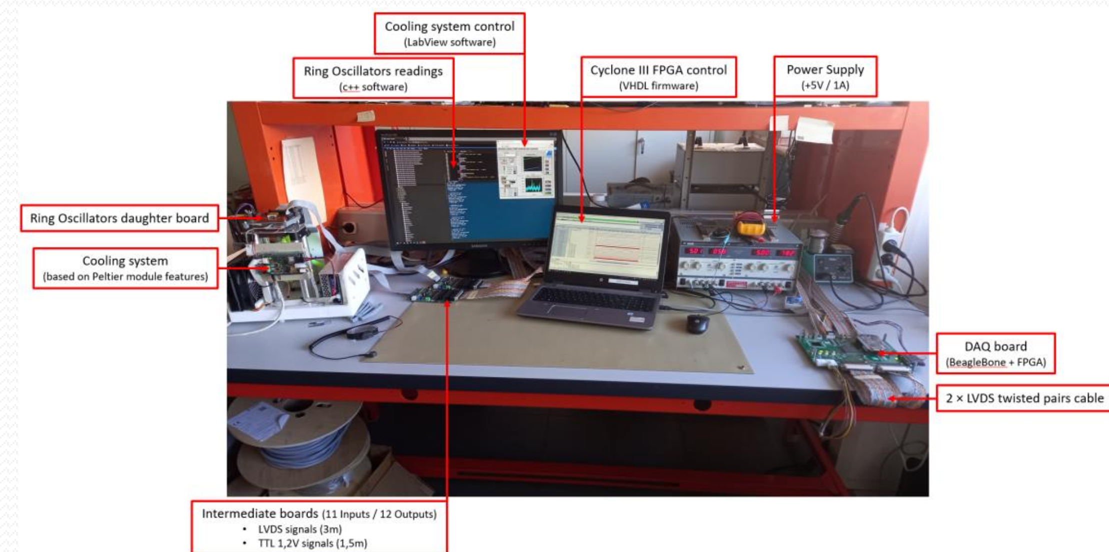
50 superimposed transient noise simulations



Design progress

- The chip prototype submitted in December 2022
- Test set-up is under preparation
  - Adaptation of the set-up based on the BB board
  - Design and fabrication of chip test boards
- Functional tests (Q4-2023)
- Irradiation test (TID + SEE) Q1-2024
- The signing of 3-way 28nm NDA was finally done
  - The CERN PDK will be used for future designs
- A new submission planned for Q3-2024
  - Dedicated to pixel array performance improvement
  - Plan to bump the readout chip with the sensor





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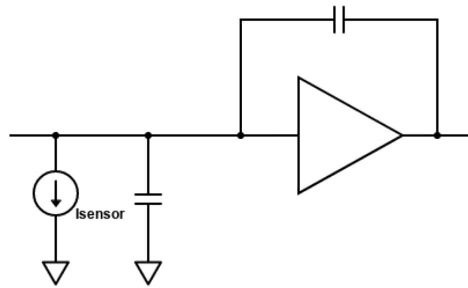
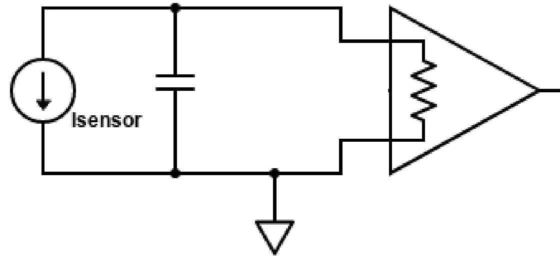
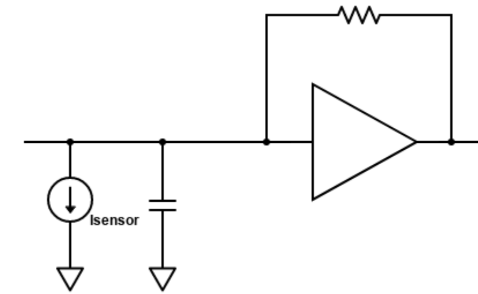
Front-end electronics and ASIC R&D





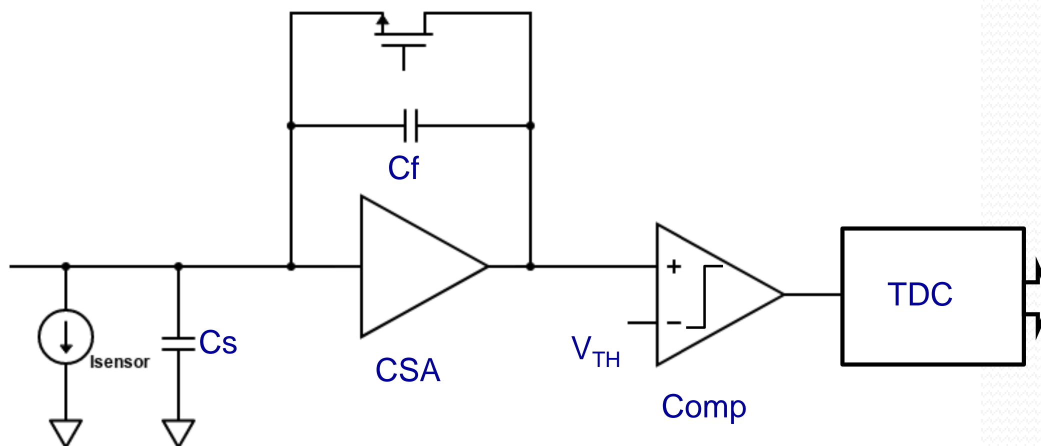


Charge amplifier (CSA)
Vout = CF×Qsensor
Slow slew rate
Less noise

Current amplifier
Iout = A×Isensor
Fast
slew rate
High noise

Transimpedance amplifier
Low Rin
Vout = RF×Isensor
High bandwidth
High noise

- The choice of the fast amplifier depends on the timing specifications and the sensor bandwidth



- Front end based on charge amplifier (CSA)
- High-resolution TDC
  - 1 TDC can be shared by several FEs
- TOA and TOT measurements

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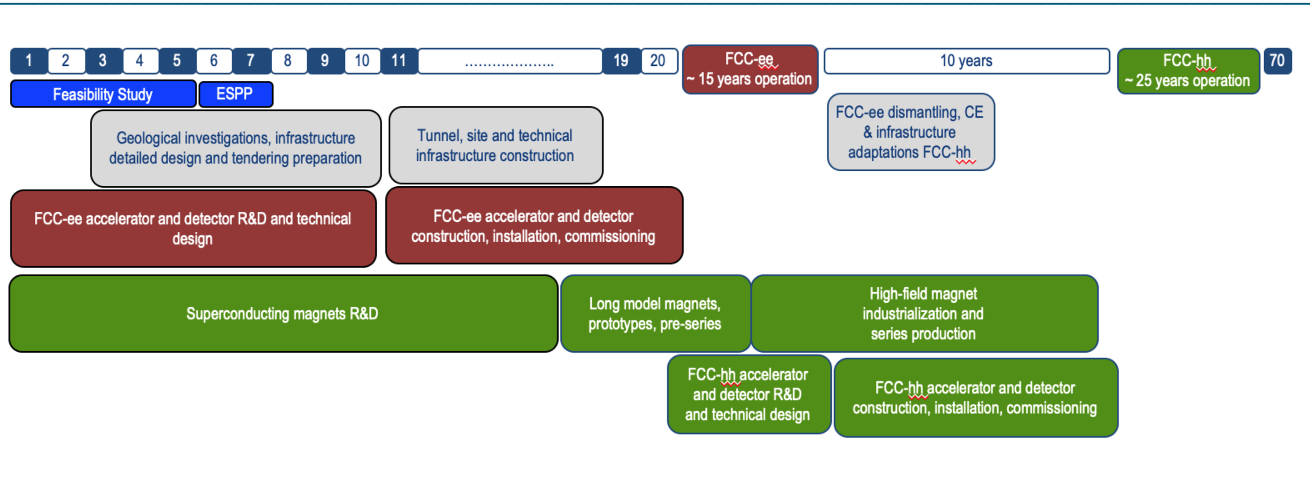
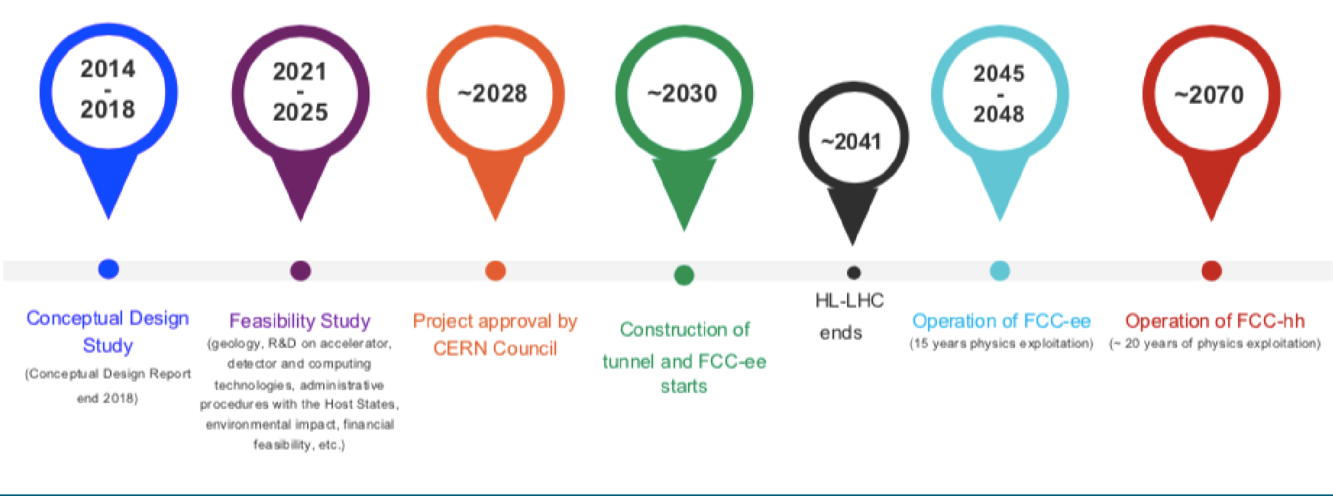
FCC estimated timeline



Technical schedule:
FCC-ee could start physics operation **in 2040 or earlier**



"Realistic" schedule takes into account:
past experience in building colliders at CERN
approval timeline: ESPP, Council decision
that HL-LHC will run until ~ 2041
ANY future collider at CERN cannot start physics operation before ~ 2045
(but construction will proceed in parallel to HL-LHC operation)

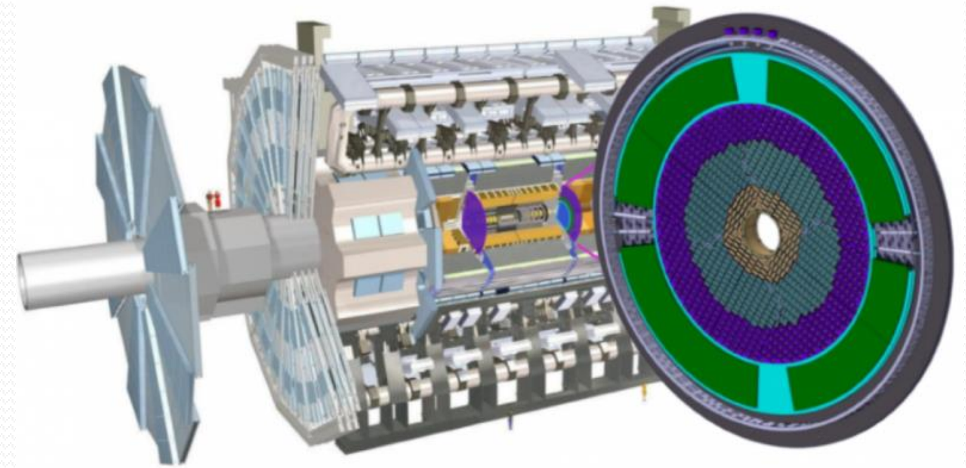
1st stage collider, FCC-ee: electron-positron collisions 90-360 GeV
Construction: 2033-2045 → Physics operation: 2048-2063

2nd stage collider, FCC-hh: proton-proton collisions at ≥ 100 TeV
Construction: 2058-2070 → Physics operation: ~ 2070-2095

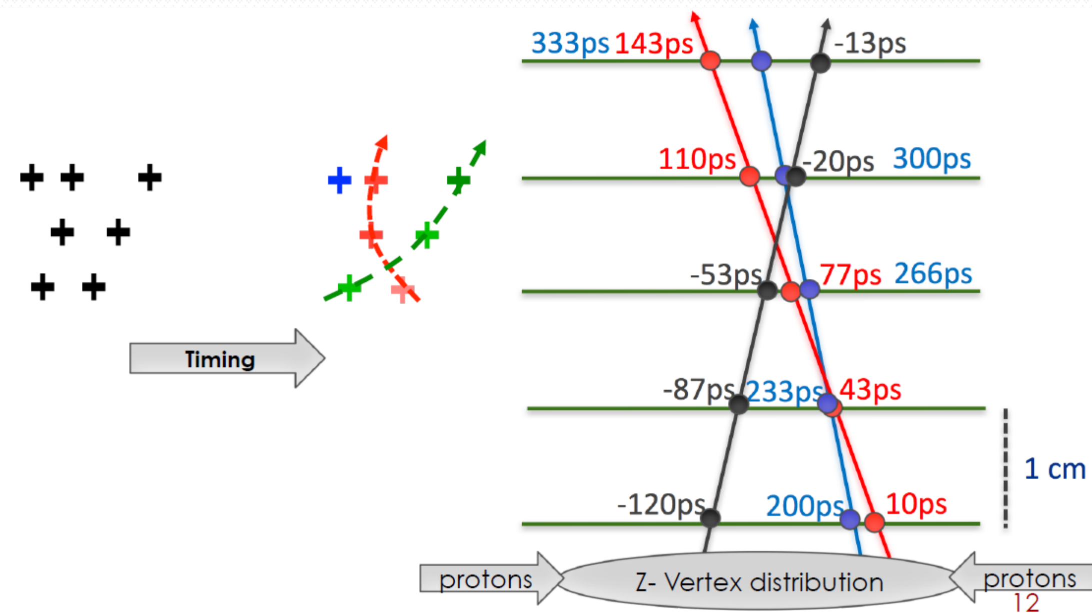
Care should be taken when comparing to other proposed facilities, for which in some cases only the (optimistic) technical schedule is shown

The effects of timing

- **Timing layers (HL-LHC)**
  - CMS and ATLAS are building **silicon-based timing detector layers** that will timestamp each track with a **precision of 30 ps**
  - ATLAS High Granularity Timing Detector (HGTD) and the CMS Timing Detector (MTD) placed in the **forward regions** (2.4<|η|<4.0)
  - Based on novel **Low Gain Avalanche Detectors (LGADs)**
  - The readout chip HGTD is an array of 15×15 channels of 1.1 mm × 1.1 mm
  - Designed with **TSMC 130 nm CMOS** process



- **4D tracking**
  - Timing information will be more important at future high-energy, high-luminosity hadron colliders with much higher levels of pileup
  - **4D tracking**: timing at **each layer** along the tracks



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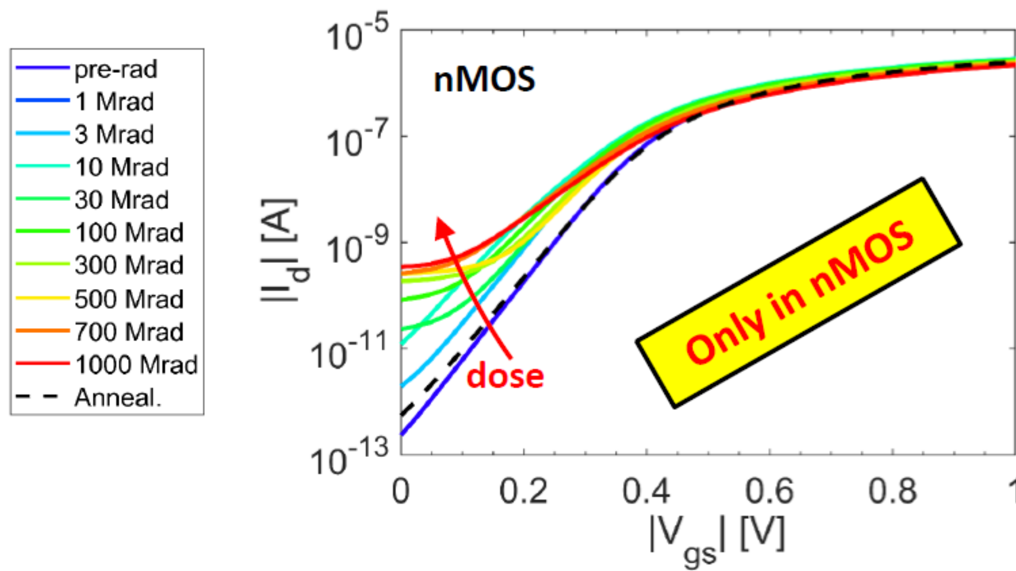
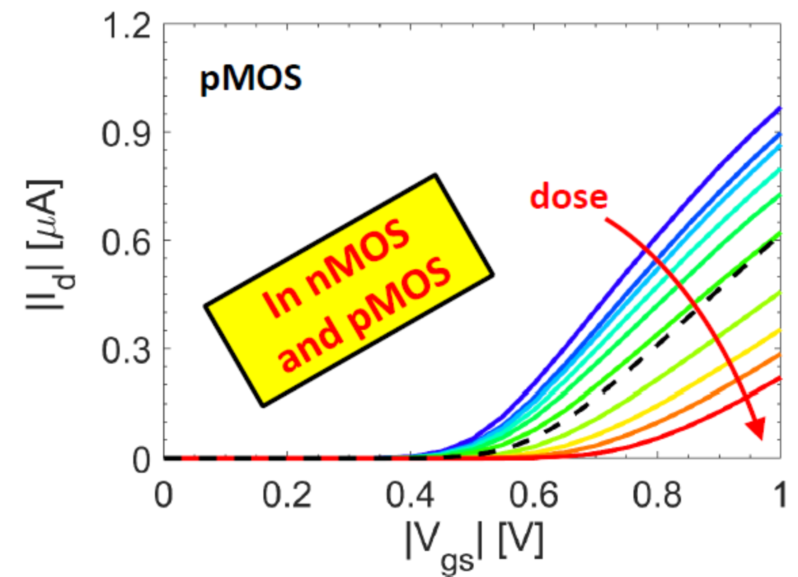
- At ultra-high doses, two dominating TID effects related to **charge trapping in STI oxides**:

1) Increase of OFF-leakage current

2) Loss of trasconductance (RINCE)



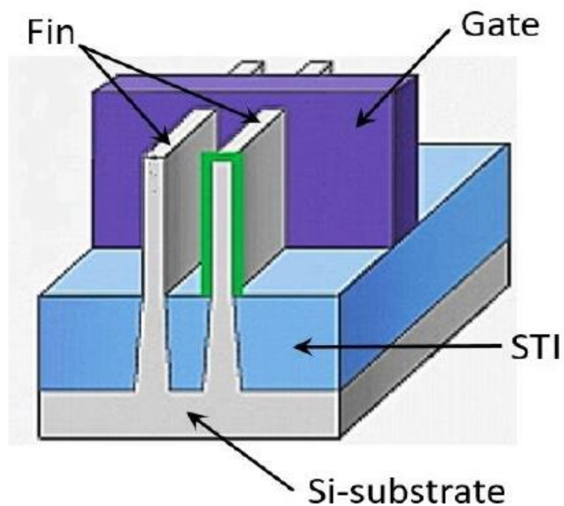


F. Faccio, et al., IEEE Trans. Nucl. Sci., 62(6), 2015; S. Bonaldo, et al. IEEE Trans. Nucl. Sci., 67(7), 2020

8

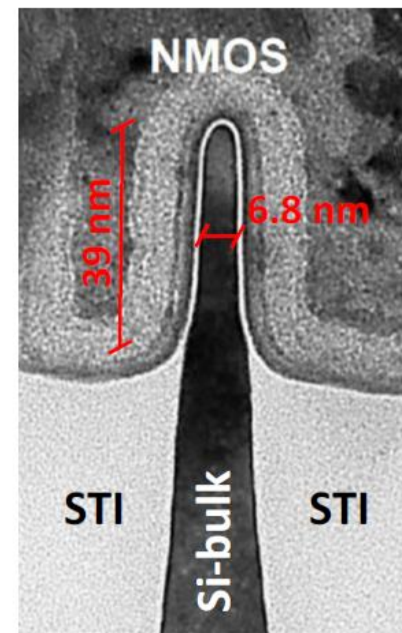
CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE
CPPM

- Better gate control over the channel
- Faster switching speed
- More drive-current per footprint
- Lower switching voltage
- **No ELT solution**



➢ Results on 16 nm bulk Si FinFET

- Manufacturer: **TSMC**
- **Tested up to 1 Grad**
- **Shallow trench Isolation (STI)**
- Designed in different combination fin/finger



9