

SiW-ECAL Contributions to DRD6

CERN, IFIC, IJClab, KEK, Kyushu,
LLR, LPNHE, Omega

SiW-ECAL Prototyping

- **2023:** Build a prototype with uniform layers
(FEV2.1 + 500 μm Sensors)
All material avail.
analysis of existing data
(prepare G4 sample ?)
- **2024:** Test in beam (standalone, w AHCAL)
Prepare setup with 2 towers
 - 7–12 layers, same ASUs + 40 Wafers (*if funding*)
 - → Dark γ , QED exp:
LUXE@XFEL, EBES@KEK, Lohengrin@ELSA
- **2025:** Test a 2 tower design : BT, Experiments
 - If funding (ANR?) prepare for 3 towers for LUXE
- **2026+:**
Far Side : new prototype → pilote module (1M ch)

Vincent.Boudry@in2p3.fr

SiW-ECAL Design for Detectors (↔ ECFA WG3 & CLD/ILD)

- **2023:** Prepare specifications for low occupancy, continuous operations ASICs
 - power, rates, etc. Test of various ASICs hypothesis, Check for active cooling needs in ECAL
 - Specify requirement on precision on timing in PFA/PID
Dedicated layers (LGADs) vs Bulk Timing
- **2024:** Prepare design
 - Optimisation of the ECAL (granul, resolutions E, t)
 - Link to other DRDs ?
 - Electronics, DAQ ↔ DRD7.1, 7.2 ?
 - Integrated cooling, *if needed* ↔ TF8.2 ?
 - Mechanics & monitoring ↔ TF 8.3, 8.4 ?
- **2025:** Blueprint (EDR) of pilote module for Higgs factory

Time scales ?

FCC-contact, 14/04/2023

Objectives:

– Simulations

- 1) study of **hadronic showers** with **time information**
- 2) study of **cooling system** required for the T-SDHCAL unit based on the present knowledge of the **Liroc ASIC** power consumption as well as the other components to be used.

3) Comparisons data–simulation

From Imad @ CALICE

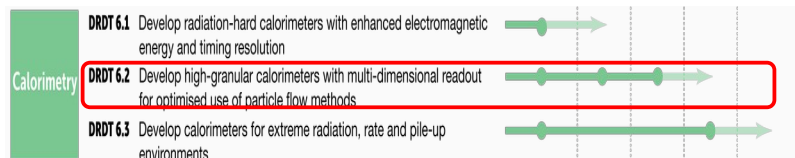
– Prototyping:

- 1) **Mechanical structure** with the **cooling system**
- 2) Conception and production of **fast-time electronics** (PETIROC/Liroc+TDC)
- 3) Conception of a **thin and large ASU** hosting the readout electronics to be associated to the MRPC in a cassette.
- 4) **DAQ system** for a few T-SDHCAL units.
- 5) Construction of a few T-SDHCAL units. Brussels, Lyon, Shanghai, GWNU
- 6) Construction of **cooling units** for the T-SDHCAL units.
- 7) **Validation** of the new T-SDHCAL units in **beam tests**
 - first in independent way and
 - then with the other SDHCAL units.



- Collaboration OMEGA + AGH Krakow + CEA Saclay
 - OMEGA : VFE and backend
 - AGH : ADC
 - CEA : TDC
- Start from HGCROC / HKROC : Si and SiPM
 - Reduce power from 15 mW/ch to few mW/ch
 - Allows better granularity or LAr operation
 - Extend to LAr (cryogenic operation) and MCPs (PID)
 - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
 - Several improvements foreseen in the VFE and digitization parts
- Prepare MPWs and/or engineering runs to get enough chips for calos
 - Already ~300 k€ for an engineering run in 130 nm
 - First run early 2024 with EICROCs and « DRD6 ROCs »
- Submit to DRD6 to have close interaction with physics performance
 - Embedded electronics and joint FE/detector optimization

Links to other DRDs/TFs



All :

- DRD7.2: ASICs, power management
- DRD7.5: DAQ, clock distrib, data
- DRD8.2: Cooling (Mostly ECAL)
- DRD8.3 & 8.4: Mechanics & Envir Monitoring, integration

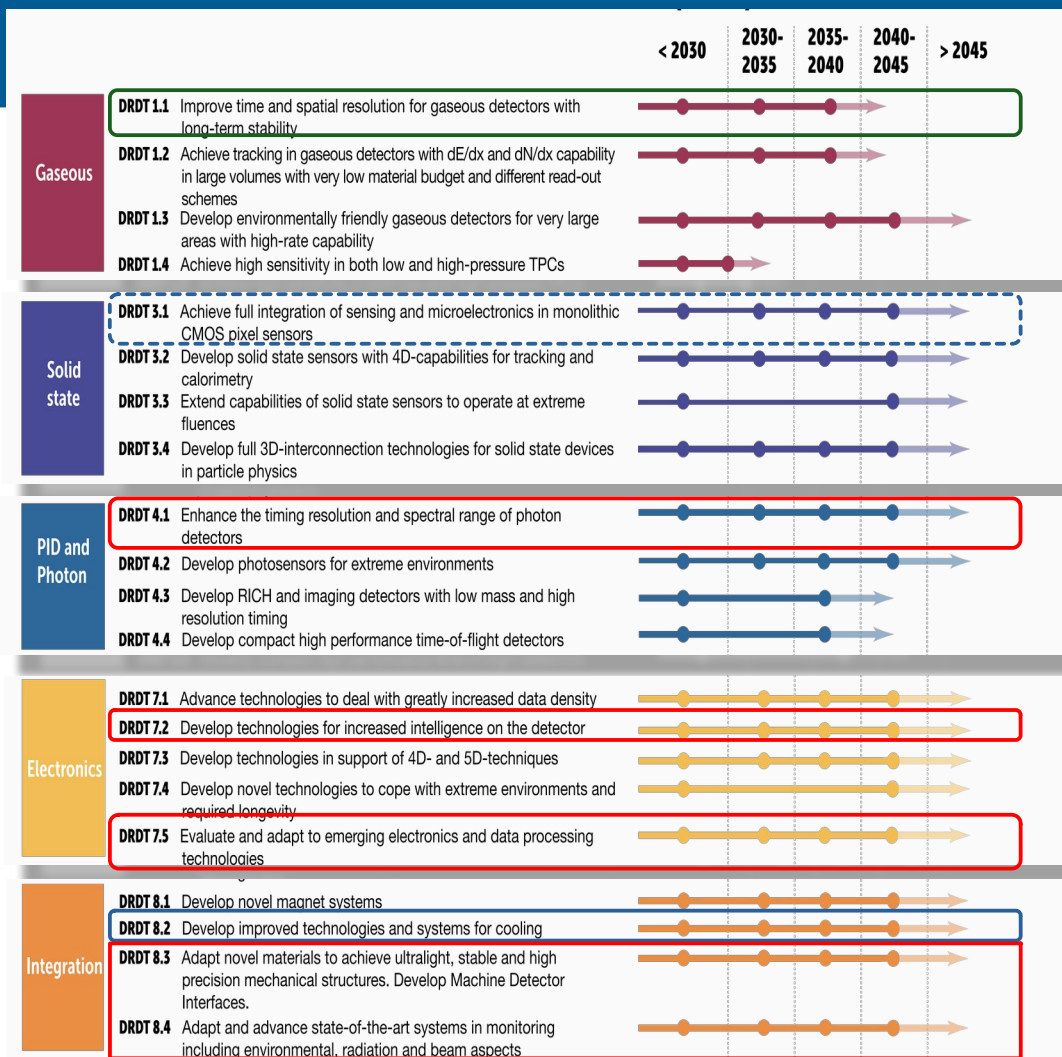
Si-ECAL, dECAL:

- DRD3.1: R&D on MAPs, SMADs
- DRD3.2: LGADs (timing layer)

T-SDHCAL:

- DRD1.1: Space & Timing resolution...

Vincent.Boudry@in2p3.fr



FCC-contact, 14/04/2023