

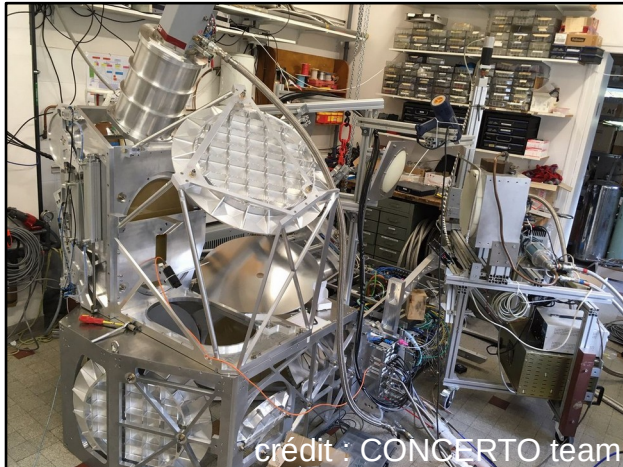
Kinetic Inductance Detector (KID) readout backend

O. Bourrion, C. Hoarau, J. Bounmy, D. Tourres, C. Vescovi, J.-L. Bouly, N. Ponchant, A. Beelen, M. Calvo, A. Catalano, J. Goupy, G. Lagache, J.-F. Macías-Pérez, J. Marpaud, A. Monfardini.



Concerto project

- Instrument for radio-astronomy (100-300GHz) @ APEX in Chili (5100m)
- Using Kinetic Inductance Detector (KID)
- Former instruments : NIKA2@IRAM, KISS(Quijote)
- In collaboration with Néel, LAM, ESO

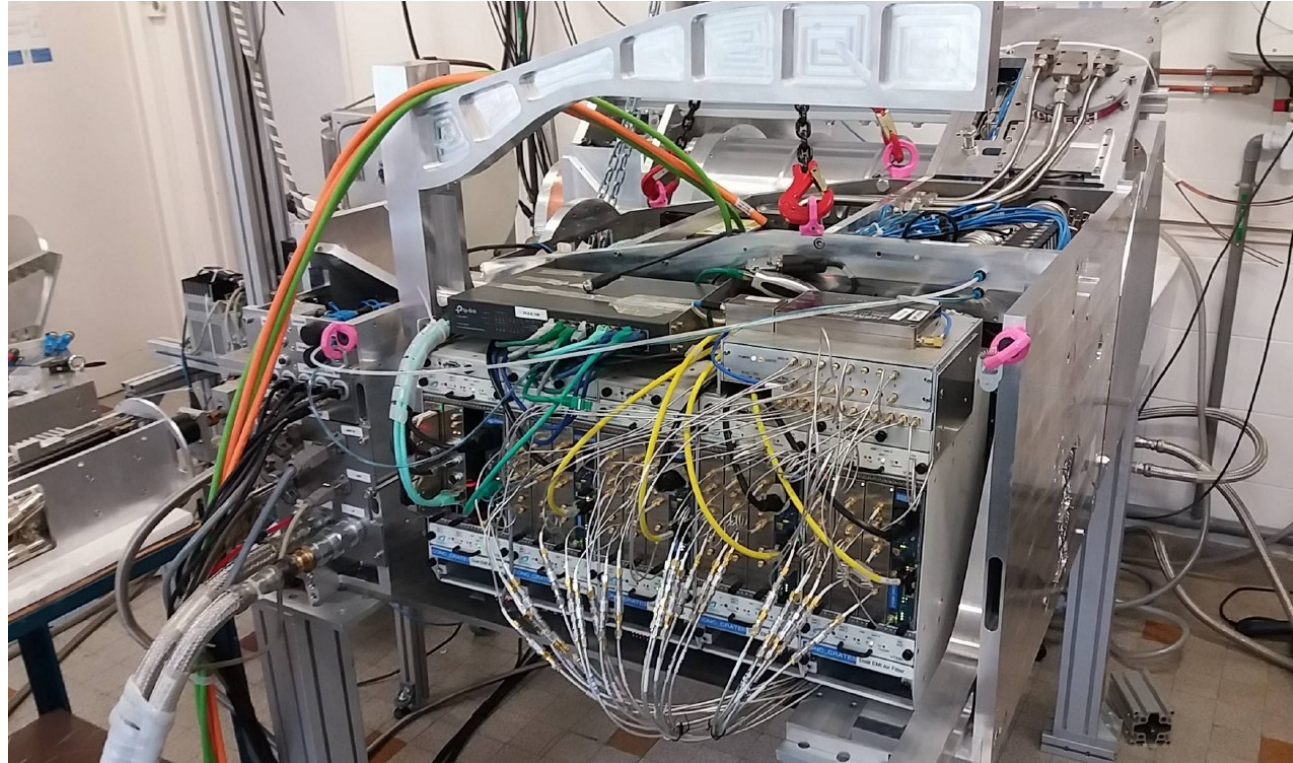


San Pedro de Atacama



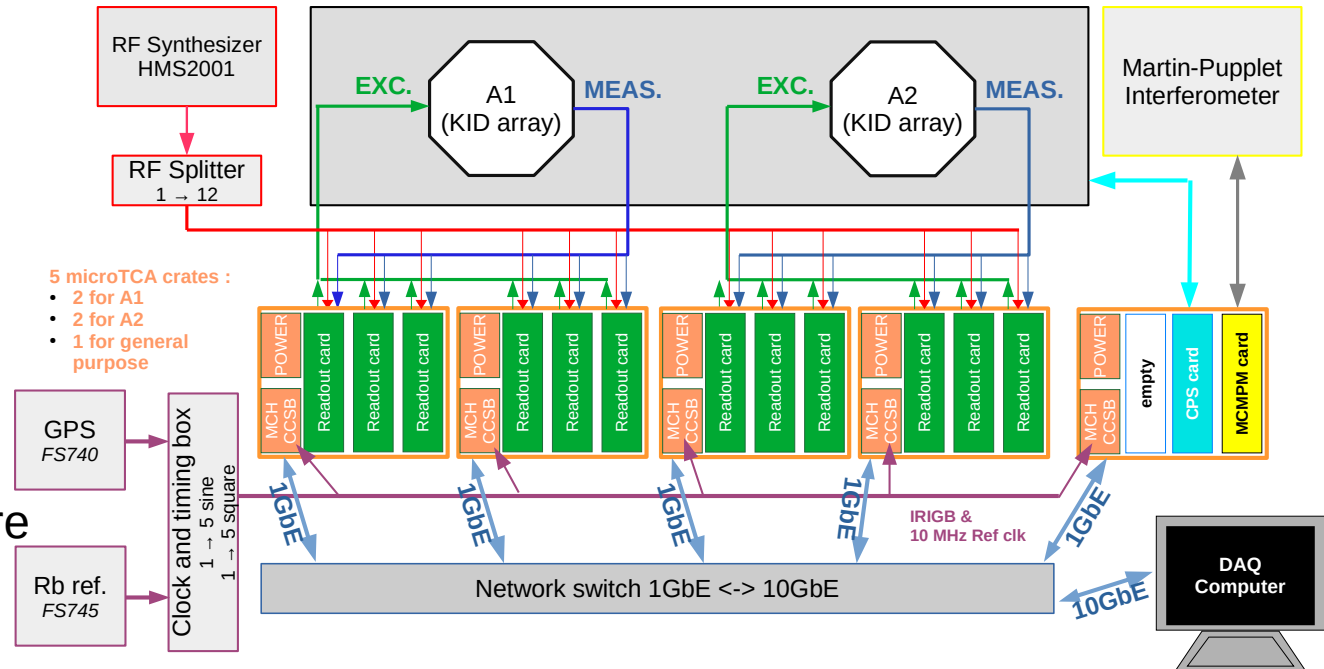
Concerto instrumentation (1/2)

- Close vicinity of the camera
- Constrained environment
 - Remote operation and maintenance
 - Less pressure (cooling!)
 - Limited volume
 - 3h round-trip by car from base
 - Access with 2 people
 - Crate tilt with instrument between° 15 and 90°
- Use of microTCA crates
 - => health monitorings



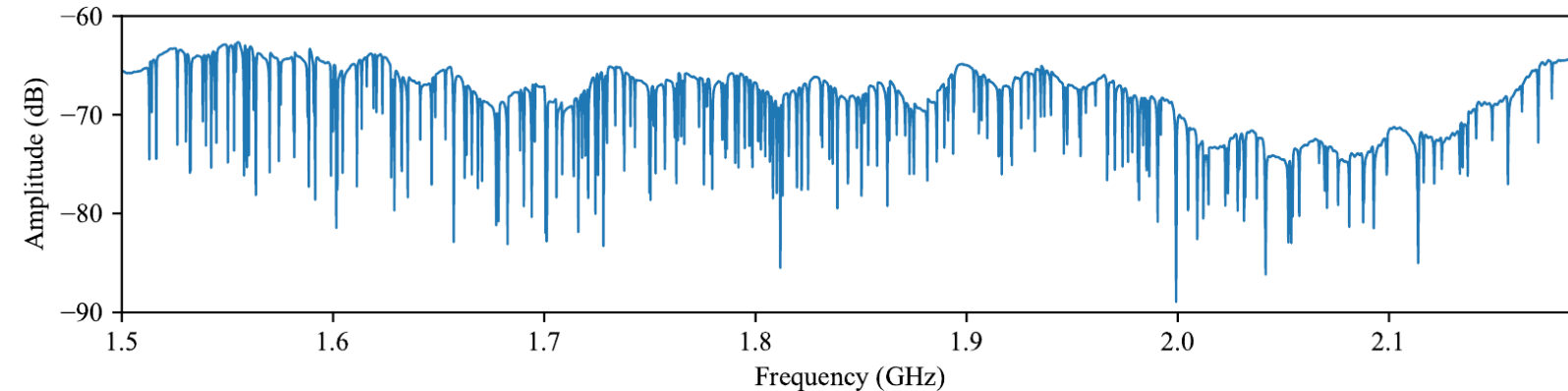
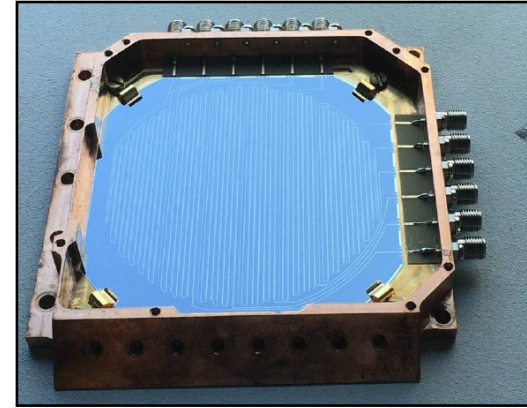
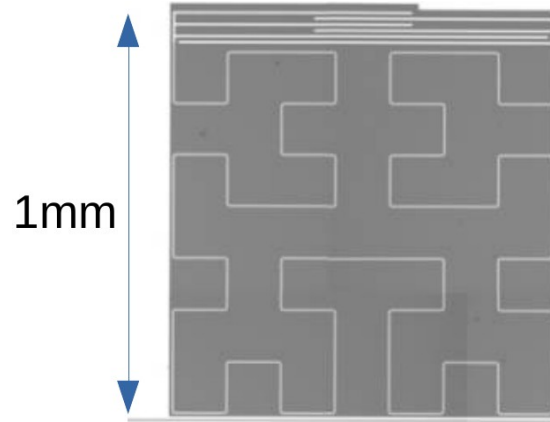
Concerto instrumentation (2/2)

- 2 KID arrays (6 feed-lines each)
- 12 readout boards
- Interferometer and cryostat control
- Timing through IRIG-B (GPS receivers)
- Common stable 10 MHz clock
- Interferometer control not discussed
- DAQ and computing infrastructure
- Remote control



KID sensors

- Superconducting devices (100 mK)
- High quality factor ($Q \sim 20^4$)
- ~ 360 pixels/feedline
- BW = 1 GHz, (1.5 GHz \rightarrow 2.5 GHz)
- ~ 2200 pixels/array



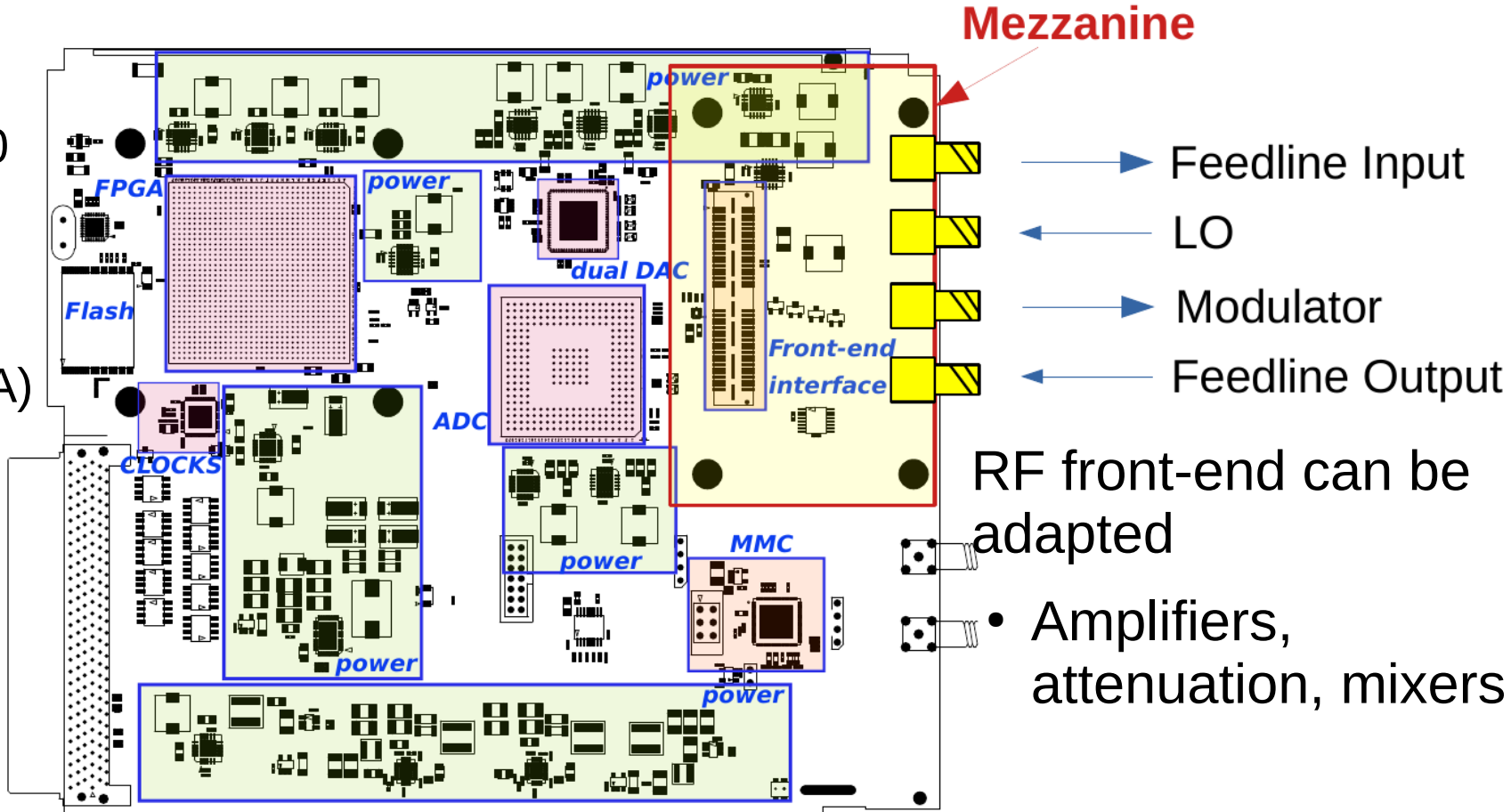
=> One readout board per line

Hardware platform description

- AMC form factor
- Xilinx KU060 FPGA
- 2GSPS converters (A/D and D/A)

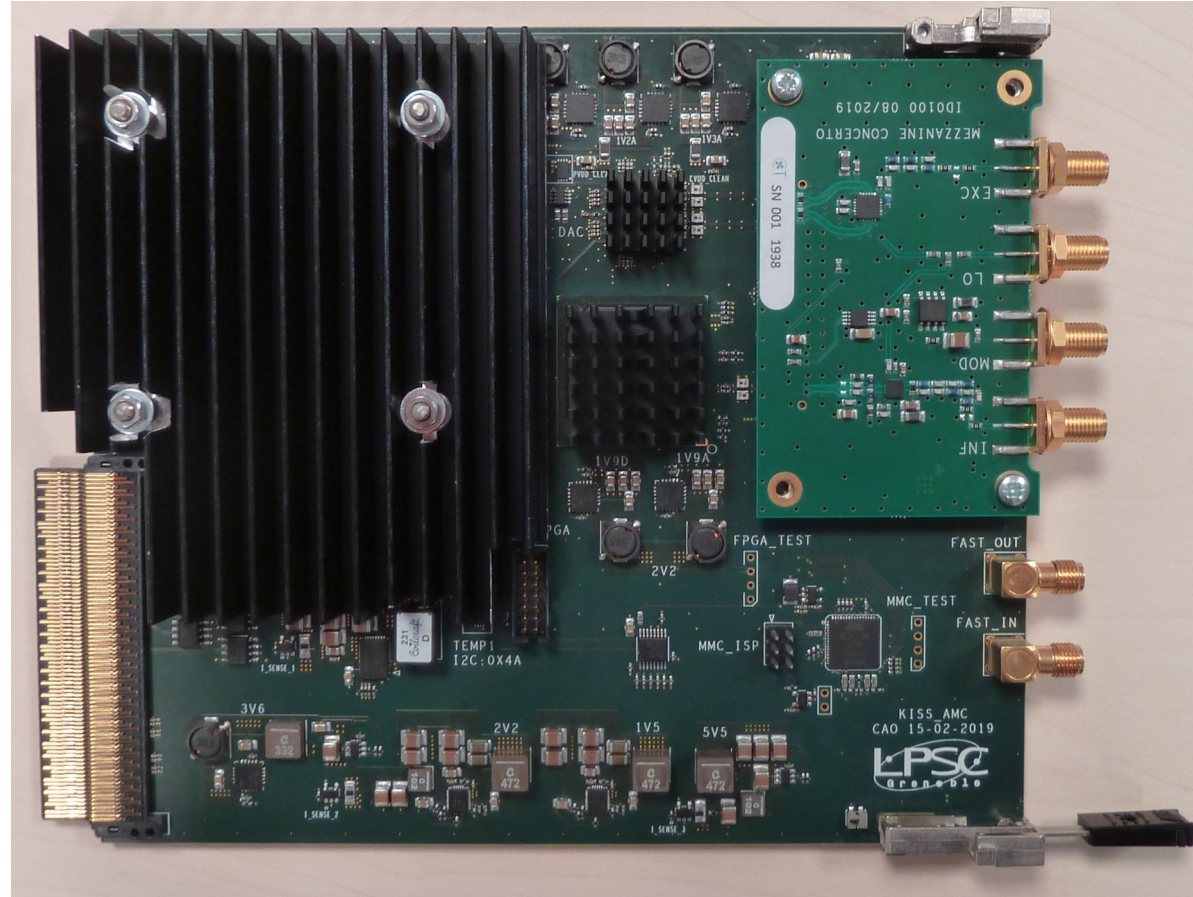
AMC :

- Alims
- Ethernet
- 10MHz
- IRIG-B

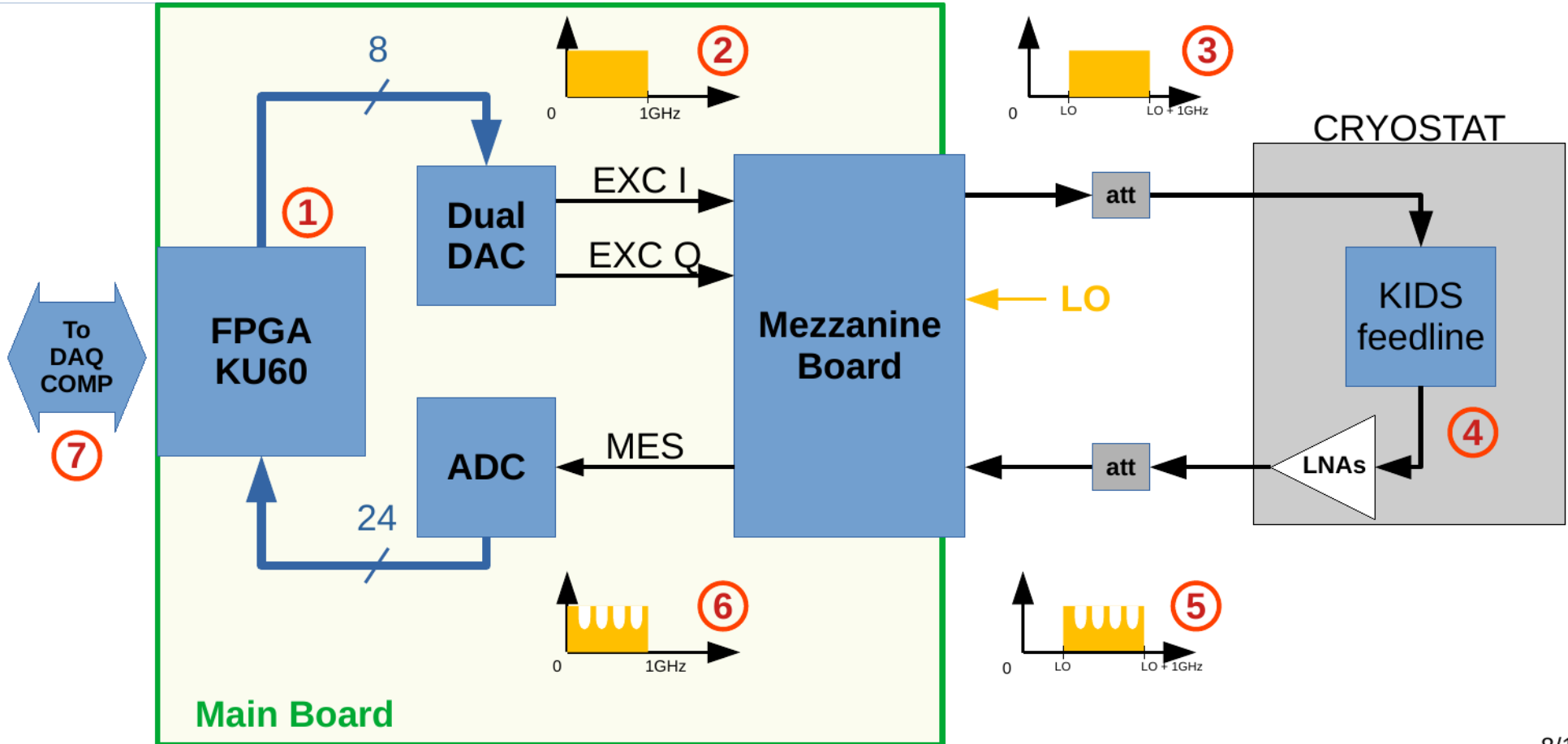


Latest generation readout board

- 12 layer PCB
- AMC form factor
- Customized heat sink (-30% convection @5100m)
- 35W/board

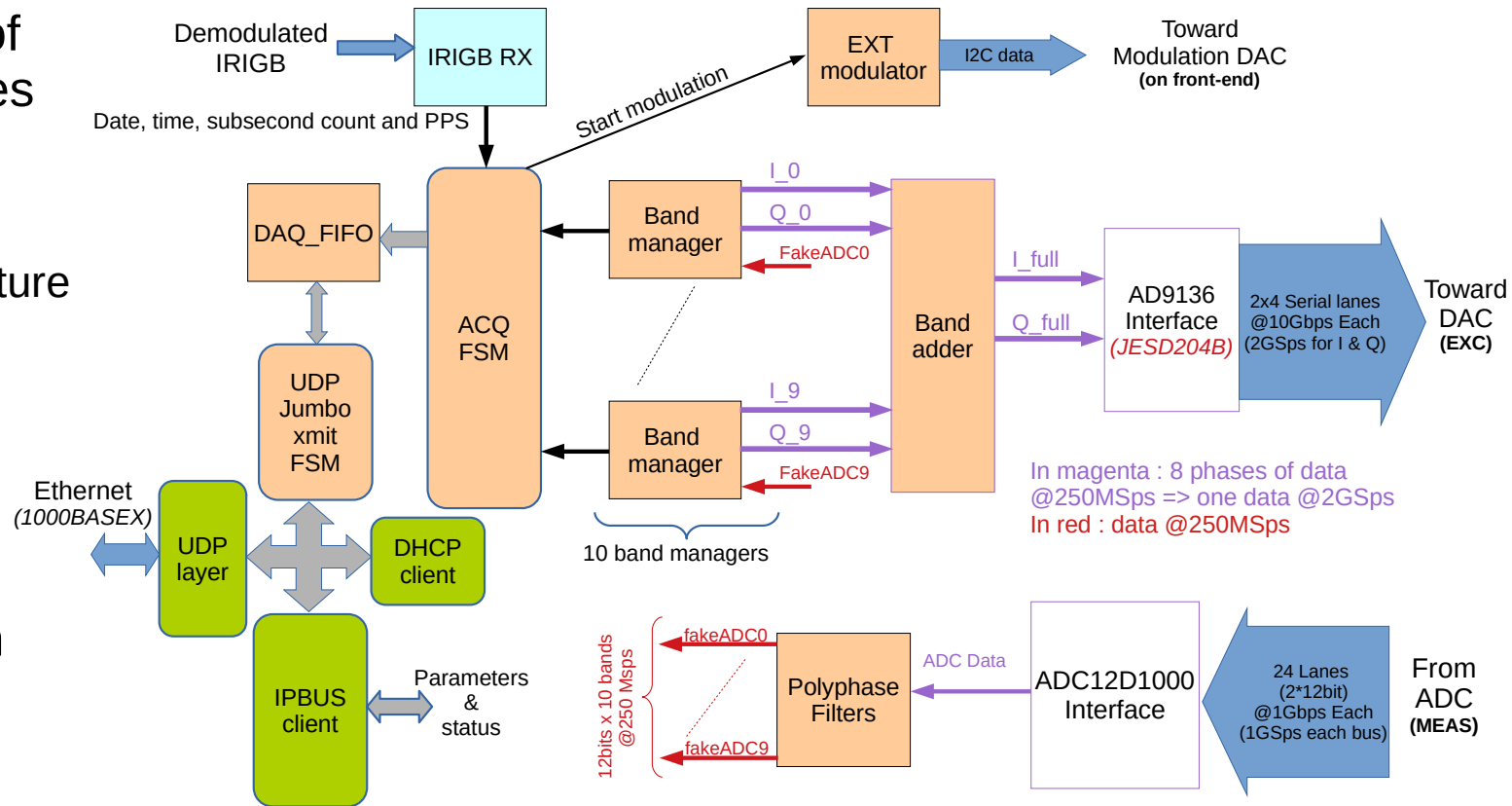


Readout principle



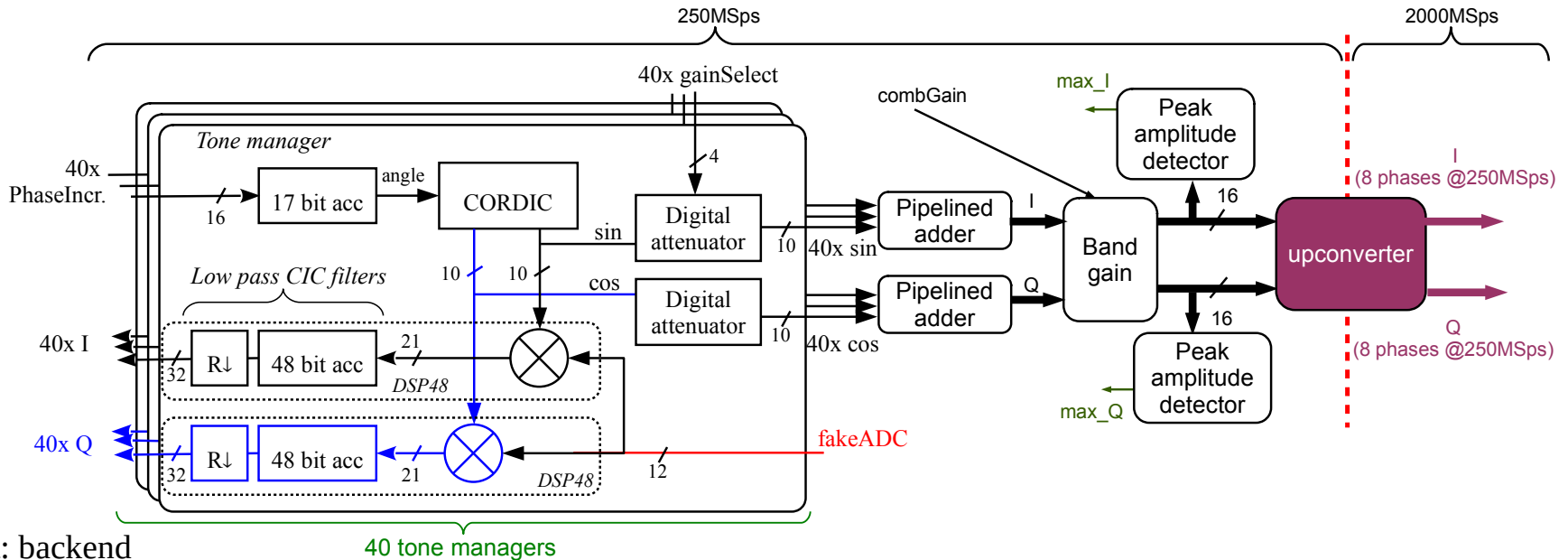
FPGA firmware overview

- 10 frequency bands of 100 MHz with 40 tones each
 - 400 generators
 - 400 In-phase/Quadrature values
- DAQ at 4 kHz
- Core at 250 MHz
- Converters at 2 GHz
- 1GbE communication



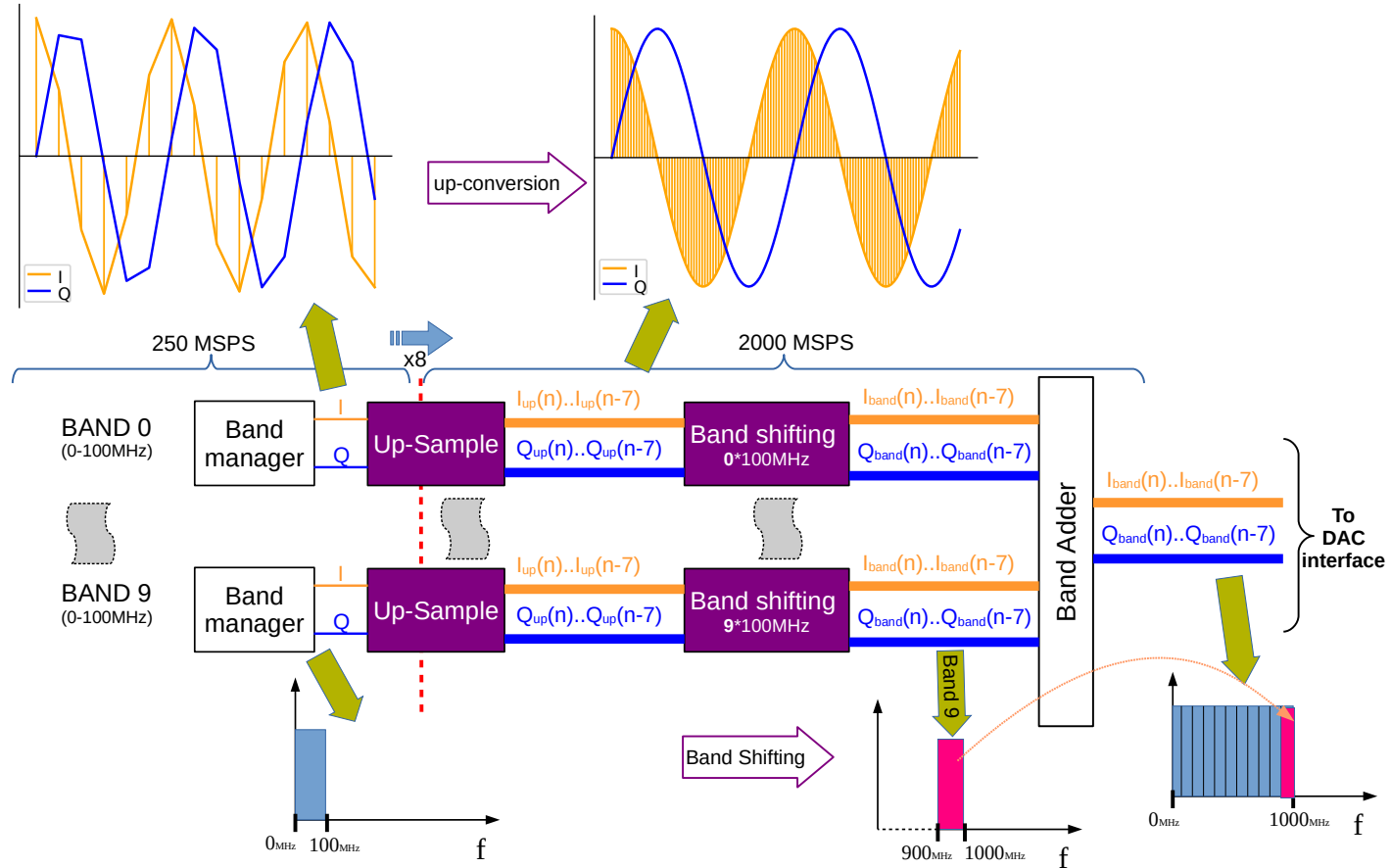
FPGA firmware – band manager

- Sine/cosine with Coordinate Rotation Digital Computer (CORDIC)
- Tone analysis with Digital Down Converters (DDC)
- Analog bandwidth 100 MHz with 40 tones
- Digital up-converter to shift signal frequency



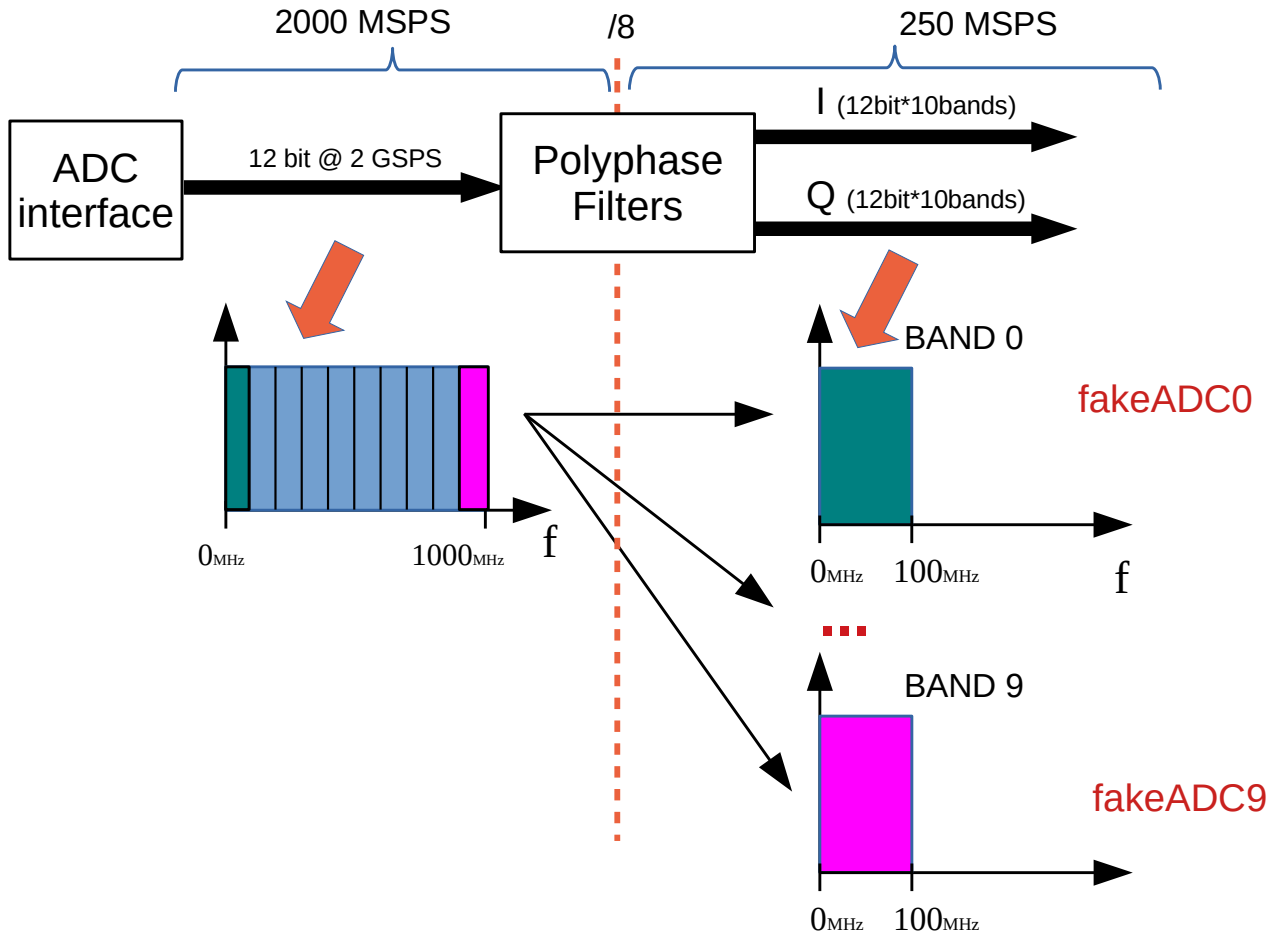
FPGA firmware – up-converter

- Up-sampling to 2GSPS
- Band shifting (x10)
- Summing of all signals
- Injection in dual DAC (IQ modulator)



FPGA firmware – polyphase filters

- Polyphase filter to
 - Down-sample
 - Filter
 - Shift in frequency



FPGA resource usage

Main block name	Sub-block portion	CLB LUT		CLB FF		DSP	
		count	% of total used	count	% of total used	count	% of total used
Ethernet layer	total	4532	2.1	4053	1.2	0	0.0
	UDP/IP stack	2730	1.3	2309	0.7	0	0.0
	DHCP	639	0.3	647	0.2	0	0.0
	ipbus	1163	0.5	1097	0.3	0	0.0
ADC interface	total	748	0.3	2244	0.6	0	0.0
LO modulator	total	142	0.1	134	0.0	0	0.0
Polyphase filter	total	18736	8.7	37674	10.9	418	21.2
DAC interface	total	1071	0.5	2192	0.6	0	0.0
IRIGB RX	total	236	0.1	502	0.1	0	0.0
Full tone manager	total	187524	87.6	288701	83.5	1555	78.8
	1 band manager (out of 10)	18050	8.4	27121	7.8	82	4.2
	band adder	2656	1.2	2672	0.8	0	0.0
	misc (unused for concerto)	2334	1.1	2421	0.7	3	0.2
	1 up-converter (out of 10)	190	0.1	1219	0.4	68	3.4
	daq_fifo	134	0.1	208	0.1	0	0.0
Miscellaneous	total	1168	0.5	10398	3.0	0	0.0
Firmware	total	214157	100.0	345898	100.0	1973	100.0

FPGA resources/type	Available	Used	% used
CLB LUT	331680	214157	64.6
CLB FF	663360	345898	52.1
DSP	2760	1973	71.5

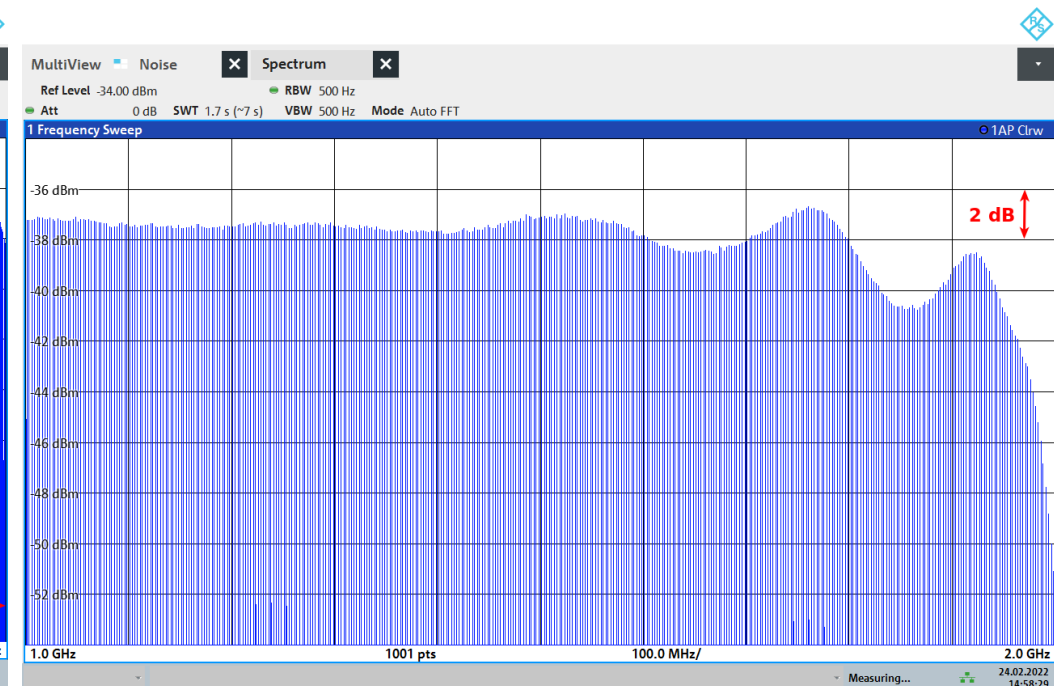
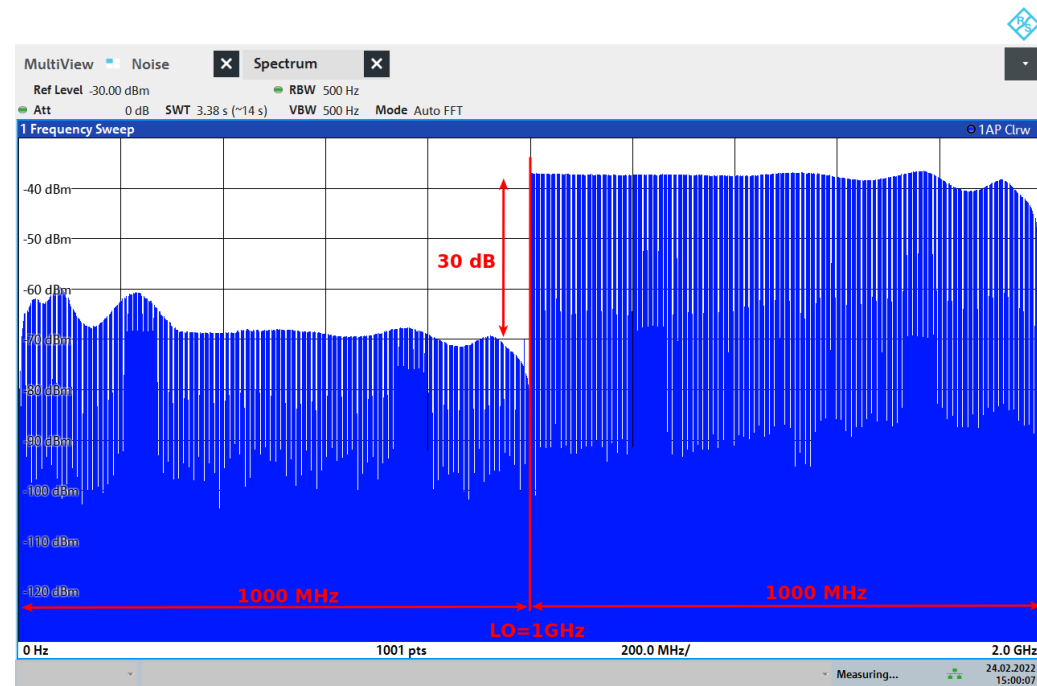
- FPGA : XCKU060FFVA1156-2
- 64.6% of the LUT ; 52.1% of the Flip-flops
- 71.5% of the DSP (about 2000 DSP running in parallel)

Kintex® UltraScale™ FPGAs

	Device Name	KU025 ⁽¹⁾	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0
Speed Grades	16.3Gb/s Transceivers (GTH/GTY)	12	16	20	32	56	64 ⁽²⁾	64
	Commercial	-1	-1	-1	-1	-1	-1	-1
	Extended	-2	-2-3	-2-3	-2-3	-2-3	-2	-2-3
	Industrial	-1-2	-1-1L-2	-1-1L-2	-1-1L-2	-1-1L-2	-1-1L-2	-1-1L-2

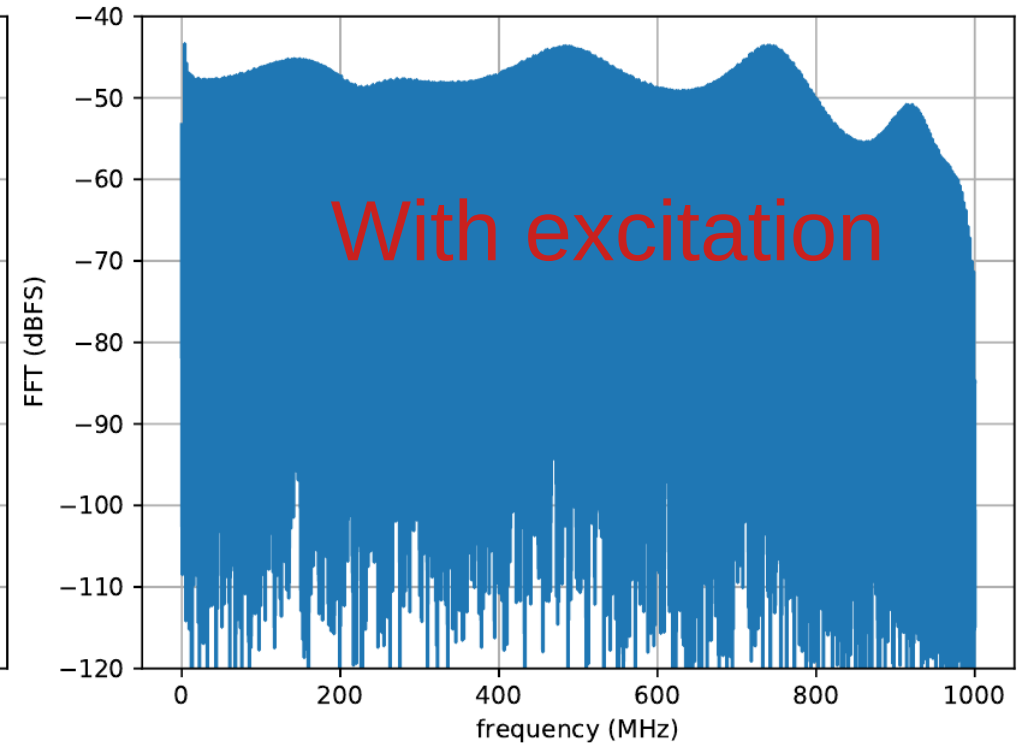
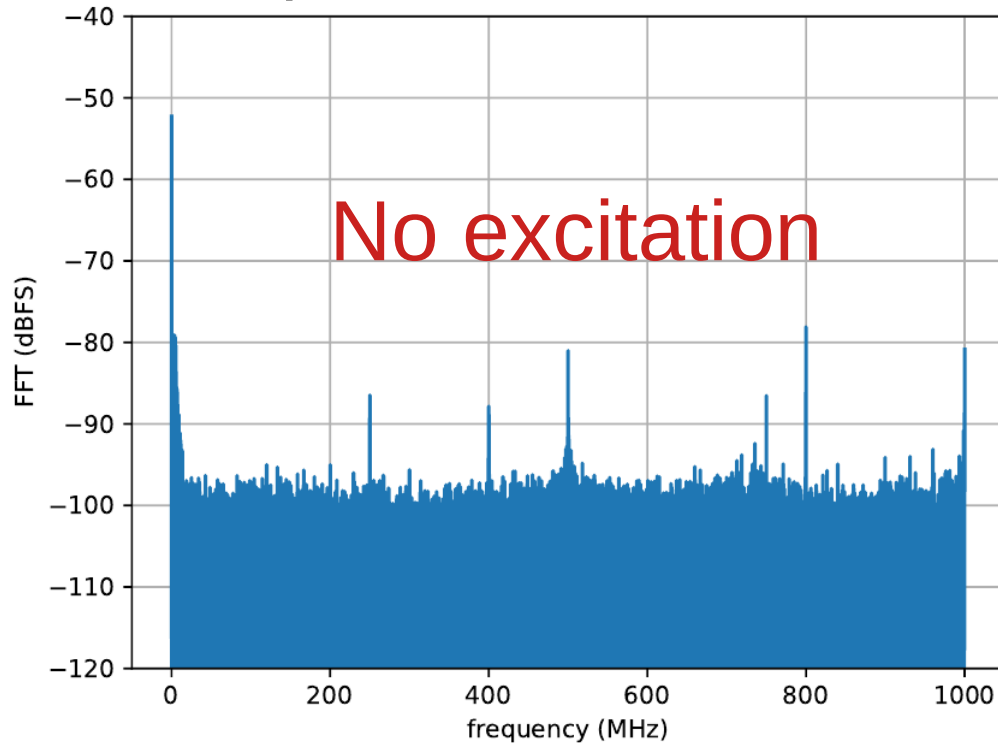
Excitation spectrum

- EXC output: 400 tones generated, shifted with LO=1GHz
- Good side band rejection; nice flatness



Loopback measurement

- Same signal, down-converted to baseband
- 65k points recorded



Summary

- Build-up on previous expertise/instruments (NIKA2, KISS)
- 2 arrays of ~2000 KIDs routinely instrumented in spectrometry (4kHz acquisition vs photometry at less than 100 Hz)
- Embedded and real time signal processing required
- CONCERTO was exploited for 2 years (April 2021- May 2023)
- More details
 - [O. Bourrion et al 2022 JINST 17 P10047](#)
 - [Julien Bounmy et al 2022 JINST 17 P08037](#)
- Future instruments aim at ~50,000 KIDs