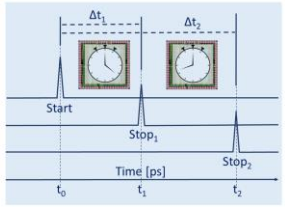
Projet de R&T IN2P3
FASTIME/Mokrane DAHOUMANE



R&T FASTIME : Fast and precise Time measurement circuit

Team members :

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GDR DI2I Meeting – 10-12 July 2023 – Subatech, Nantes

Outline

- Introduction
  - Scientific Context
  - Technological objective
- Project organization
  - Phases, Schedule and project structure
- Detectors and Specifications
- Description of the FASTIME 1st prototype circuit (Phase1):
  - Circuit description and simulation results
- Testbench design
- Conclusions and perspectives

Scientific Context

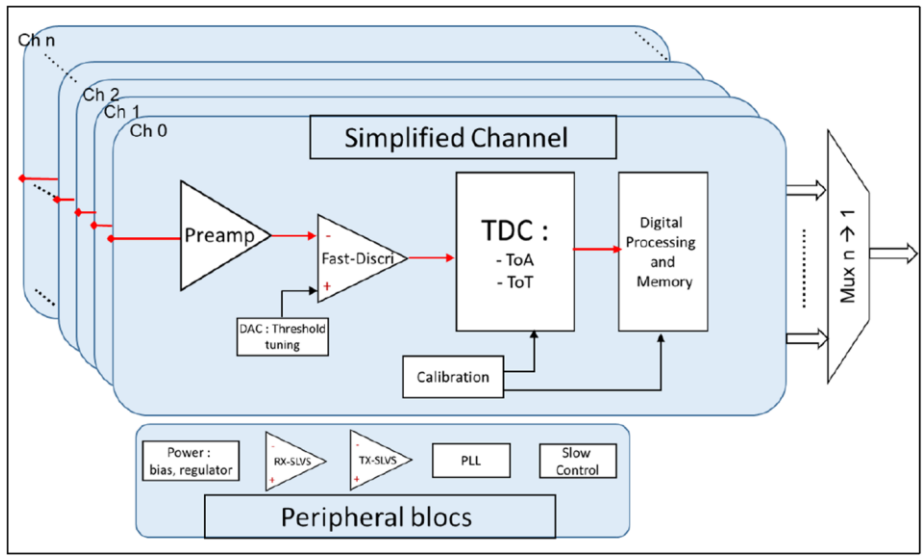
- FASTIME is an R&T/IN2P3 project which aims to develop an **integrated electronics** (ASIC) for very **fast time measurement** with an **accuracy** in the order of a **picosecond (rms)**.

- Such a resolution is becoming increasingly necessary in many areas, for example :
  - In future **High Energy Physics** experiments in order to **reduce the pile-up** by ~1000,
  - in future generations of medical imaging (PET) with 20-fold dose reduction at equivalent SNR
  - or for other applications (like future generation of **time-accurate pixel detectors**) whose temporal resolution, which approaches the picosecond, must not be degraded by the readout electronics.

- This proposal is based on the **expertise** and **synergy** of several IN2P3 laboratories (IJCLab, IP2I-Lyon, LP2I-Bordeaux, LPC-Caen, LPC-Clermont and Omega).

Technological Objective : development of a multichannel prototype

- FASTIME aims to **overcome** current **technological limitations** that degrade temporal resolution and/or counting rate
- The final objective is to produce a **multi-channel prototype** (ASIC) which integrates a **full-chain** for time measurement.
- The main building blocks of the chain are:
  - **An input stage (Fast Front-End):** which is a fast preamplifier, very critical because it depends closely on the characteristics of the detector to be read,
  - **A fast discriminator (Fast-Discri)**
  - **A high-precision TDC** (two architectures are integrated and associated with a **DLL**)
  - And peripheral blocks (DAC, Bias, PLL, SLVS-Tx, SLVS-Rx...)
- Choice of TSMC130nm process :
  - **maturity** and **sustainability**, **performance**...
  - high **expertise** of the community in this technology.
  - transfer to finer technologies is feasible:
    - example: TSMC 65nm or FD-SOI 28 nm…



Simplified diagram of the prototype circuit integrating a "complete" chain of time measurement

Project Organization : project phases

- FASTIME is 3-year R&T project: from January 2021 to December 2023
- The realization of FASTIME takes place in two main phases preceded by a pre-study of ~5 months.

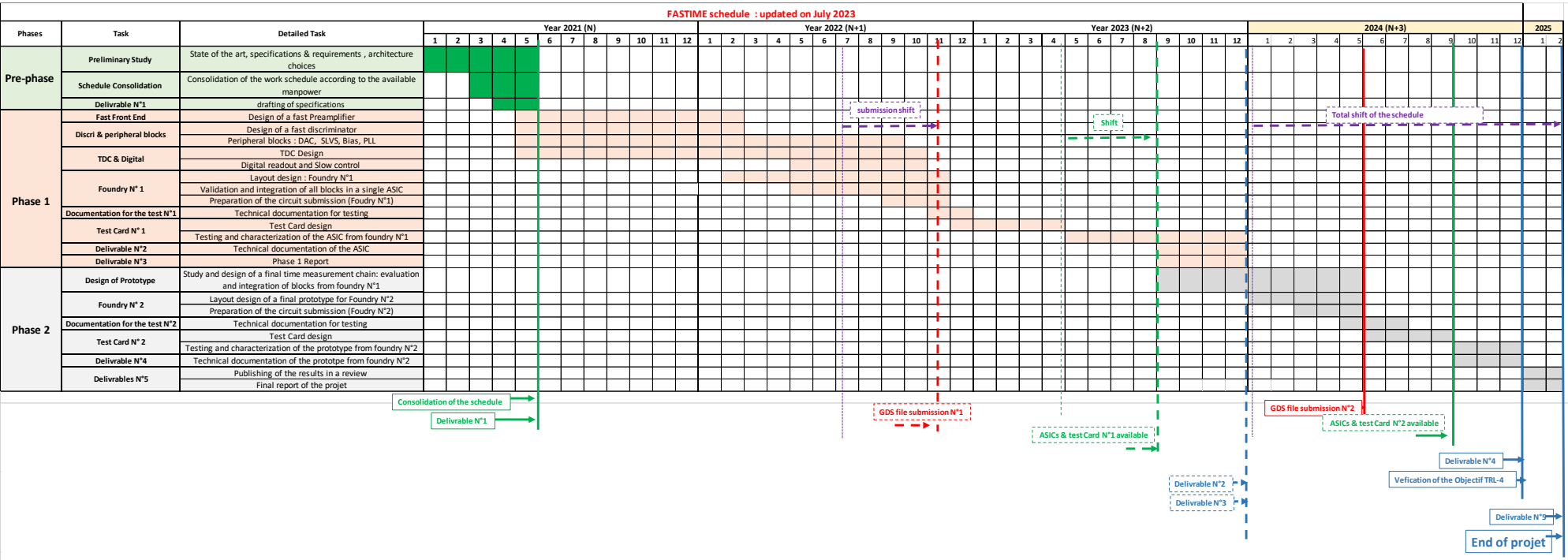
- **Pre-phase of the project was completed (2021):**
  - Theoretical study and review of the state of the art in different communities (IN2P3, CERN…)
  - Consolidation of schedules and specifications and allocation of human resources,
  - Choice of architectures to be implemented.

- This pre-phase is followed by **two phases** of realization:

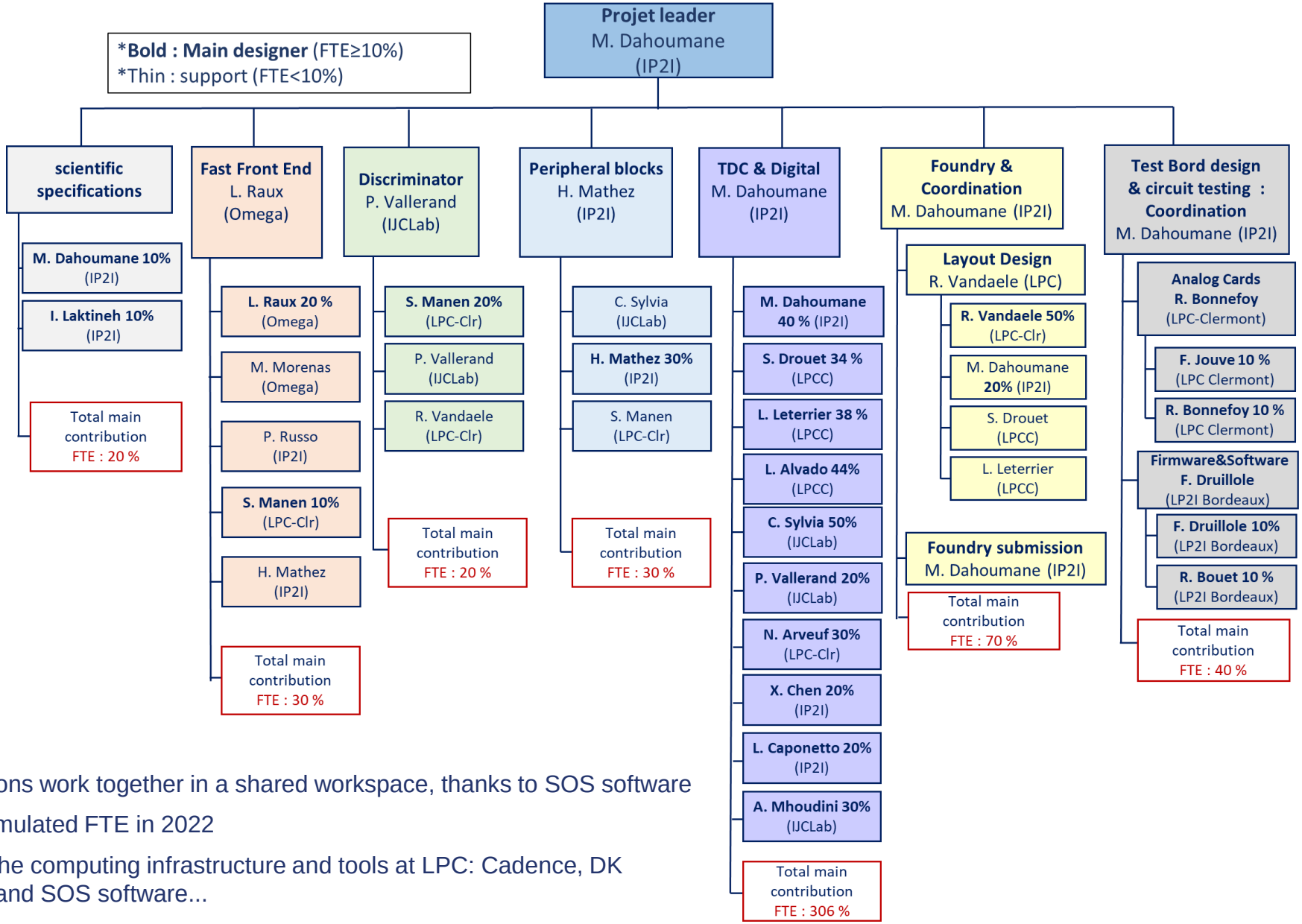
- **Phase 1 : design and characterization of a multichannel ASIC in order to evaluate different blocks:**
  - 4 Channel ASIC integrating a full chain: FFE + TDC+ Digital (readout & I2C Slow control)
  - Integration of two TDC architectures and two FFE architectures.
  - The circuit was submitted on **November 9th 2022** and packaged within a CQFP144 package
  - The testbench design is ongoing

- **Phase 2 : Realization of a final protype:**
  - Selection and integration of the most performant architectures and options that have been evaluated in phase 1.
  - Foundry submission is foreseen at the end of Q2 of 2024.
  - Writing documentation and publications.

Project Organization : schedule



Project Organization : FASTIME organization chart

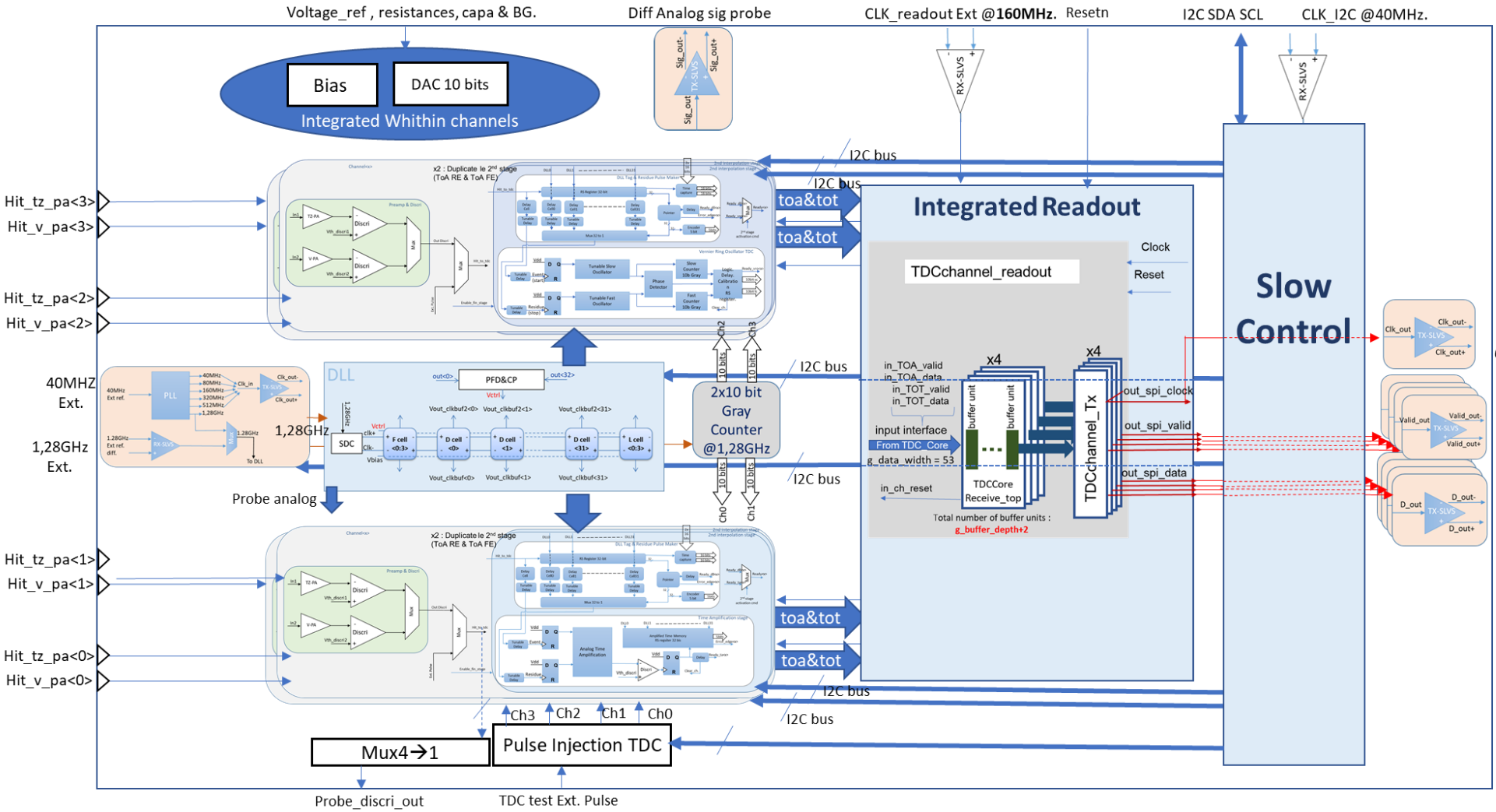


- 19 persons work together in a shared workspace, thanks to SOS software
- 4,35 cumulated FTE in 2022
- Use of the computing infrastructure and tools at LPC: Cadence, DK 130nm and SOS software...

Detectors and specifications

Detector type /Application	NCP/MCP /PICMIC	SiPM/ToF PET
Temporal precision (rms)	1 ps rms	3 ps rms
Dead time	100 ns	10 ns
Detector Supply Voltage	~1k V to 2k V	20-80 V
Power dissipation	---	< 10 mW/channel
Readout frequency (en Différentiel)	160 MHz	160 MHz
Dynamic range	100 fC to 1 pC	5-2500 photoelectrons
Number of channels (on the detector)	16	64
Det. Capa. (total seen by FEE)	46 pF	60-1300 pF/SiPM (capa. of one micro-cell ~80-100 fF)
Coupling	AC : Detector under High Voltage	DC
Impedance of detector line	37 ohm/channel	50 Ohm
Charge collection time	20ps/200ps	--
Signal rise time	~1ns	~80-100 ps (rise time of one micro-cell)
Temperature	0 to 85 °C	0-20 °C (in general, SiPM are cooled in order to limit DCR)
Counting rate	1 MHz/CM2	~1.6-4 Mcps (for one matrix of 64 SiPM coupled with CeBr3 cristals)

FASTIME ASIC: general diagram of a 4 channel ASIC

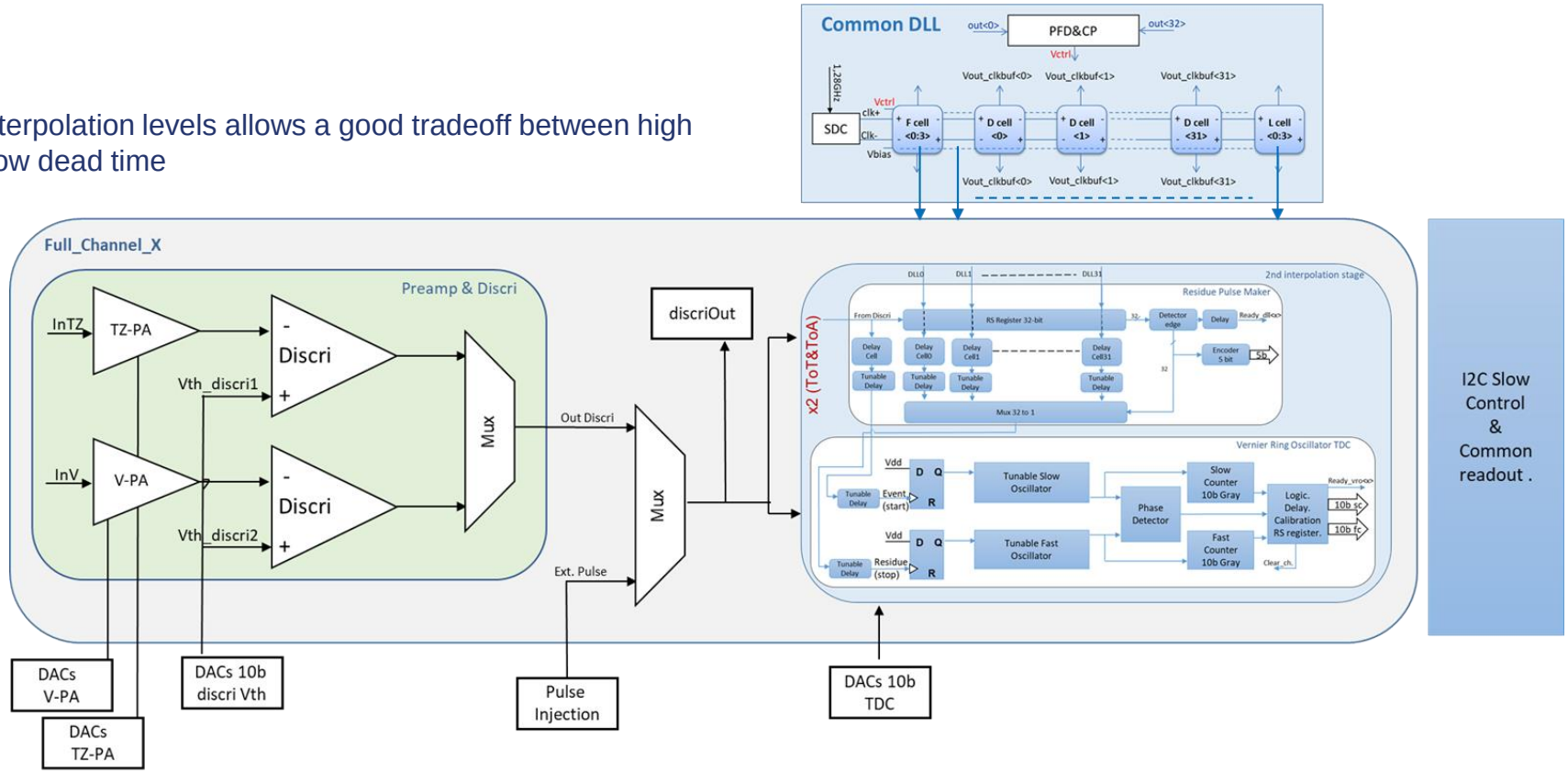


- A 2-stage interpolation TDC with a DLL as 1st interpolation stage and a coarse 10-bit Gray counter .
- 4 Channel integrating a full chain: FFE + TDC+ Digital (readout & I2C Slow control)
- 2 Ch. Vernier TDC and 2 Ch Time-Amplification TDC (2nd interpolation stage)
- Voltage Preamplifier and TZ-Preamplifier and a fast discri.

FASTIME ASIC: operating principle

- A common DLL (1st level of interpolation) distributes its 32 signals on the 4 channels of the asic
  - A 10-bit Gray counter (coarse counter) running at 1,28 GHz provides the Corse Time
  - For each hit signal (InTZ, InV or ExtPulse), the state value of the DLL is memorized with a resolution of 24 ps (LSB of the DLL)
  - The DLL signals are sent to a 2nd interpolation stage which quantifies the DLL residue with an accuracy of 1 ps rms.
  - Two architectures of the 2nd interpolation stage:
    - Vernier Ring Oscillator TDC and Time-Amplification TDC
    - Both are Associated with a Residue Pulse Maker block..

- The use of 2 interpolation levels allows a good tradeoff between high precision and low dead time

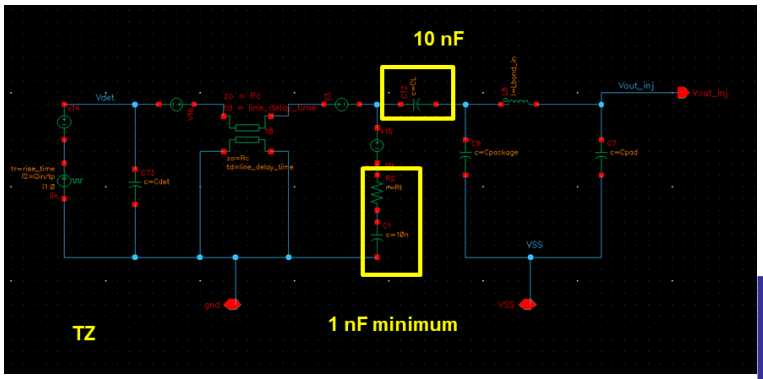


Architecture and performances of sub blocks: Fast Front End and Fast Discri

- **Two architectures :**
  - FFE 1 : Trans-Impedance Preamplifier
  - FFE 2 : Voltage Preamplifier :
    - expression of Jitter (Cf. course of C. De La Taille @Omega) : $\sigma_t^J = \frac{\overline{e_n}.Cd}{Qin} \times \sqrt{\frac{tr_{PA}^2 + td^2}{2.tr_{PA}}}$ $\sigma_t^J = \frac{\overline{e_n}.Cd}{Qin} \times \sqrt{td}$
      - Substantially the same formula for both architectures.

- The performance is limited by Cd, it depends also on the input signal amplitude and on the noise of PA.
- There is un optimum between BW of PA and drift time of the Detector.

- **Detector electrical model:**



- **Jitter simulation of PA+Discri**
  - Transient noise
  - Transient + AC-noise

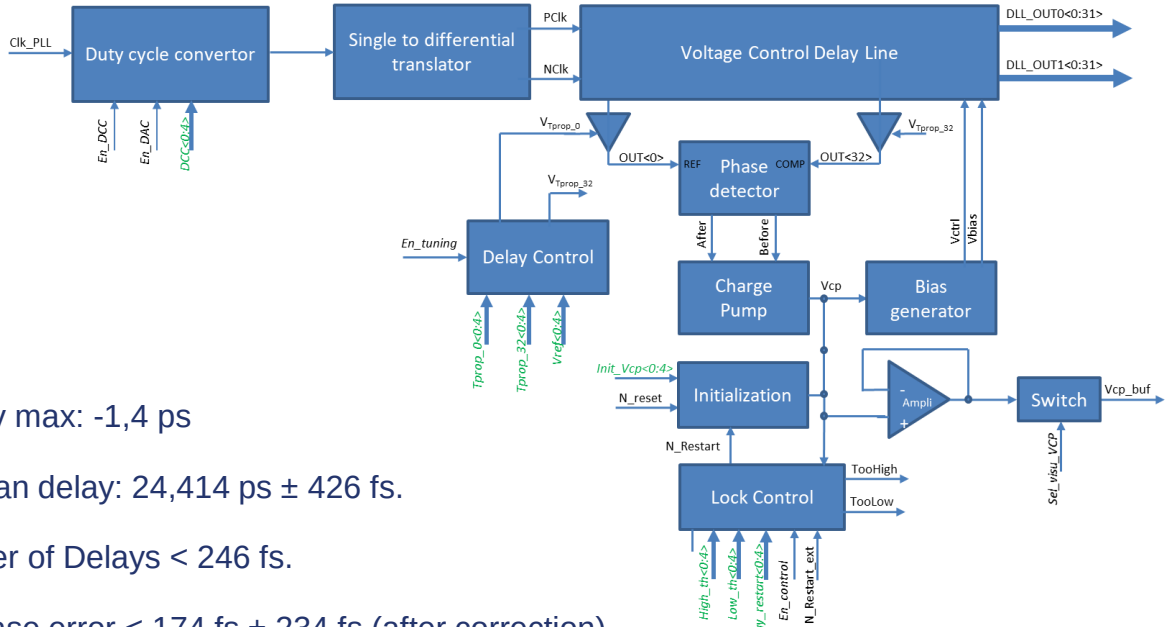
Jitter PA+Discri (Qin_min 100fC)	Trans-impedance Preamplifier (Vth = -20 mV)		Voltage Preamplifier (Vth = -10 mV)	
	ToA (ps rms)	ToT (ps rms)	ToA (ps rms)	ToT (ps rms)
Schematic	8,14	47	6,46	191,2
Layout	9,37	38	8,1	159,4

For a maximum signal (1pC)
➔ Jitter ~1ps rms.

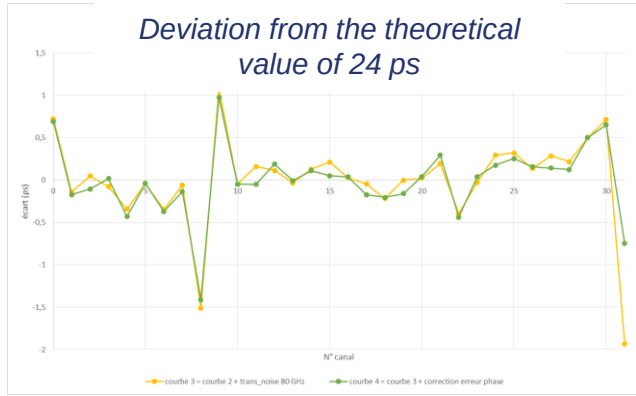
RMS noise ~1 mV rms for both preamplifiers.

TDC: 1st stage of interpolation based on a DLL

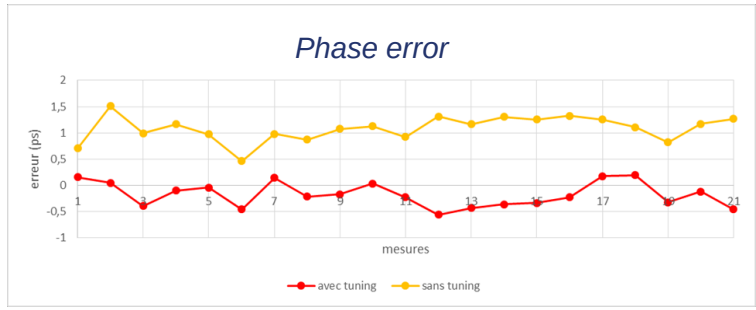
DLL composed of 32 Delay Cells with 24 ps unit delay and a CLK@1.28GHz

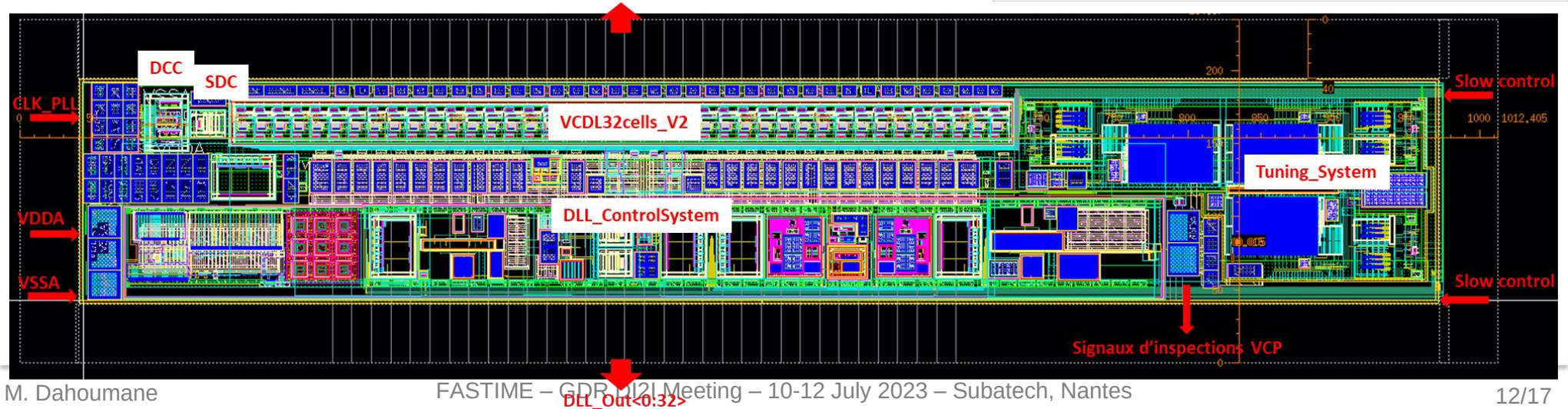


post-layout simulation results:
self bonding 5 nH, transient noise 80 GHz



- Dev max: -1,4 ps
- Mean delay: 24,414 ps ± 426 fs.
- Jitter of Delays < 246 fs.
- Phase error < 174 fs ± 234 fs (after correction)

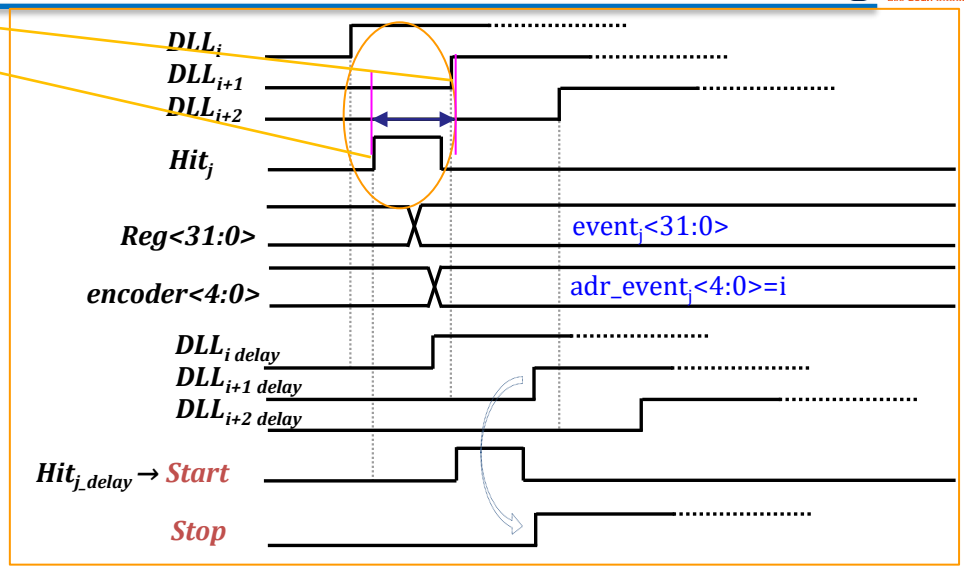


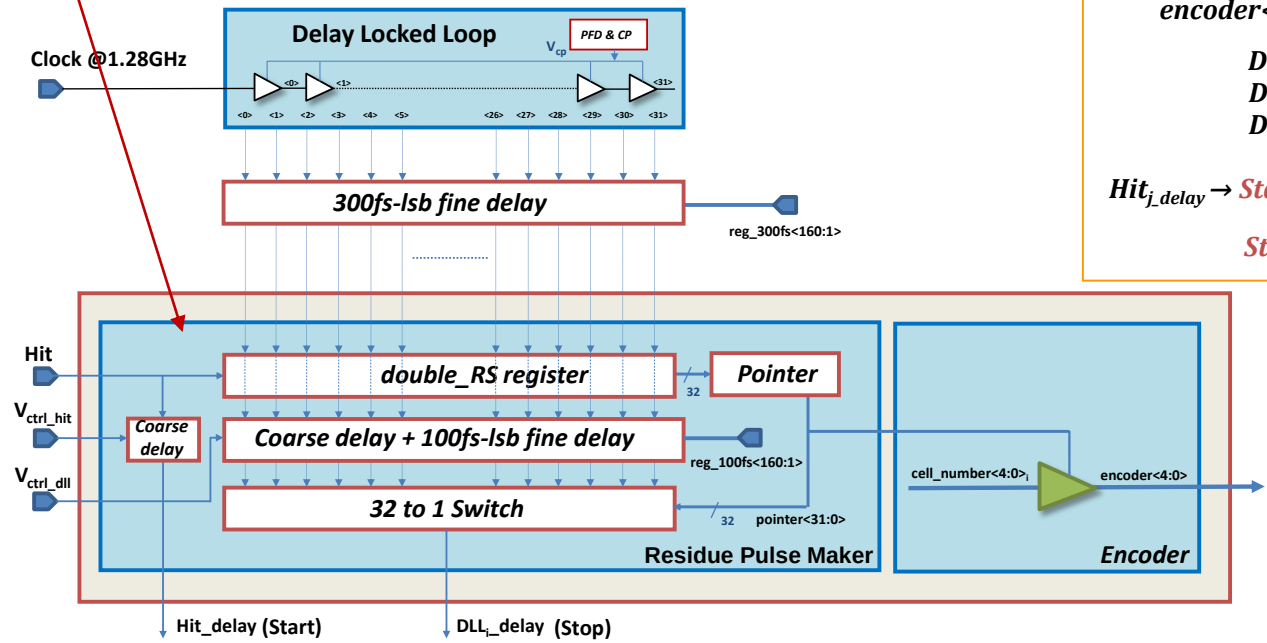


TDC 2nd stage of interpolation: DLL Residue Pulse Maker

The 2nd interpolation stage measures the **interval between** the **hit** and the **next DLL output** (this corresponds to DLL quantization error)

So, we need to a stage that generates this residue:
Residue Pulse Maker.



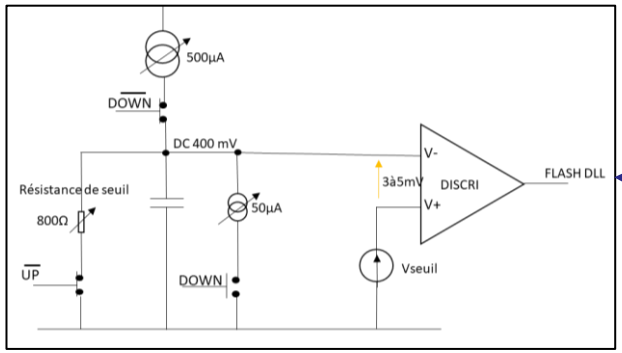


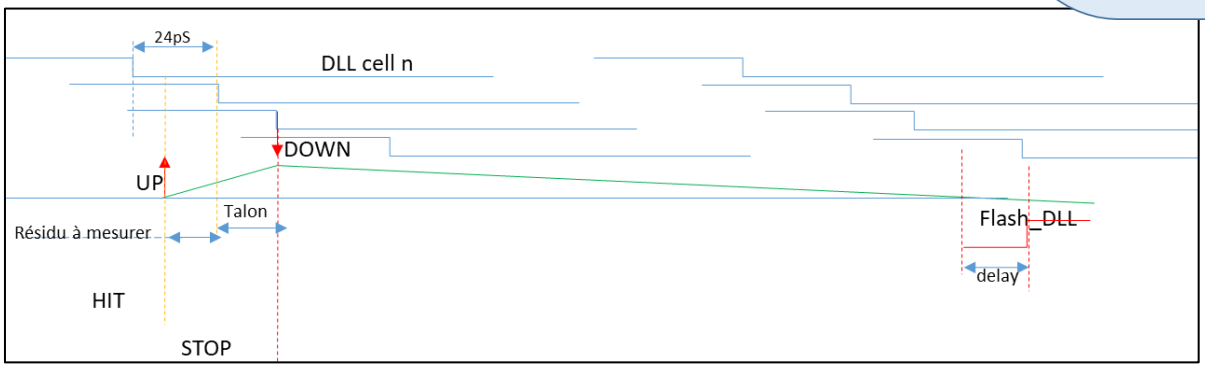
Functioning:

- Store the DLL state → delay the 32 DLL outputs → command a mux to select the desired DLL output.
- Inserting fine-tuning delays (100fs & 300fs on 5 bits):
  - Calibration and correction of the DLL DNL, ensure that the start arrives always before the stop of the TDC on the 2nd stage.
- **Very critical because the delay is greater than the duration of the input signal pulse (~390ps)**
- **Tuning range: 400ps to 680ps**

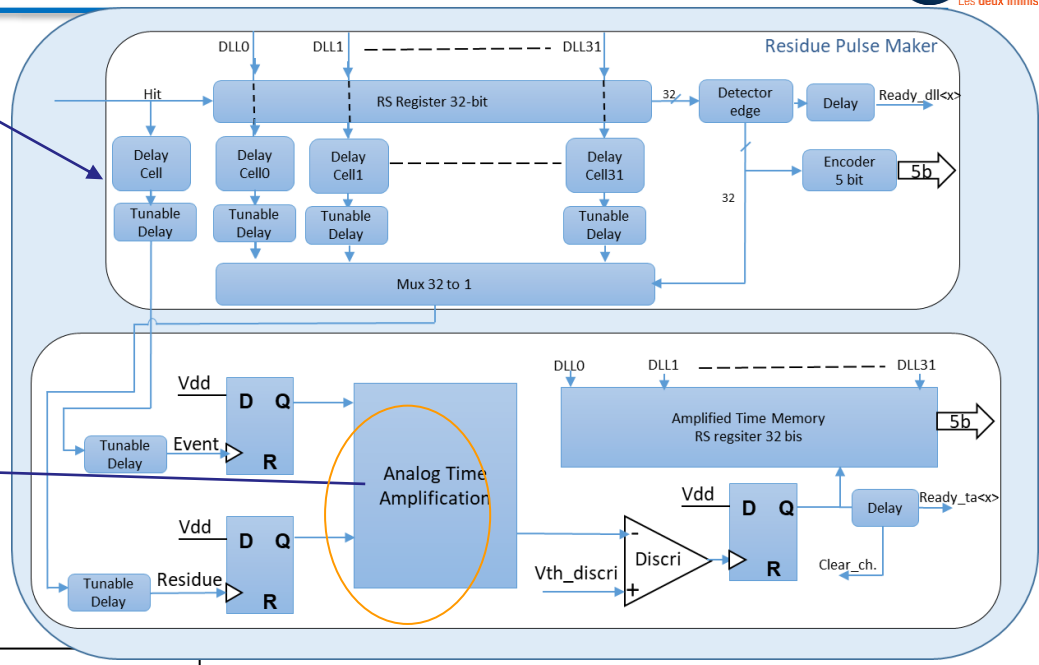
TDC 2nd stage of interpolation: Time-Amplification TDC

- The time-amplifier is based on a **dual ramp integrator**.
- Amplification factor: 10 adjustable with10b DAC controlled by I2C





RPM



➢ Simulation of RPM+TA :

- skill analysis program to automate simulations (results saved in a file)
- Data analysis is done offline
- A substantial calibration phase will be necessary

➢ Simulation of TA : transient noise

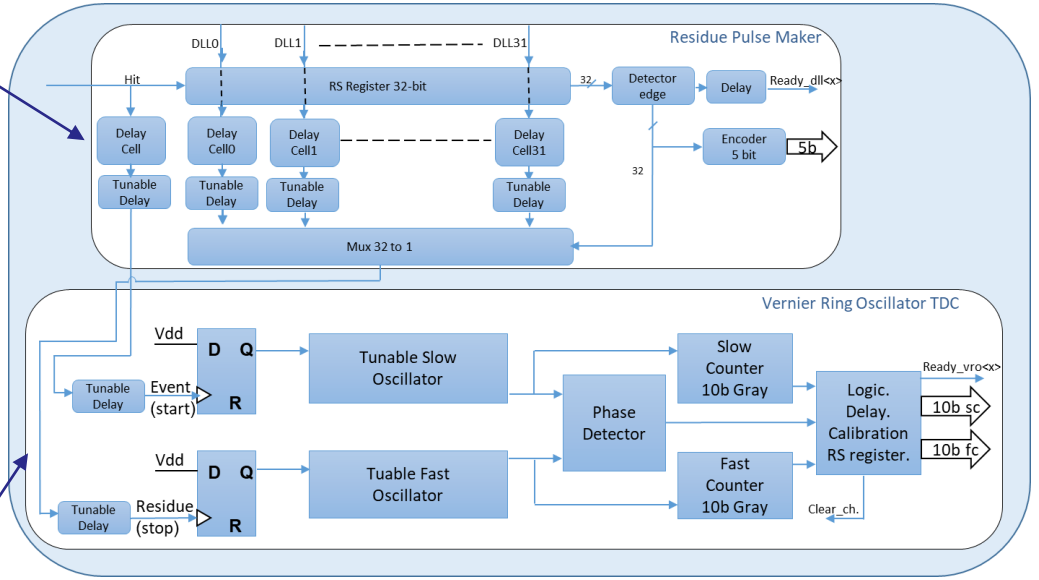
- Jitter of the output signal (flash_DLL) for a residue of 48ps => 14ps ptp (it corresponds to an equivalent jitter of **1,4ps** taking into account the amplification factor of 10).

TDC 2nd stage of interpolation: Vernier Ring Oscillator TDC

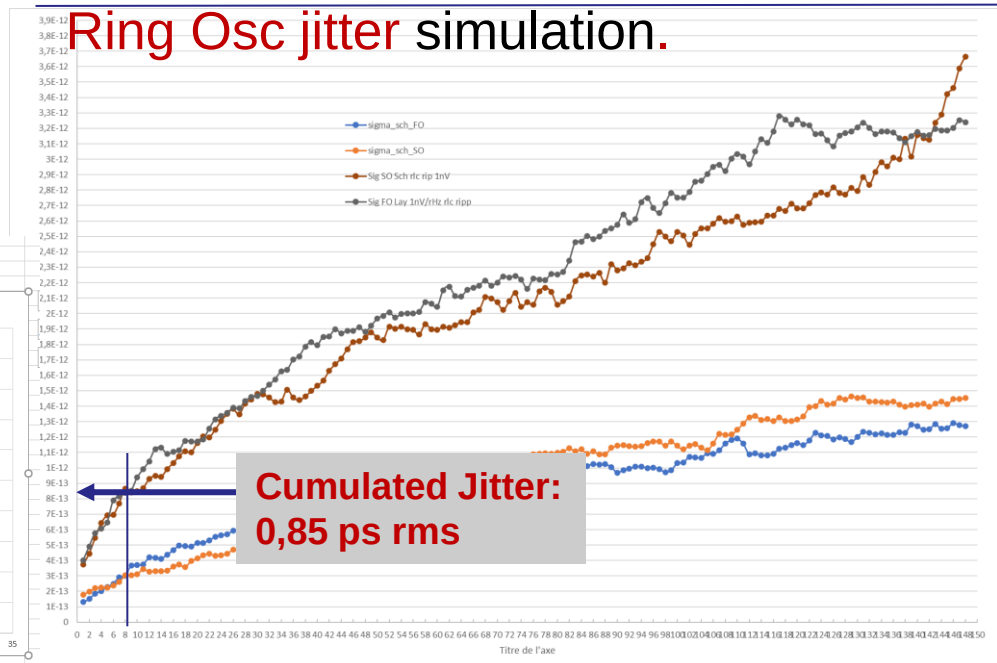
- The dynamic range of the Vernier input signal is 24 ps (quantization step of the DLL)
- The LSB of the Vernier TDC is set to 3 ps: to ensure that the quantization noise (lsb/sq.root12) is less than 1 ps rms
- The slow and fast oscillators run at ~1ns period with a difference of 3 ps between the two (LSB).
- The maximum conversion time is (24ps/3ps)*1ns= ~8ns
  - Dead time constraint <10ns (satisfied).

RPM

VRO TDC

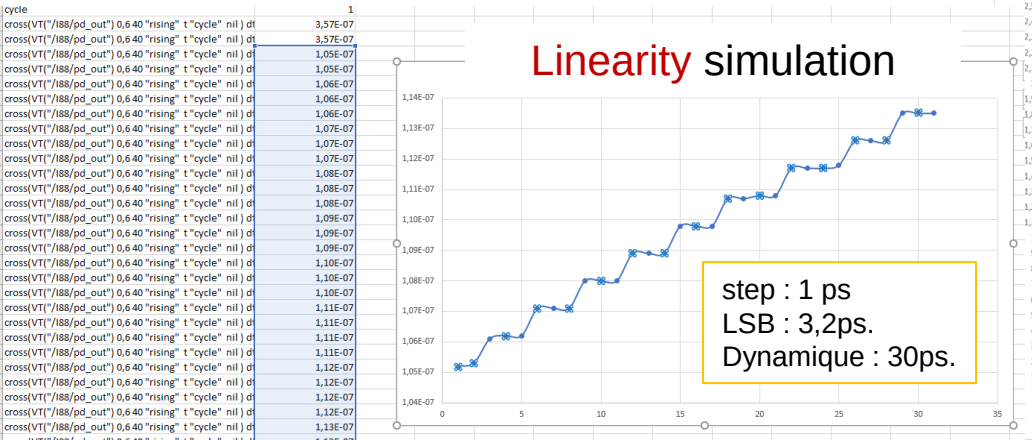


Ring Osc jitter simulation.



Cumulated Jitter: 0,85 ps rms

Linearity simulation

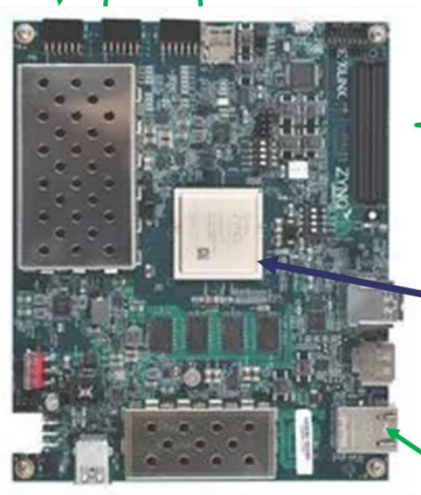


step : 1 ps
LSB : 3,2ps.
Dynamique : 30ps.

Testbench : Material description

PMOD : 5 I/O including one I2C link

2x PMOD : 12 I/O



FMC LPC :

- 64 single-ended or 32 LVDS signals
- 2 clock I/O
- 2 GTH links (multi-gigabit)

SoC Zynq:

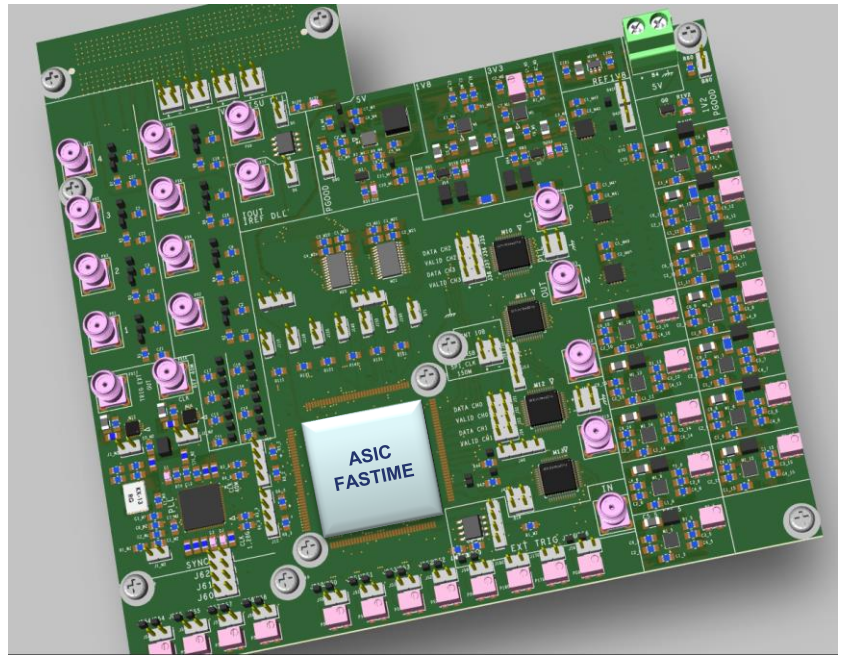
- 4 Cortex A53 processors
- 1 Cortex A42 processor
- LUT
- BRAM
- DSP

Ethernet Base100/1000

Liaison USB:

- JTAG (configuration)
- Processor console

ZCU104 Evaluation Board and its Useful external functions (LP2I Bordeaux)

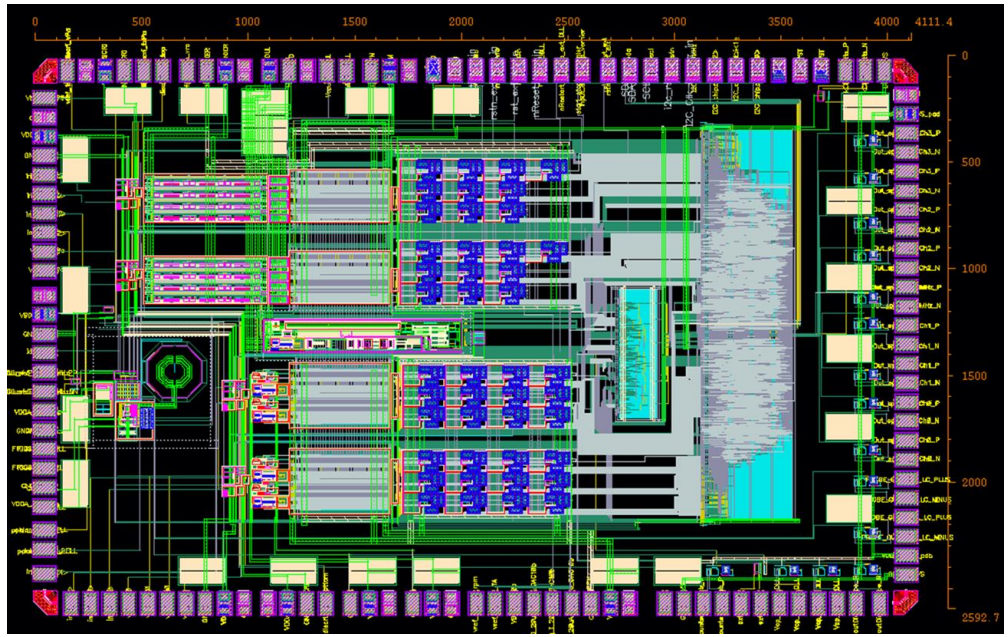


Analog mezzanine card (3D image generated by cadence tool - LPC Clt)

Test Software and User Interface is under development (LP2I Bordeaux)

Conclusions & perspective

- FASTIME : an R&T started on January 2021 for a duration of 3 years.
- FASTIME is a collaboration between 6 IN2P3 laboratories:
  - IJCLab, IP2I Lyon, LP2I Bordeaux, LPC-Caen, LPC-Clermont et Omega
  - Synergy and Sharing of designs and expertise (SOS software, periodic meetings, atrium, the in2p3 box, etc.)
- La phase 1:
  - A 4-ch prototype was fabricated in TSMC130nm process on November 2022
  - Testbench is ongoing and tests will start by September 2023



- Phase 2:
  - Selection and integration of the most performant architectures and options that have been evaluated in phase 1.
  - Design of a final prototype : foundry submission is foreseen at the end of Q2 of 2024.

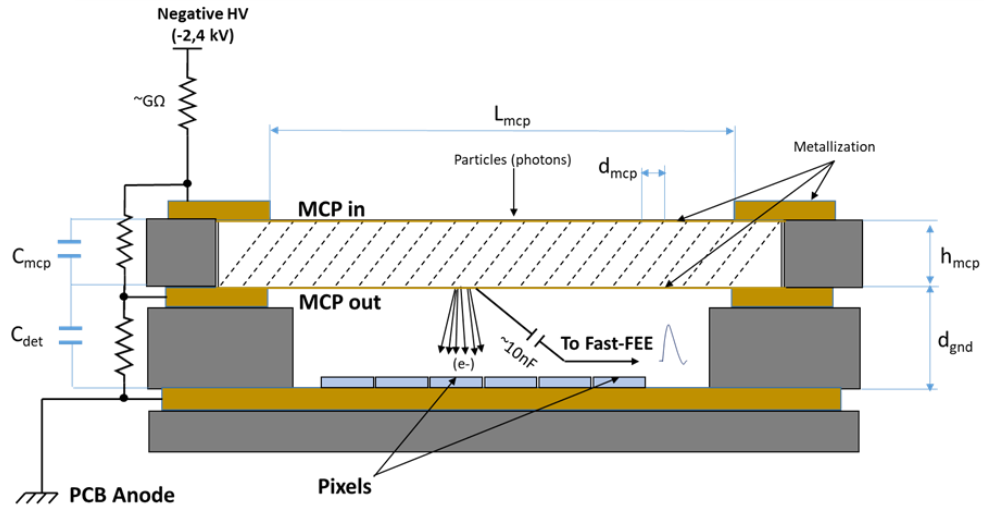
Perspectives beyond FASTIME:

Migrating this design to thinner process nodes (ex 65nm, 28 nm) could improve its speed and resolution.

Thank you for your attention

Backup slides

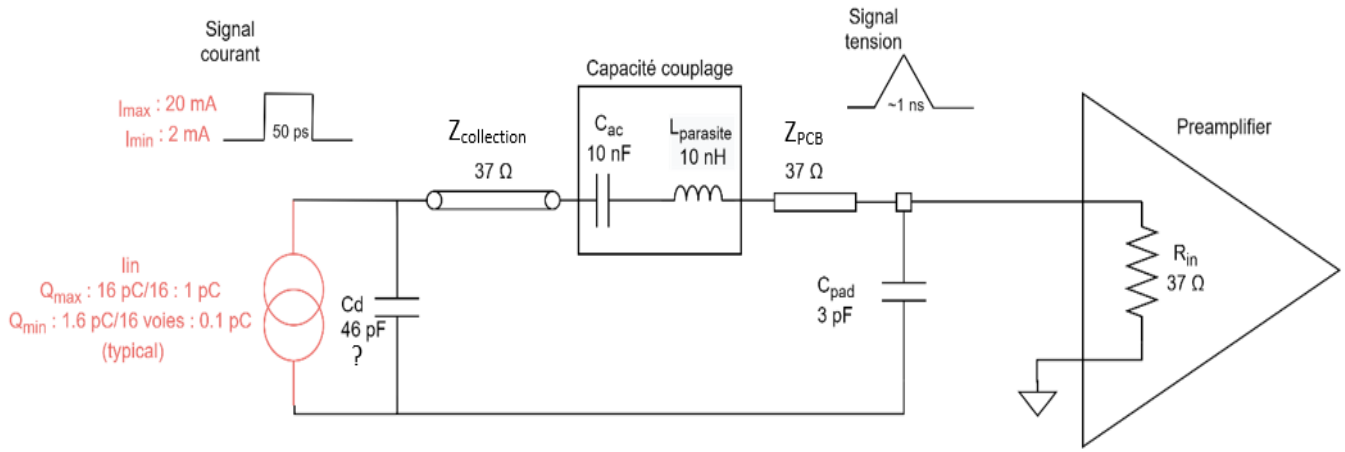
Detector & specifications: electrical model of PICMIC detector



Simplified diagram of the PICMIC setup

L_{mcp}	2.5 cm
h_{mcp}	--
d_{gnd}	0.6 mm
d_{mcp}	2.5 µm
C_{mcp}	**35 pF**
C_{det}	**11 pF**

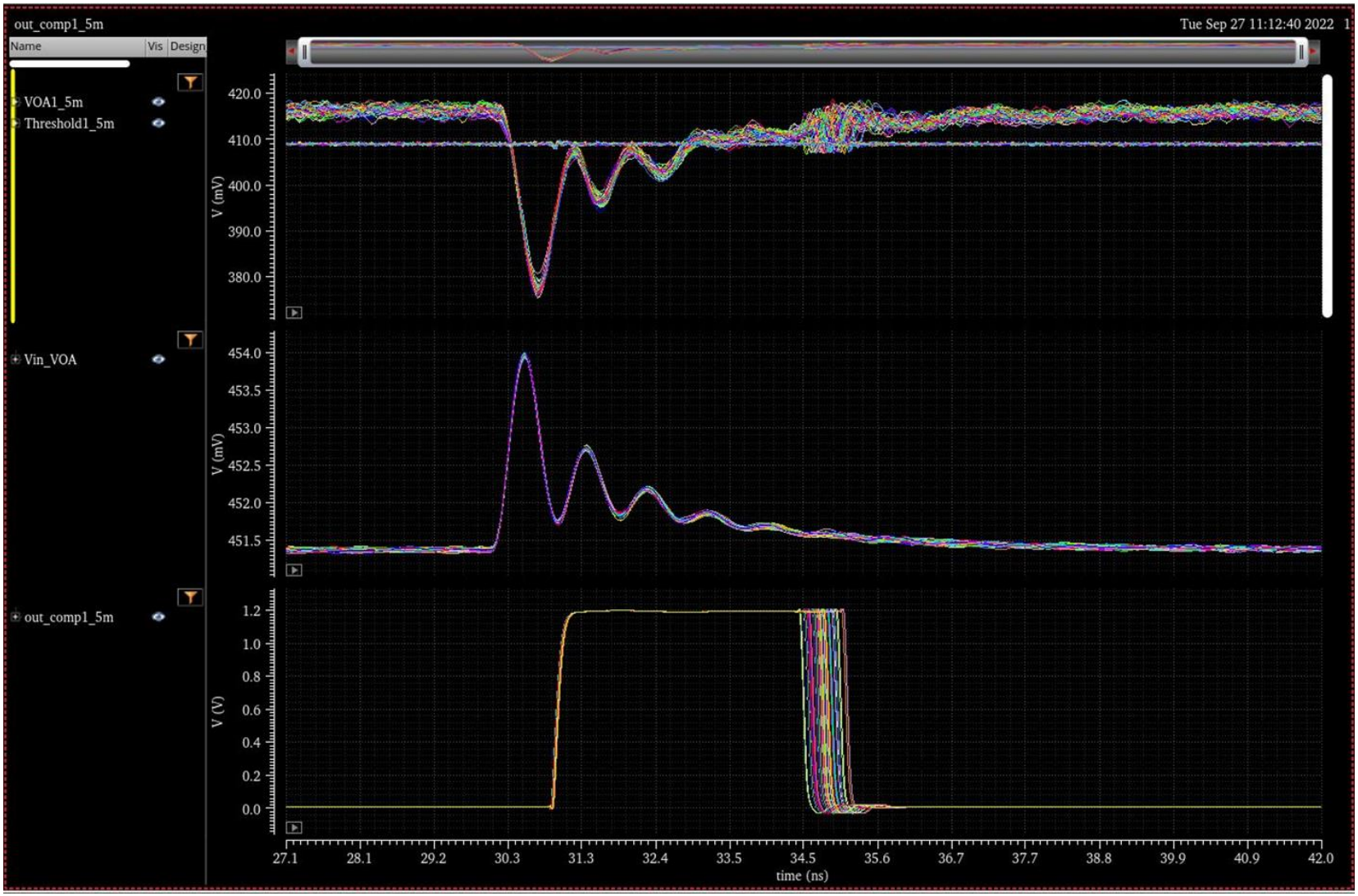
measured characteristics of a channel of the picmic timing sensor



Electrical model of PICMIC detector seen by front end

Jitter of VPA+Discri

av_extracted TR noise (50 IT), Vth = - 10 mV



Jitter of TZ-PA+Discri

av_extracted TR noise (50 IT), Vth = - 30 mV