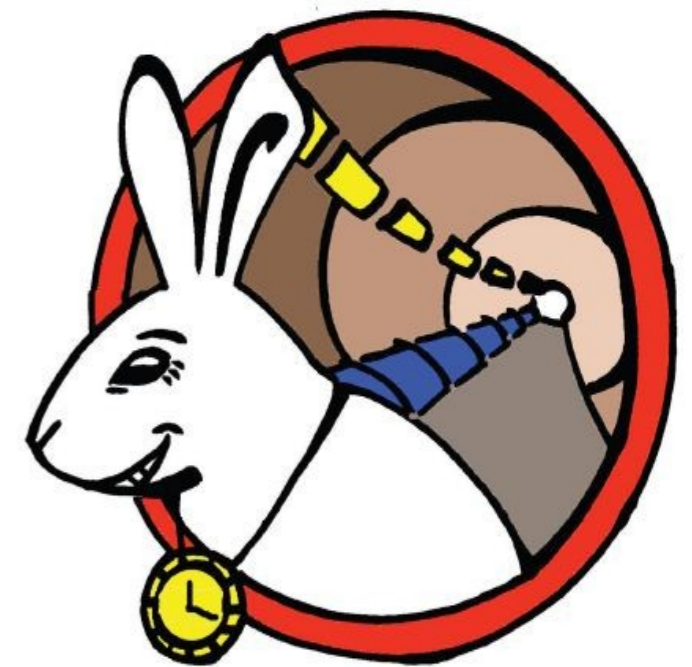


The WhiteRabbit & The R & T TIMED

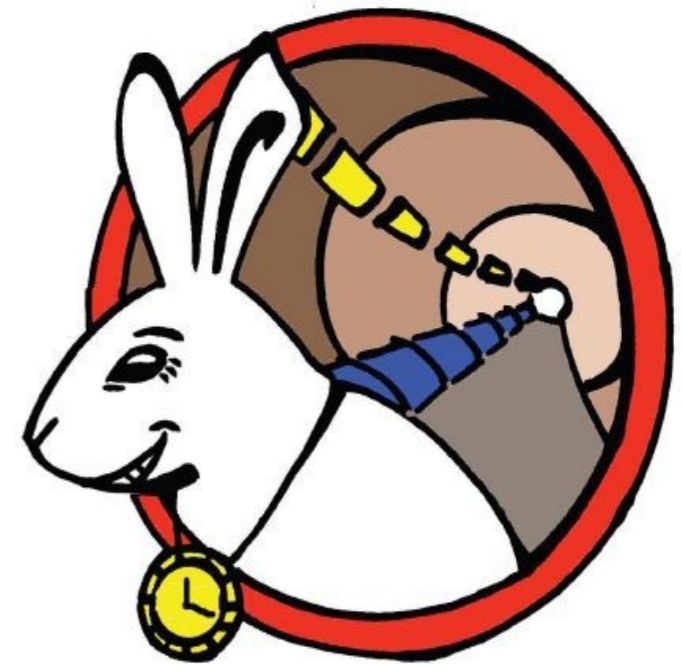


Antoine Back, Chafik Cheikali, **Daniel Charlet**, Eric Plaige, Paul-Eric Pottie,
Monique Taurigna, Cédric Viou

Outline

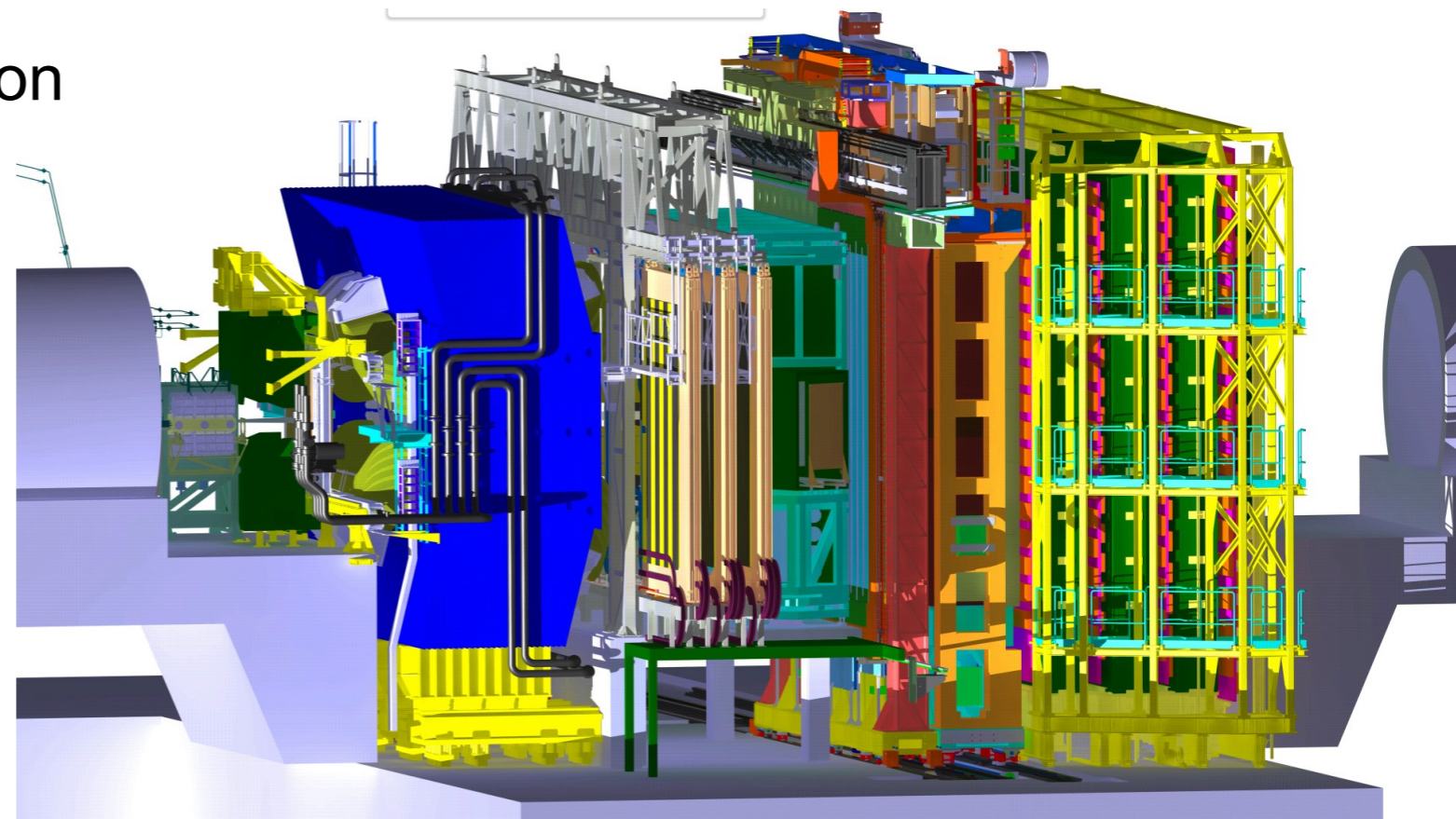
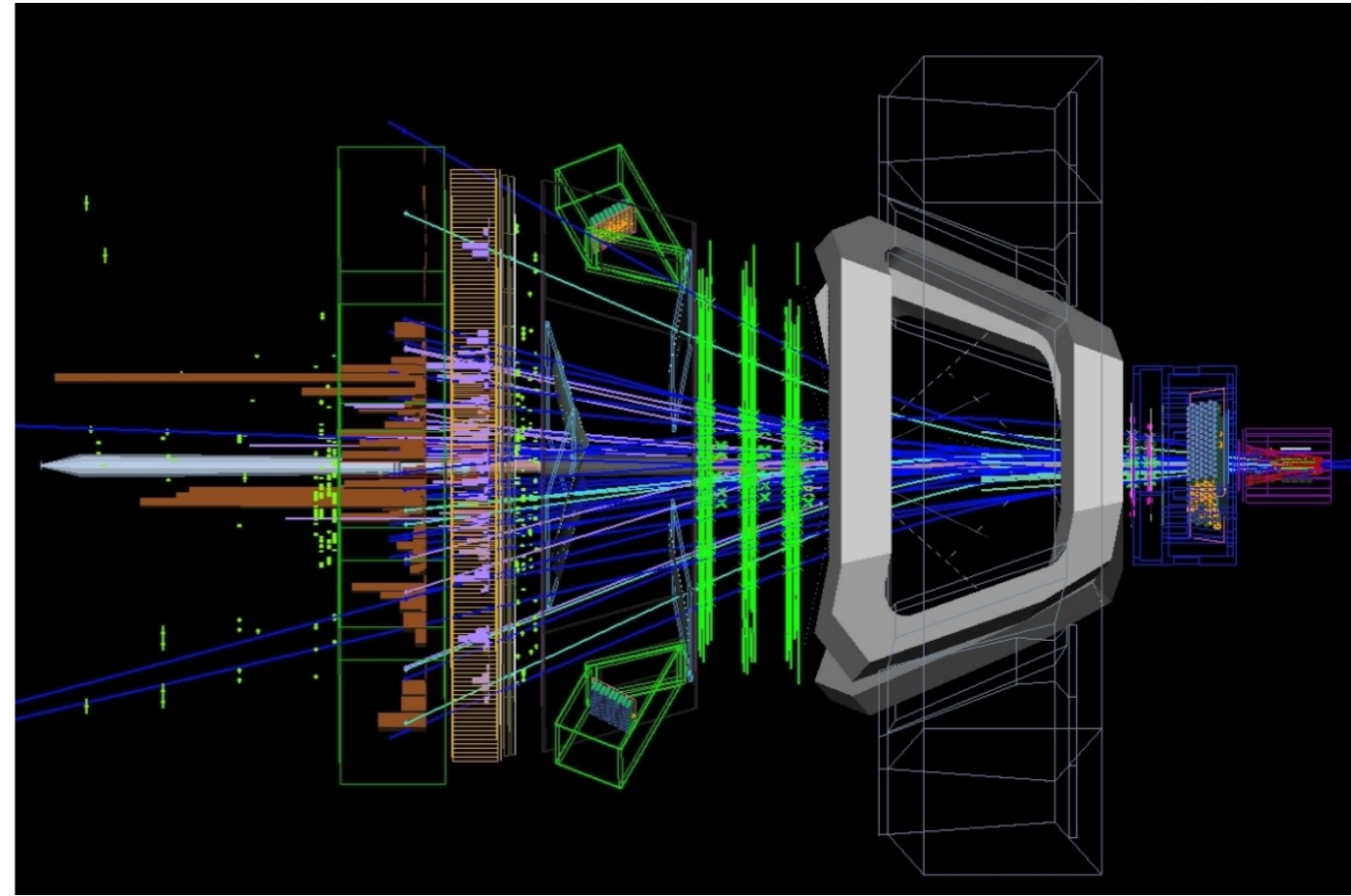
- WhiteRabbit promising sector
- WhiteRabbit theory of operation
- System WhiteRabbit
- WhiteRabbit enhancement : R & T Timed

White Rabbit



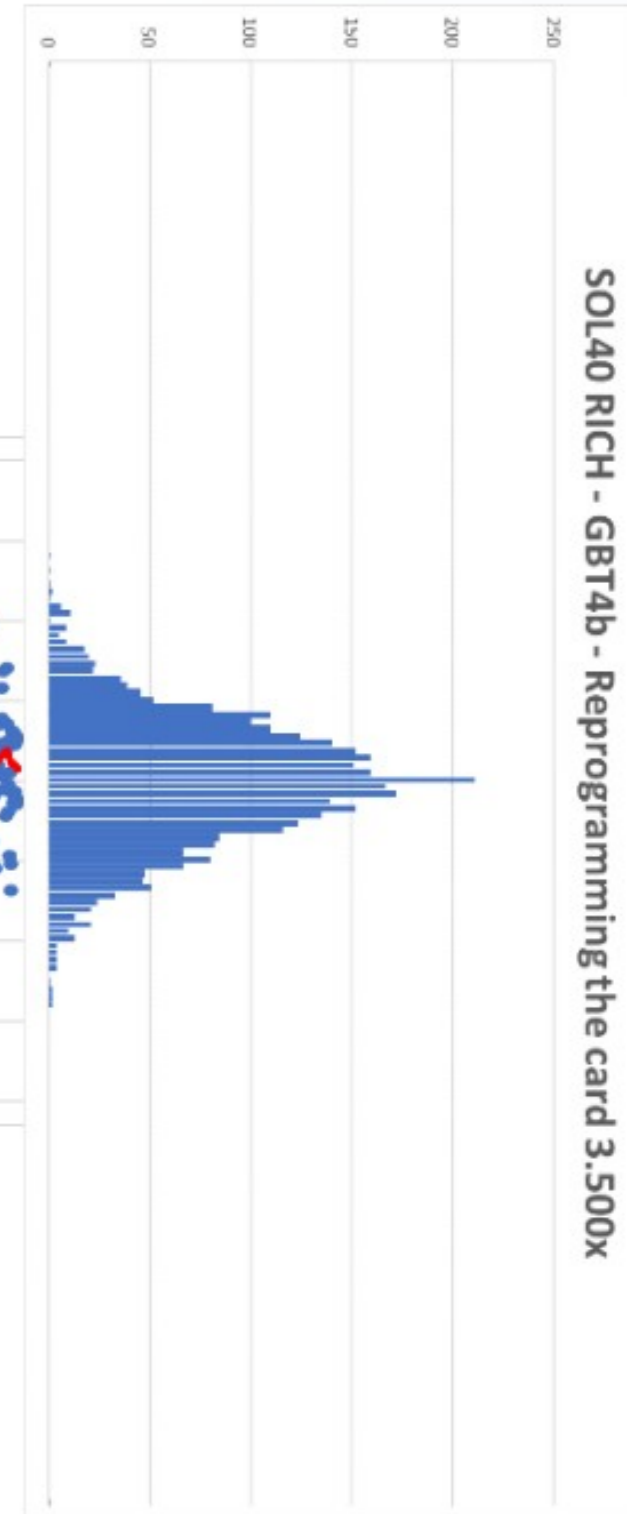
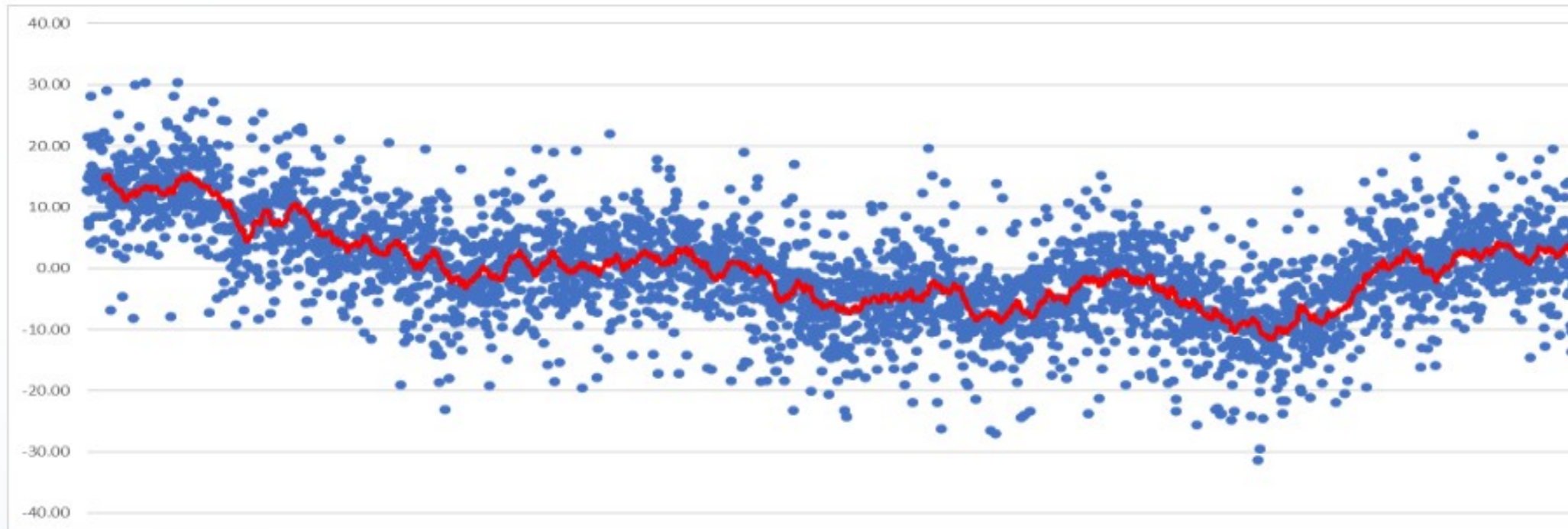
WR Motivations : Multi-detectors LHCb

- LHCb detector
- 7 sub-detectors
- 20m x 20m
- Further million of acquisitions chanel
- All systems must be synchronize with the same clock (40MHz)
- A complex and long calibration time is mandatory
- Clock drift during physic aquisition



Clock drift over time

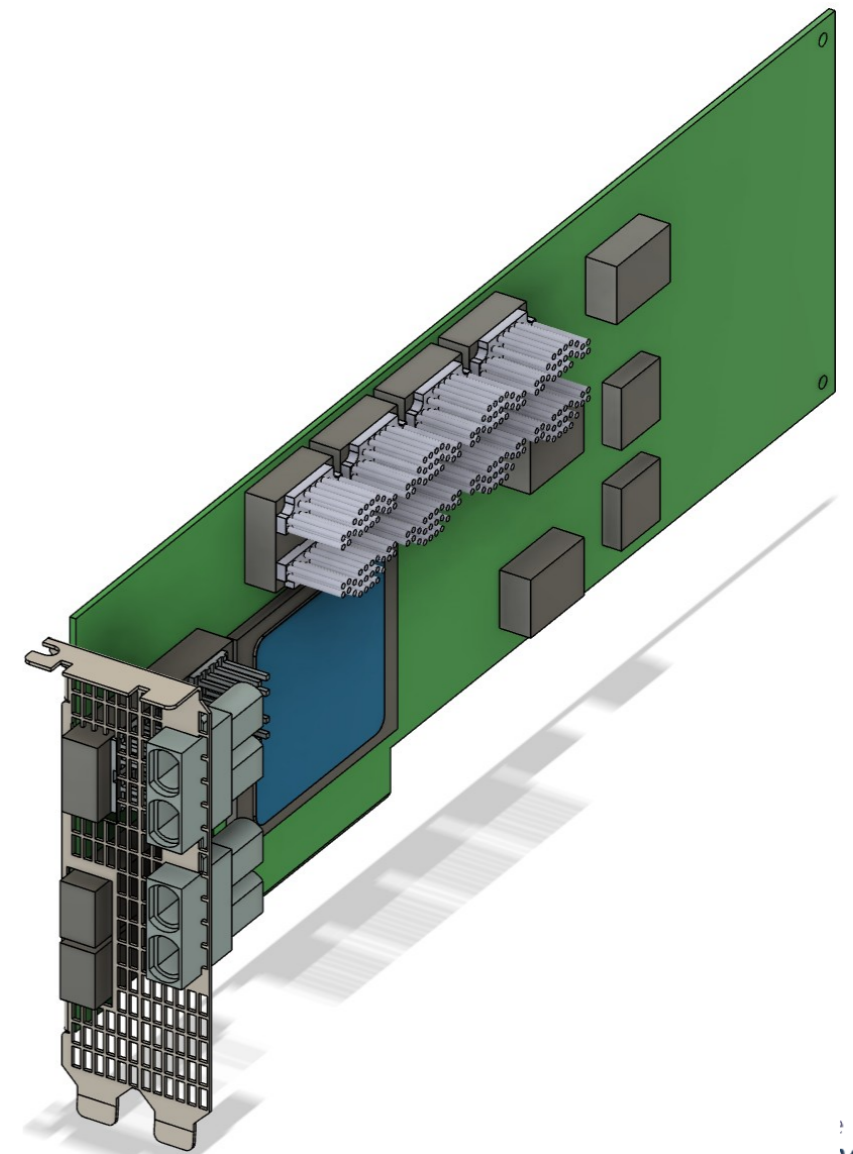
SOL40 RICH – GBT4b – Reprogramming SOL40 3500x
 Over 5 days of test
 Center of recovered clock distribution drifted over ~25ps
 Most likely due to temperature



The resolution of the SOL40 PLL shift is ~100ps

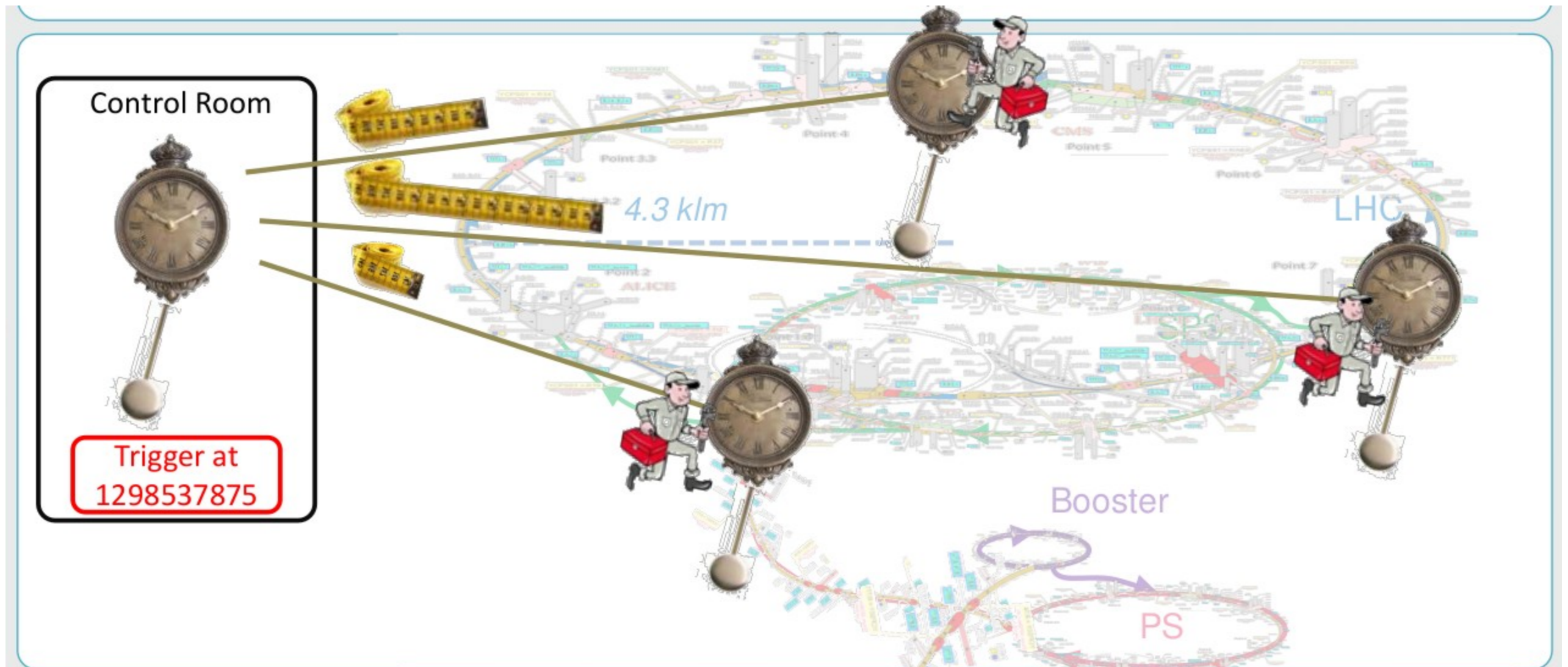
WR Motivations : Multi-detectors PCIE400

- Data acquisition and event formatting board for the futur LHC upgrade
- More than to 500 boards for a detector
- WhiteRabbit clock distribution (5ps)
- Foreseen characteristics
 - ▶ Agilx7 M-series AGMF039R47A1E2V
 - ▶ No DDR memory
 - ▶ Use of PC RAM or HBM2e instead
 - ▶ Up to 48x26Gbps NRZ for FE
 - ▶ PCIe Gen 5 / CXL or 400GbE
 - ▶ Low jitter PLL < 100 fs RMS
 - ▶ White Rabbit clock distribution (3ps/13ps) (SFP+)



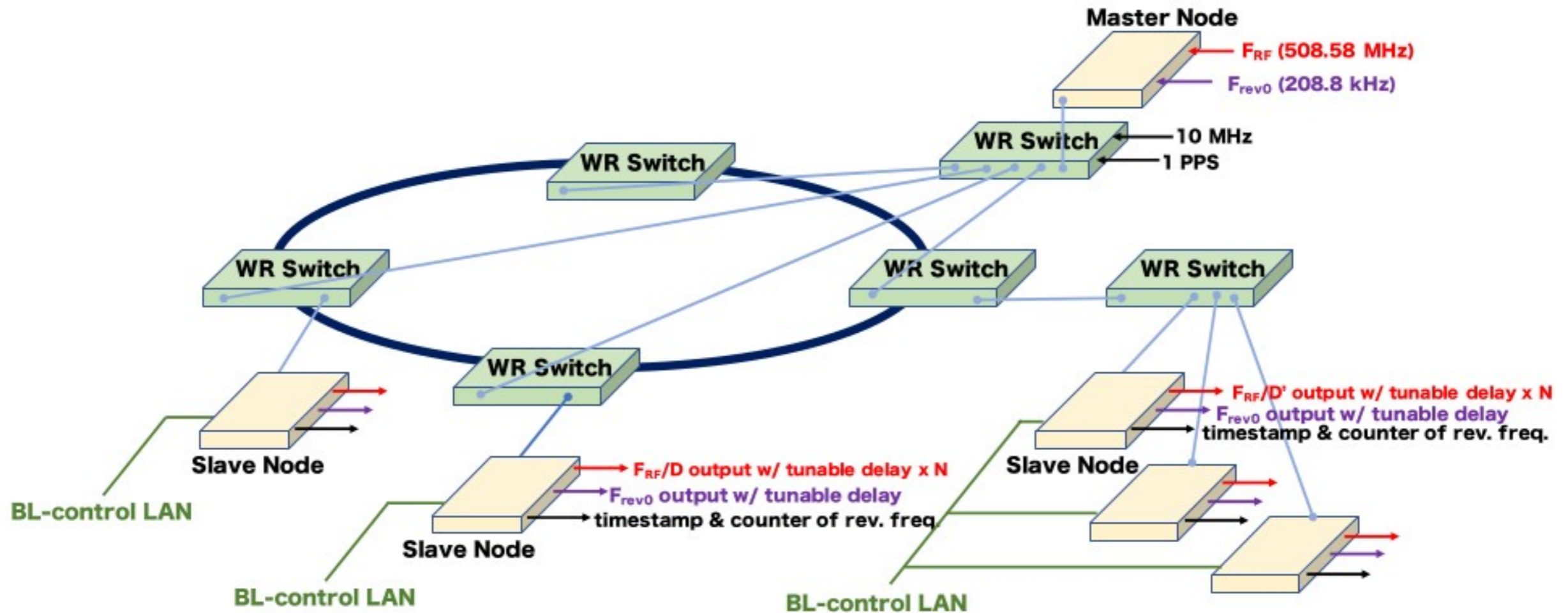
Accelerator : Master oscillator distribution

- Real-timed communication system : tight time constraints
- Long distances between nodes : long transmission delays
- Numbers of nodes : several hundred
- Dynamic changes to the numbers of nodes : not easy



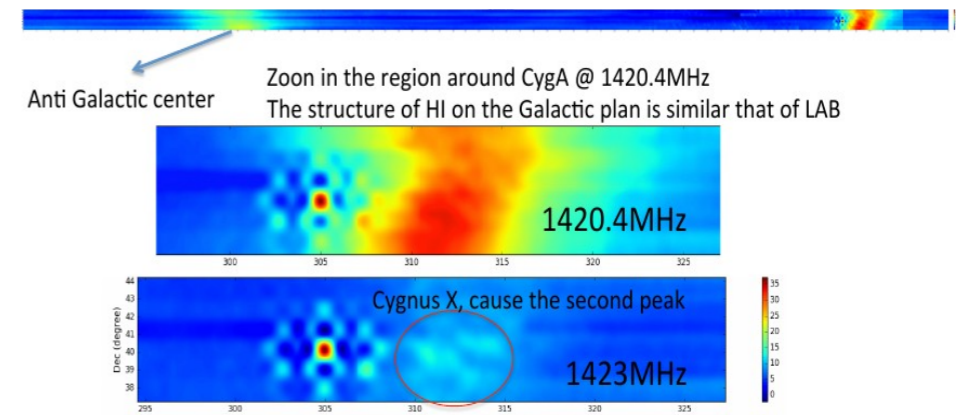
Accelerator : Master oscillator distribution

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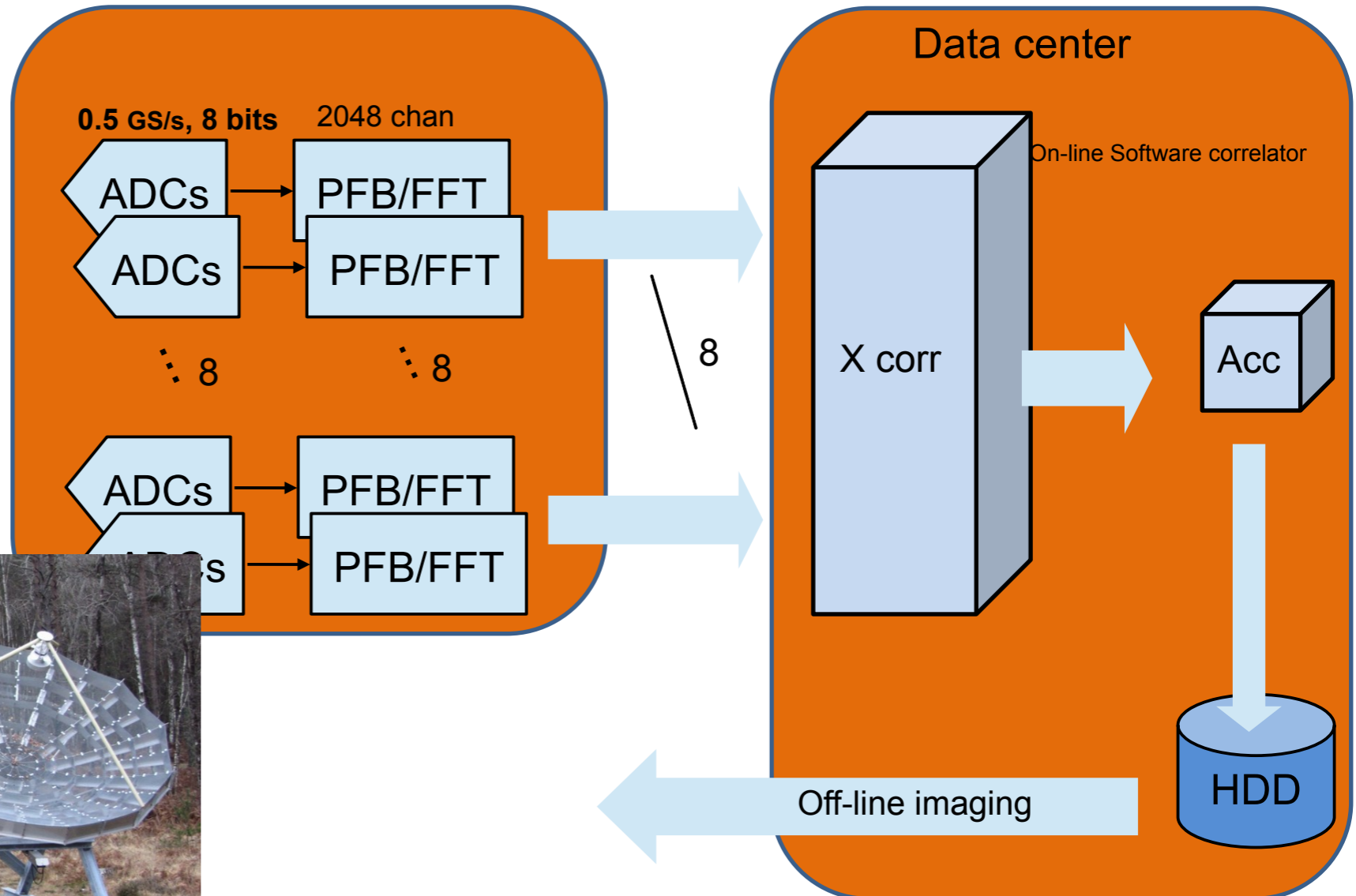
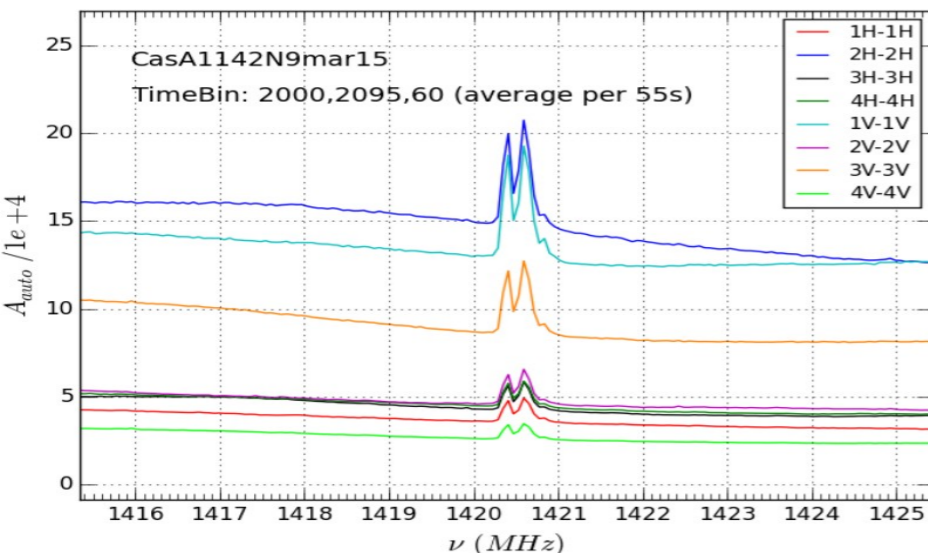


WR motivations : Radio astronomy PAON IV

Radio telescope demonstrator for mapping in 3D of the atomic hydrogen in the universe

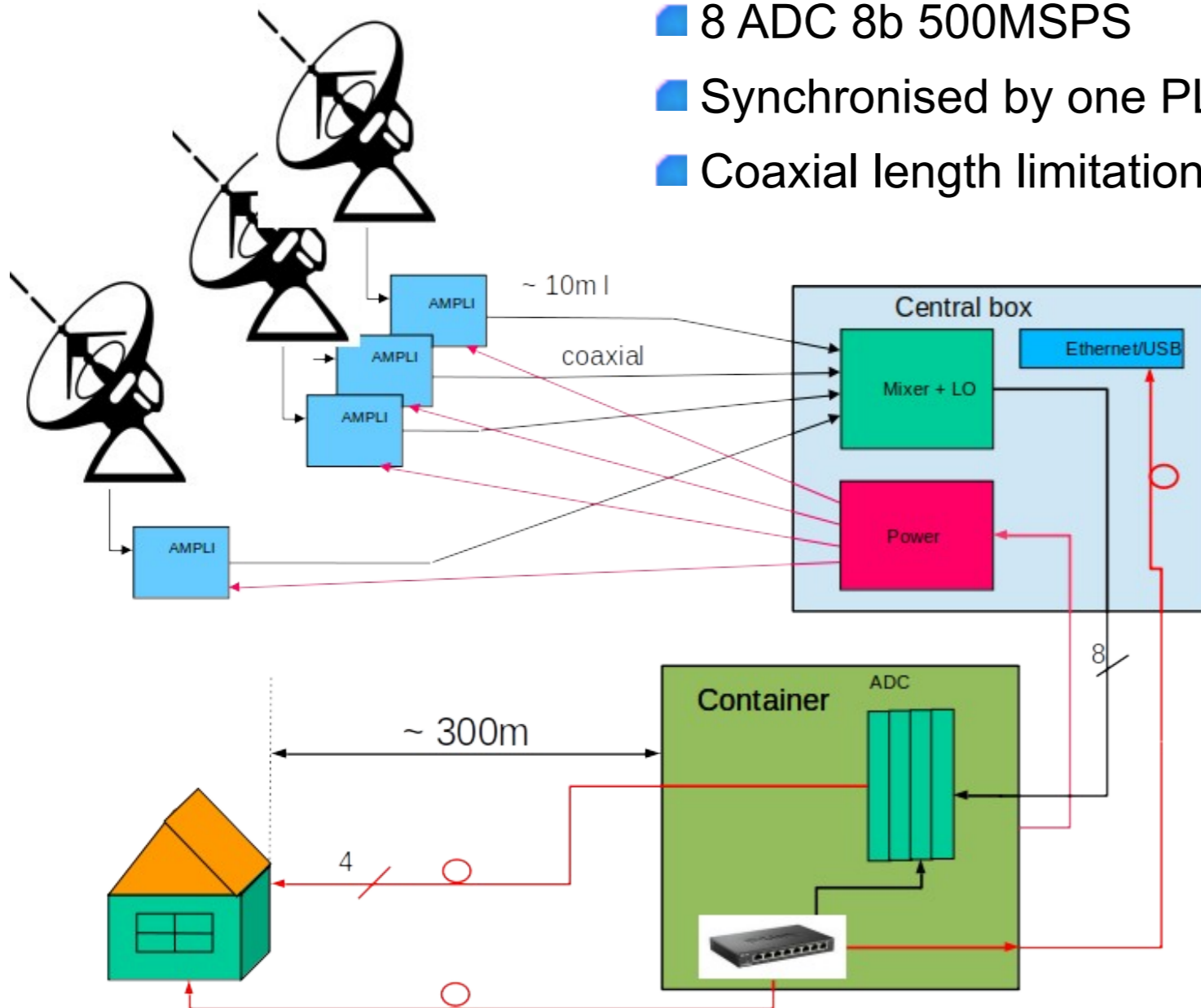


shelter

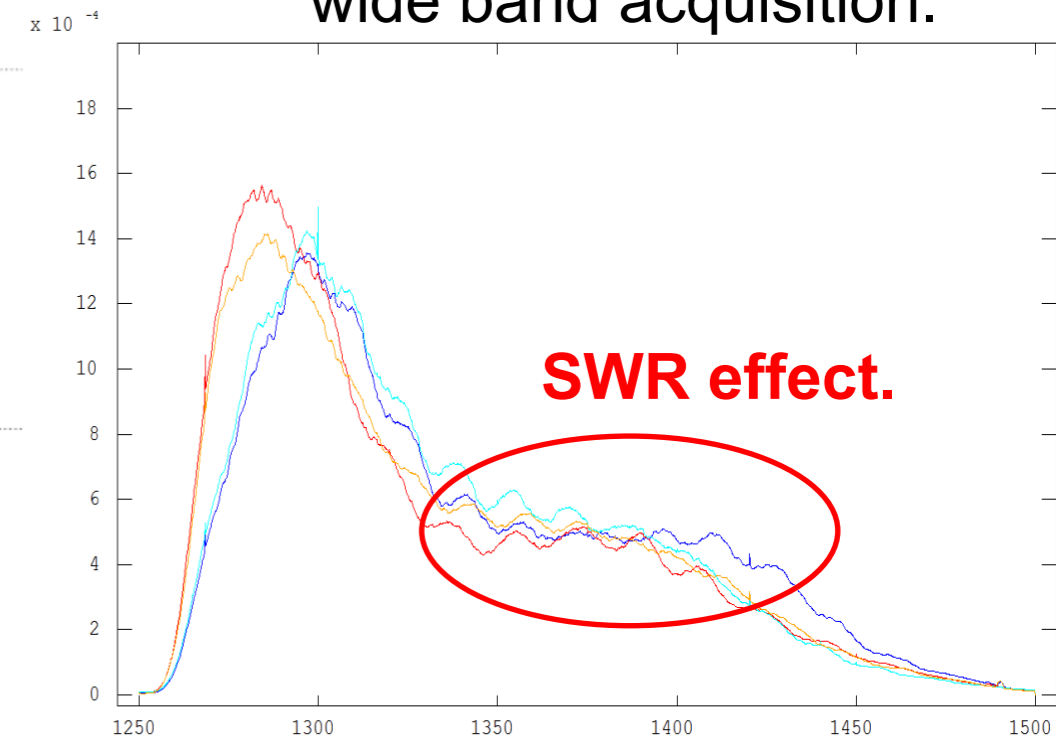


PAON IV : previous architecture

- Interferometer 4 radio dishes of 5m
 - Centralized coding architecture
 - High bandwidth : 250MHz
 - 8 ADC 8b 500MSPS
 - Synchronised by one PLL
 - Coaxial length limitation

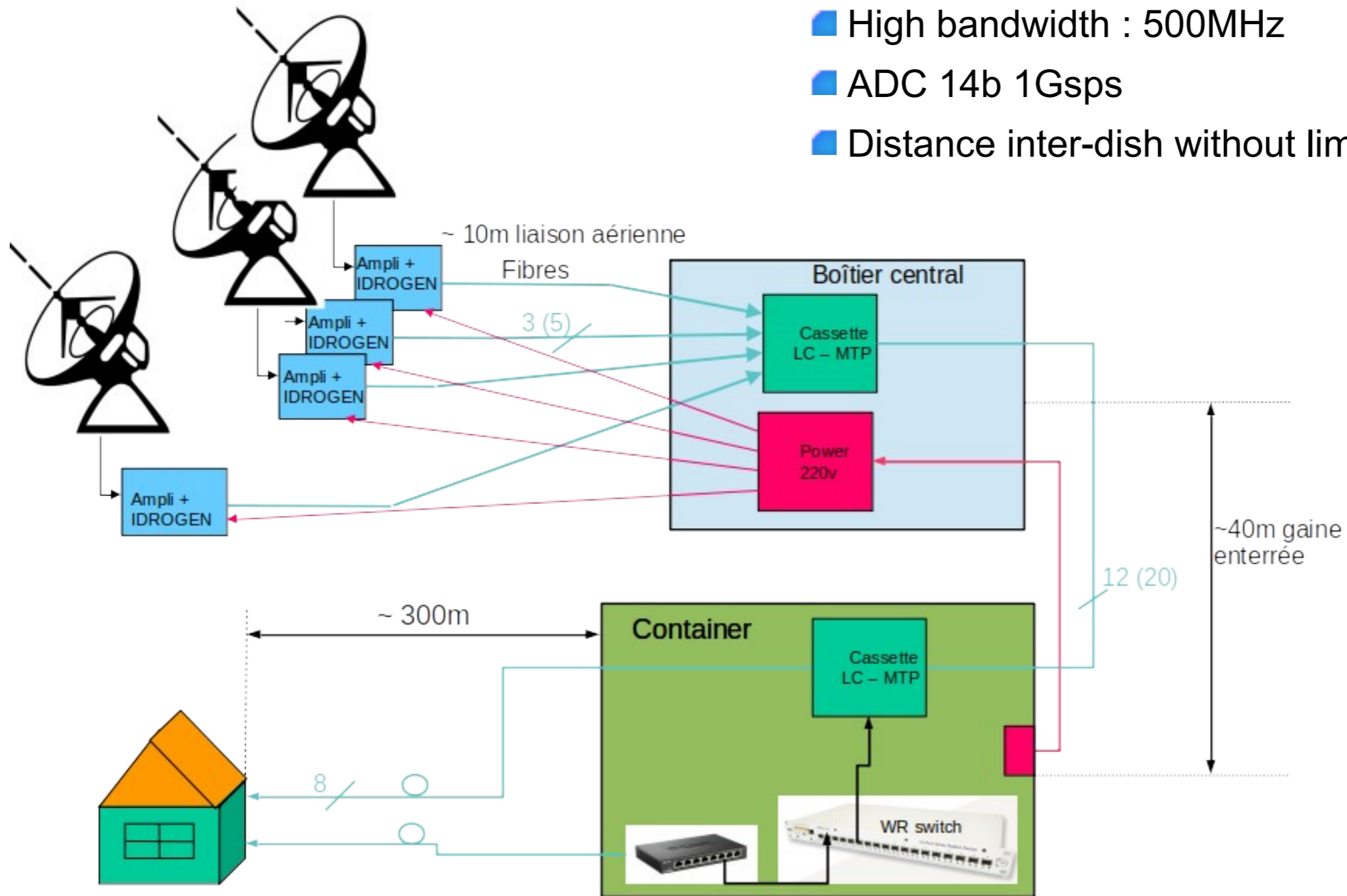


SWR depends of:
RF cable length,
Adaptation mismatch,
wide band acquisition.

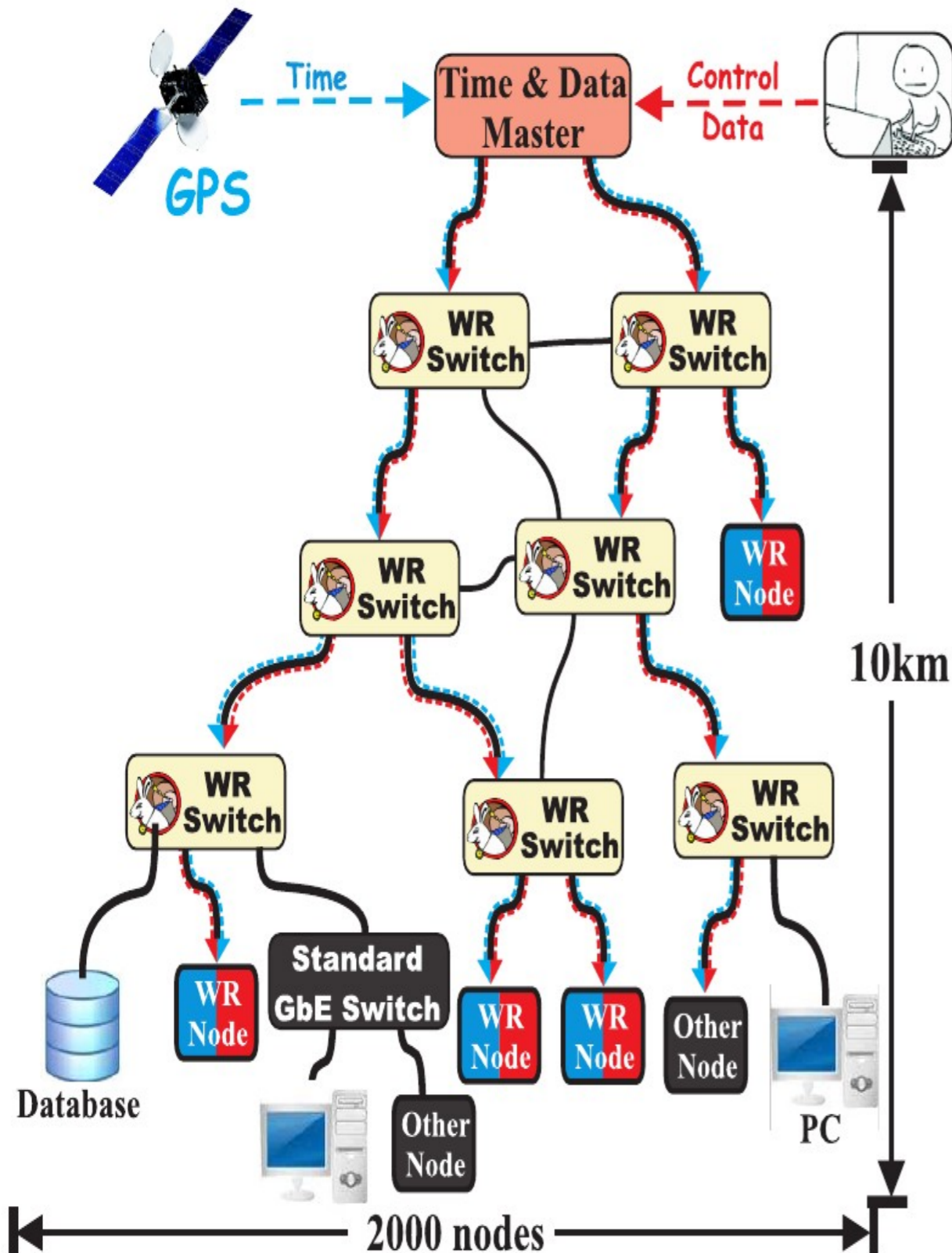


PAON IV : new architecture

- Interferometer 4 radio dishes of 5m
 - Synchronised by the WhiteRabbit
 - High bandwidth : 500MHz
 - ADC 14b 1Gsps
 - Distance inter-dish without limitation

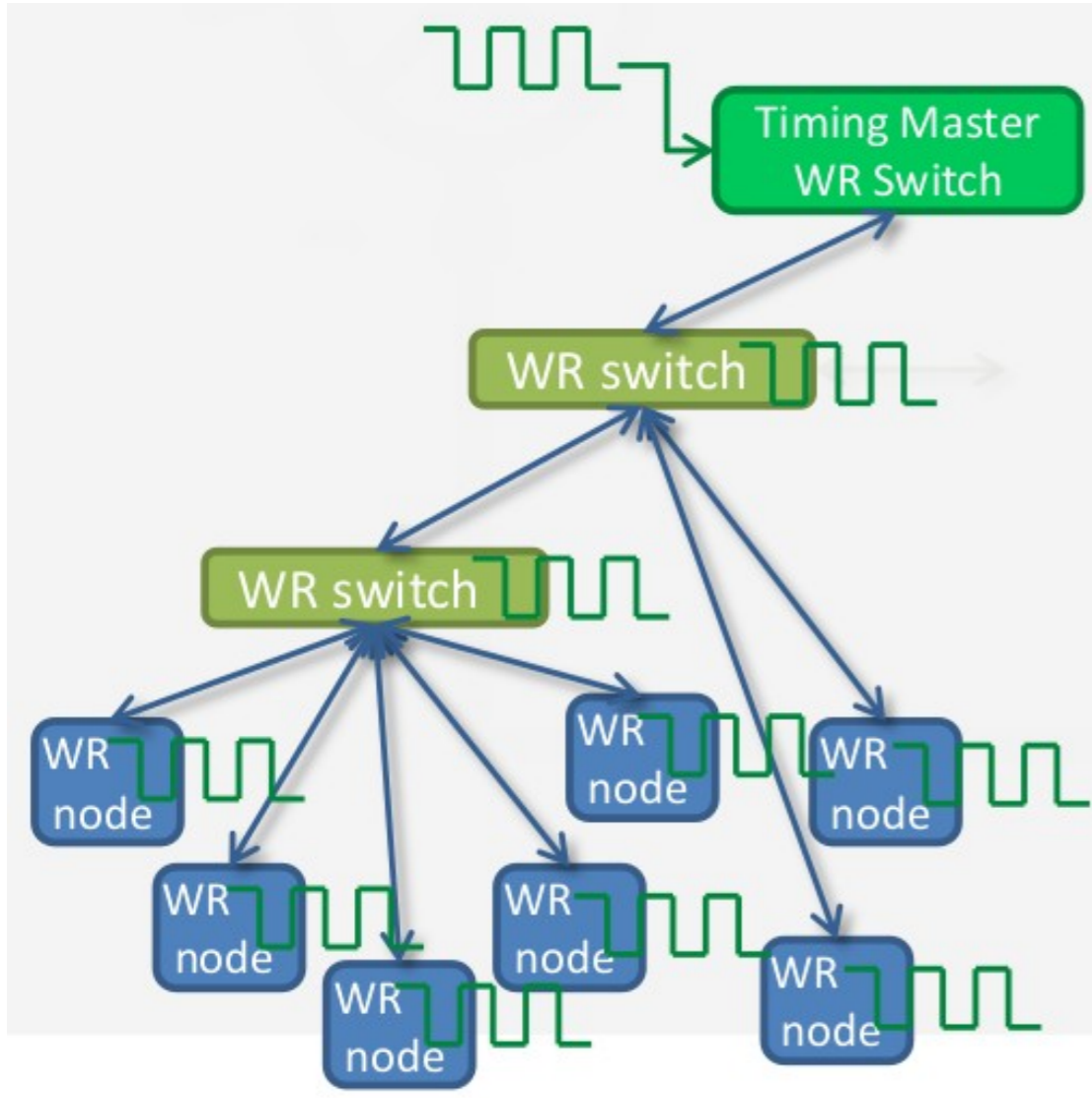


White Rabbit principle : Enhanced Ethernet



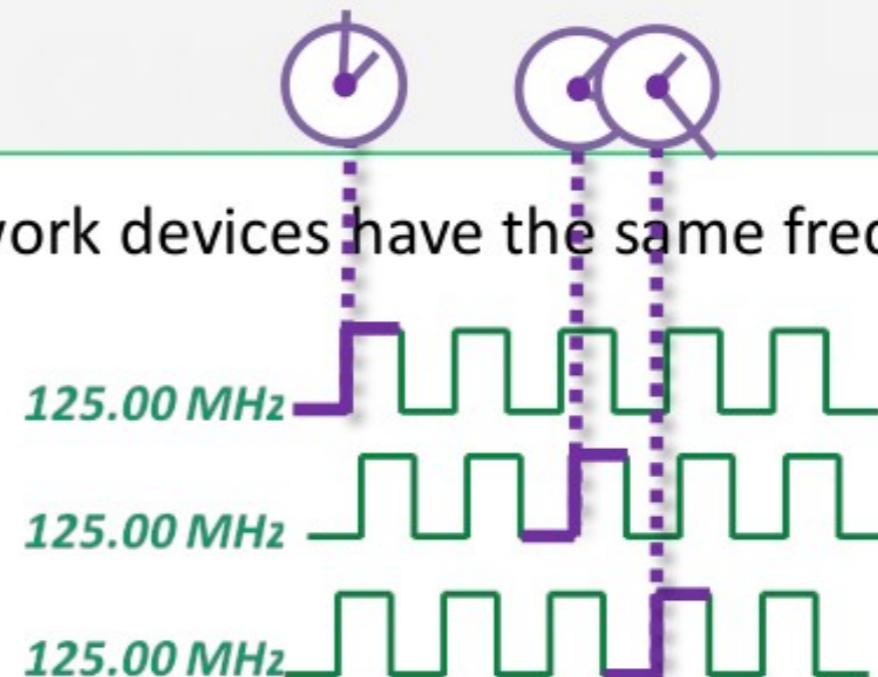
- An extension of Ethernet which provides :
 - Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
 - Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.
- Technology overview
 - Precision Time Protocol (IEEE1588)
 - Synchronous Ethernet
 - DDMTD Phase tracking (Digital Dual Mixer Domain) ...
- Delivering signal :
 - Clock : usually 10MHz ;
 - $80\text{MHz} < \text{IDROGEN} < 3\text{GHz}$ (LMK4828)
 - Pulse per seconde
 - Temps Atomic International (48b)

Synchronous Ethernet (Sync-E)

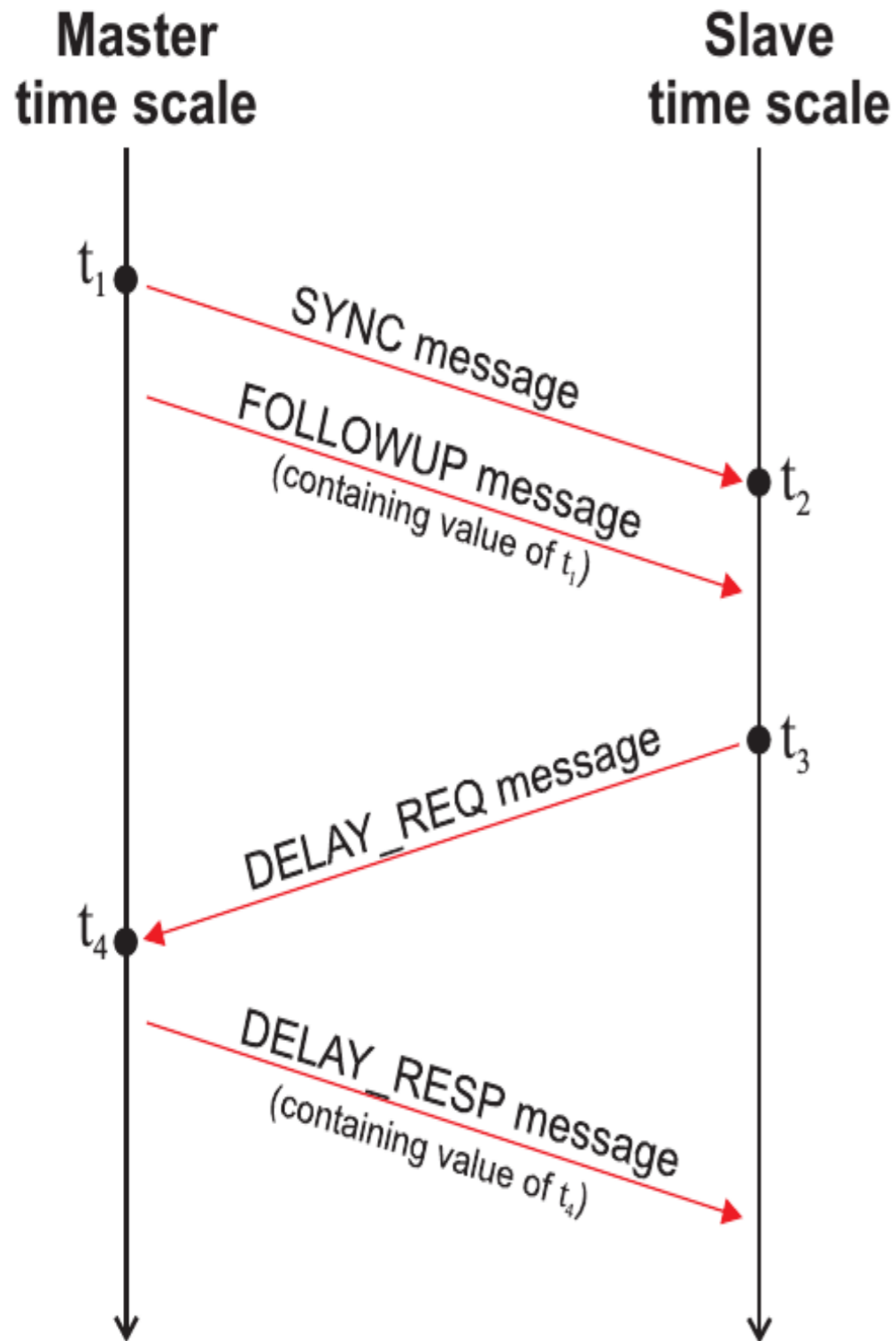


- All network nodes use the same physical layer clock,
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip(PHY)
- A master and unique clock for the whole network
- Synchronous digital hierarchy
- High precision clock definition, 20 better than standard Ethernet clock

○ All the network devices have the same frequency!



Precision Time Protocol (IEEE1588)



- Packet-based synchronization protocol
- Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.
- Link delay evaluated by measuring and exchanging packets tx/rx timestamps
- PTP is used only for compensation of the clock offset

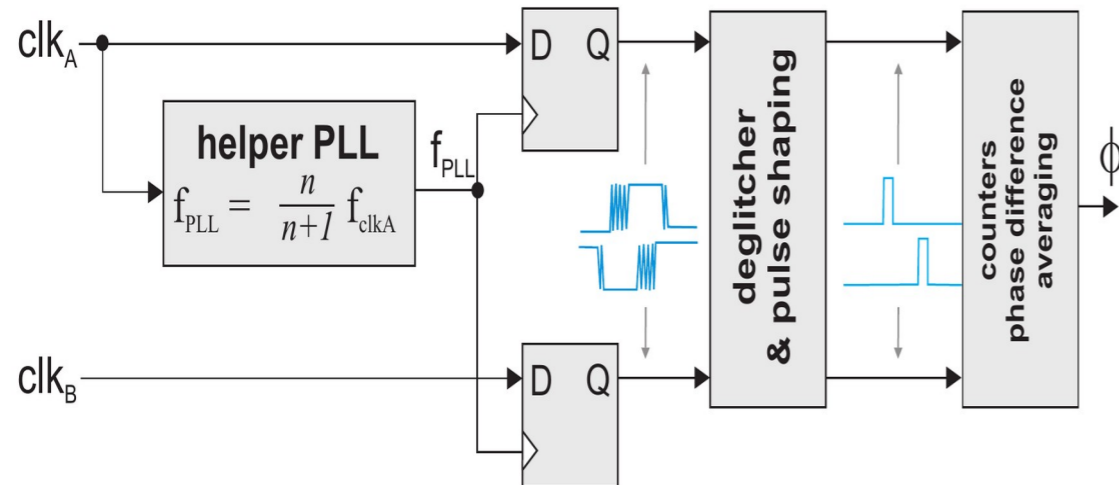
Having values of $t_1 \dots t_4$, slave can:

- calculate one-way link delay:

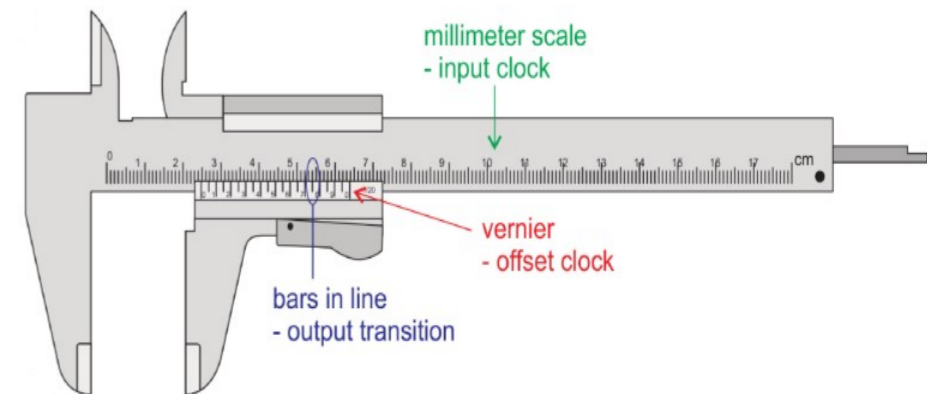
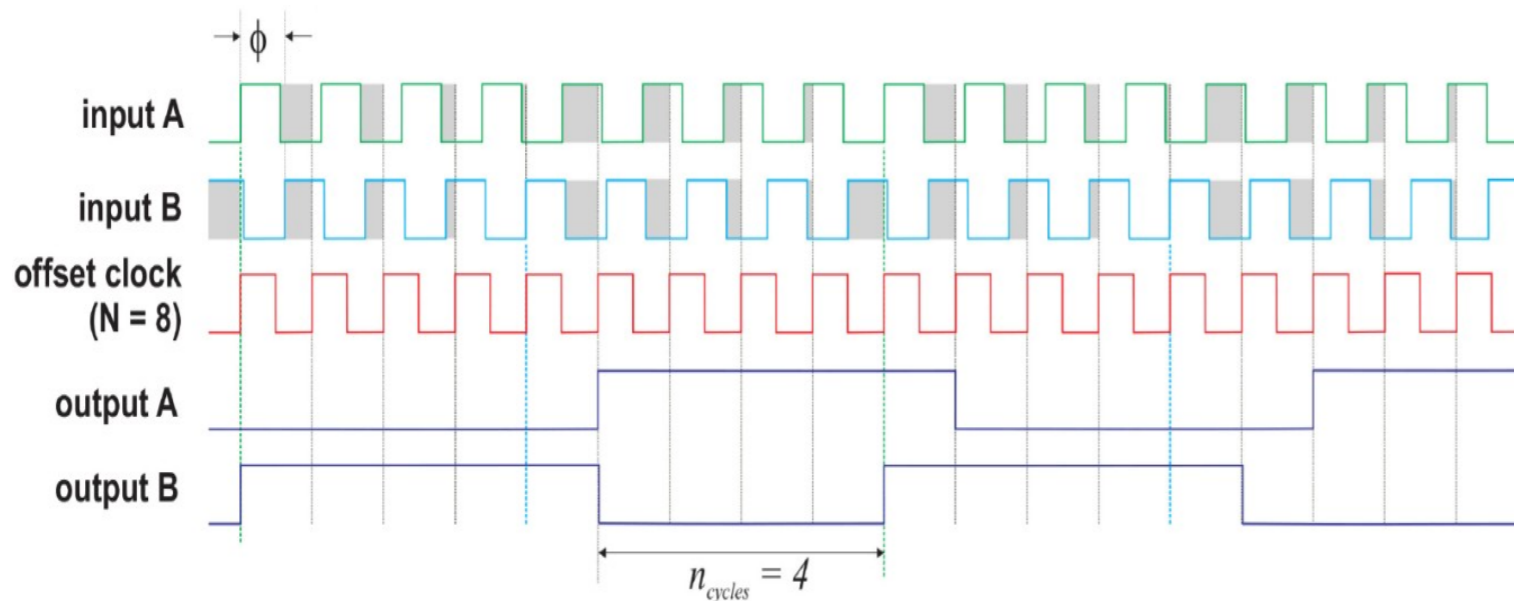
$$\delta ms = ((t_4 - t_1) - (t_3 - t_2)) / 2$$

- synchronize its clock rate with the master by tracking the value of $t_2 - t_1$
- compute clock offset:
offset = $t_2 - t_1 + \delta ms$

Digital Dual Mixer Time Domain phase detector (DDMTD)

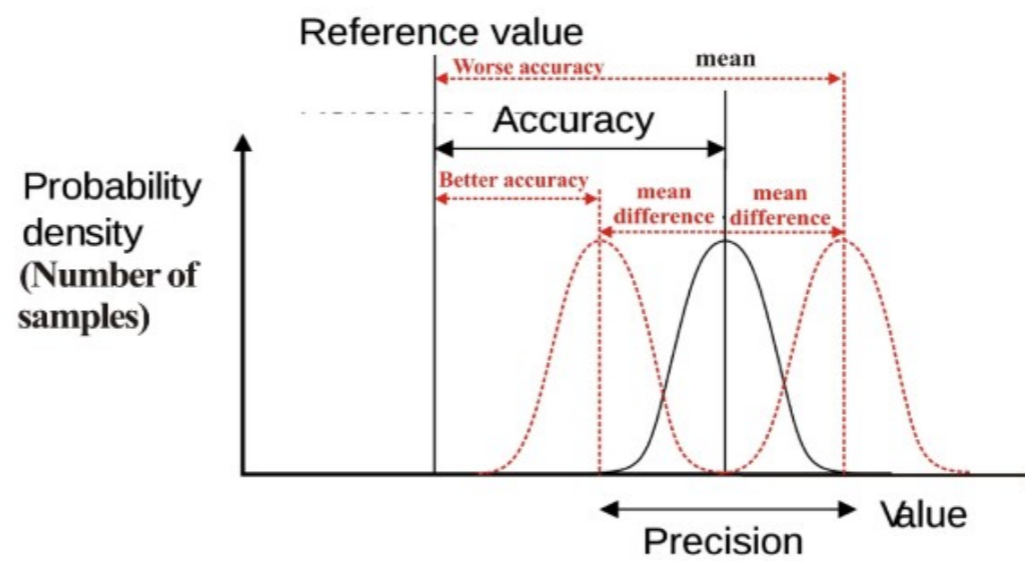


- Measure the phase shift between transmit and receive clock on
- the master side, taking the advantage of Synchronous Ethernet.
- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes measured by the master.

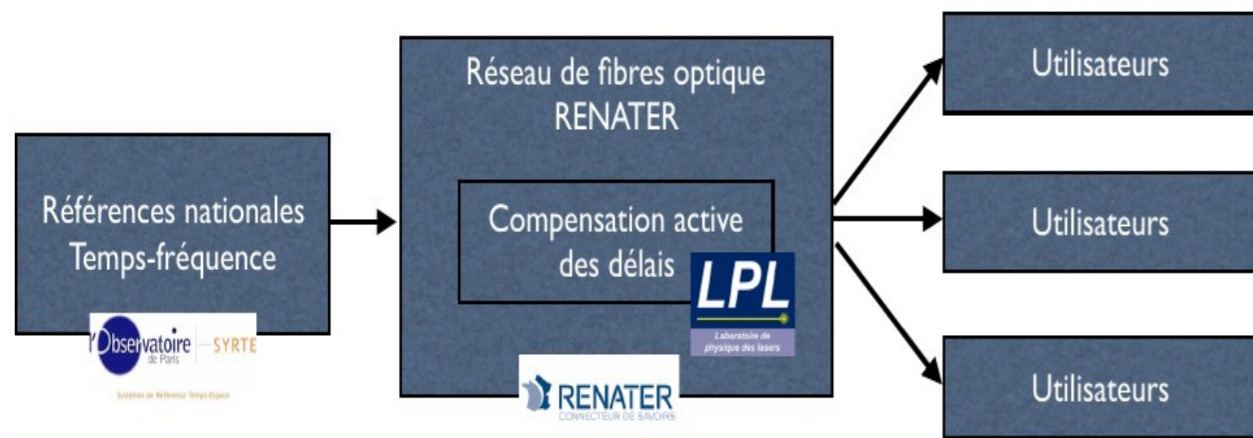


WhiteRabbit performance

System	accuracy	note
GPS	10ns -200ns	Propagation in non-stationary disruptive environment. Problem of the mutli-way
GPS-IPPP	2 – 3 ns	Resolution of phase ambiguities using RIMEX data. More complex implementation
WR switch without calibration	500ps - 100ns	Swich Orollia : Master configuration
WR switch with calibration	200ps – 2 ns	Swich Orollia : Master configuration
IDROGEN	13 ps	Swich Orollia : Grand Master configuration
IDROGEN with external synchronisation	3 ps	2 IDROGEN board on WR switch configure in Grand Master and synchronyse by T+ REFIMEVE
IDROGEN & external function	300fs	Aim of T+REFIMEVE



Time & frequency distribution : T+REFIMEVE



- For long time stability reference clock is mandatory
- International time reference provider
- Optical fiber distribution



Signal provided by T-REFIMEVE		Stability @1s	Stability @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1 st pillar - 10 MHz (White Rabbit)	10^{-12}	10^{-15}	10^{-14}	10^{-15}
	2 nd pillar - 1 GHz	10^{-13}	3×10^{-16}	10^{-14}	2×10^{-16}
Time	1 st pillar (White Rabbit)	1 ns	1 ns	10 ns	10 ns
	2 nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps
Optical frequency (194,5 THz - 1542 nm)	Today	10^{-15}	3×10^{-16}	10^{-14}	2×10^{-17}
	Expected progress in 5 years	10^{-16}	2×10^{-17}	10^{-14}	10^{-18}

```
WR PTP Core Sync Monitor v 1.0
Esc = exit

TAI Time:          Thu, Jan 1, 1970, 00:03:48

wru1: Link up (RX: 685, TX: 281), Mode: WR Slave  Locked  Calibrated
IPv4: BOOTP running

PTP status: slave

Synchronization status:

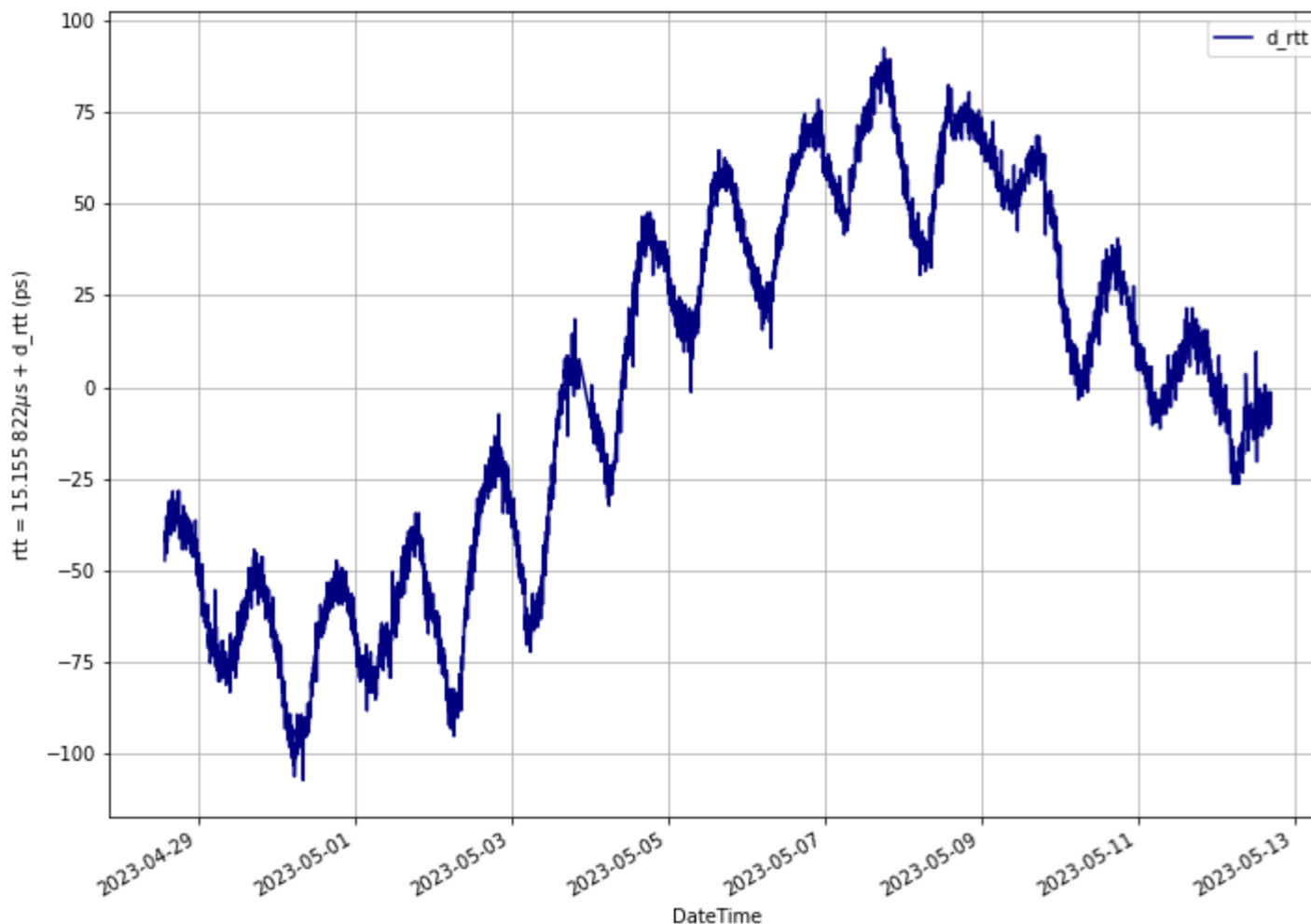
Servo state:      TRACK_PHASE
Phase tracking:   ON
Synchronization source:
Aux clock status:

Timing parameters:

Round-trip time (mu): 691831 ps
Master-slave delay:  349132 ps
Master PHY delays:  TX: 46407 ps, RX: 168643 ps
Slave PHY delays:   TX: 46407 ps, RX: 175043 ps
Total link asymmetry: -6433 ps
Cable rtt delay:    255331 ps
Clock offset:       0 ps
Phase setpoint:     528 ps
Skew:                5 ps
Manual phase adjustment: 0 ps
Update counter:     174
--□
```

● WR debugging

- Small operating system include in the WR core
- Serial communication by USB or Ethernet
- Status of the link : Delay, transceiver
- Control of the link : PPS, configuration



- WR supervision at LAC laboratory
- Monitoring at user equipment level
 - Fibers time propagation delays
 - 1.4Km of fiber
 - 5 levels of network stratum
 - 10 days of measurement
 - Zen-TP system

Off the shelf system

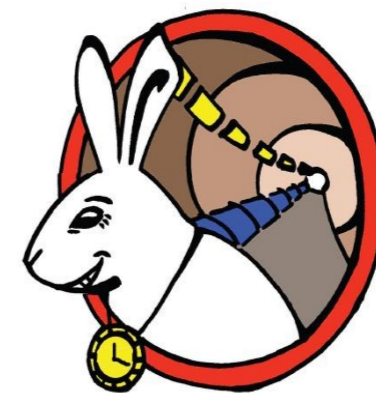
- Seven Solution (Orollia) :
 - WR-Zen : Low jitter WR master
 - WRS : switch 18ports
 - WR-LEN : WR node



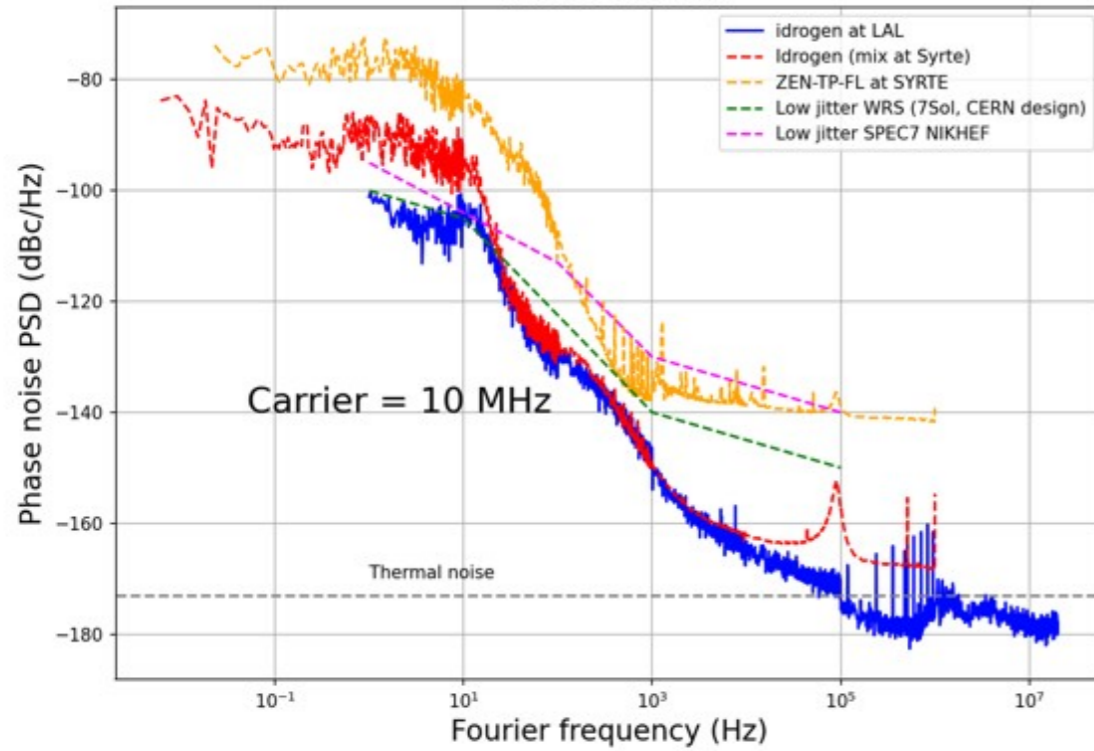
Low phase noise WR -PTP : IDROGEN board



- High performance WR low jitter node
- High performance data acquisition system
- FMC+ carrier board
- Design & realization by IJCLAB
- Firmware by Nancay Observatory
- Clock expertise and qualification by SYRTE
- Measures at SYRTE and IJCLAB



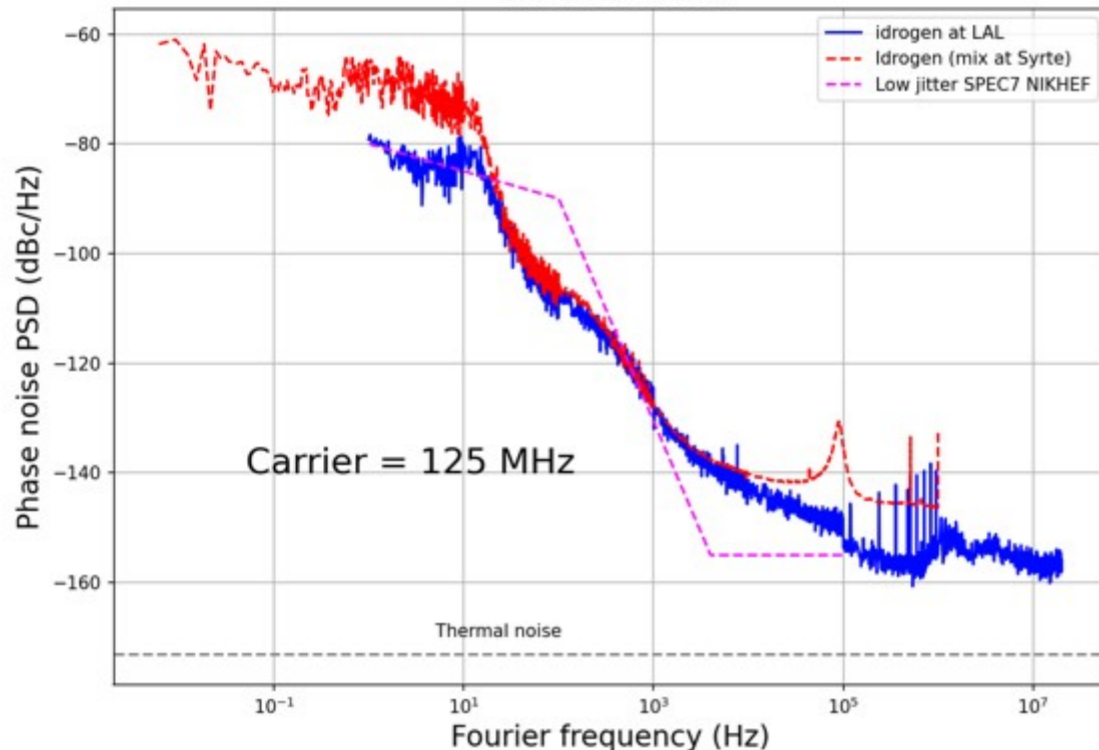
Phase noise comparison of improved WR device
- 2020 state of the art -



- Transfer from one WR switch to two IDROGEN boards with a short link (few meters)
- For the test we measure the phase difference between 2 nodes (IDROGEN board)

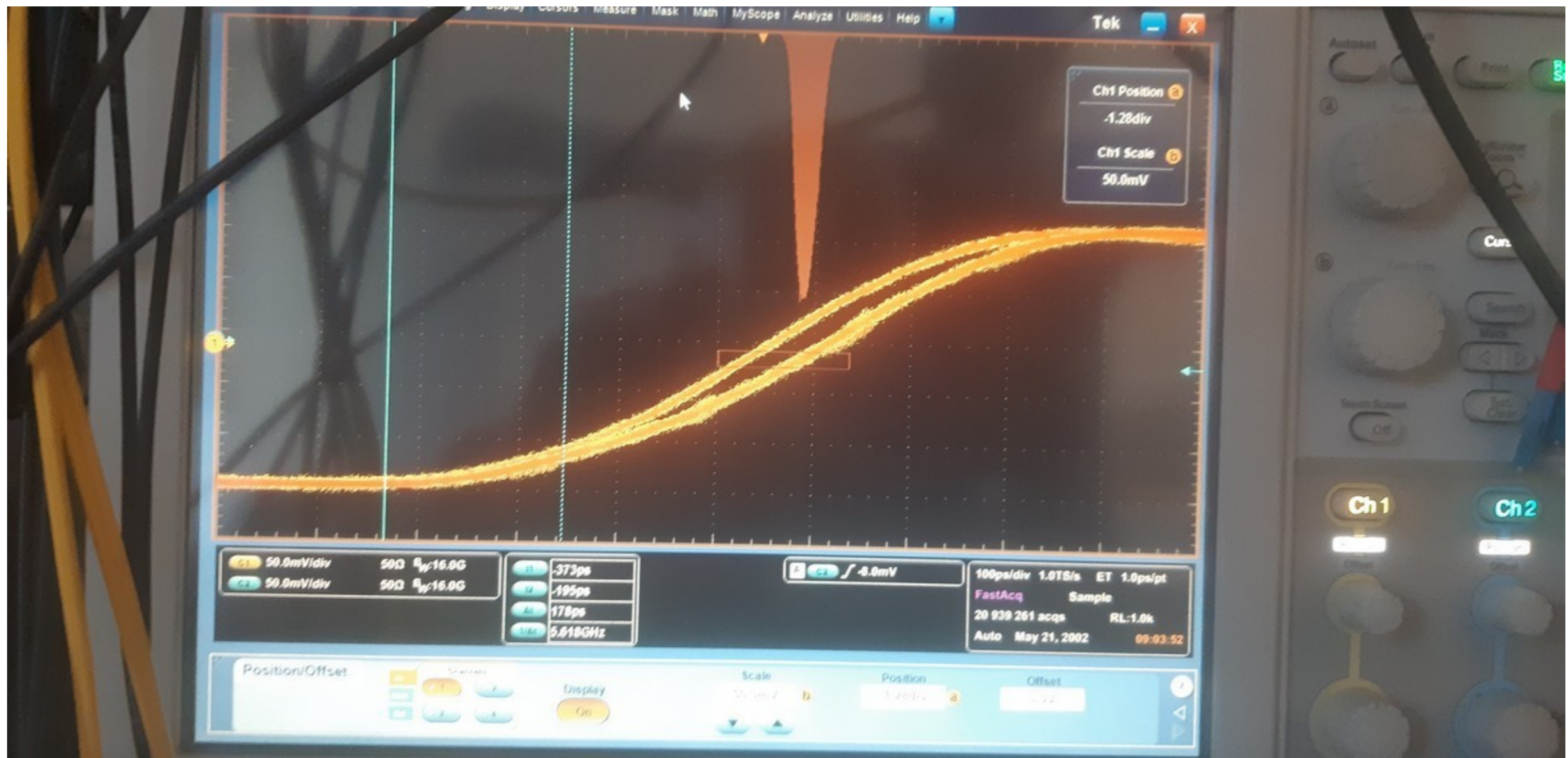
- Best result, one order of magnitude than the « challenger »
- Clock phase jitter
- PPS time precision 3ps RMS

Phase noise comparison of improved WR device
- 2020 state of the art -

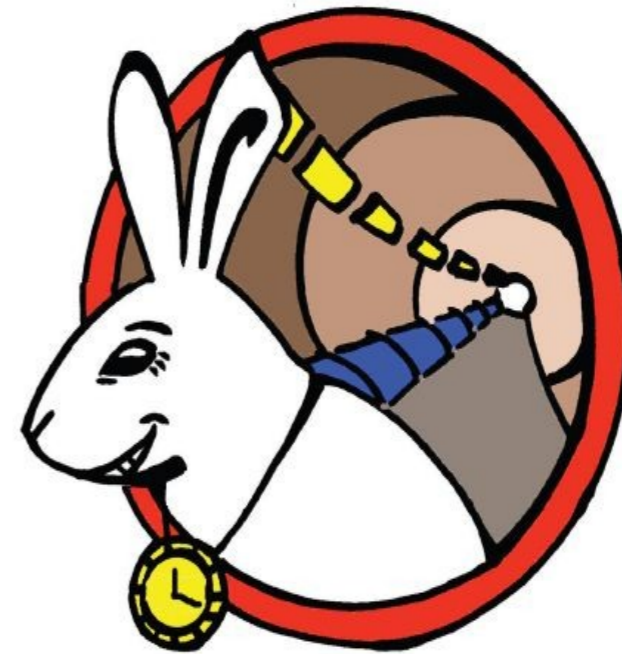


Pulse Per Second : IDROGEN

- PPS 2 IDROGEN board
- 25m & 125m of optic fiber
 - ~50ps of dispersion of the PPS with calibration



R & T TIMED

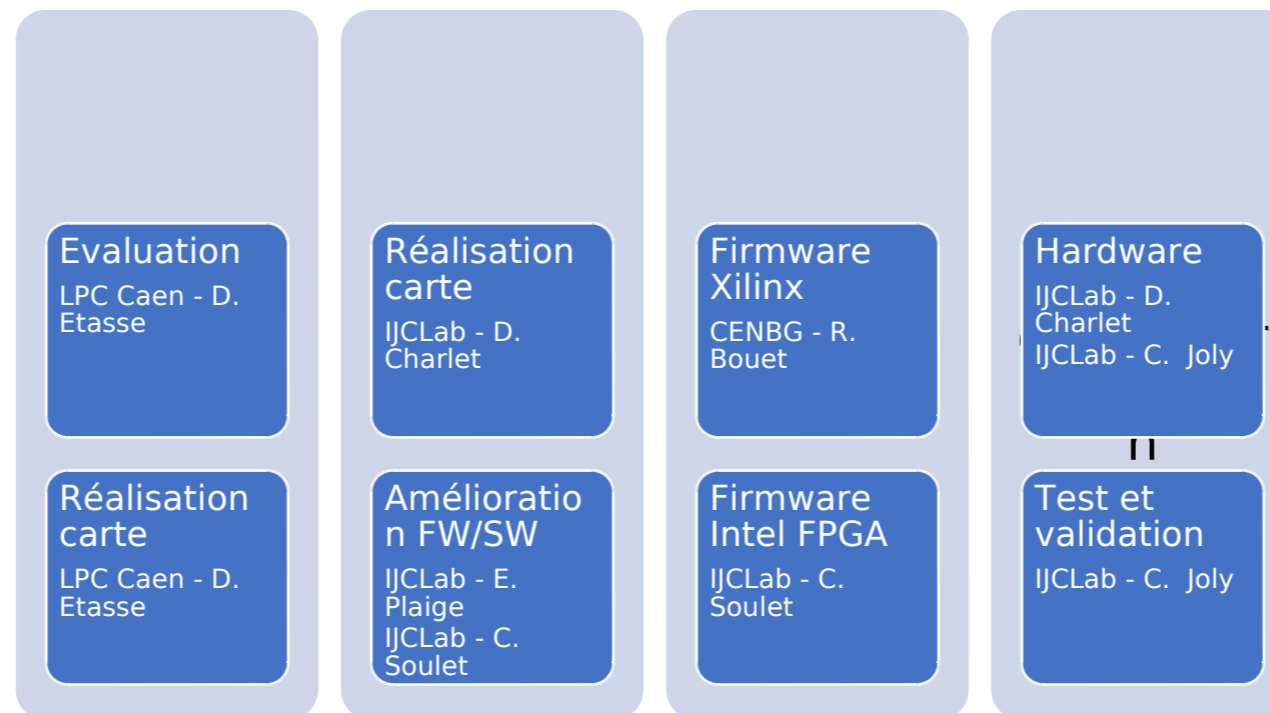


Research & Technology : TIMED

- Observatory of Paris & IN2P3 laboratories collaboration
- Extended domain of WhiteRabbit : Crate implementation
- WhiteRabbit node simplification of technical integration
- Improvement of WR performance
- Integration of external components by firmware function
- High stability frequencies distribution

Research & Technology : TIMED

- 5 Laboratories , 2 instituts
- Shedules : 3 years
- Budget : 66K€
- Contributions :
 - LPC Caen : Integration of WR in a crate (Off the shelf evaluation)
 - LP2IB : WR external VCXO integration
 - LPSC : Integration of WR in a crate (custom development)
 - IJCLAB : WR simplification, enhance WR, WR ref design, master oscillator
 - Observatoire de Paris : enhance WR

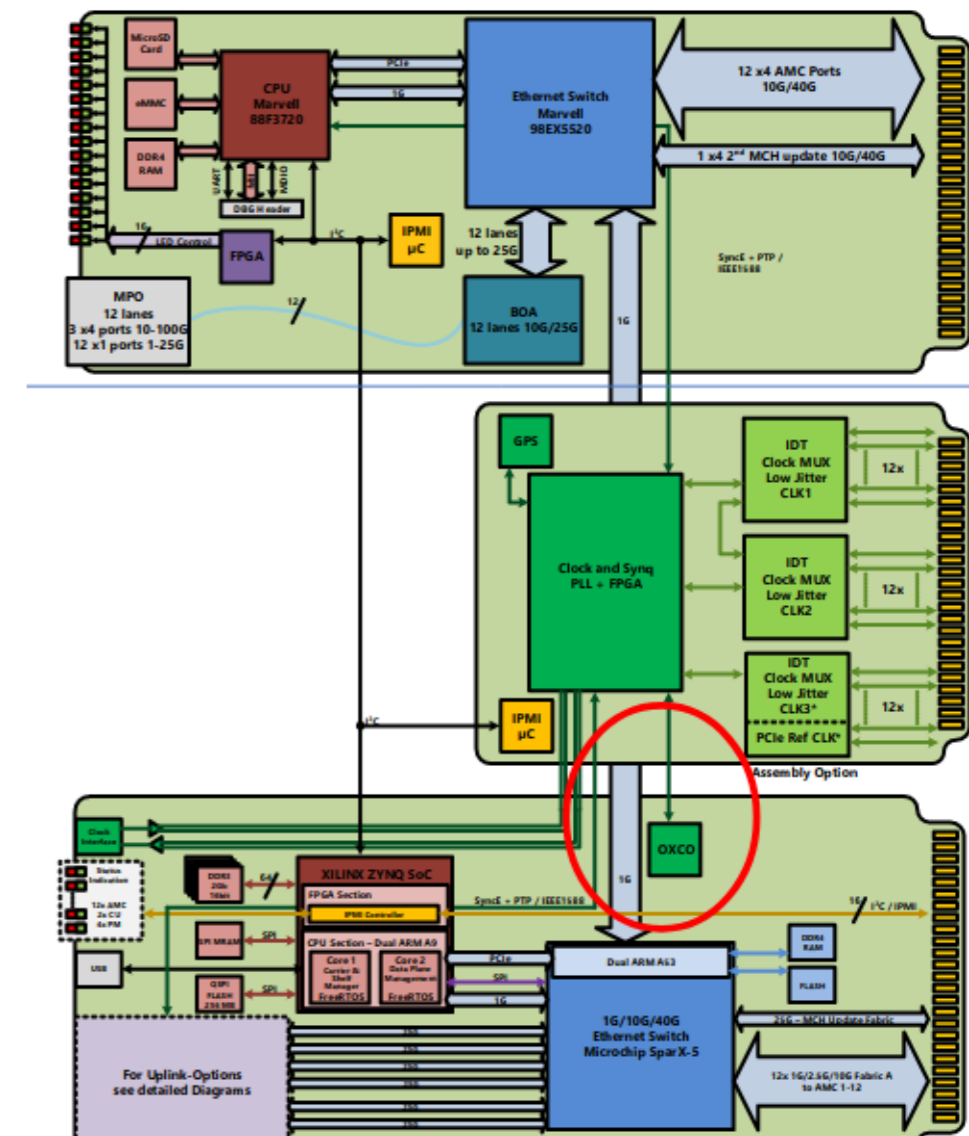
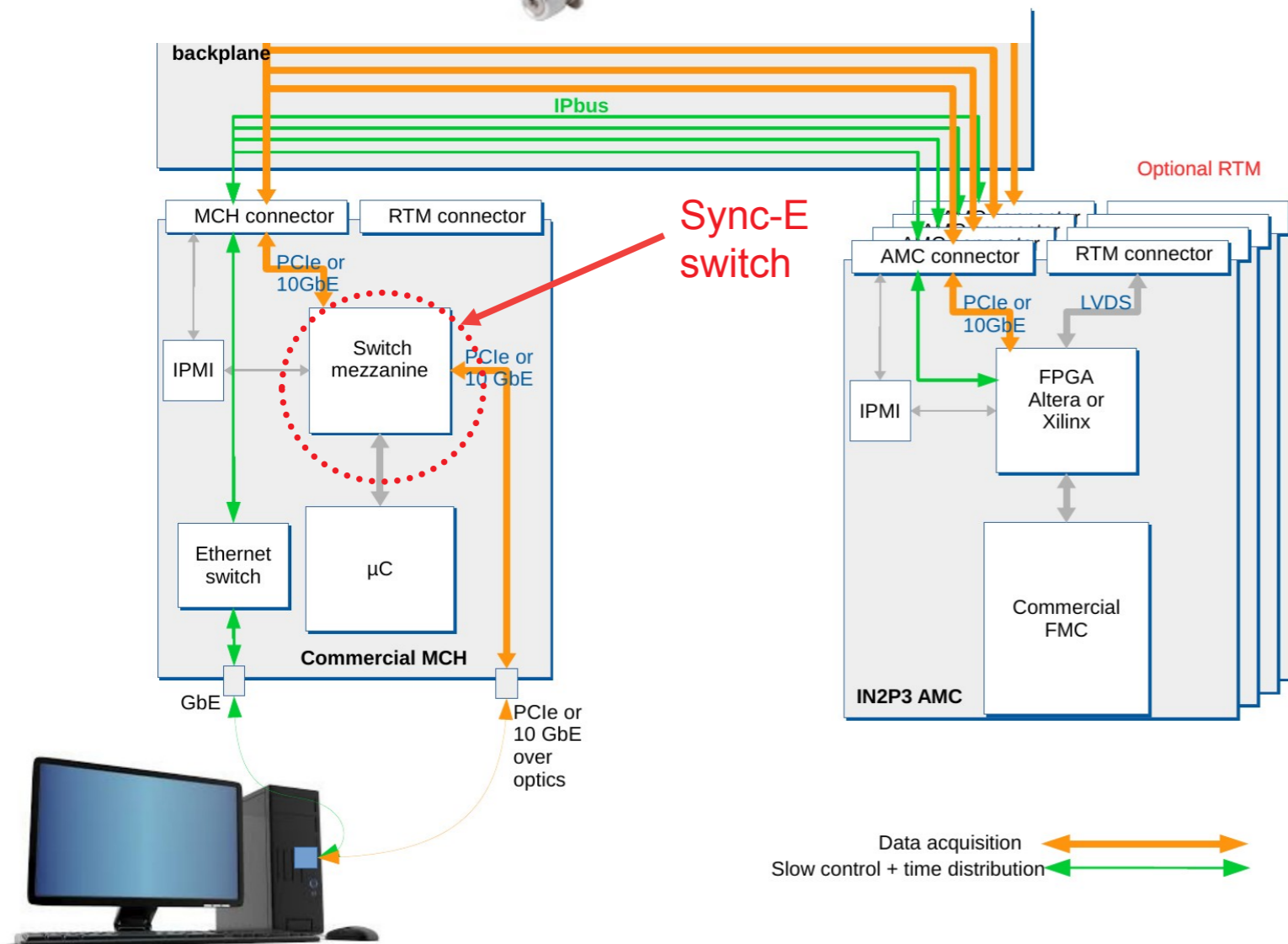


R & T TIMED 1 : WR Crate integration



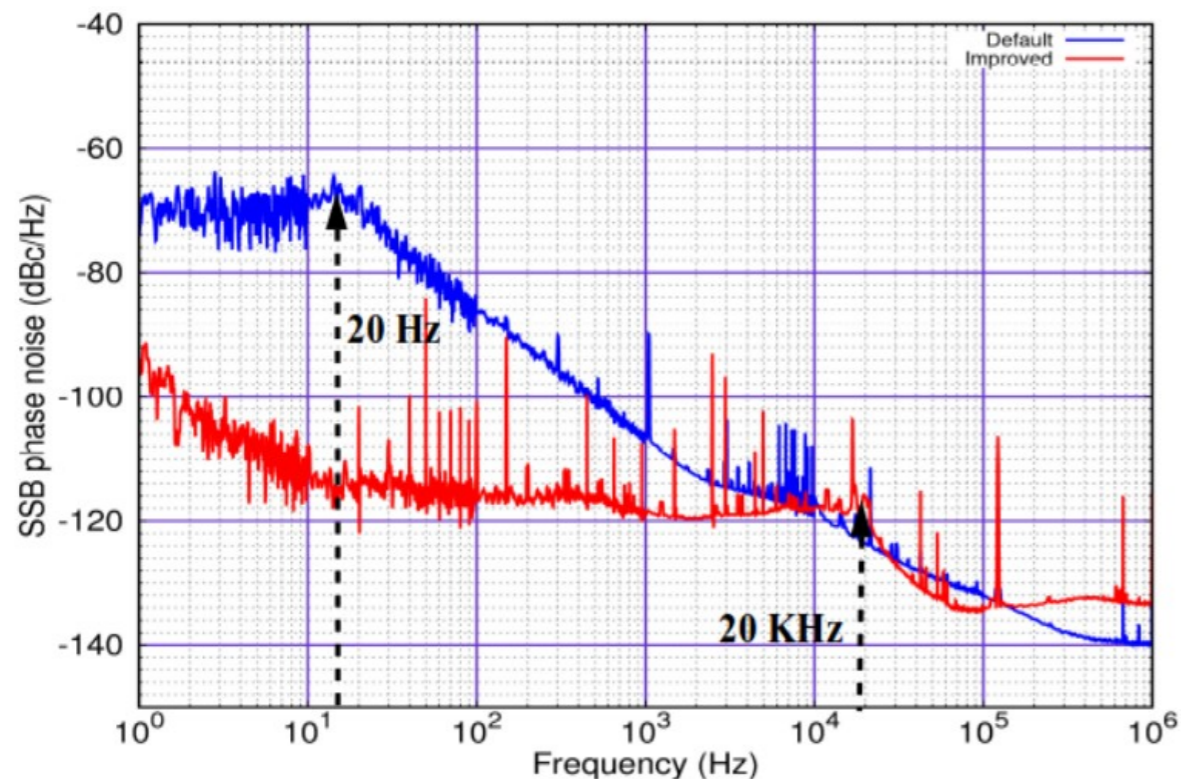
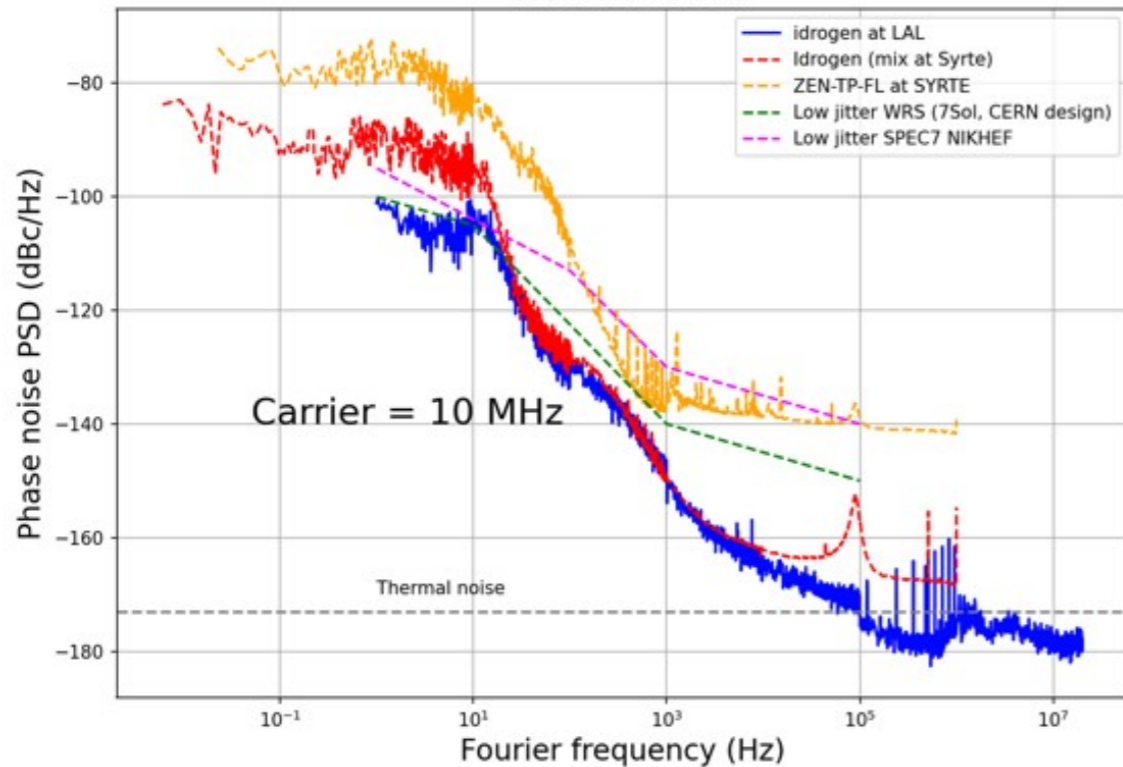
WhiteRabbit on μ TCA

- Only switch functionality (no master)
- WhiteRabbit on copper link
- Sync-E function on MCH board
- NAT-MCH-4
 - IEEE1588V2 compliant switch



R & T TIMED 3 : Increasing performances

Phase noise comparison of improved WR device
- 2020 state of the art -

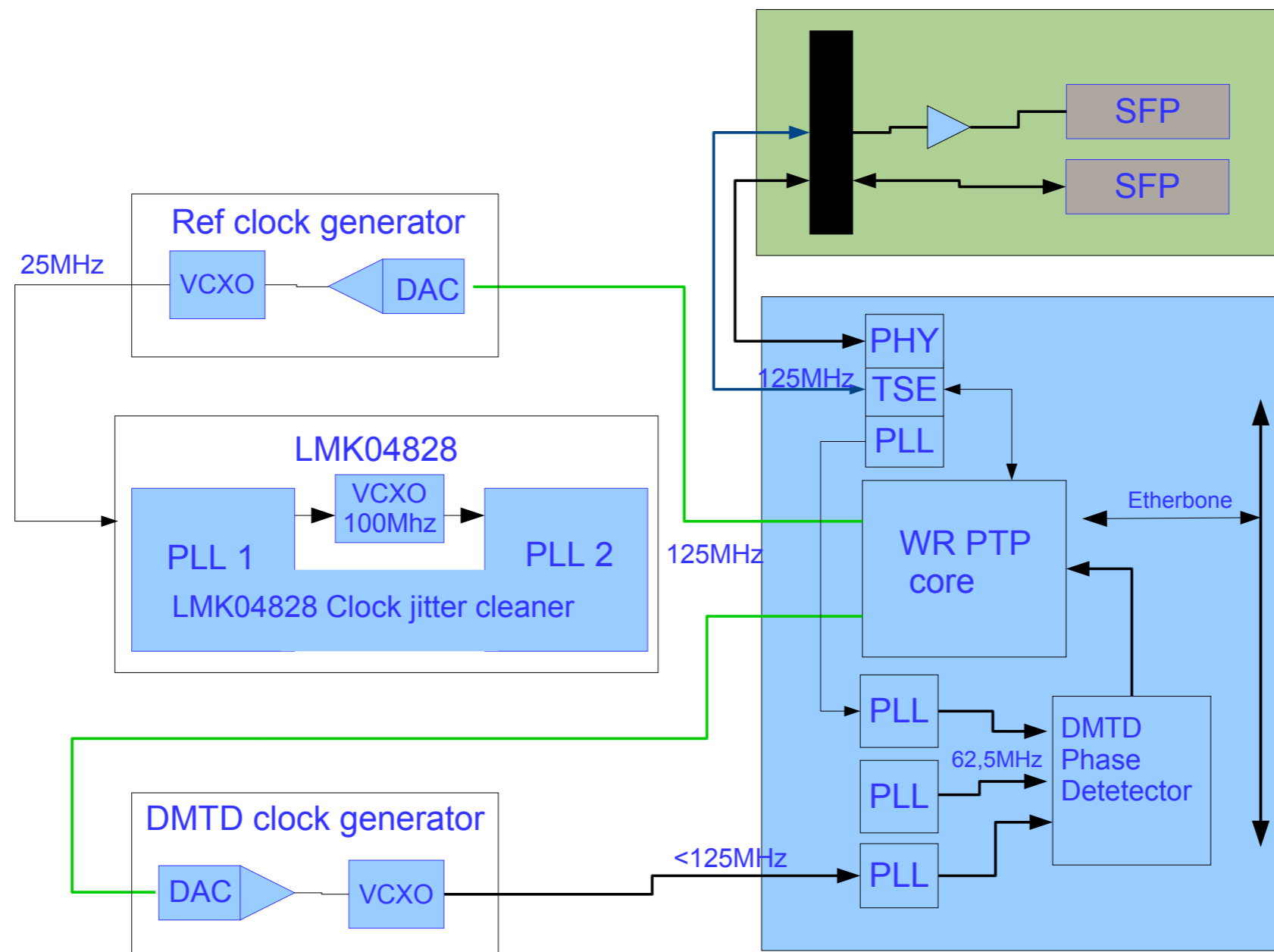


- Collaboration with Paris Observatory Laboratory
 - Goal 1 : ~ 1ps
 - Goal 2 : < 100fs
- Soft PLL modification
 - Decreases the response time of software PLL
 - μ P upgrading : Replacement of the universal μ P based on logic bloc by dedicated μ P (NIOS) or hardware μ P (SOC)
 - Gain integrator optimization
- Increased PLL bandwidth of the GM Local oscillator
- Components upgrading
 - VCXO selection
 - Increased internal Frequency (PLL number reduction)
- Modification of WR principle
 - phase modulation and demodulation of an ultra-stable optical carrier
 - Replacement of message protocol by timecode
 - Phase measurement in optic

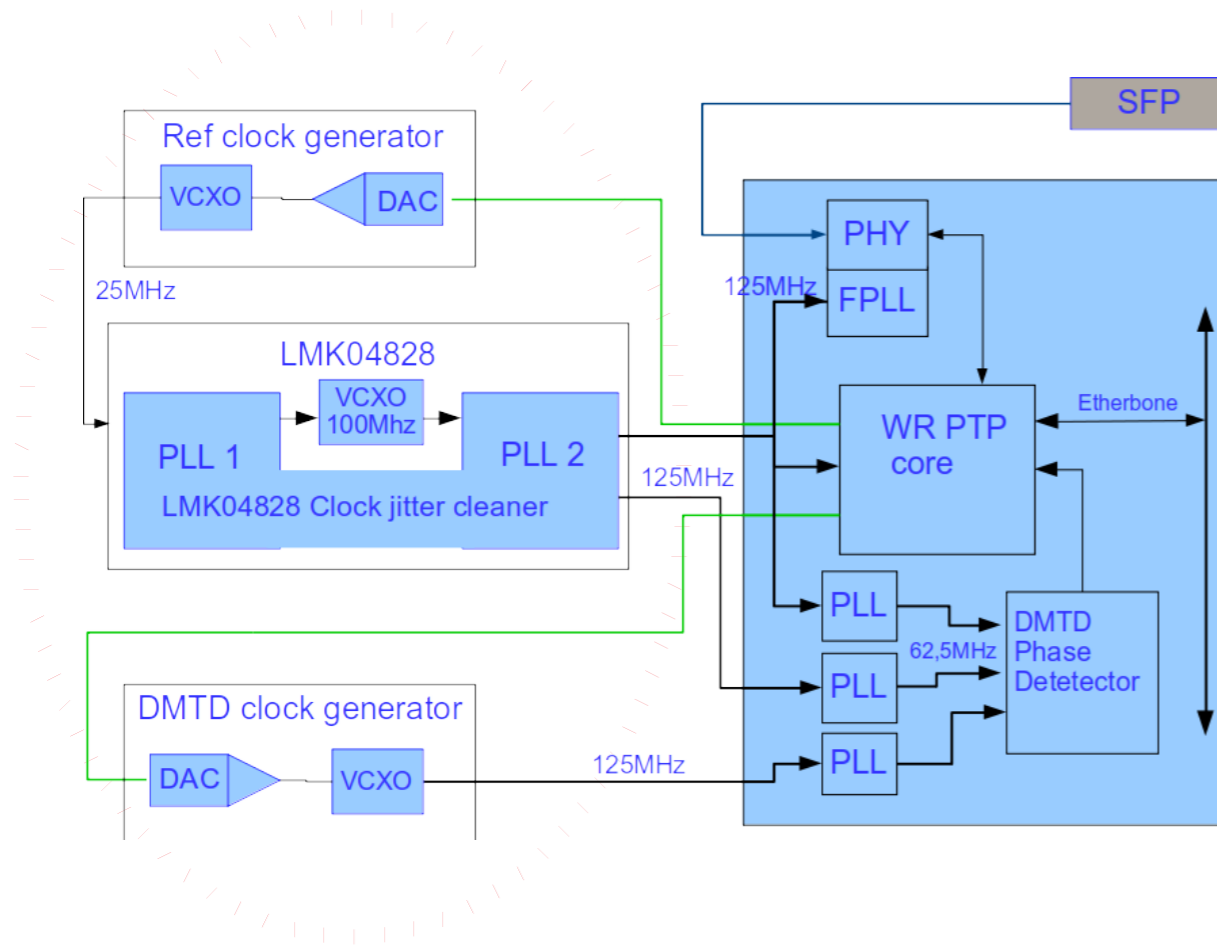
- The White Rabbit is a technological breakthrough
- A majority of new physics experiences will use the WR protocol : CERN detector & accelerator, KEK, Hyper Kamiokande, Einstein telescope...
- A lot of physics experience will be upgrade using WR : CERN experiences, ...
- The new development will offer new physics opportunities :
 - Multi-messenger astronomy
 - Geodesie chronométrique relativiste
 -

R & T IMED 2 : Simplification of WR integration

- Replacement of GXB by DDR I/O (up to 800MHz capability)
 - IP Native-PHY by IP TSE Pcs only (FMC in production)
 - Integrated PHY functionality replaced by RTL code (limitation by FPGA type)
- Integration of external PLL by internal one



R & T TIMED 4 : Firmware integration



- External PLL integration
 - Internal reconfiguration
 - µP Software upgrade
- VCXO integration
 - Derived from video IP
- FPGA manufacturer dependent
- More challenging that I can imagine ...

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs



XAPP589 (v2.3) April 29, 2015

All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)

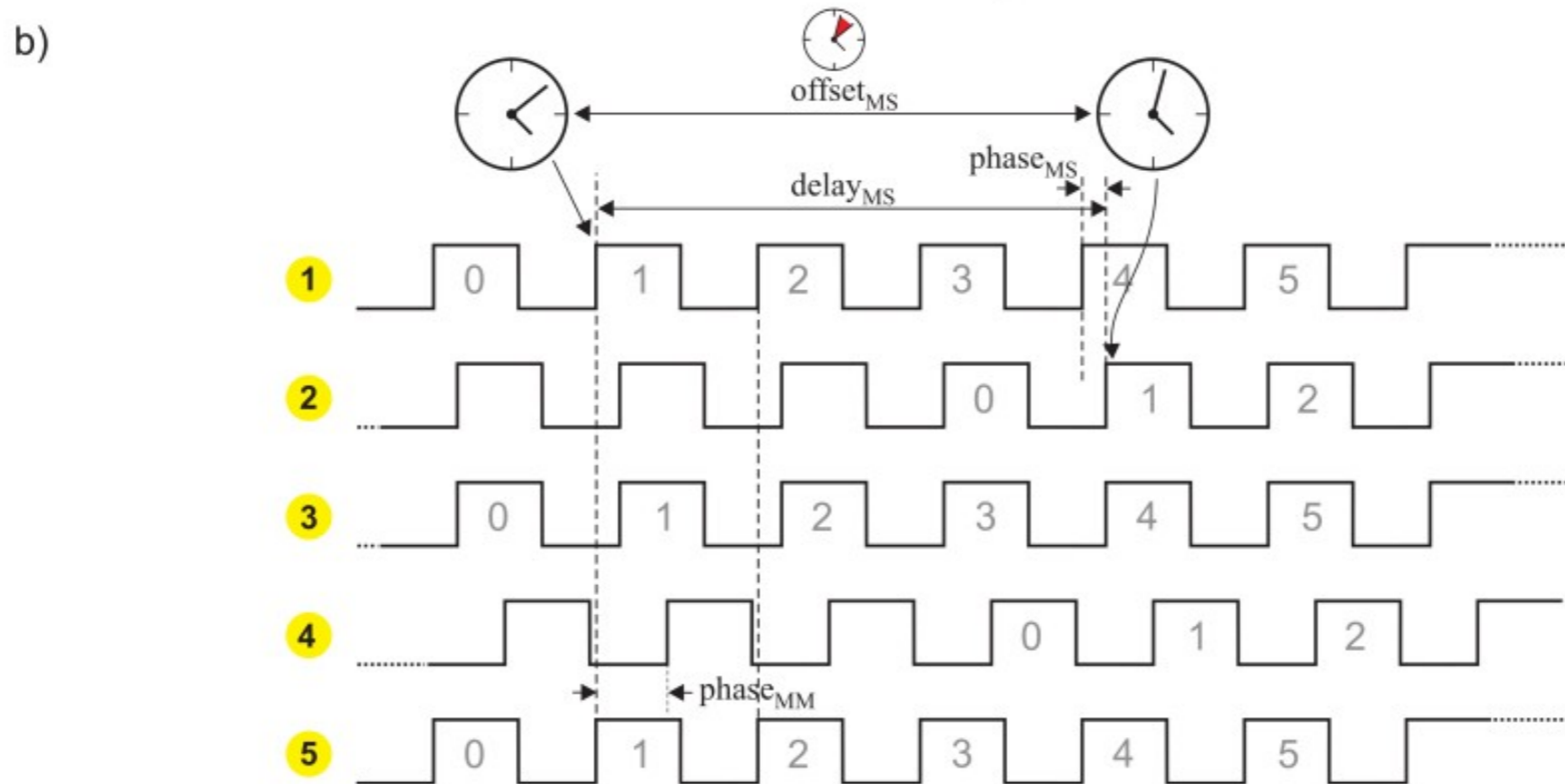
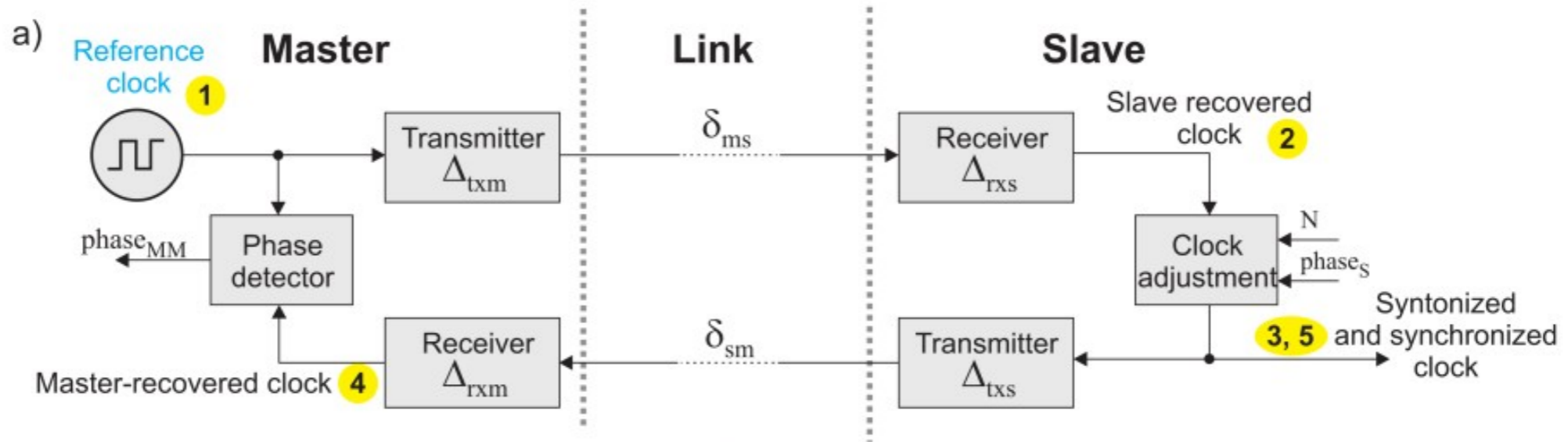
Authors: David Taylor, Matt Klein, and Vincent Vendramini

Summary

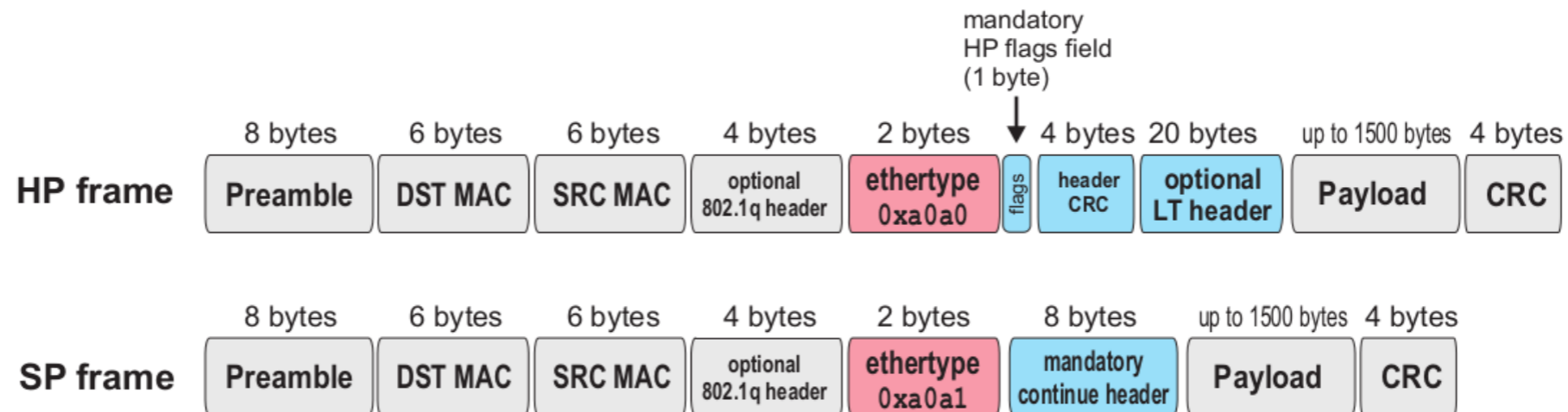
This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

Note: In this application note, *transceiver* refers to these types of transceivers:

WR : Fine delays adjustment



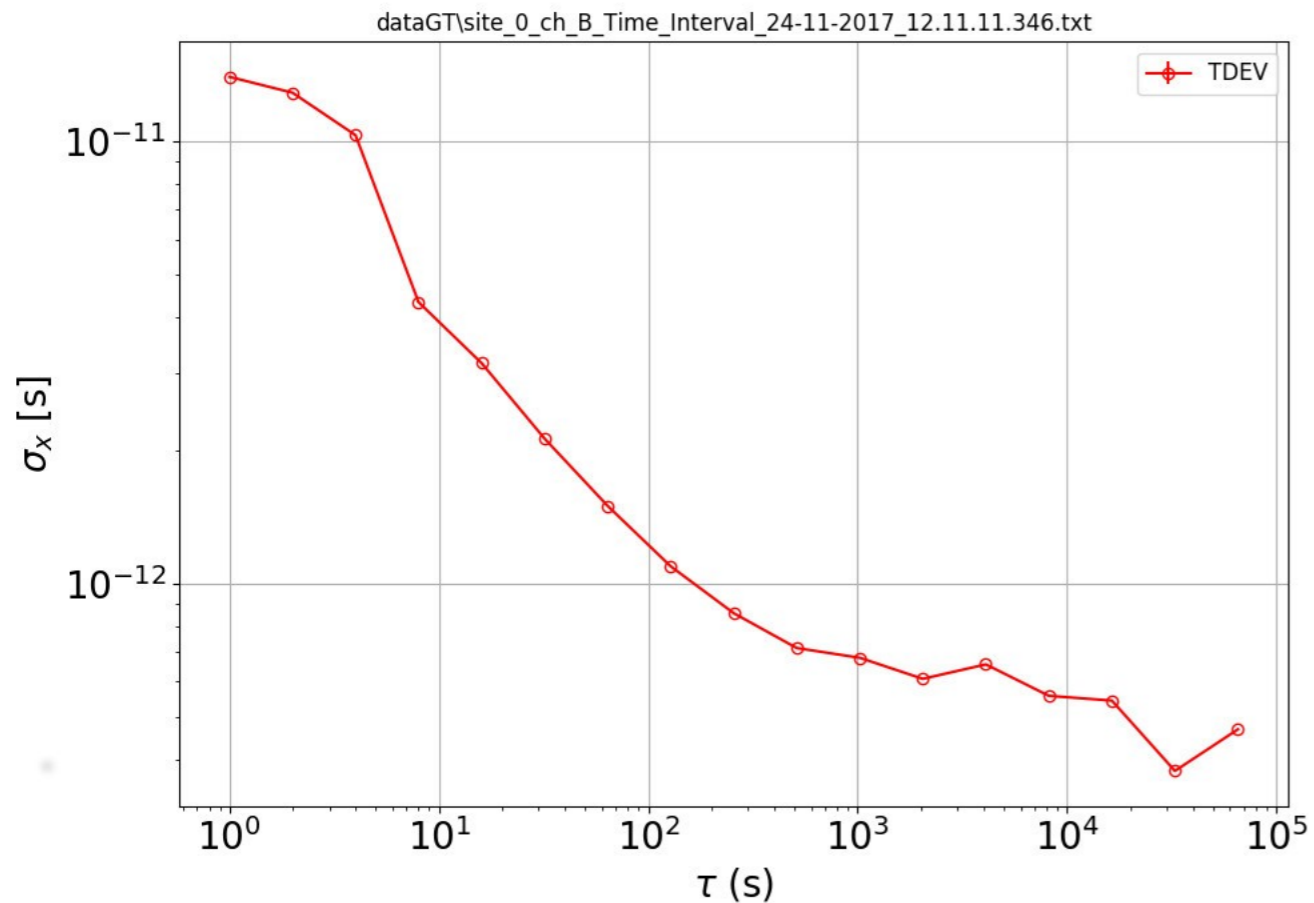
WR protocol



- Traffic divided into High Priority (HP) packets and Standard Priority (SP) packets.
- HP packets use a special value in the Ethertype field of the frame.
- Quality of Service (QoS) in the 802.1Q VLAN standard does this and more \Rightarrow will study full compliance in the future.
- HP packets can preempt other types of packets “on-the-fly”.

Signal to be provided by T-REFIMEVE

		Stability or relative stab. @1s	Stability or relative stab. @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1st pillar - 10 MHz (White Rabbit)*	1,00E-12	1,00E-15	1,00E-14	1,00E-15
	2nd pillar - 1 GHz	1,00E-13	3,00E-16	1,00E-14	2,00E-16
Time	1st pillar (White Rabbit)*	1 ns	1 ns	10 ns	10 ns
	2nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps [§]
Optical frequency (194,5 THz/1542 nm)	Today	1,00E-15	3,00E-16	1,00E-14	2,00E-17
	Expected progress in 5 years	1,00E-16	2,00E-17	1,00E-14	1,00E-18



● IDROGEN version -1

■ 400fs after 1000s

■ Same design as IDROGEN

■ IDROGEN system qualification Test

- With SYRTE test setup