Intel® FPGA with Integrated ADC/DACs

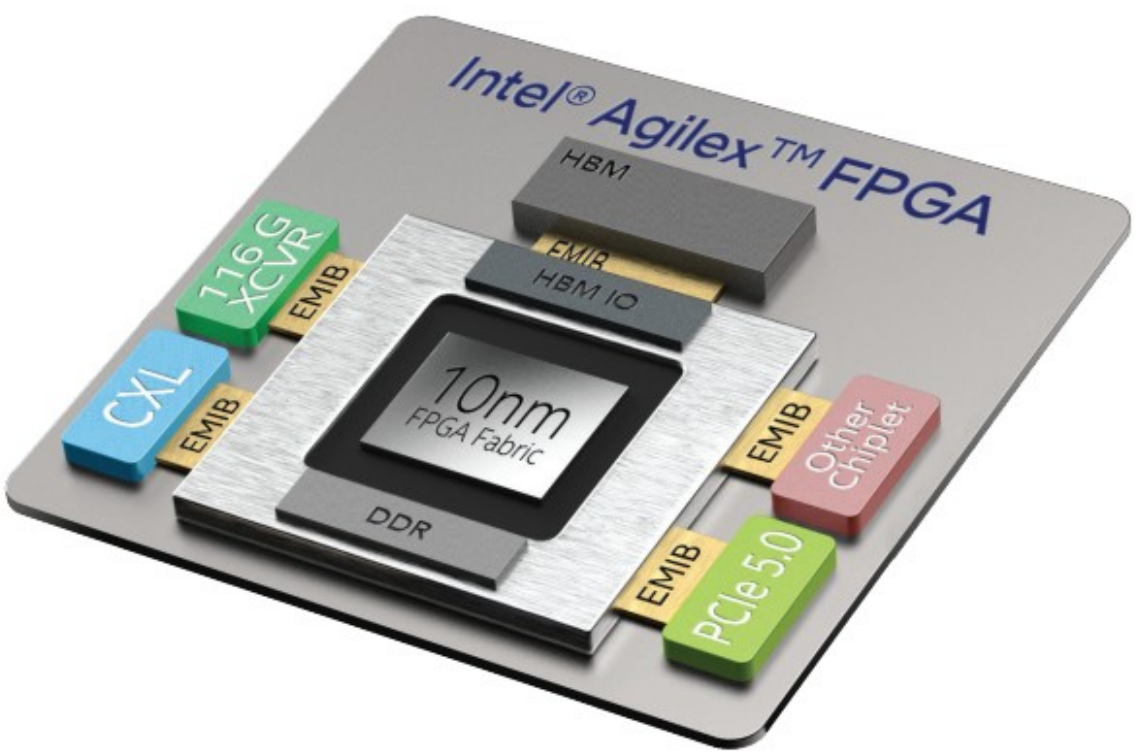
intel®

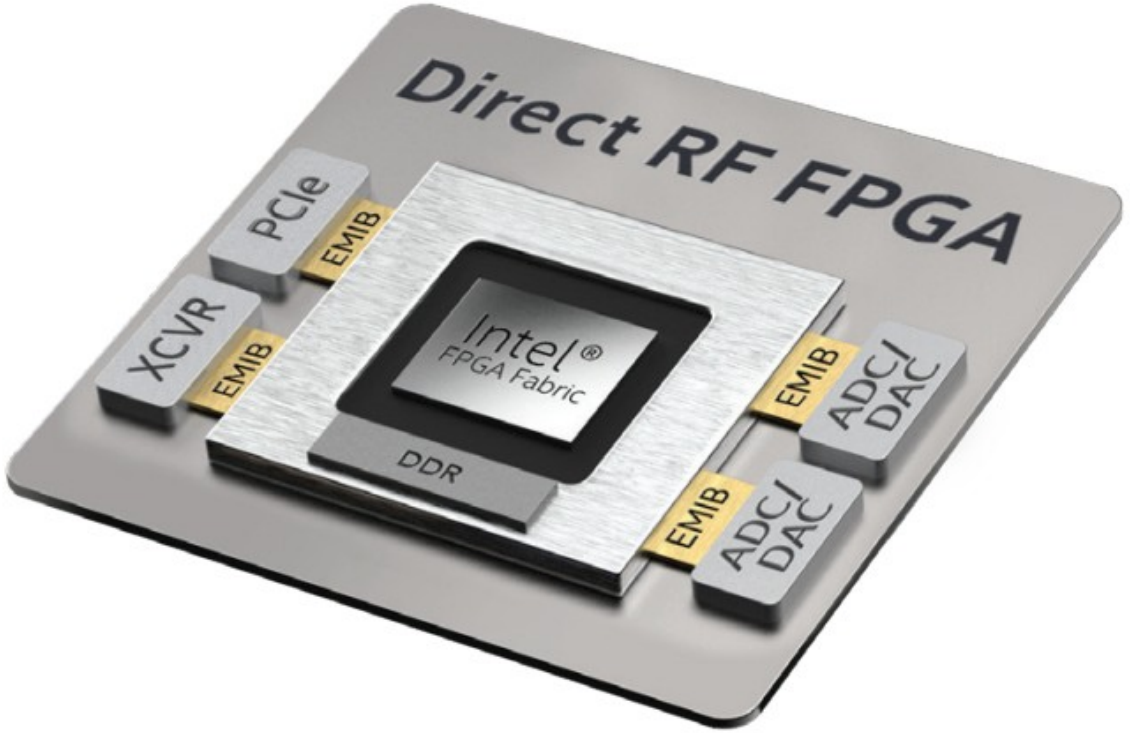
REW All Digital Beamforming Transformation

- All digital beam forming required for future threats including swarm of drones
- Reduction in SWAP* requirements drive need for heterogeneous integration
- Thousands of array elements in a given system with data converter at each element will radically change market dynamics

* SWAP = Size, Weight and Power

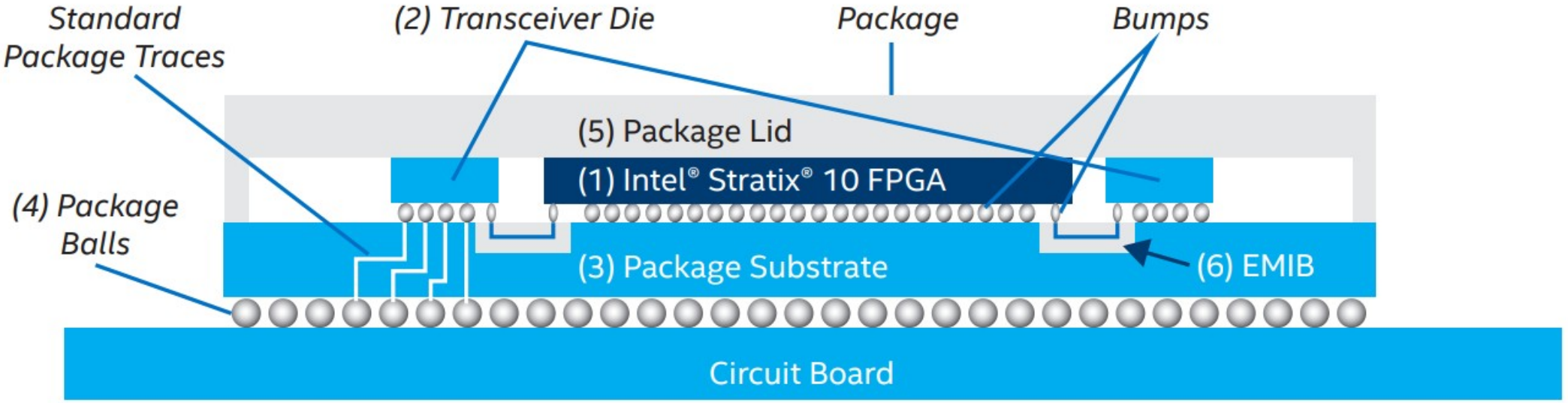
EMIB embedded multi–die interconnect bridge





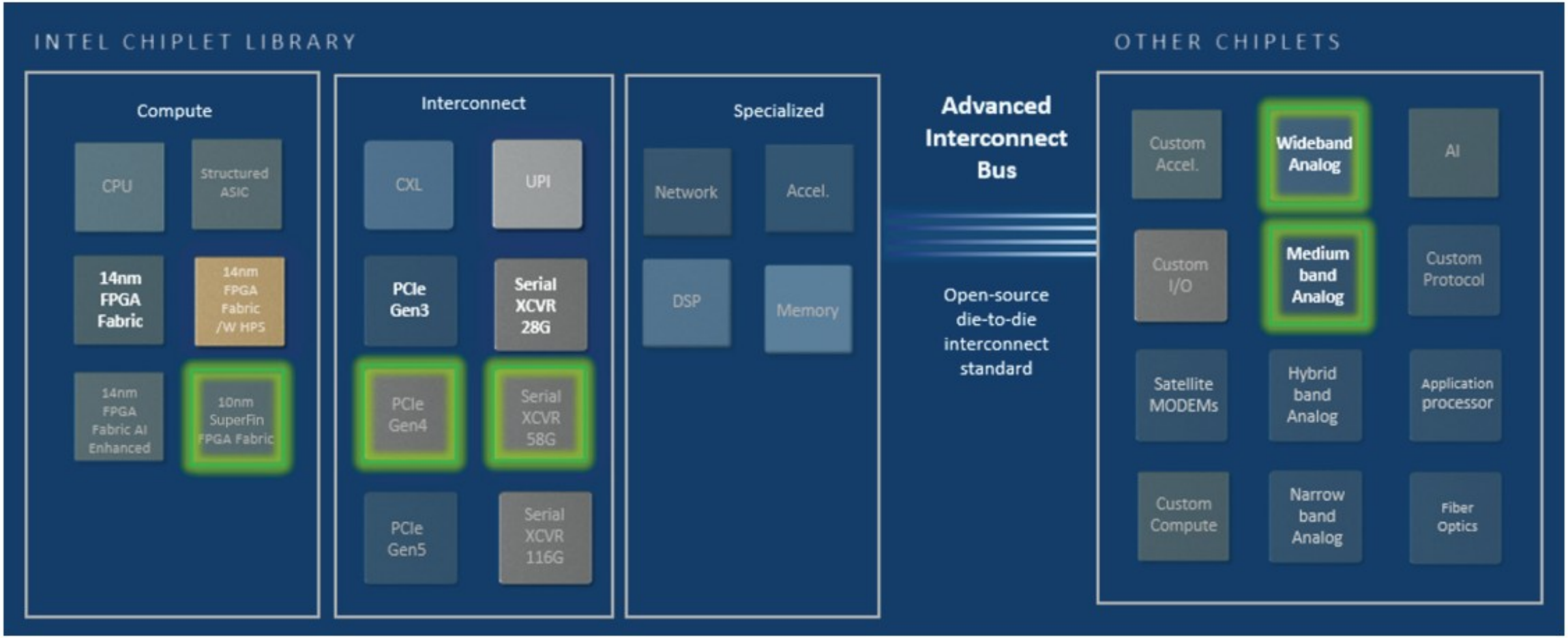
https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/analog-rf-fpga.html
https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/fpga-integrated-data-converter-solution-brief.html

EMIB technology



- Allows integration of high-performance analog converter chiplets regardless of process node, foundry, or IP provider with Intel® FPGA
- Provide lower latency versus JESD204c
- Provide lower power per bit versus JESD204c

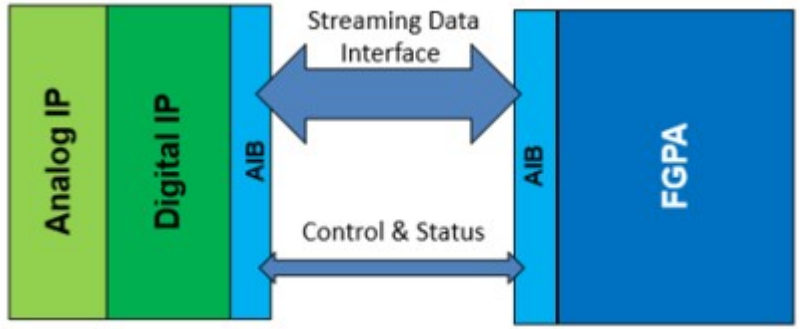
Chiplets



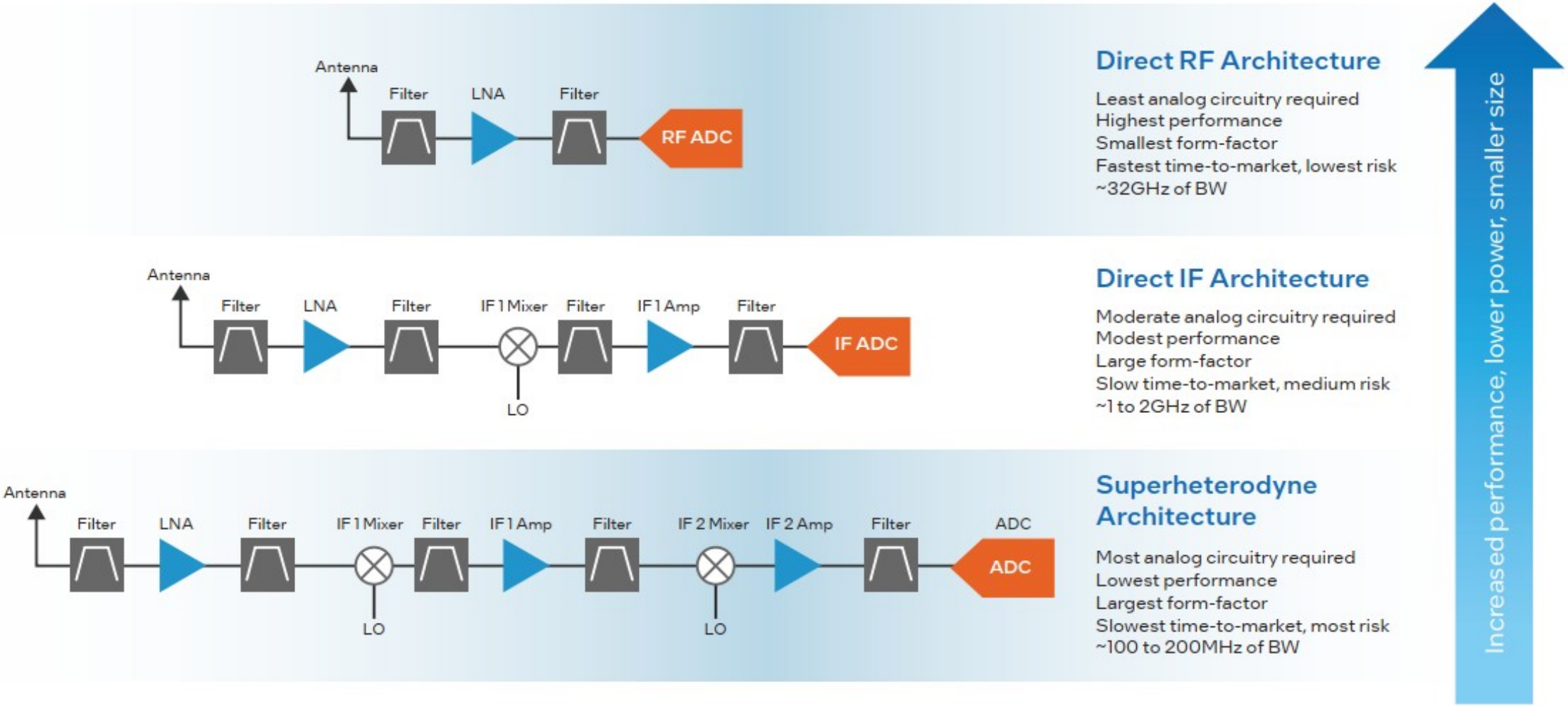
https://www.intel.com/content/www/us/en/products/docs/programmable/direct-rf-series-fpga-white-paper.html

AIB Overview

- Support peer-to-peer high bandwidth parallel communication
- Open to download from Intel Website
- Versatile per-channel clocking in both directions
- Streaming or transactional protocols can be implemented on top of AIB
- AIB’s flexible IO cell permits arbitrary TX, RX, clock and control mapped by the protocol layer above



Why Direct RF?



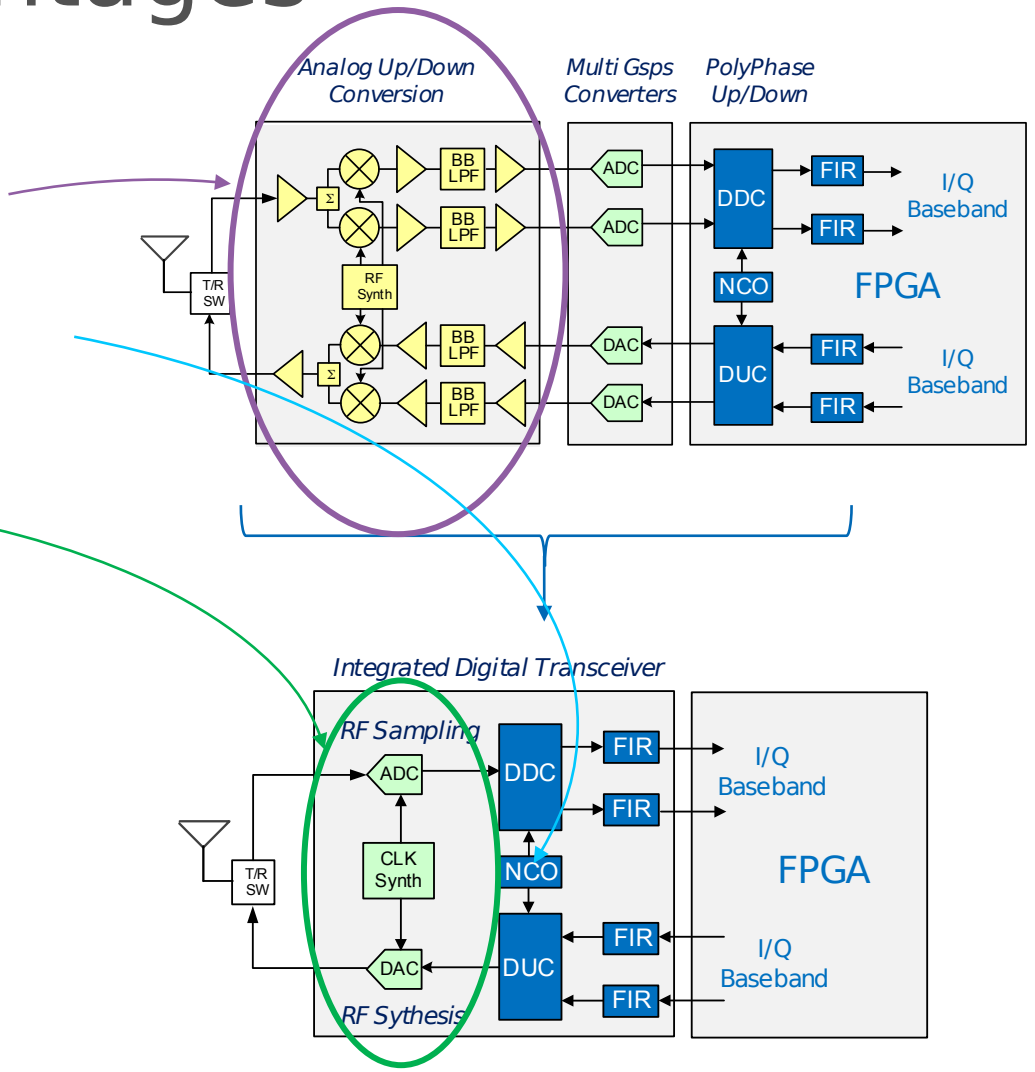
https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/analog-rf-fpga.html

Direct RF Sampling Advantages

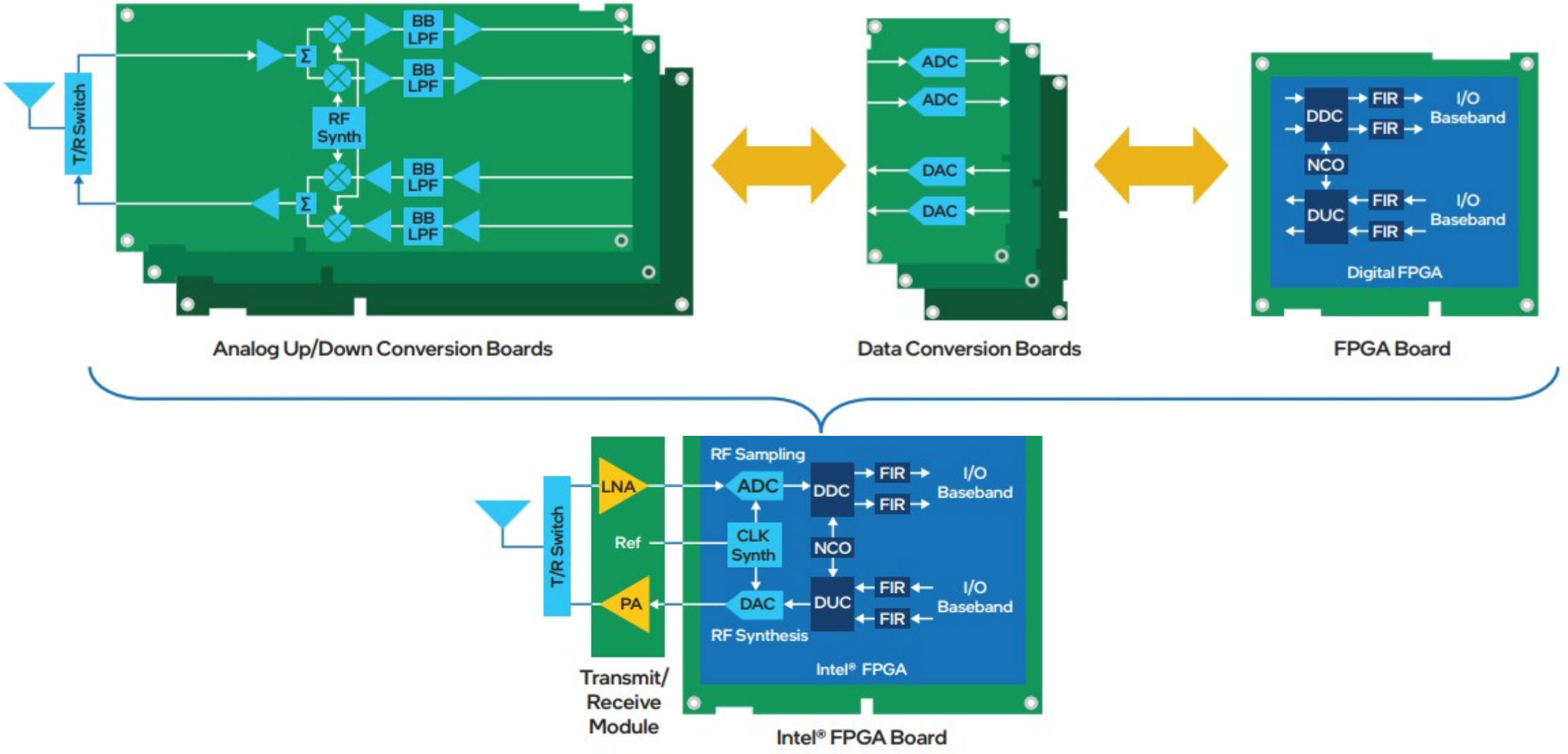
- Eliminates analog tuner circuitry
- Provides real-time frequency agility
  - Multi-mode radar / EW
- Provides wider bandwidths
  - EW countermeasures

Advantage in Size, Weight, Power, Cost, and Capability

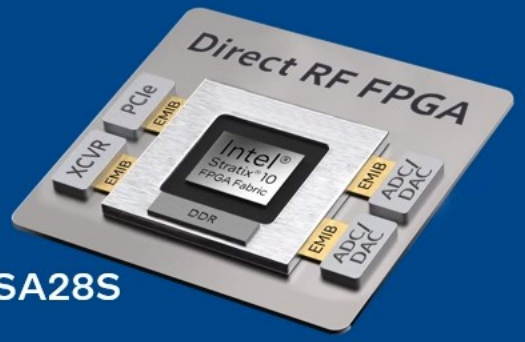
Up to 90+% Savings in Size



Integration



Intel® Stratix® 10 AX and Intel Agilex® 9 FPGA Direct RF-Series



1SA28S

Intel® Stratix® 10 AX FPGA

Intel® Stratix® 10 FPGA 2.8 MLE
+
8-Channels ADC/DAC

AGRW014

Intel Agilex® 9 FPGA Direct RF-Series

Intel Agilex® FPGA 1.4 MLE
+
4-Channels ADC/DAC

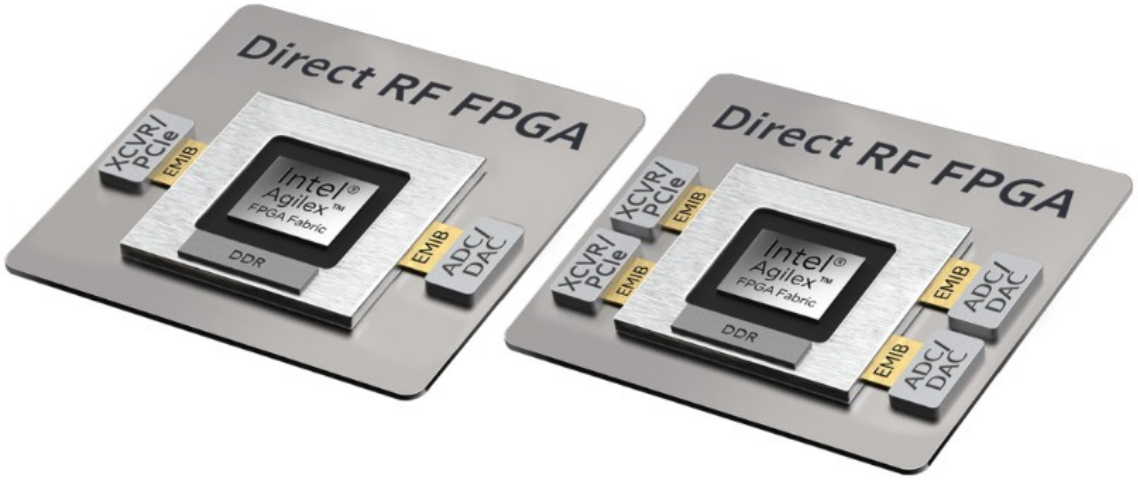
AGRW027

Intel Agilex® 9 FPGA Direct RF-Series

Intel Agilex® FPGA 2.7 MLE
+
8-Channels ADC/DAC

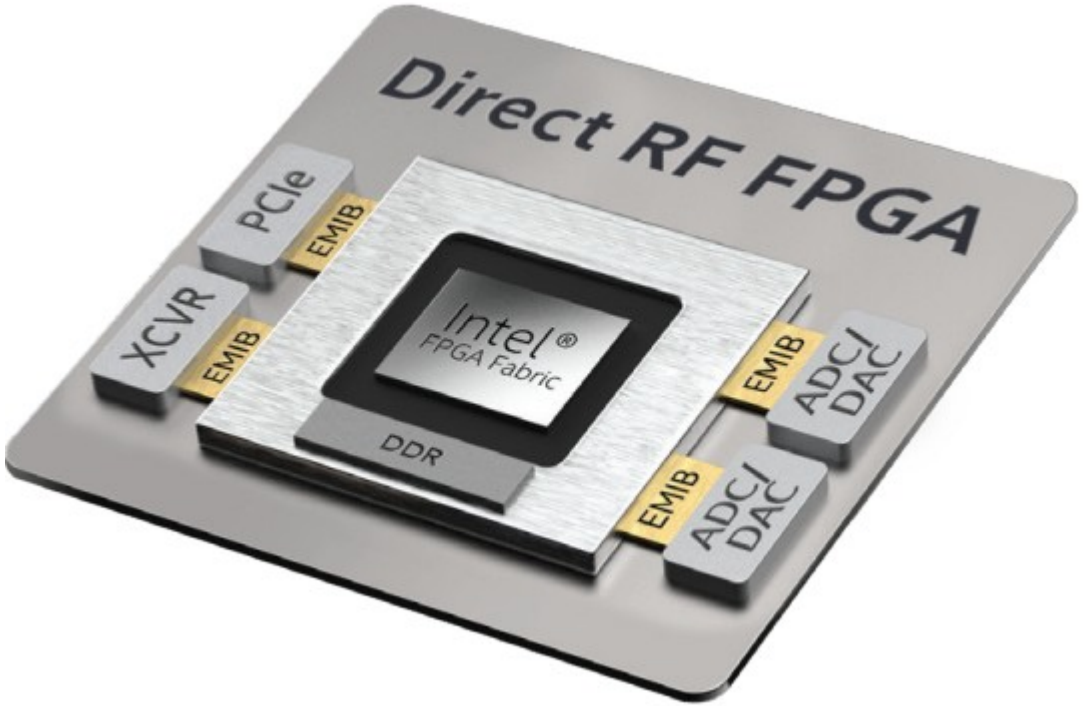
Devices familly

- Agilex based



Product Name	Logic Elements (LE)	18x19 Multipliers	# of ADC/DAC	Sample Rate (Gsps)	# of Bits Resolution	Embedded Memory (Mb)	Quad Core ARM	XCVR's	PCIe	Package
Intel® Agilex™ Direct RF-Series SoC FPGA AGRW014	1437	9020	4/4	64/64	10/10	190	Yes	58G PAM-4, 32G NRZ	4.0	45x32
Intel® Agilex™ Direct RF-Series SoC FPGA AGRW027	2693	17056	8/8	64/64	10/10	287	Yes	58G PAM-4, 32G NRZ	4.0	52.5x42.5
Intel® Agilex™ Direct RF-Series SoC FPGA AGRM027	2693	17056	20/16	4/12	14/14	287	Yes	58G PAM-4, 32G NRZ	4.0	56x45

Intel® FPGA with Integrated ADC/DACs



- up to 64GSPS sample rate
- EMIB technology
- AIB physical layer protocol

Overview

Stratix 10

Agilex

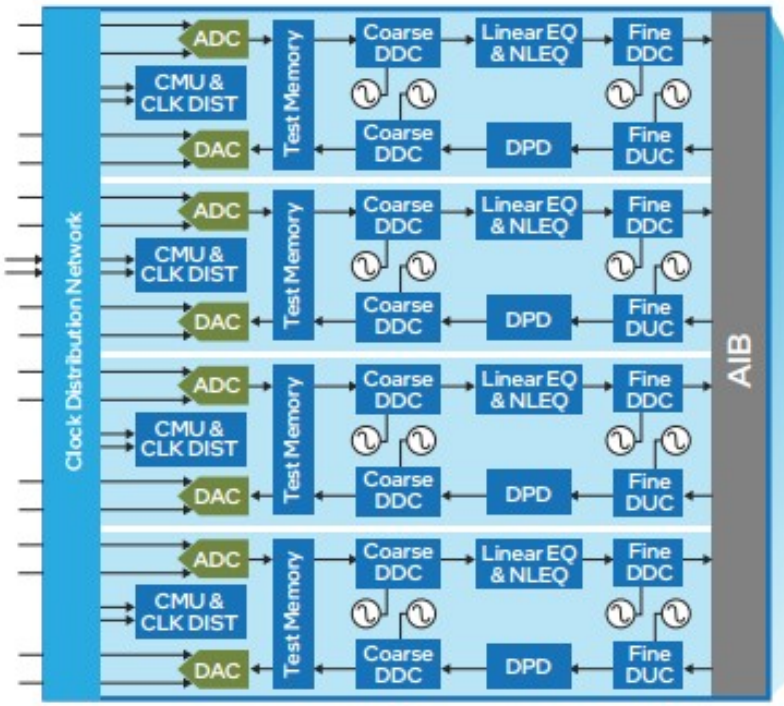
Product Name	Logic Elements (LE)	18x19 Multipliers	# of ADC/DAC	Sample Rate (Gsps)	# of Bits Resolution	Embedded Memory	
Intel® Stratix® 10 AX SOC FPGA 1SA28	2753	11520	8/8	64/64	10/10	244	2 A tiles
Intel® Agilex™ Direct RF-Series SoC FPGA AGRW014	1437	9020	4/4	64/64	10/10	190	1 A tile
Intel® Agilex™ Direct RF-Series SoC FPGA AGRW027	2693	17056	8/8	64/64	10/10	287	2 A tiles
Intel® Agilex™ Direct RF-Series SoC FPGA AGRM027	2693	17056	20/16	4/12	14/14	287	

Wide Band

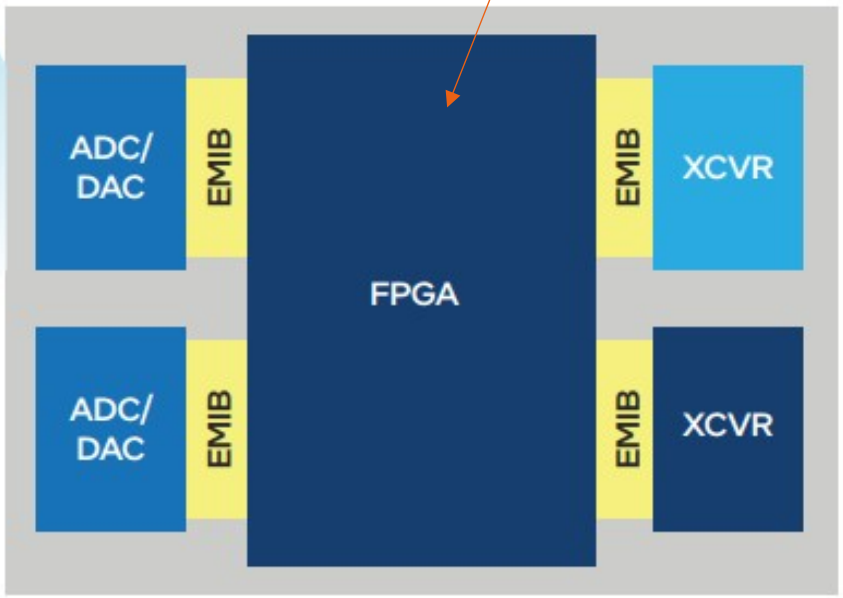
Mid Band

https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/analog-rf-fpga.html

Schematic Representation



high-density, high-performances FPGA



8 ADC and 8 DAC per device

running 64GSPS per ADC or DAC

Block diagram

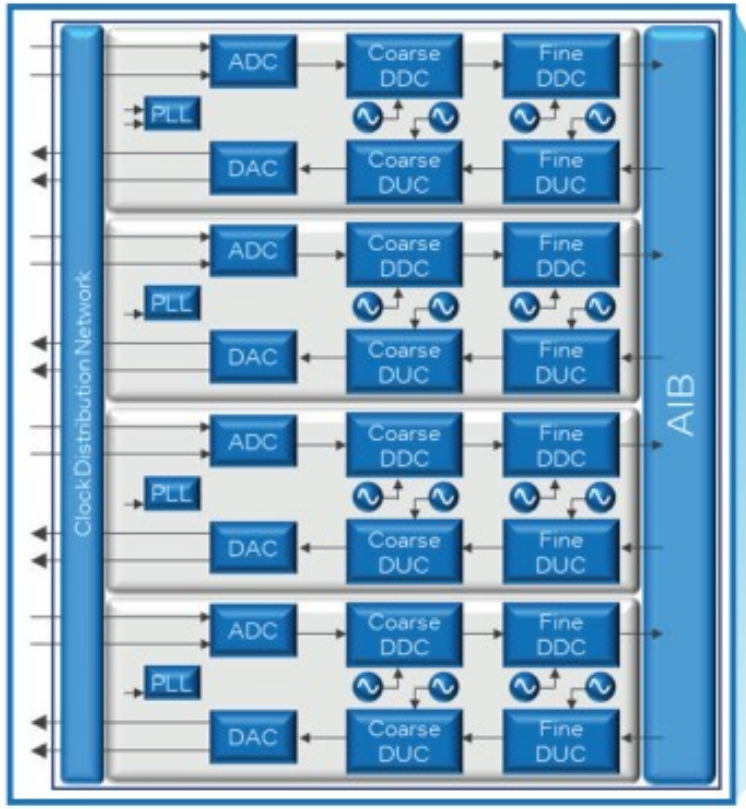
Coarse DDC

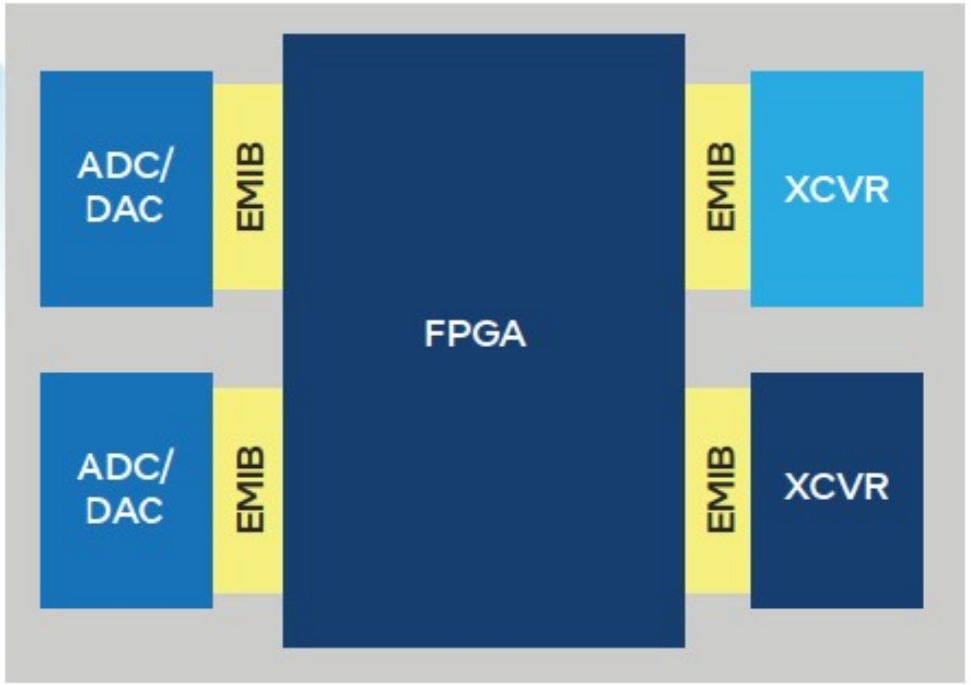
Coarse DUC

Fine DDC

Fine DUC

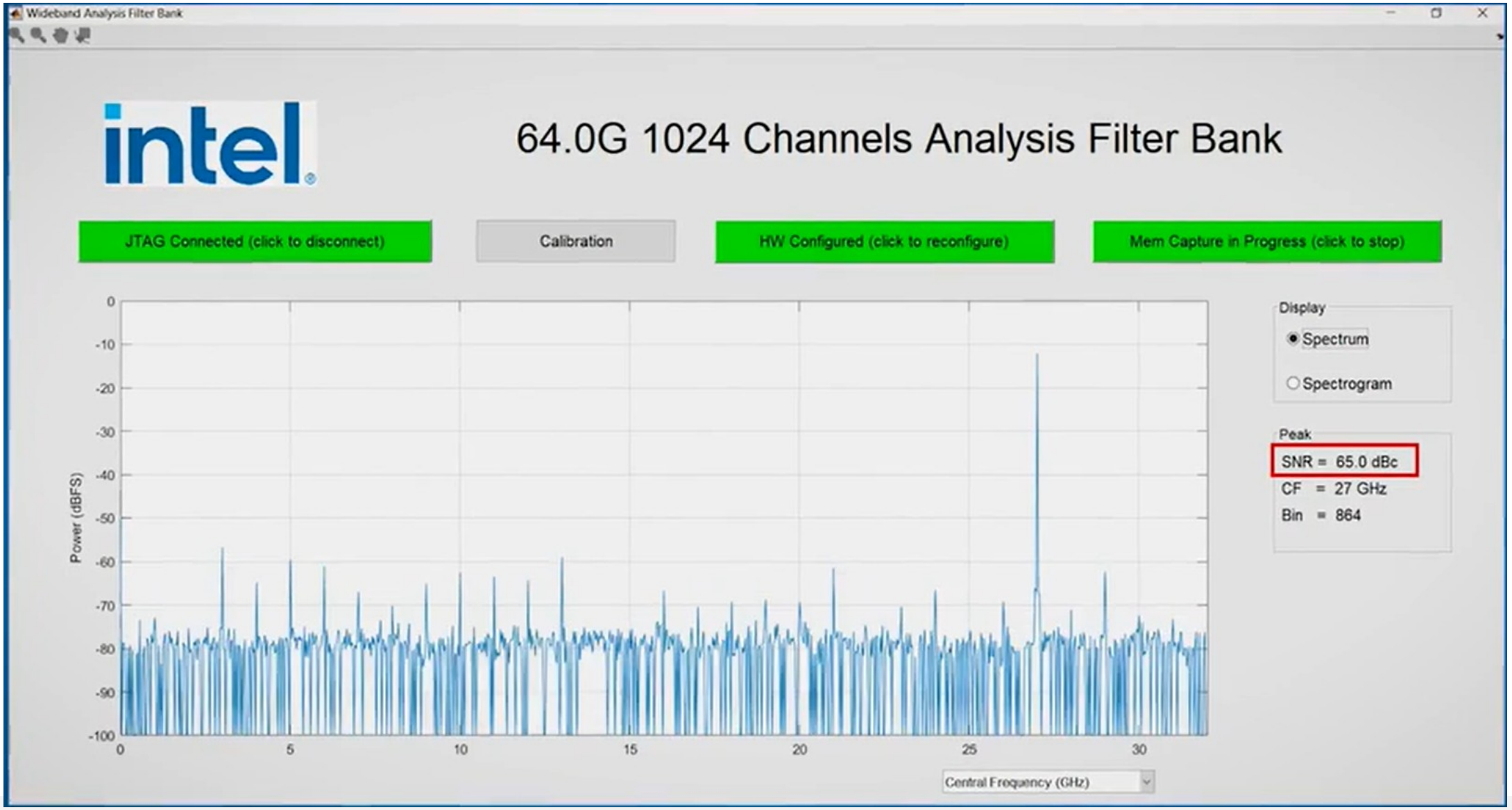
NCOs



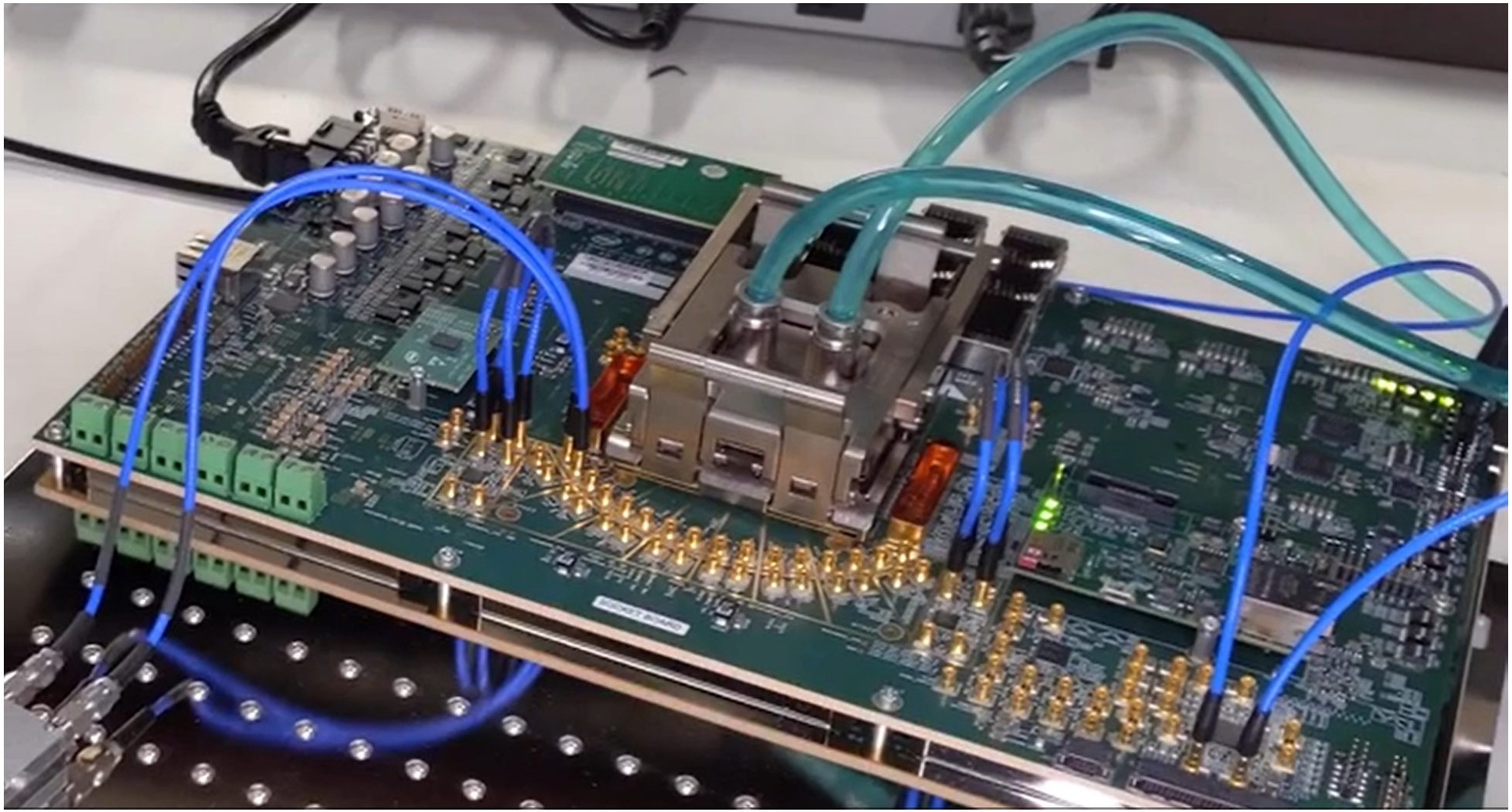


https://www.intel.com/content/www/us/en/architecture-and-technology/programmable/fpga-integrated-data-converter-solution-brief.html

Analog performance: 25GHz of instantaneous bandwidth with a 65 dBc SNR

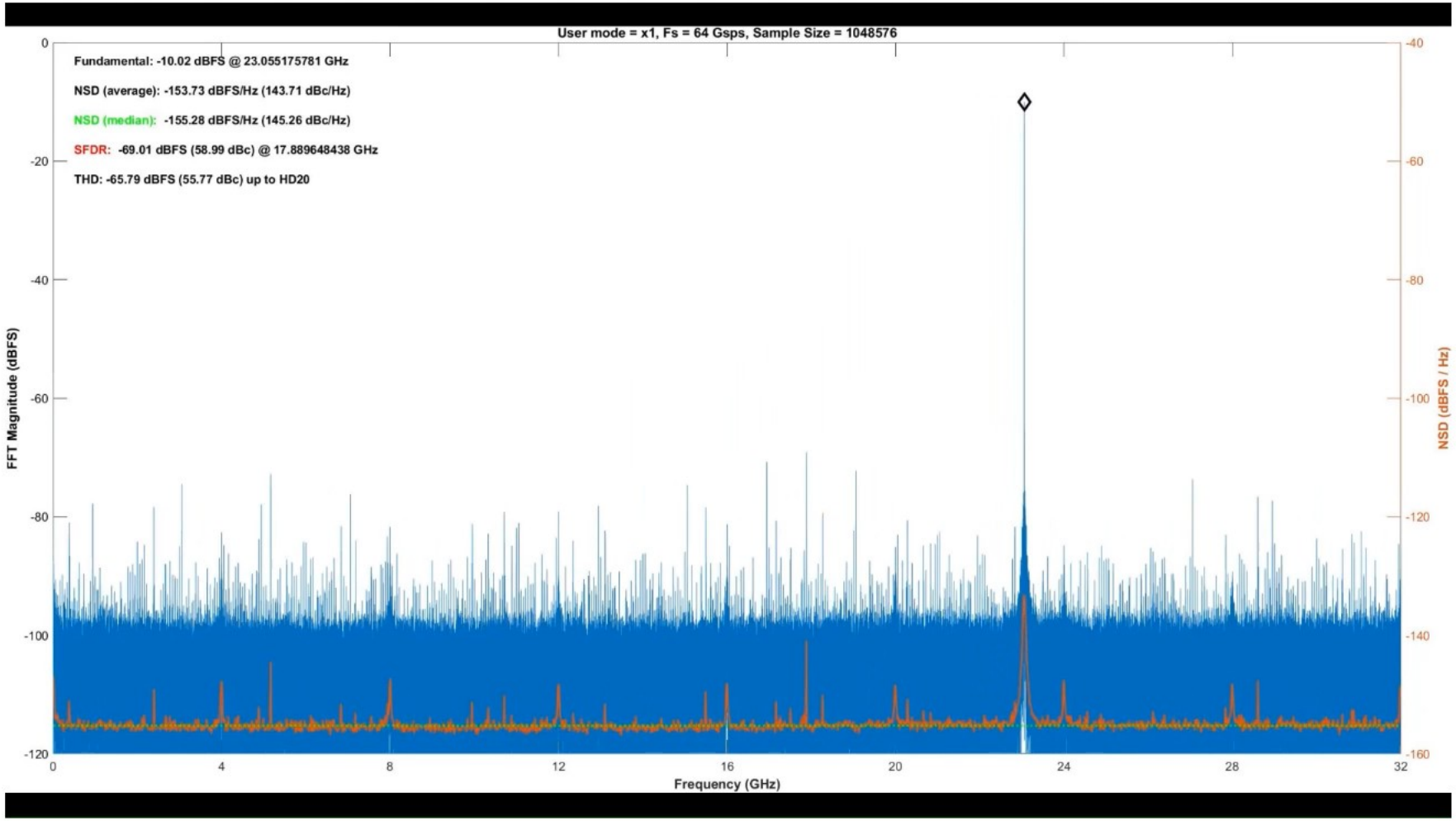


Intel® FPGA with Integrated ADC/DACs board

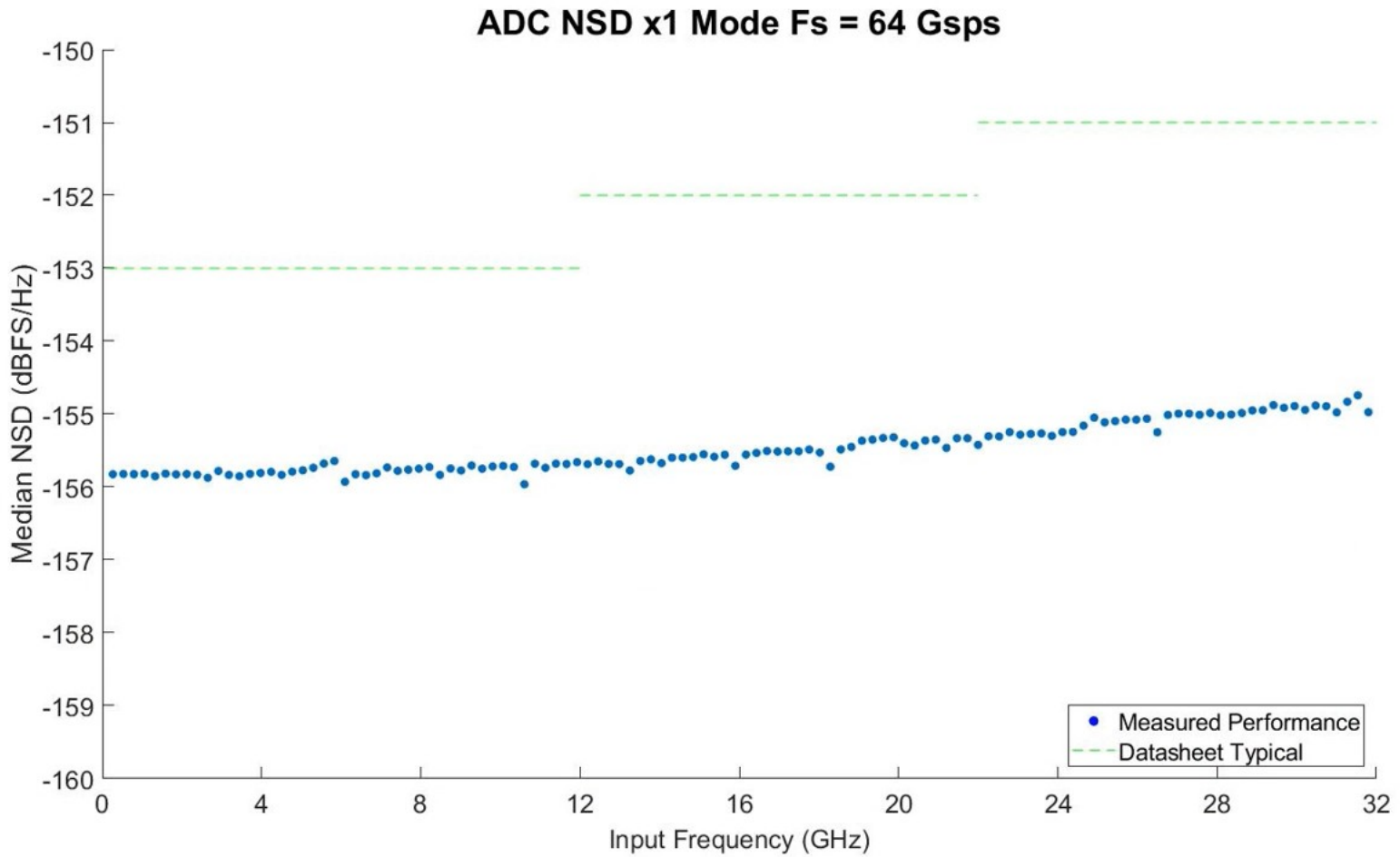


RF performance sweeps

ADC NSD Sweep

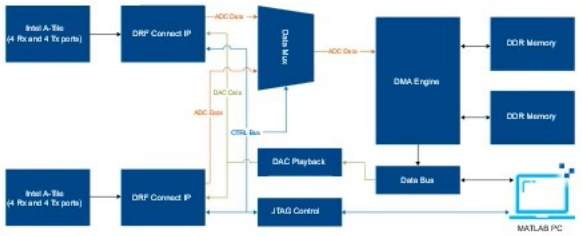


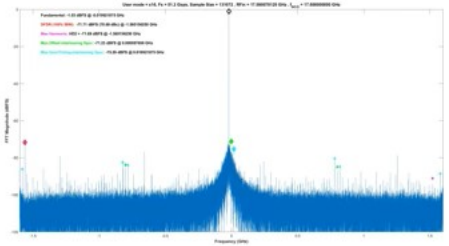
ADC NSD Performance Summary



ADC Spurious Demo

Fs = 51.2 Gsps
Decimate by 16
RF input level = -1 dBFS
Sweep (16 GHz, 19 GHz)





Intel Agilex® 9 FPGA Direct RF-Series Spurious Frequency Calculator

Intel A-tile ADC Spur Calculator

Note: predicted spur locations in this calculator are based on the ADC architecture. Only spur locations, not magnitude are shown. Spurs at some locations may have a very low magnitude and not be visible above the noise floor.

User should fill out boxes in Orange.

Parameter	Value	Unit	Allowed entries	
Fs	64	Gsps	(40, 64)	1. Enter the sample rate.
Fundamental	12.58496	GHz	(0.1, 36)	2. Enter fundamental RF input frequency.
NCO entry option	frequency		[drop down]	3. Select to enter NCO by *frequency* or *coarse step* . Fill out 3a or 3b, accordingly.
NCO frequency entry	12	GHz		3a. Enter the *NCO frequency*.
Coarse NCO step entry	22	step	(-64, 63)	3b. Enter *coarse NCO step* .
Decimation factor	16		[drop down]	4. Select decimation factor.
NCO frequency	12	GHz		NCO frequency result calculated from User inputs.
IBW	4	GHz		IBW result calculated from User inputs.

Highlighted spur locations are present inside the IBW.

Harmonic Calculator

Name	Harmonics (GHz)
Fundamental	0.585
HD2	13.170
HD3	14.245
HD4	1.660
HD5	-10.925
HD6	-0.490
HD7	12.095
HD8	15.320
HD9	2.735
HD10	-9.850
HD11	-1.565
HD12	11.020
HD13	16.396
HD14	3.811
HD15	-8.774
HD16	-2.641
HD17	9.944
HD18	17.471
HD19	4.886
HD20	-7.699

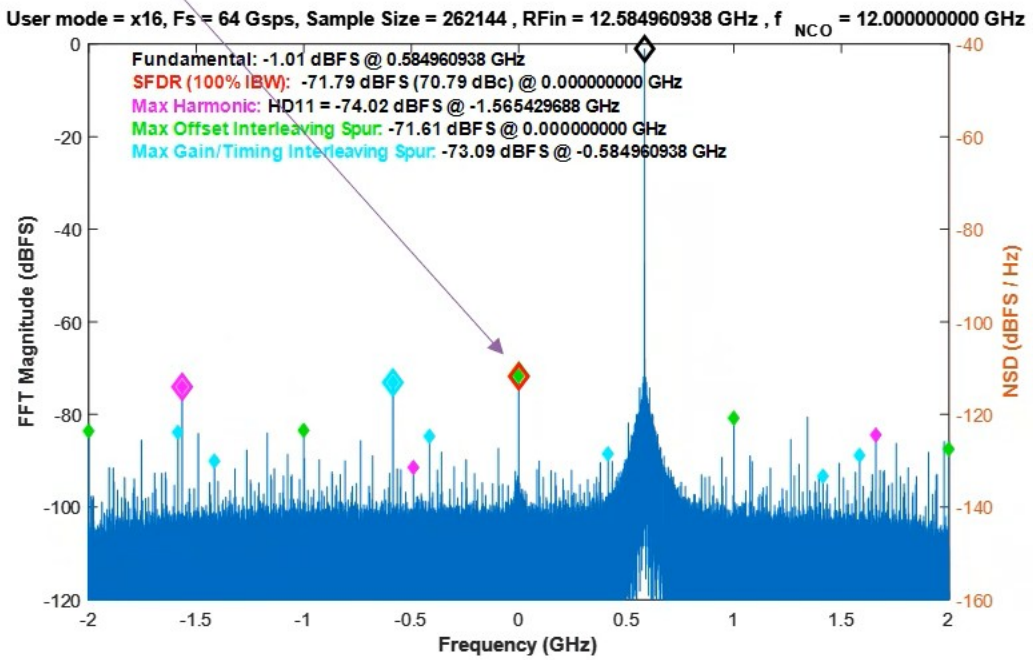
Interleaving Spur Calculator

Index	Gain and Phase Spurs (GHz)		Offset Spurs (GHz)
32	0.585	0.585	-12.000
0	-0.415	1.585	-11.000
1	-1.415	2.585	-10.000
2	-2.415	3.585	-9.000
3	-3.415	4.585	-8.000
4	-4.415	5.585	-7.000
5	-5.415	6.585	-6.000
6	-6.415	7.585	-5.000
7	-7.415	8.585	-4.000
8	-8.415	9.585	-3.000
9	-9.415	10.585	-2.000
10	-10.415	11.585	-1.000
11	-11.415	12.585	**0.000**
12	-11.585	13.585	1.000
13	-10.585	14.585	2.000
14	-9.585	15.585	3.000
15	-8.585	16.585	4.000
16	-7.585	17.585	5.000
17	-6.585	18.585	6.000
18	-5.585	19.585	7.000
19	-4.585	19.415	8.000
20	-3.585	18.415	9.000
21	-2.585	17.415	10.000
22	-1.585	16.415	11.000
23	-0.585	15.415	12.000
24	0.415	14.415	13.000
25	1.415	13.415	14.000

Sampler Spur Calculator

Spur Index	Spurs (GHz)
1	-8.000
2	-4.000
3	0.000
4	4.000
5	8.000
6	12.000
7	16.000

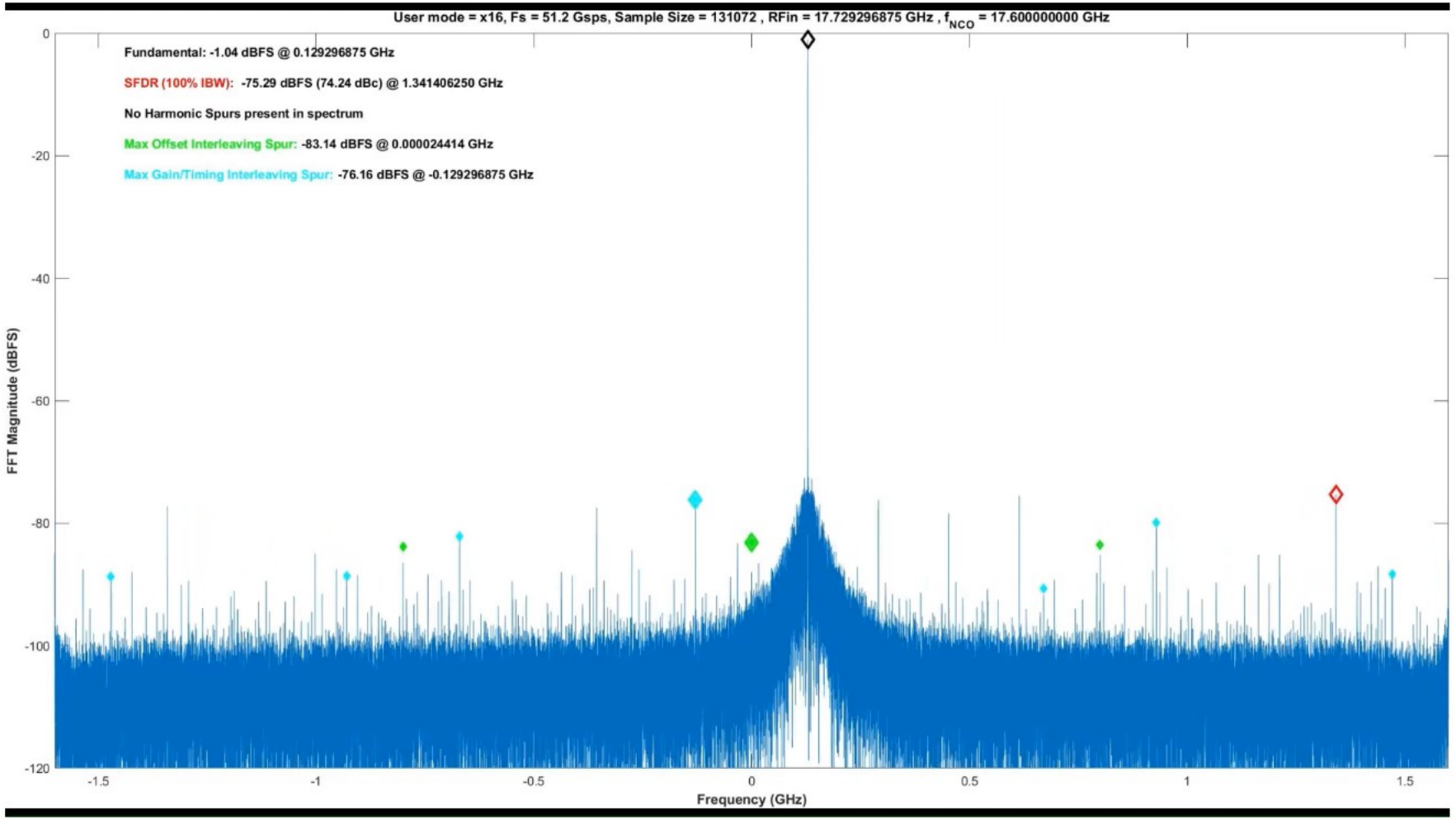
Largest spur



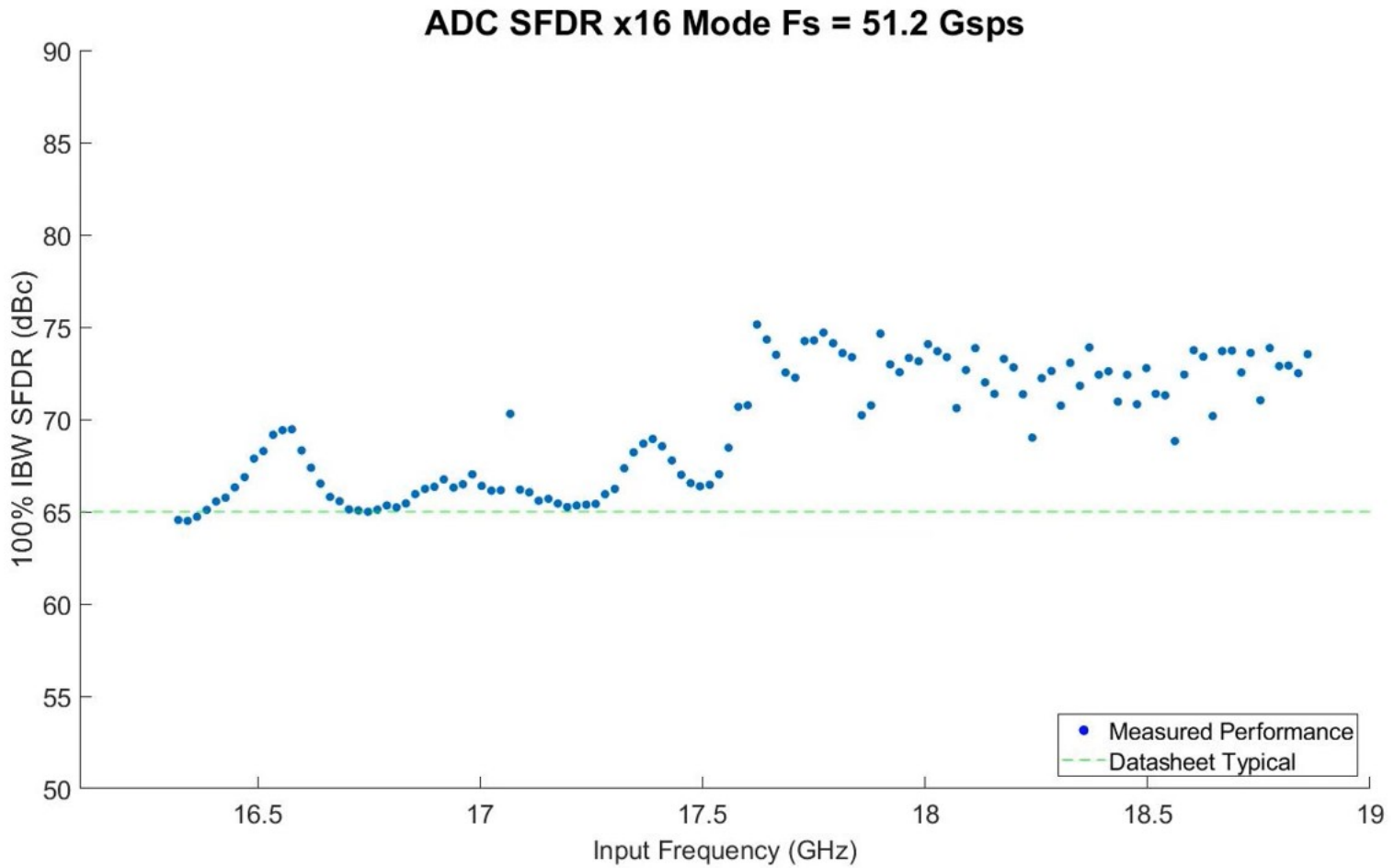
Excel-based Spur Calculator

EVP Spur Calculator analysis mode

ADC Spurious Performance Sweep

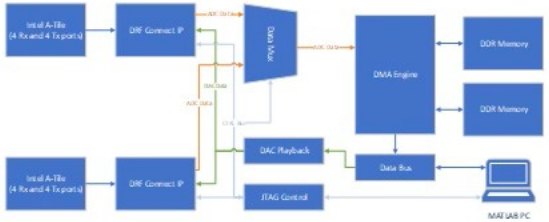


ADC Spurious Performance Summary

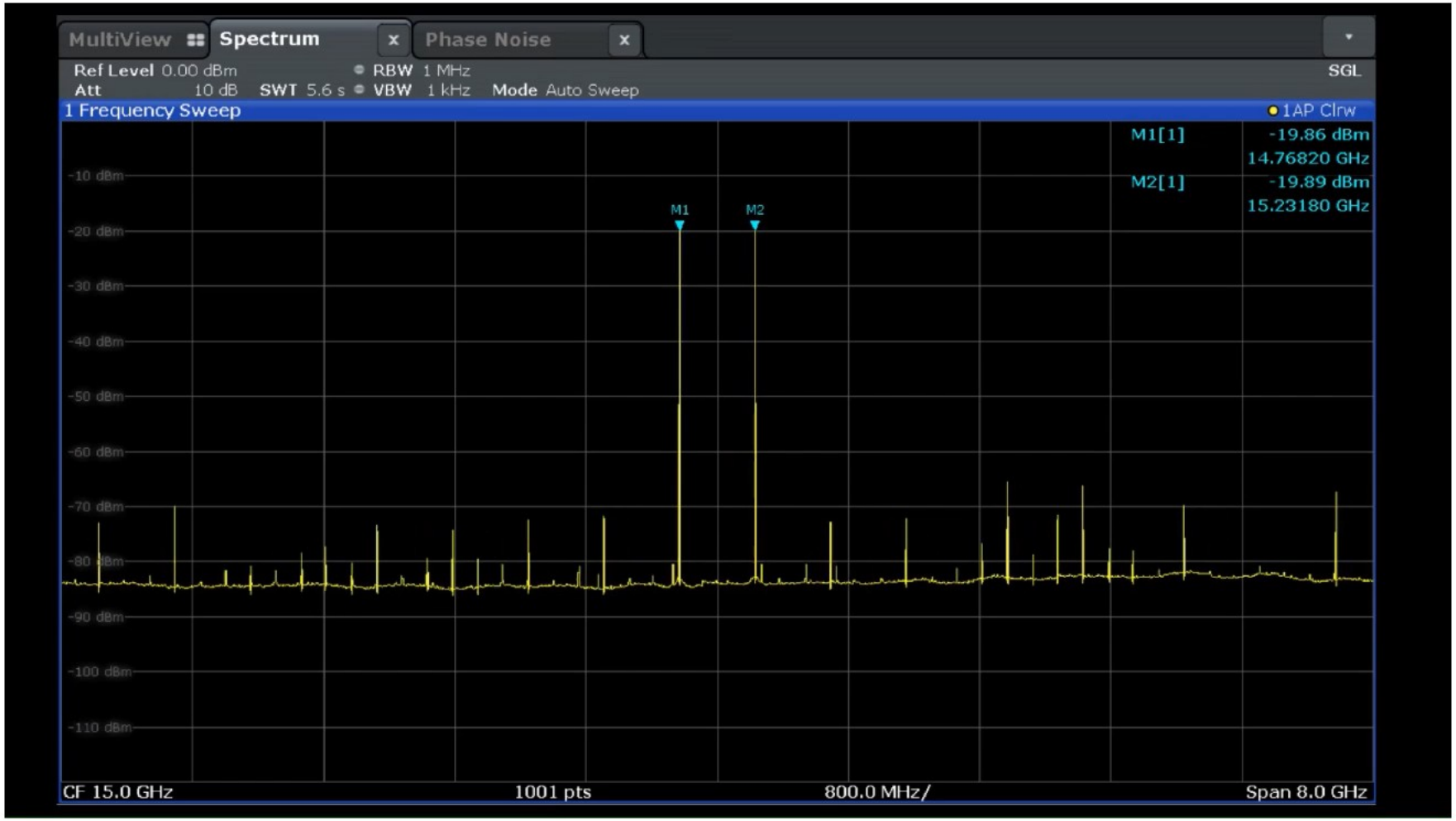


DAC IMD Demo

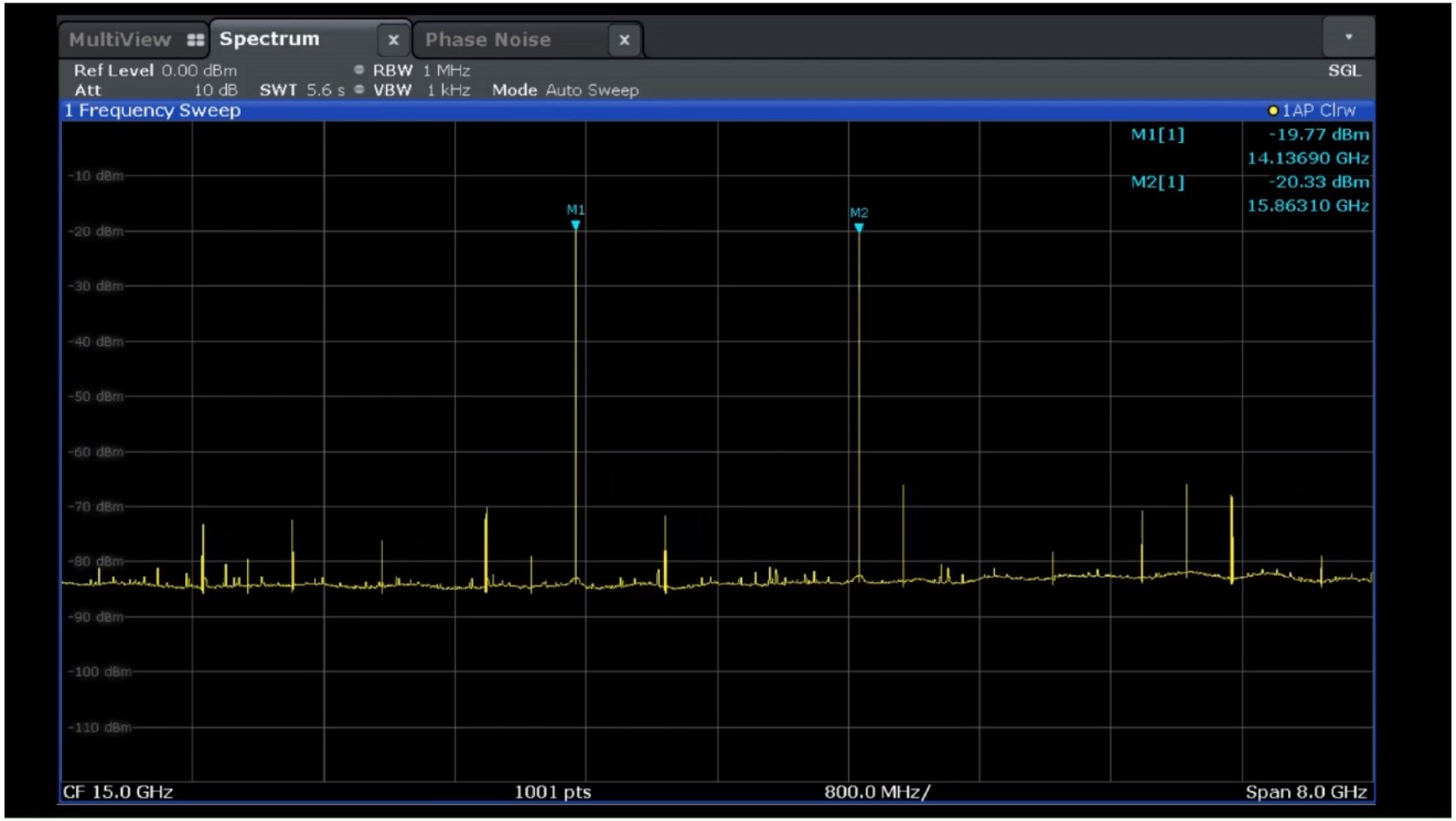
Fs = 64 Gsps
Interpolate by 8
Two tones: RF output level = -7 dBFS
Sweep tone spacing, level, and f_C = (12 GHz, 18 GHz)



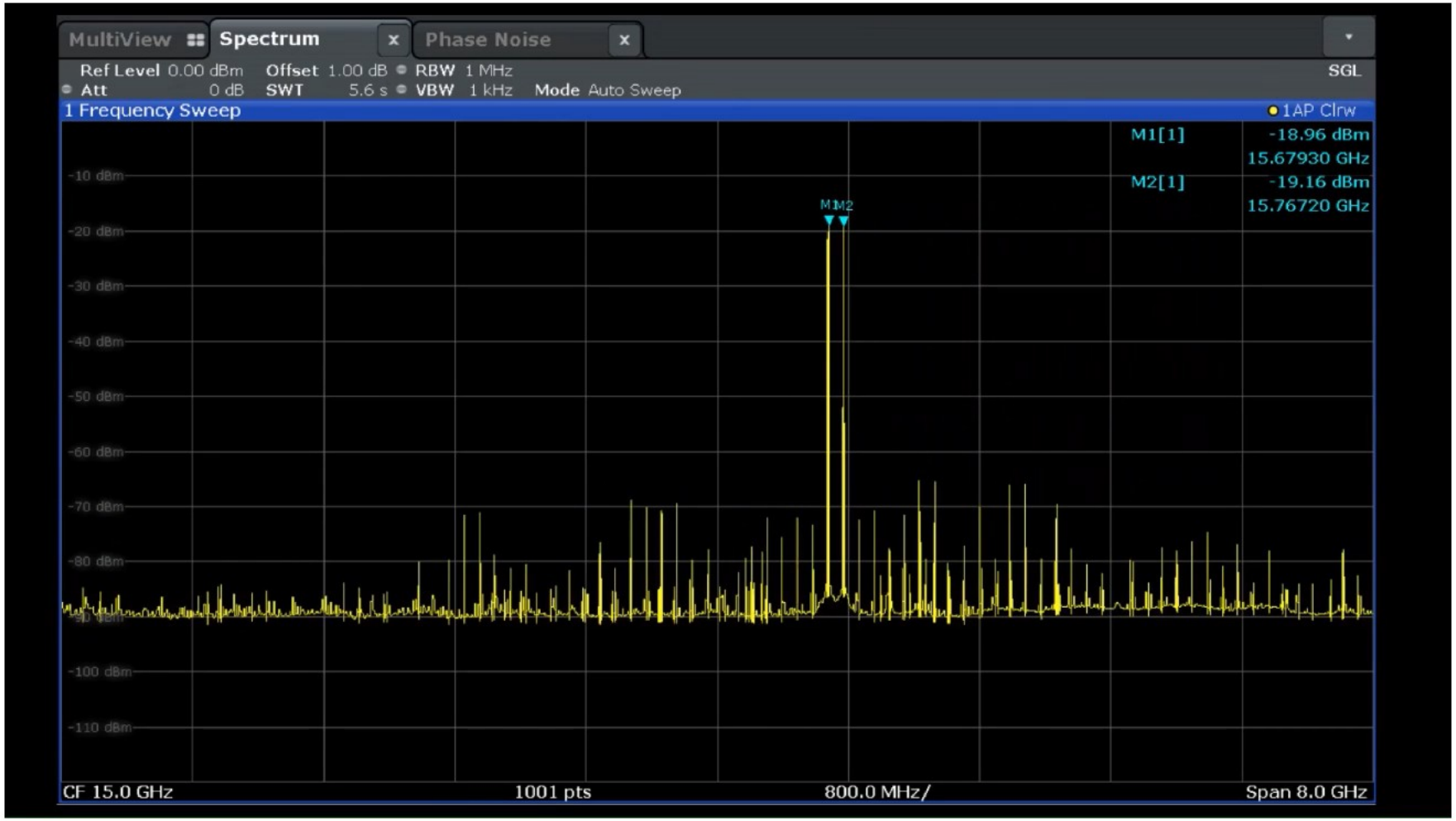
DAC IMD Sweep



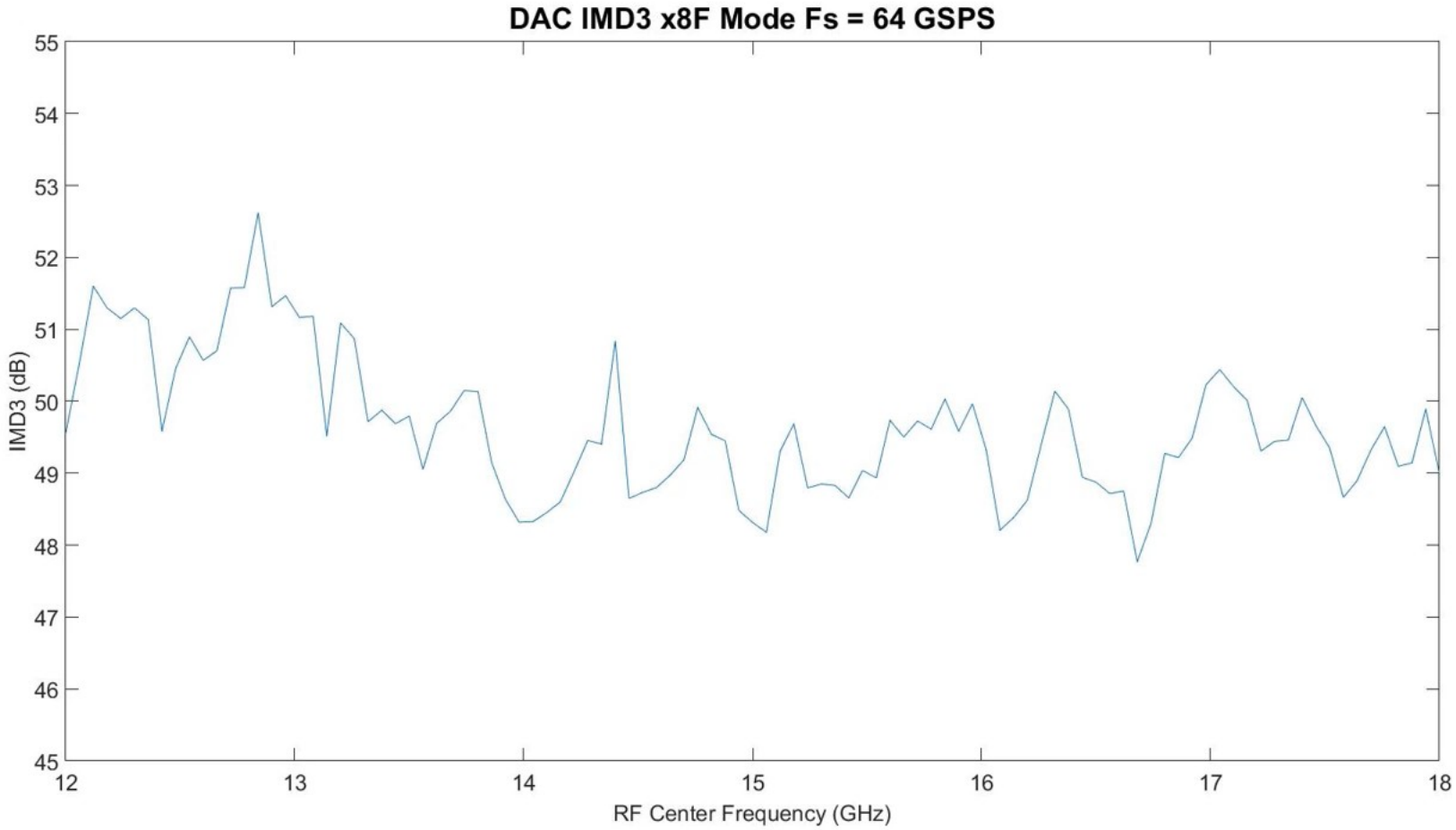
DAC IMD Sweep



DAC IMD Sweep



DAC IMD Performance Summary

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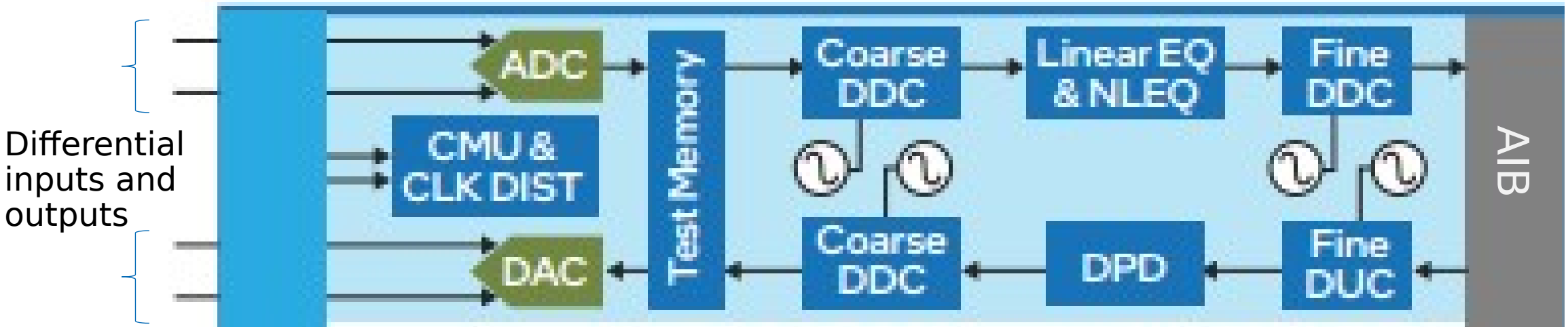
ADC/DAC details: 64Gsps with 25GHz of instateneous bandwidth and with a 65 dBc SNR



Data converter chiplets include Numerically controlled Oscillators (NCOs) and integrated Digital Up Converters (DUCs) and Digital Down Converters (DDCs) that eleminate a substantial amount of analog circuitry

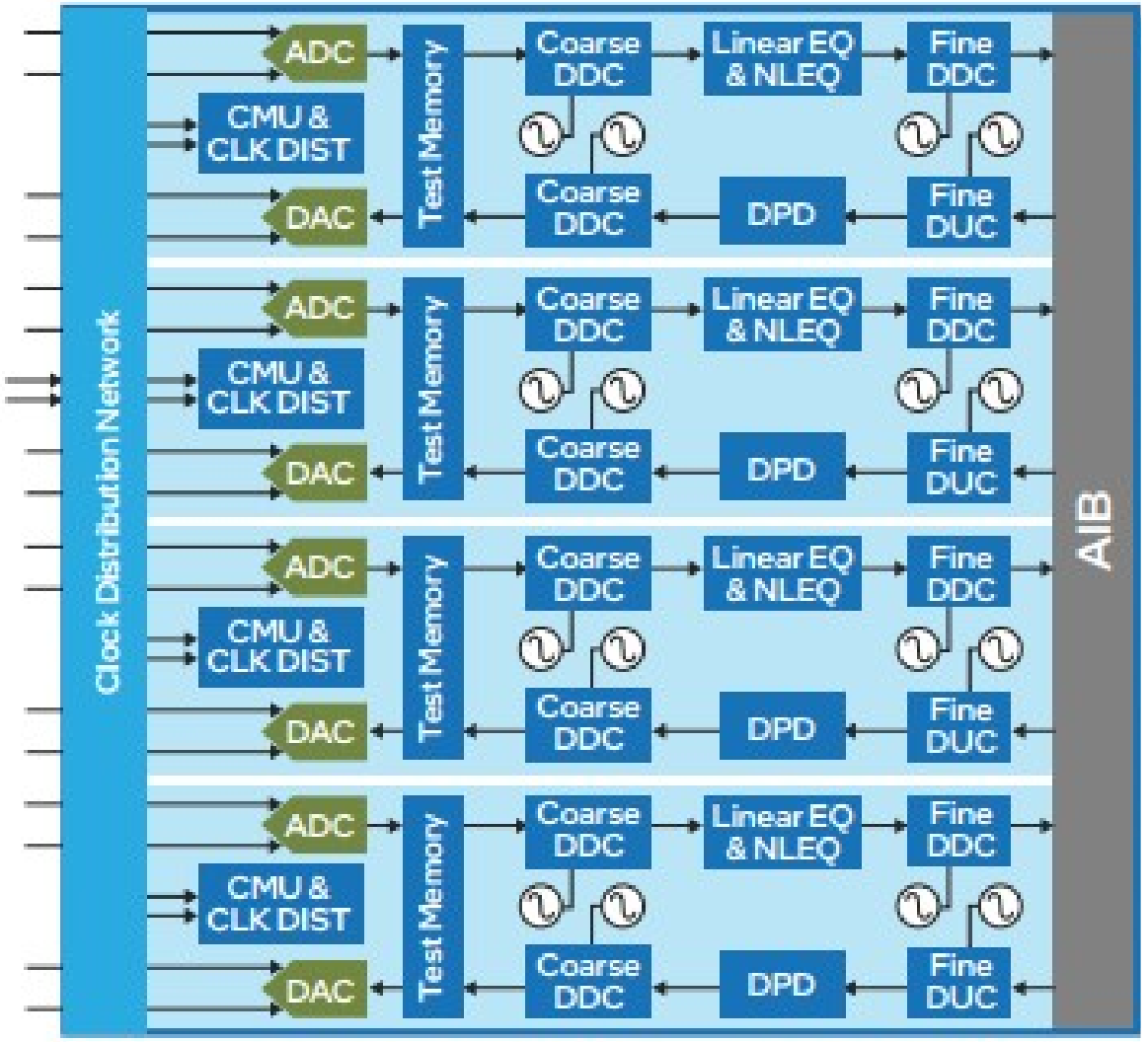
Tile architecture

Clocking

- Clock Distribution Network
- External clocking
- Per channel CMU pll

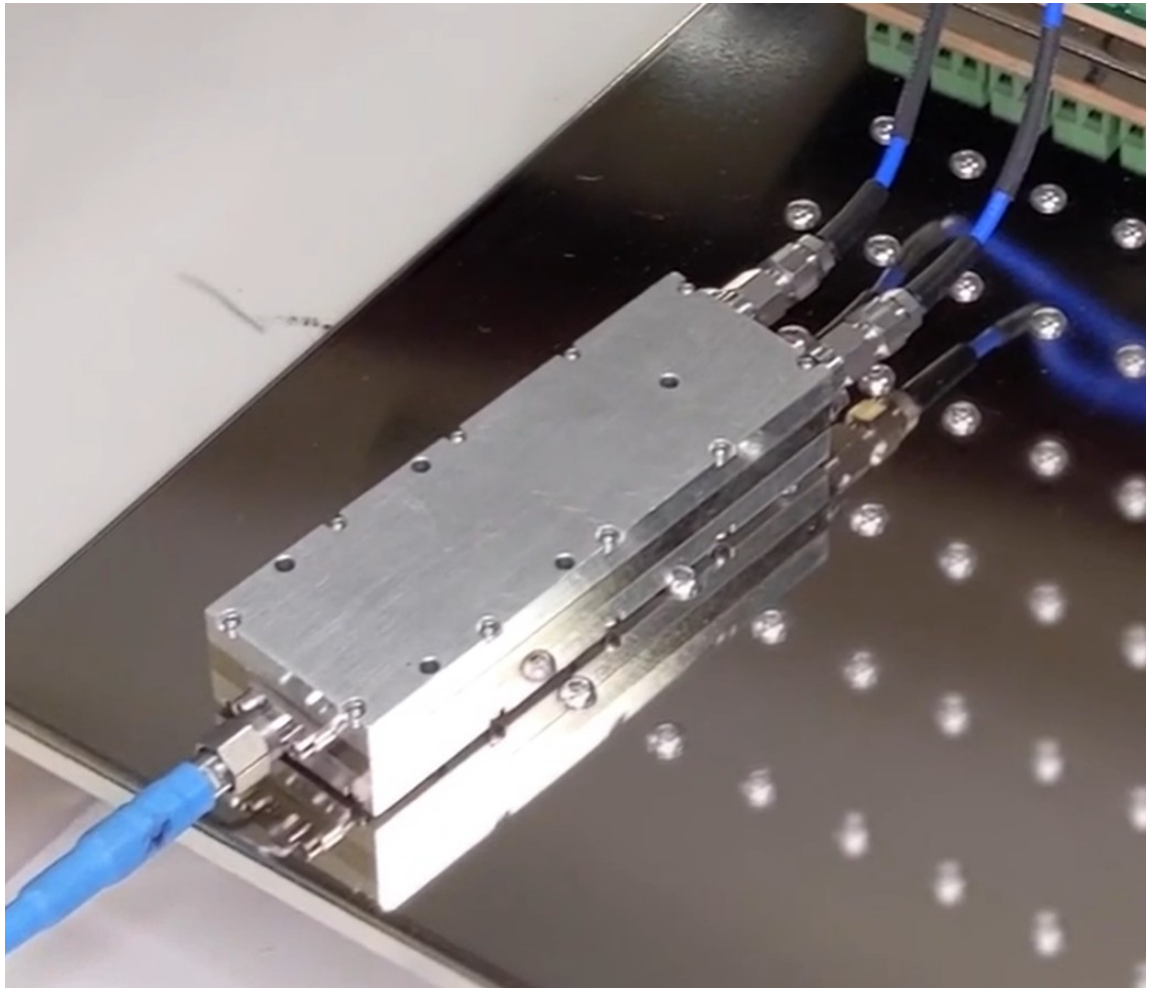
AIB

- Data flexibility
- 1Tbit bandwidth



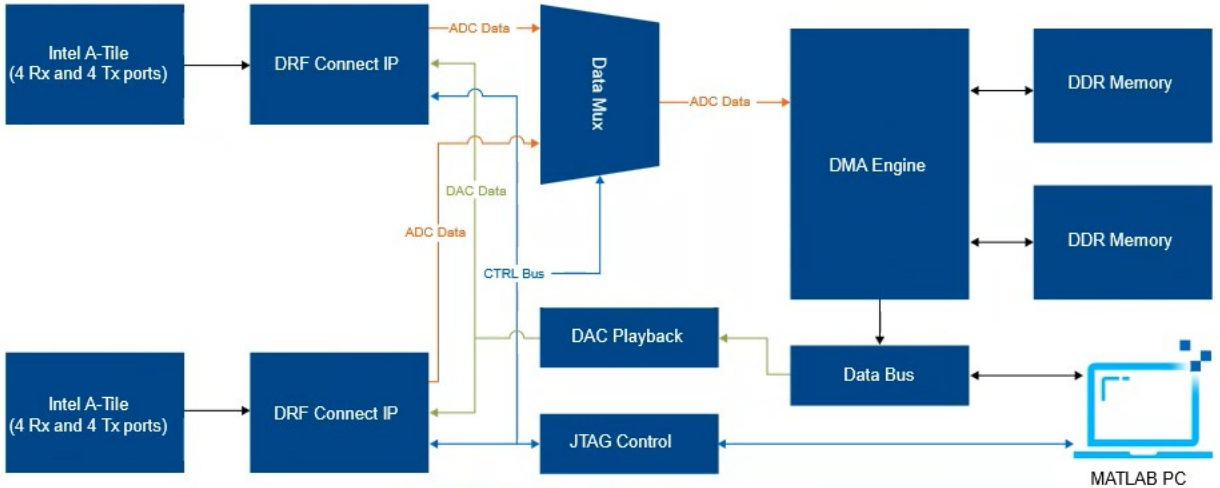
Differential inputs

- A wideband balum is used to convert from common mode to differential inputs

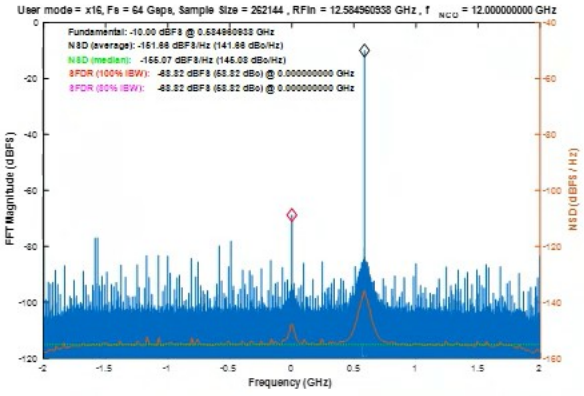


Intel Agilex® 9 FPGA Direct RF-Series Evaluation Platform (EVP)

Testbench enablement

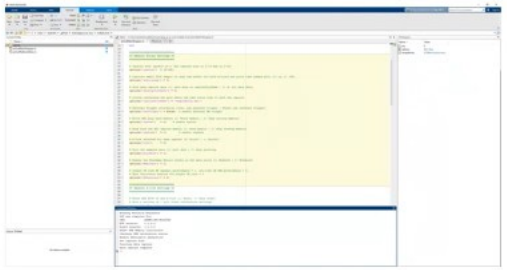


EVP Block Diagram

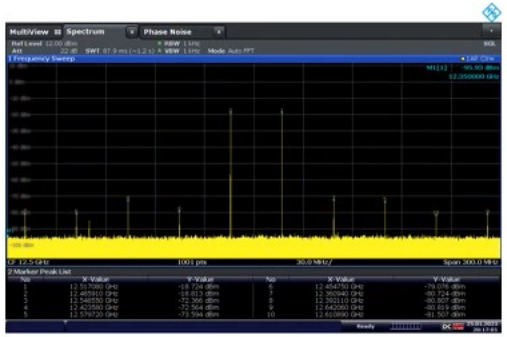


ADC capture

Intel Agilex® 9 FPGA Direct RF-Series Development Kit



MATLAB script interface



DAC capture

ADC NSD Demo

Fs = 64 Gsps
No decimation
RF input level = -10 dBFS
Sweep entire first Nyquist zone