SiW-ECAL for CALICE, LUXE and Higgs Factories

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Plan

Introduction

Problématiques et buts : les detecteurs aux usines à Higgs

Prototypes (≤2026)

- CALICE
- LUXE

Developpements (≥2026)

pour les usines à Higgs/Top/EW (HET)

Compléments :
ASICs [CdlT]
DRD calo [RP]

Highly-Granular ECAL at Higgs Factories for Particle Flow Approach based detectors

Full Reconstruction of single particles

- Charged measured mostly from trackers
- Neutrals only measured from calorimeters

➡ **Large Tracker**

- Precision and low X_0 budget
- Pattern recognition

➡ **High precision on Si trackers**

- Tagging of beauty and charm

Large acceptance

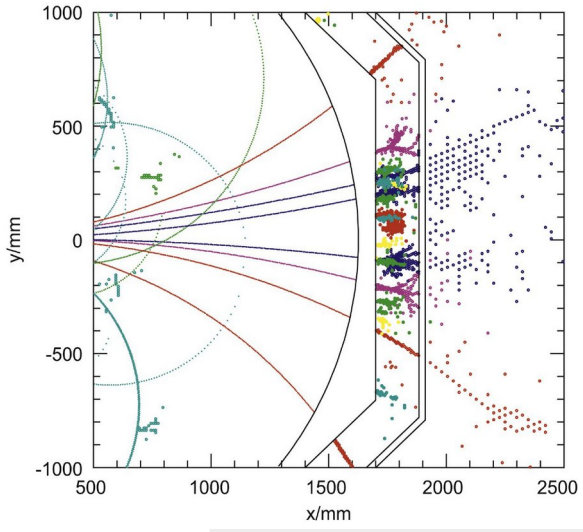
➡ **Highly Granular Imaging Calorimetry**

Particle Flow Algorithms : **ECAL**

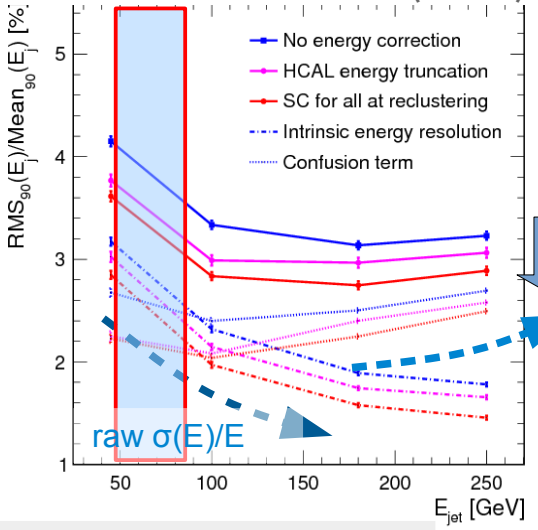
- Jets = 65% charged Tracks + 25% γ ECAL + 10% h^0 E+HCAL
- TPC $\delta p/p \sim 5 \cdot 10^{-5}$; VTX $\sigma_{x,y,z} \sim 10$ μm

τ tagging + timing

H. Videau and J. C. Brient, "Calorimetry optimised for jets," (CALOR 2002)



Pandora PFA: EPJ C77 (2017) 10, 698



Software Weigthing

Confusion (cluster misattrib, merging)

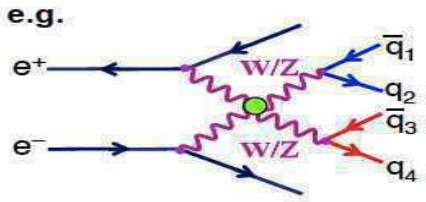
Low E jets ⇒ where PFA brings most

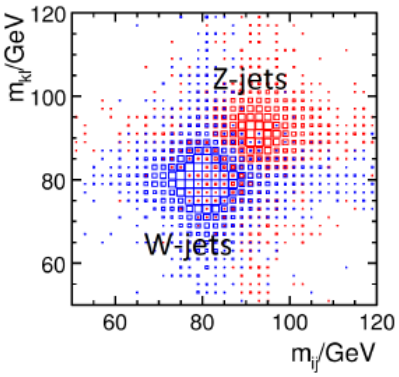
Particle Flow Detectors at Higgs Factories

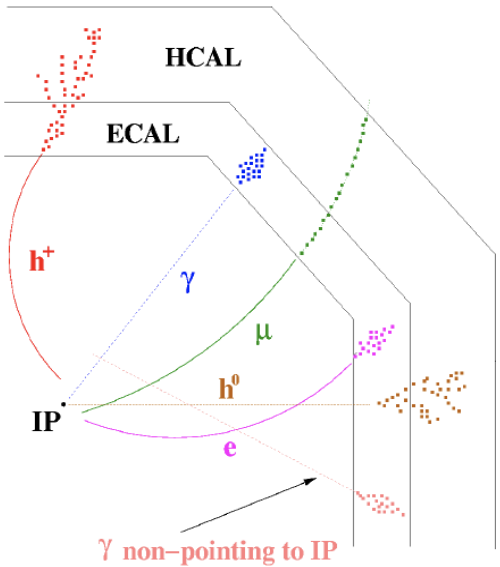
Basis: sep of H → WW/ZZ → 4j

– $\sigma_Z/M_Z \sim= \sigma_W/M_W \sim= 2.7\% \oplus 2.75\sigma_{sep}$

$\Rightarrow \sigma_E/E$ (jets) < 3.8%



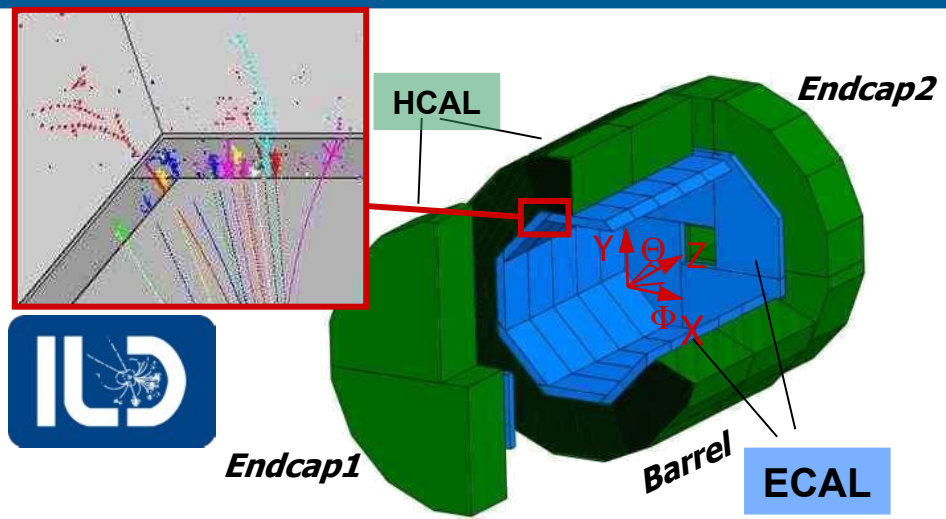




Particle Flow ECAL should :

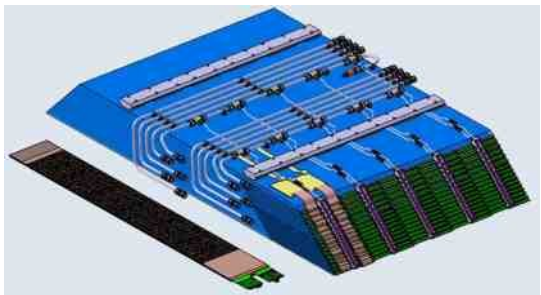
- spot tracks & showers from charged ($h^{\pm}$, $e^{\pm}$)
- measure Photons in jets & Tau physics (γ vs π_0)
- measure 2/3 of neutral hadrons interacting in the ECAL
- measure Time-of-Flight (10's ps)

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (E, (θ,φ), t)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)

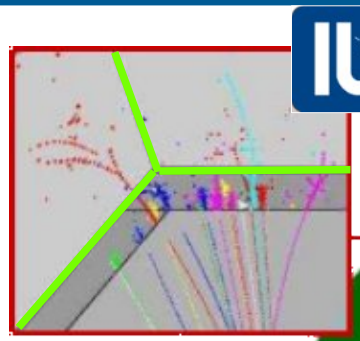


SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design: Sensor+RO≤2mm
  - Allows for ~any pixelisation
  - Robust technology
  - Excellent signal/noise ratio: ≥10
  - Intrinsic stability (vs environment, aging)
  - Albeit expensive…
- Tungsten–Carbon alveolar structure
  - Minimal structural dead-spaces
  - Scalability

To be assessed by prototypes

Modular & Transverse Constraints



HCAL

Endcap2

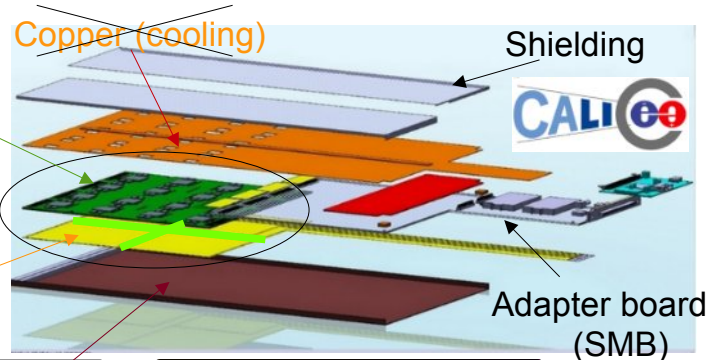
Endcap1

Barrel

ECAL

B = 3.5 T

PCB (FeV)
16 SK2 ASICs
1024 channels
ASU
Wafer (4)

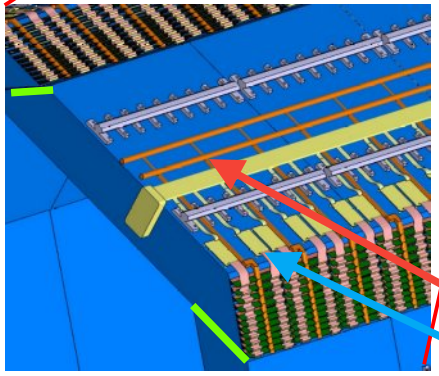


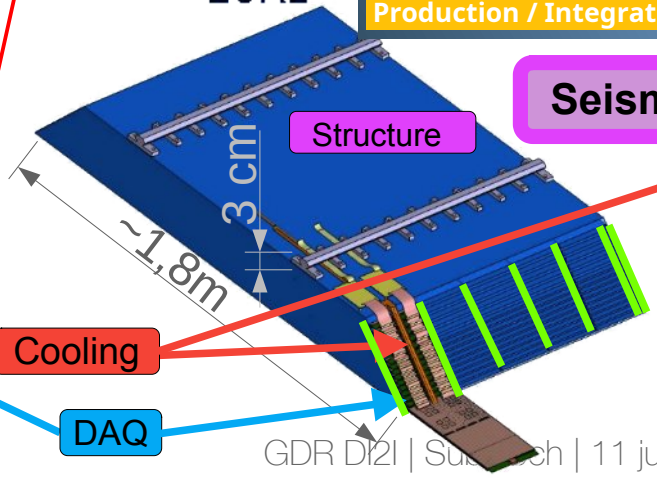
Carbon+W

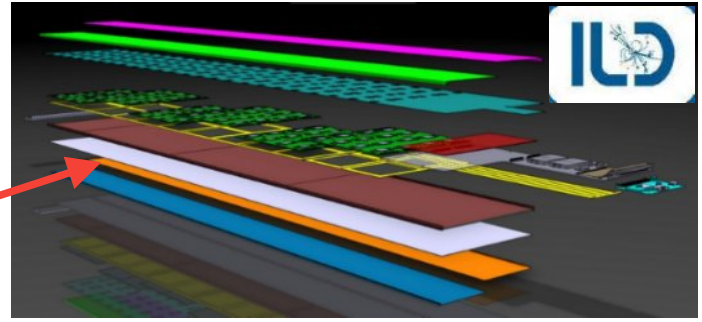
U layout of a **short slab**

- Physical
- Instrumental
- Electronics
- Mechanical
- Thermal
- Production / Integration

Seismic







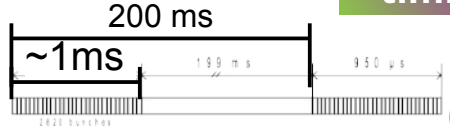
U layout of a **long slab**

+ timing

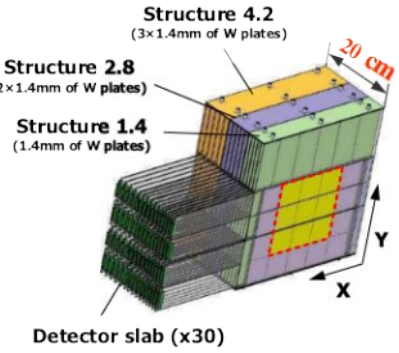
Cooling

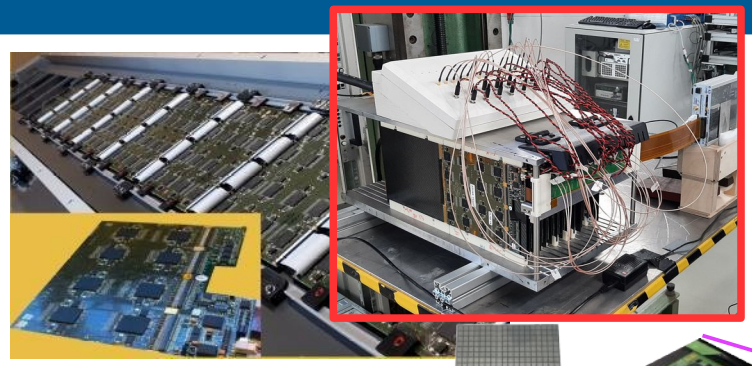
DAQ

PP ↔ Cont

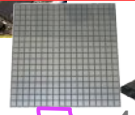


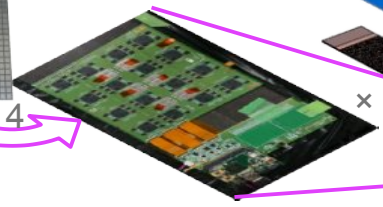
Timeline of SiW-ECAL Prototypes

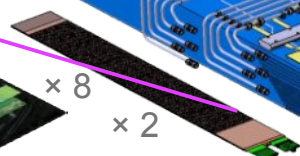


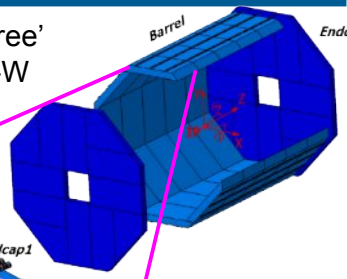


'dead space free'
Carbon Fibre-W
Structure









Physical (2005-11)

- 1×1 cm² on 500µm 6×6 cm²
  Pad glued on PCB
  Floating GR
- × 30 layers (10k chan).
- External readout
- Proof of principe

Technological (now)

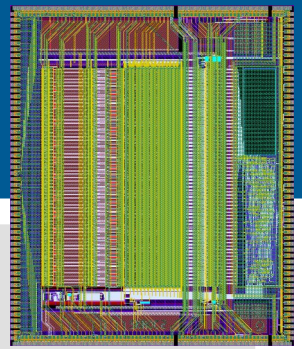
- Embedded electronics
  - Power-Pulsed, Auto-Trig, delayed RO
  - S/N = (MPV/σ_{Noise}) ≥ ~12 (trig)
- Compatible w/ 8+ modules-slab
- 5×5 mm² on 320–650µm 9×9 cm²
  × 26–30 layers
  - 8k (slab) ~ 30k (calo) channels

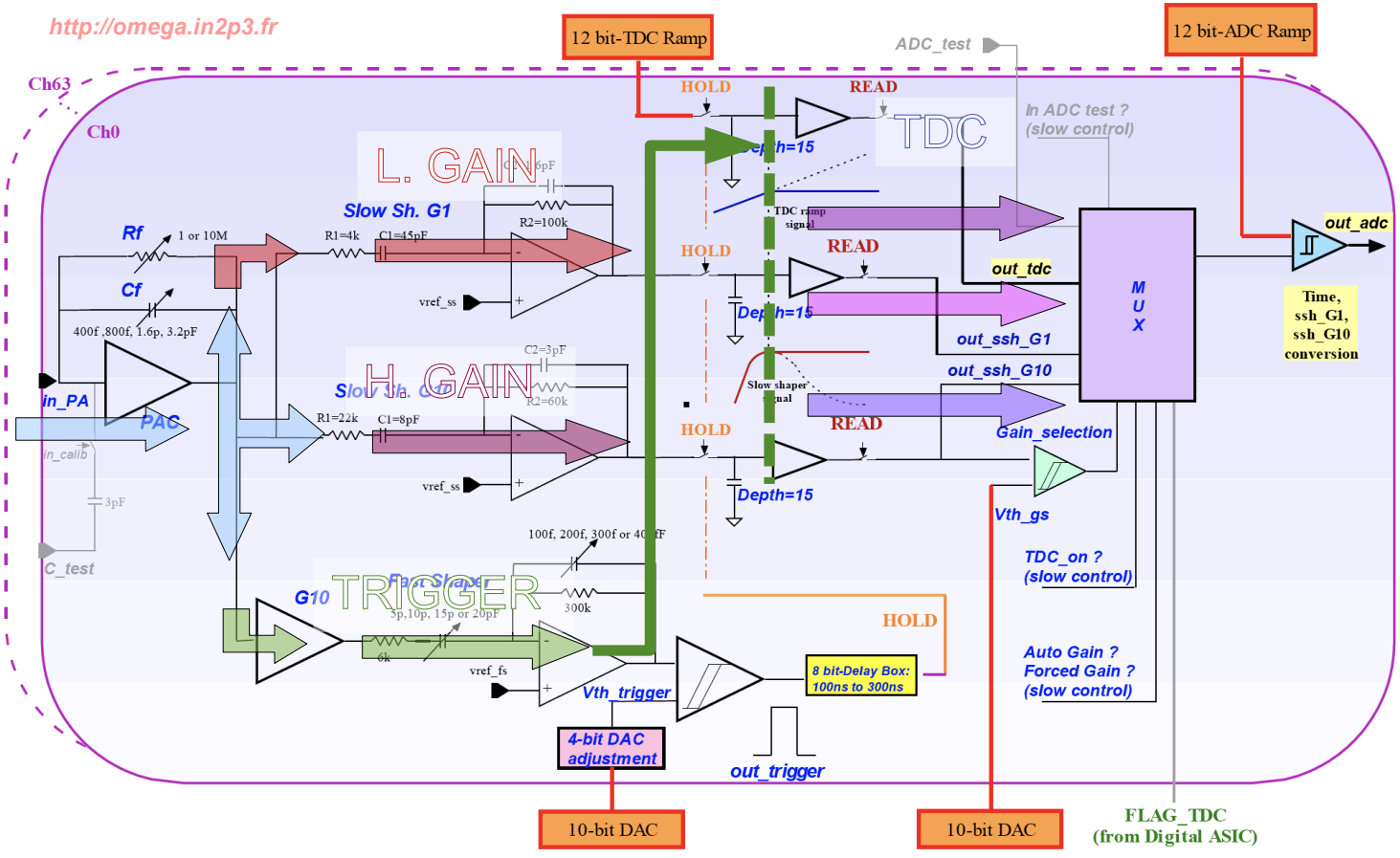
We are here

Pilote ➡ Full Detector

- 1M
  70M channels
- on 750µm 12×12 cm² 8" Wafers ?
- Pre-industrial building
- Full integration (⊃ cooling)
- Final ASIC

SKIROC2 / 2A Analogue core



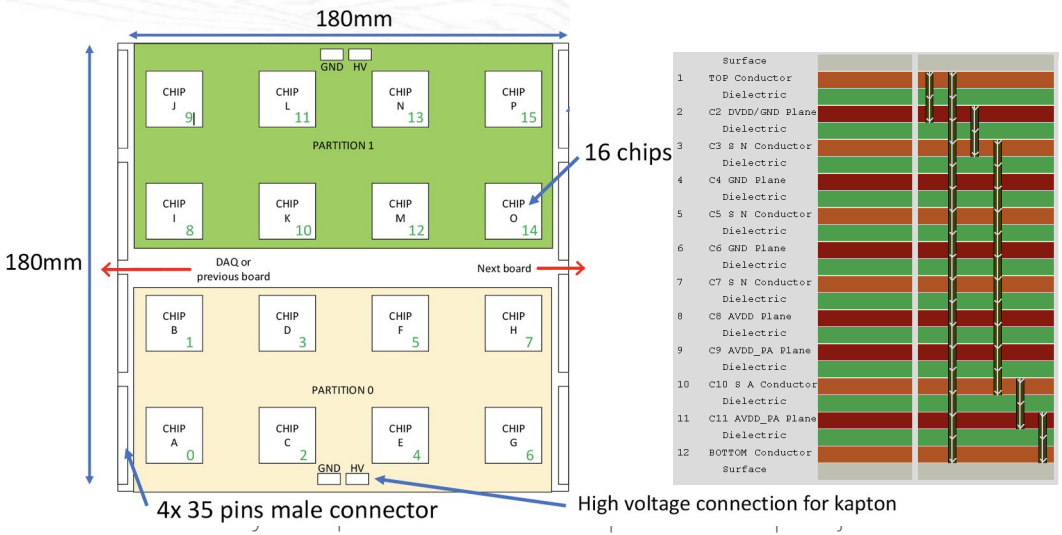


- **64 channels**
- **Auto-triggered**
  - per cell adj.
  - 1 cell triggers all
- Preamp
  + **2 Gains** + Auto-select
  + **TDC** (~1.4ns)
- 15 (×2) analogue memories
- Dyn range 0.1 ~ 2500 mips
  - mip in 320 µm (4 fC)
  - 12 bits ADC's
- *616 config bits*
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-Pulsed

FEV's : 15 years of R&D

Most complex element:
electro-mechanical integration

- Powering, Distrib / Collect signals from ASICs, Analog & Digital with dyn. range ≥ 7500
  - Single End operation → Chaining for 8–10 boards
- **Mechanical** placer & holder for Wafers
  → ≤ 50µm lateral precision, flatness
- **Thickness** constraints → Calorimeter Compactness

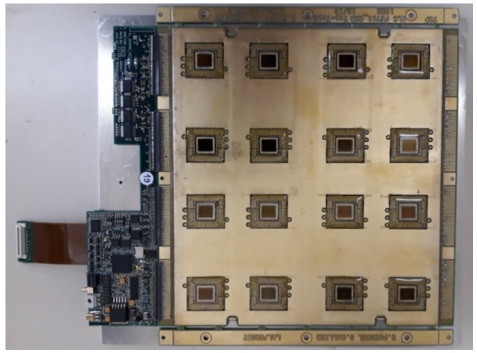


Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, ≤ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st PCB proto	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	S/N ≤ ~ 14 (H Gain), no Power Pulsing retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, Power Pulsing
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (H Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	10 units	Noise issues
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 (12)$_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	FEV11, 12 13 Compact Calo Long Slab	SK2 & SK2a (⊃timing) 8 ASUs	Improved S/N Timing enabling
1st working COB, new DAQ	2019	FEV-COB	2×1/4 ASUs Cont. power.	Technical
2nd tech ECAL	20–22	5 types FEV's	H. Gain, Cont. Power	320, 500, 650 µm

Present ‘FEV-zoo’

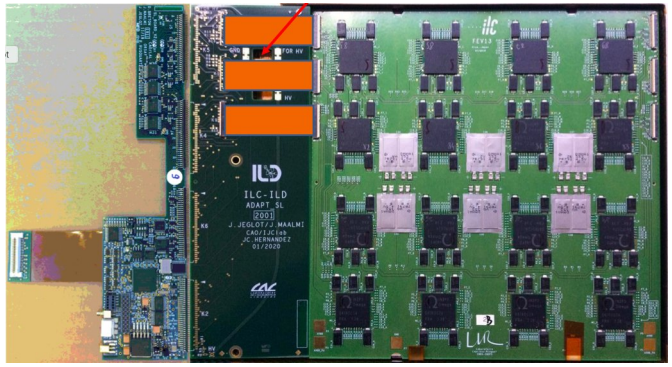
FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main “Working horses” since 2014



FEV-COB

- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible



FEV13

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

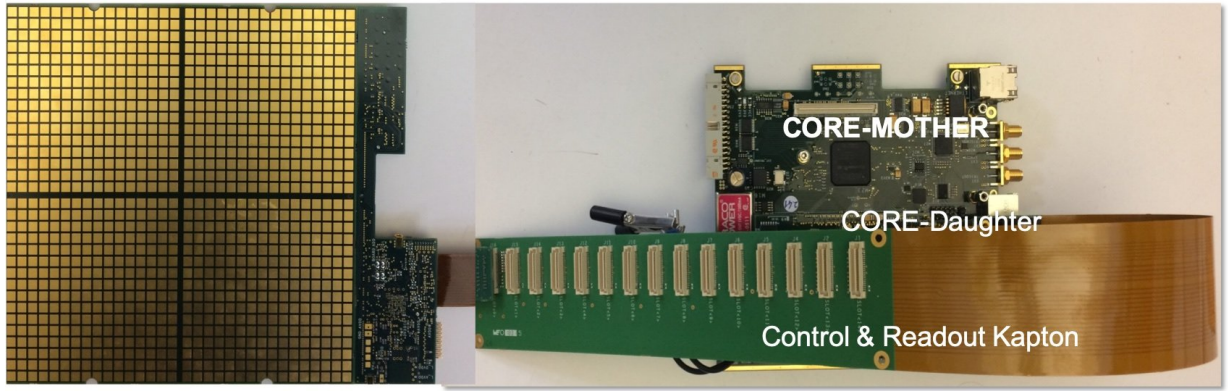
Compact DAQ readout

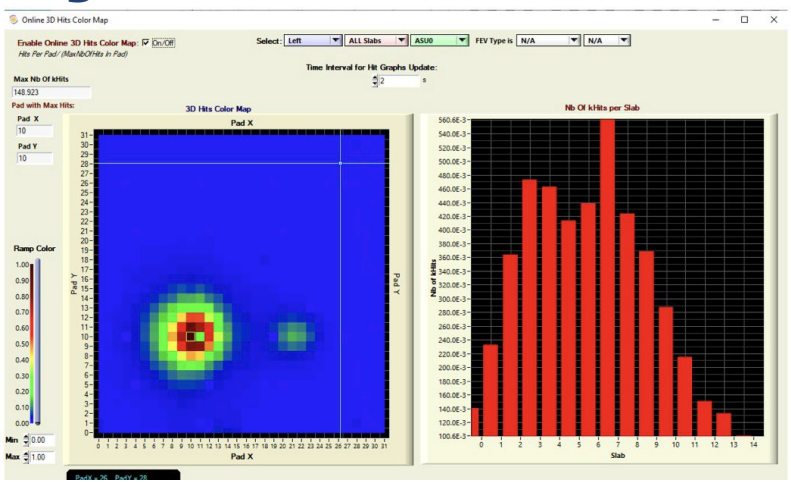
“Dead space free” granular calorimeters → ~ 30 mm space ECAL-HCAL

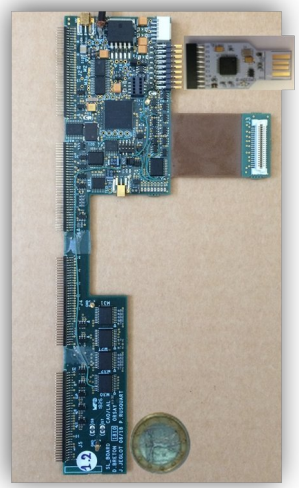
- Compact DAQ
- in use in BT since 2019

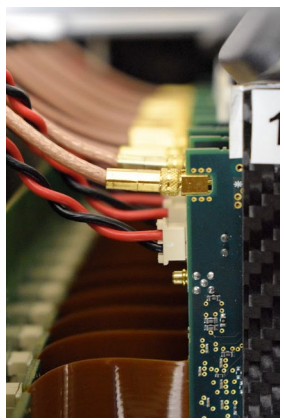
LabWindows + scriptings

- Full debug system
- ↔ EUDAQ
  - Combined running









Acquisition software

Written in C under Labwindows CVI

- Handle whole detector
- Two sides with 15 SLABs
- 5 ASU per SLAB

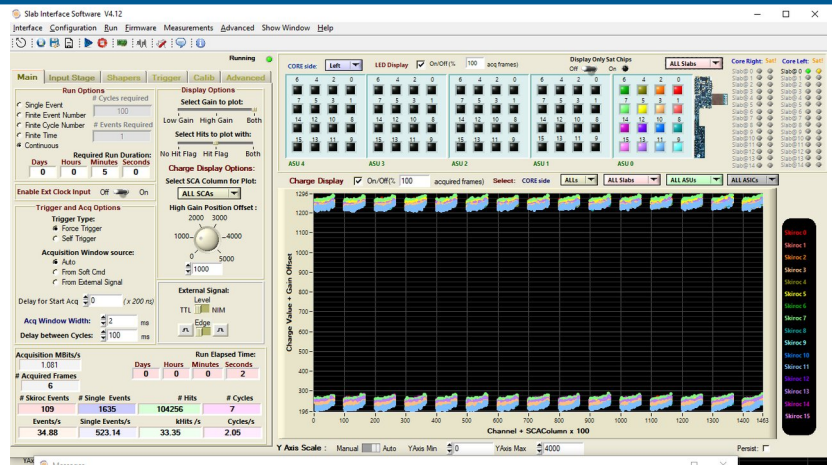
Make advanced measurements

Hardware automatically detected

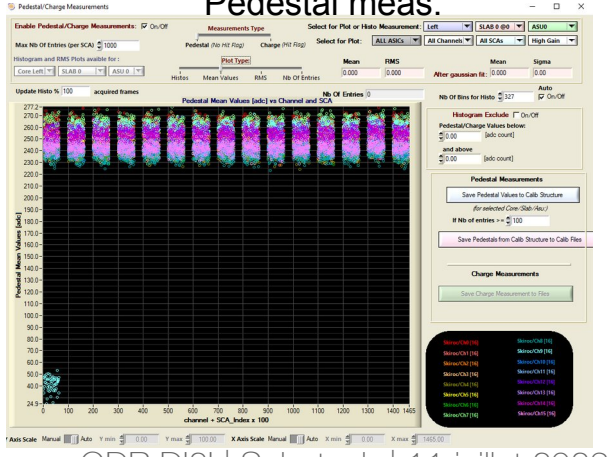
- Number of SLAB
- FEV type + number of ASU

Slowcontrol:

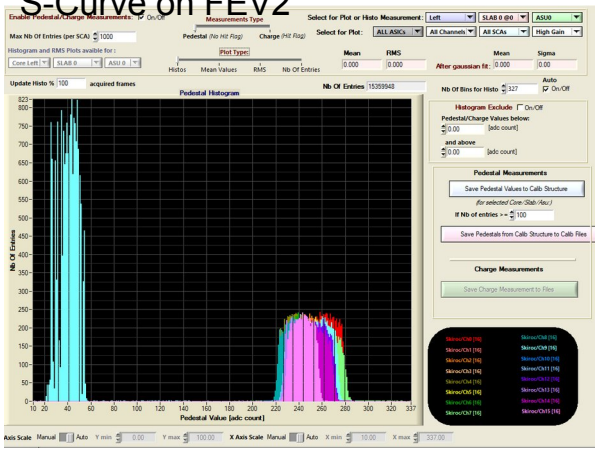
- All parameters programmable
- Integrated analysis



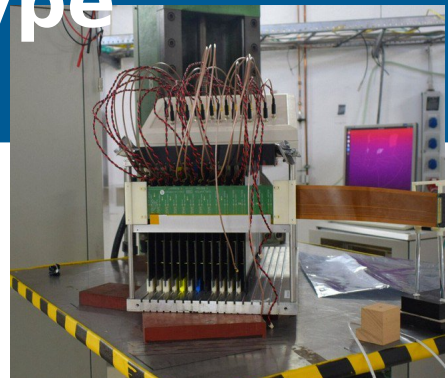
Pedestal meas.



S-Curve on FEV2



CALICE SiW-ECAL Technological Prototype
Beam tests (… at last!)



Nov. 2021 + March 2022 : electrons of 1–6 GeV (4th attemp…)

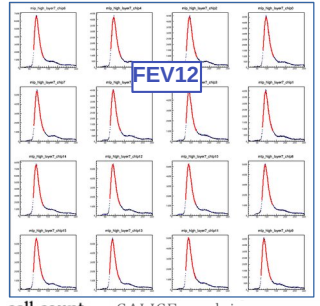
- 15 layers of 1024 cells + Compact "ILD-like" DAQ
  - 5 types de VFE boards (FEV10, 11, 12, 13, COB) ⊗ 3 Wafer thicknesses (320, 500, 650 µm)
  - 2 Tungsten absorbers configurations.

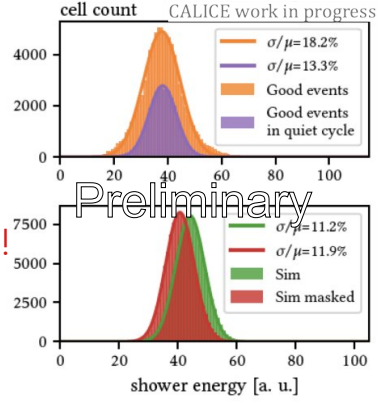
~3 weeks of commissioning and training

- Mechanical structure
  (adding or removing the tungsten plates)
- Hold values, Gain optimization, Threshold optimization,
  single cell calibration, etc
  - ~500k fits (15 boards × 16 ASICs × 64 ch × 15 SCAs × 2 gains)
- Test of combined DAQ : ECAL + AHCAL
- Full simulations (⊃ cell masking)

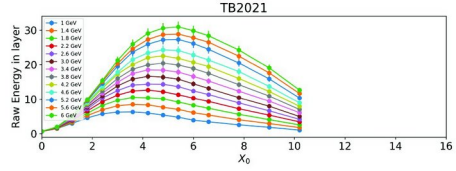
1st full shower profiles & resolutions

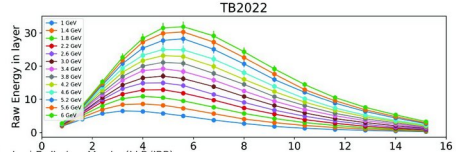
- Filtering needed (retriggers, events splitting, …)

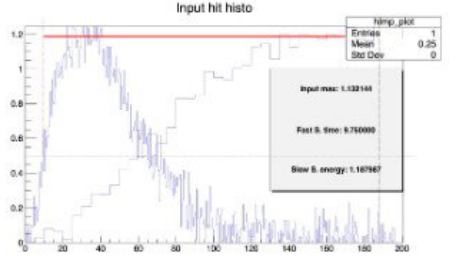


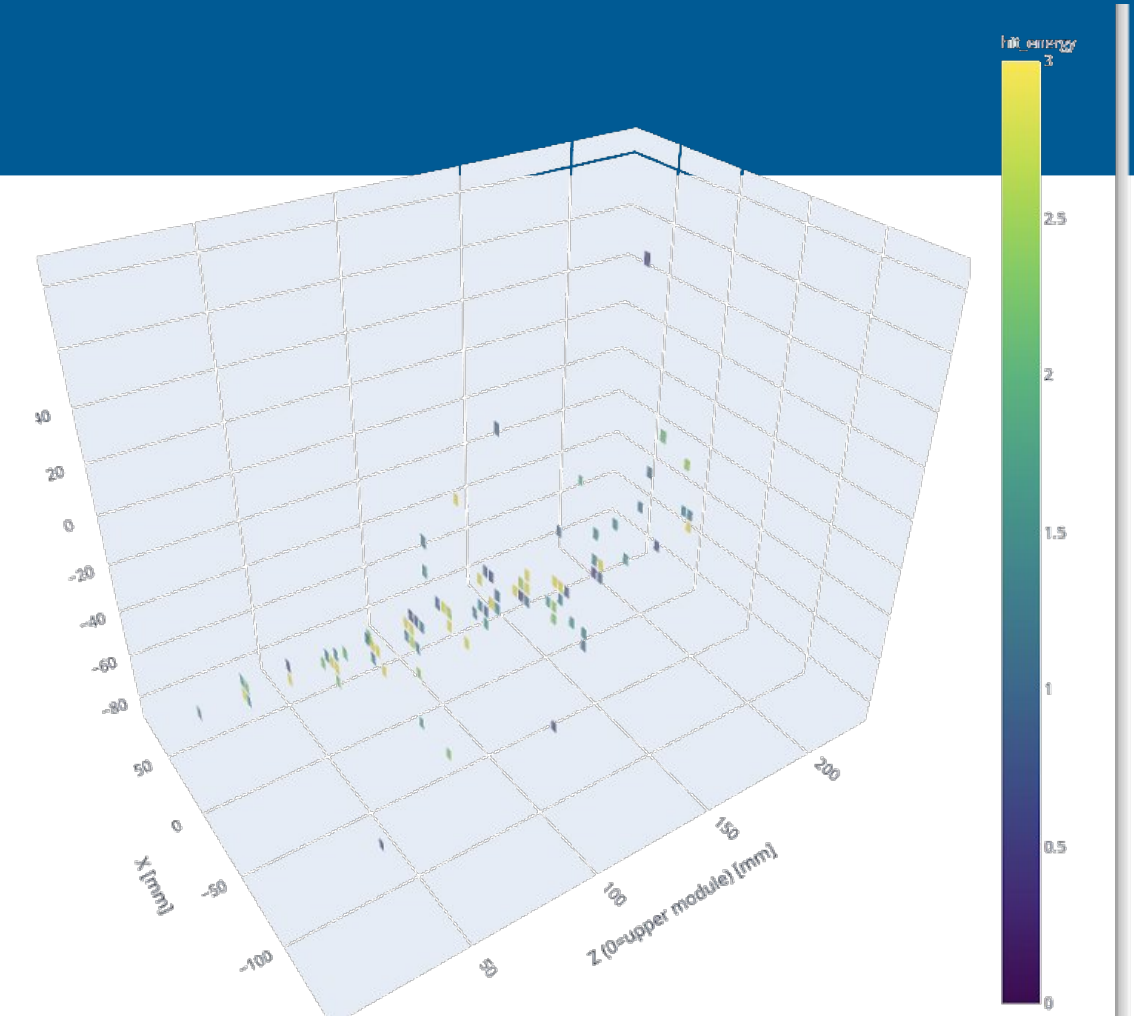


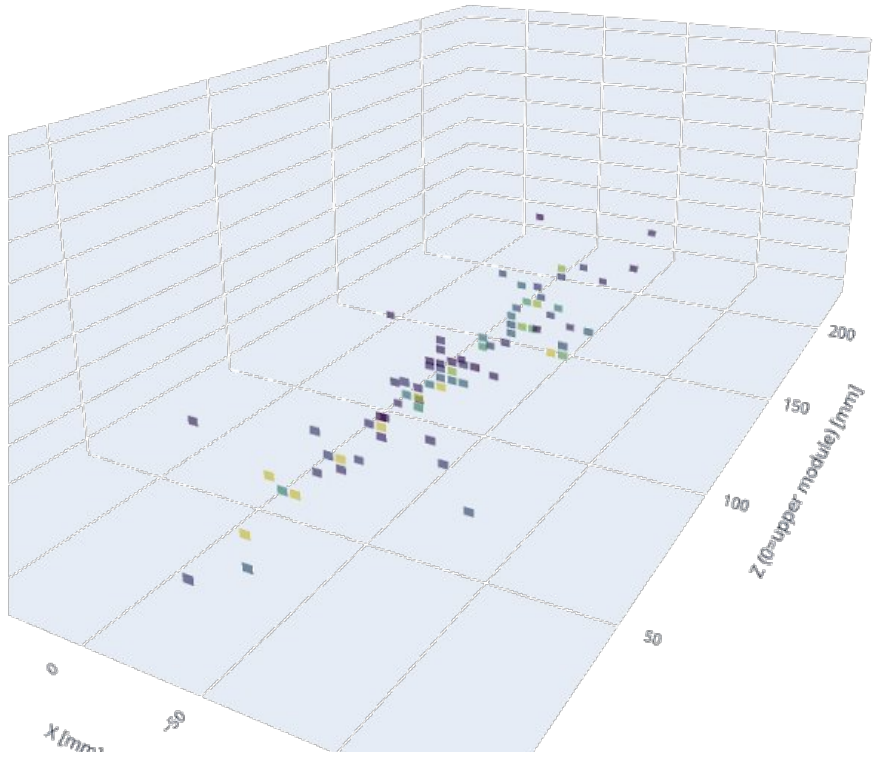
J. Kunath,
PhD, Prelim !





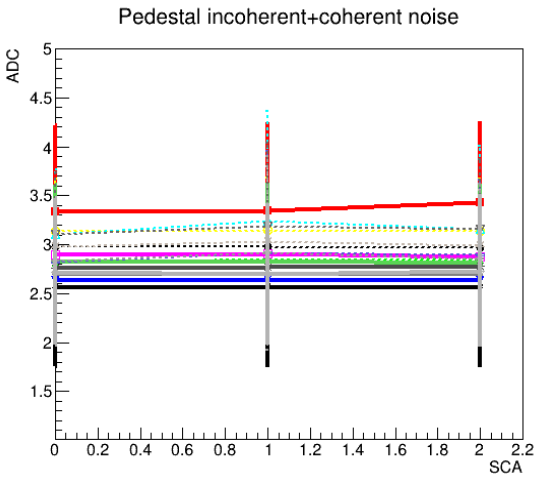



X [mm]
Z (0=upper module) [mm]

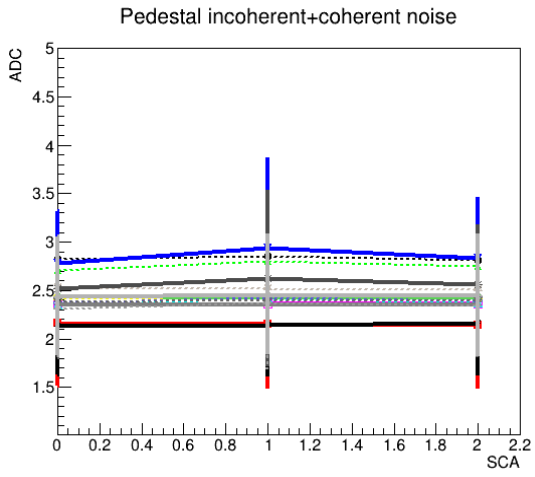

Z (0=upper module) [mm]

Pedestal widths, 1st memory cells, per asic

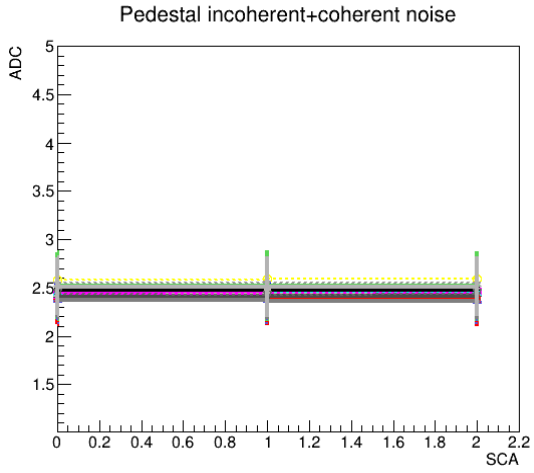
COB



FEV12



FEV13



- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors

Beam test: CERN

2 weeks in June @ SPS-H2

- SiW-ECAL + AHCAL

  15 layers, 1 configuration W

- Running : 75% of time :
  - e : 10, 20, 40, 60, 80, 100, 150 GeV
  - μ : 50, 150 GeV
  - π : 10, 20, 70, 100, 150, 200 GeV

Two issues:

- Increased delaminations of wafers on the edges

  under investigation; main suspects:

  Too much handling; Small batch production; Glue aging

- Collective wafer trigger at high energy (≥20 GeV)
  - linked to HV distribution

Electron

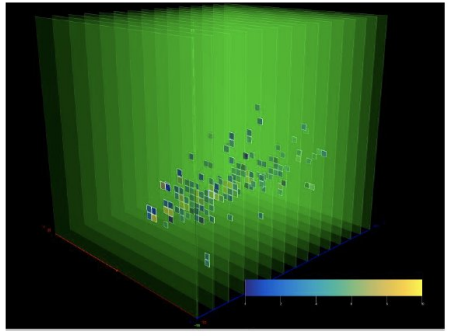


Fig. Simulation e- 10 GeV

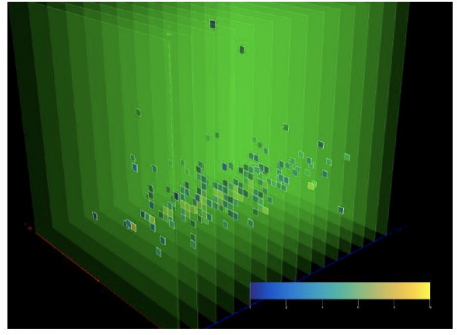


Fig. Reconstructed e- 10 GeV

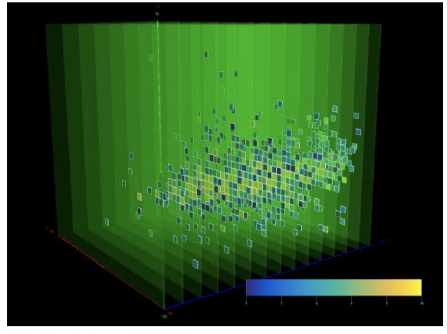


Fig. Simulation e- 100 GeV

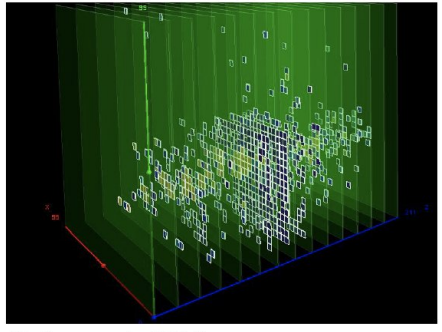
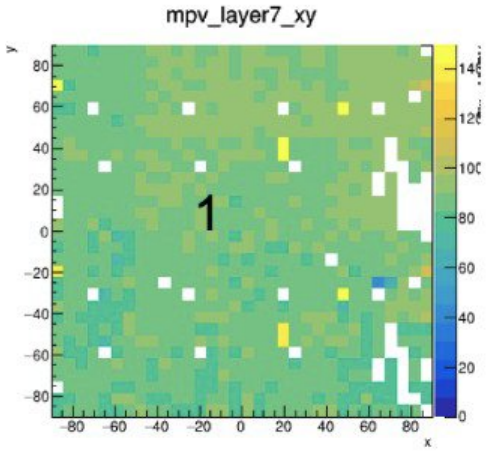
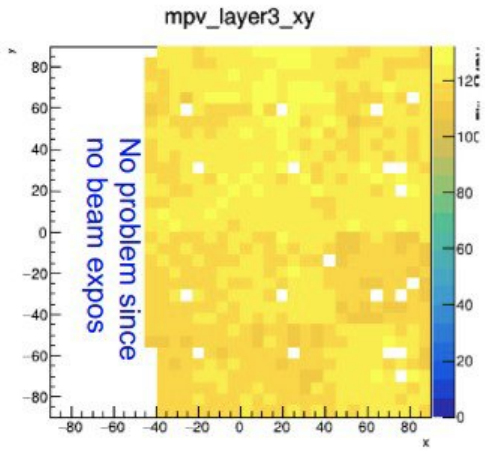
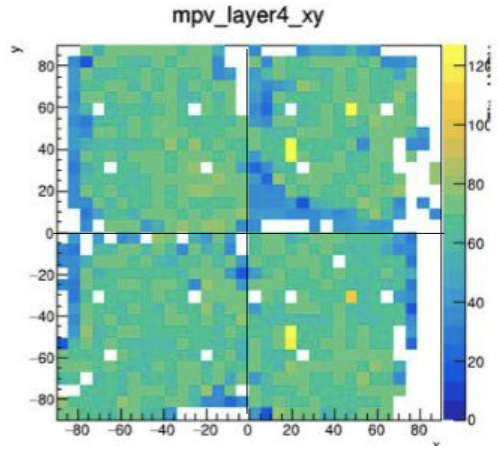


Fig. Reconstructed e- 100 GeV

MIP calibration





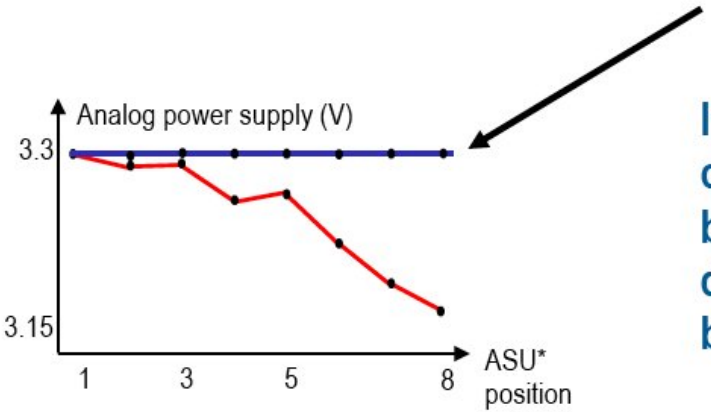


- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected

... and not so good layers

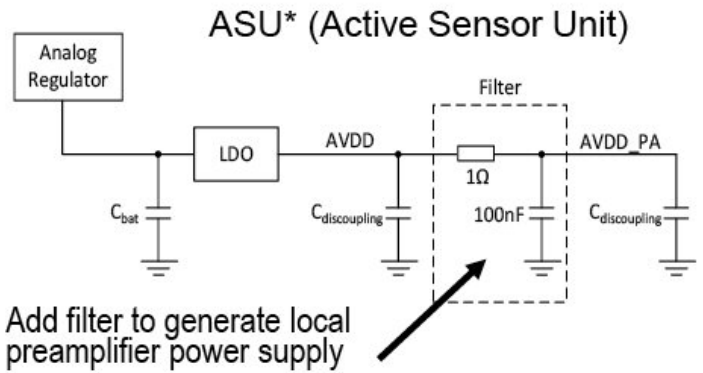
- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months

Power distribution dedicated for LONG SLAB

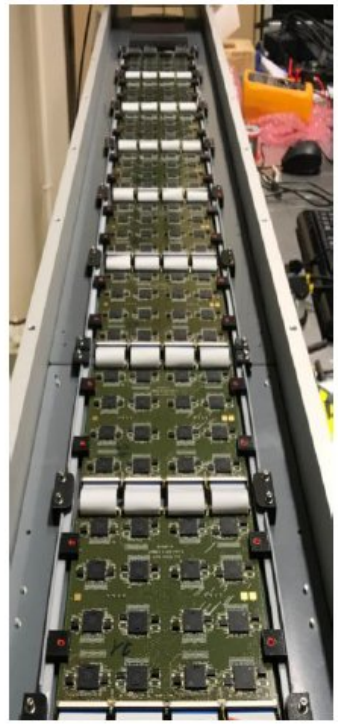


Expected results

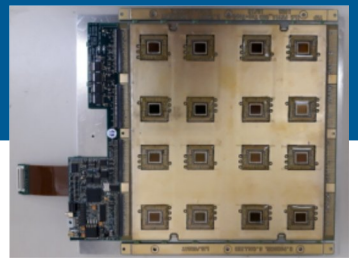
In the electrical long SLAB, 8 boards are chained and due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.



→ We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop and reduce common noise.

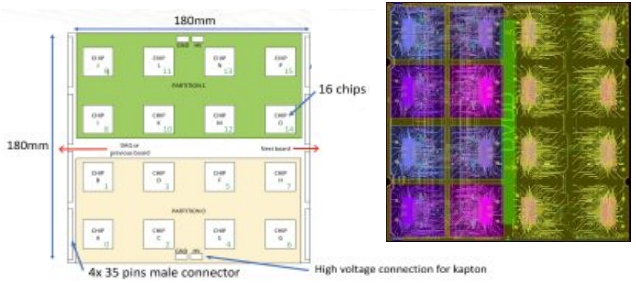


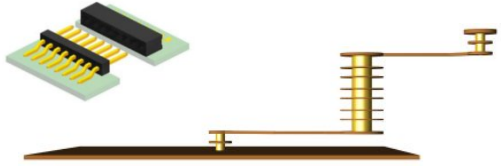
New front end board FEV2.0 (2021)

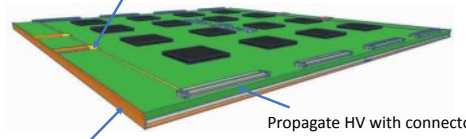


Observation from previous test beam @ DESY 2018 with electrical long SLAB:

- Voltage drop
- Clock configuration integrity
- Power pulsing

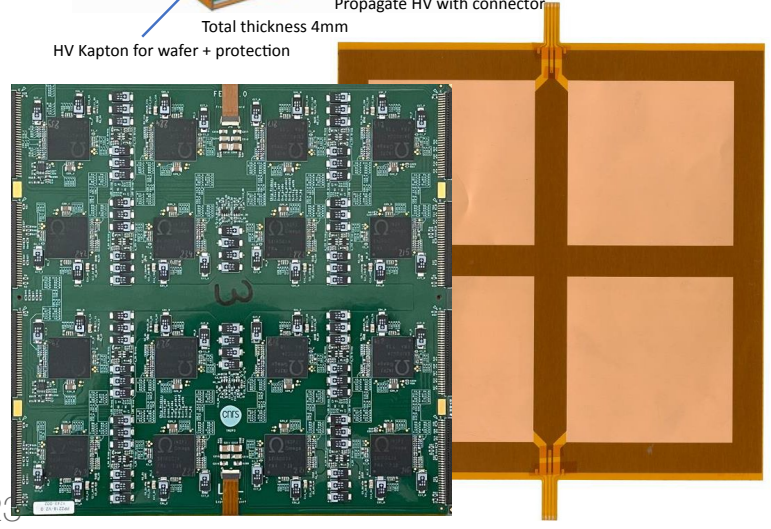






New feature of FEV 2.0:

- 1 LDO (low drop out) per SK2A on analog power supply
- 1 LDO per 4 SK2A on digital power supply
- Add buffer on configuration clock (every 8 SK2A)
- Driving HV (up to 350V) + add filter for each wafer
- Improve shielding for analog signal and power supply



6 months delayed due to cabling problem components supply

LUXE

Physics:

- QED in High Fields:
  $e+n\gamma \rightarrow e\gamma$, $\gamma+n\gamma \rightarrow ee$
  - Schwinger's limit
- BSM: Axions Like Pseudo Scalar, …

Beams:

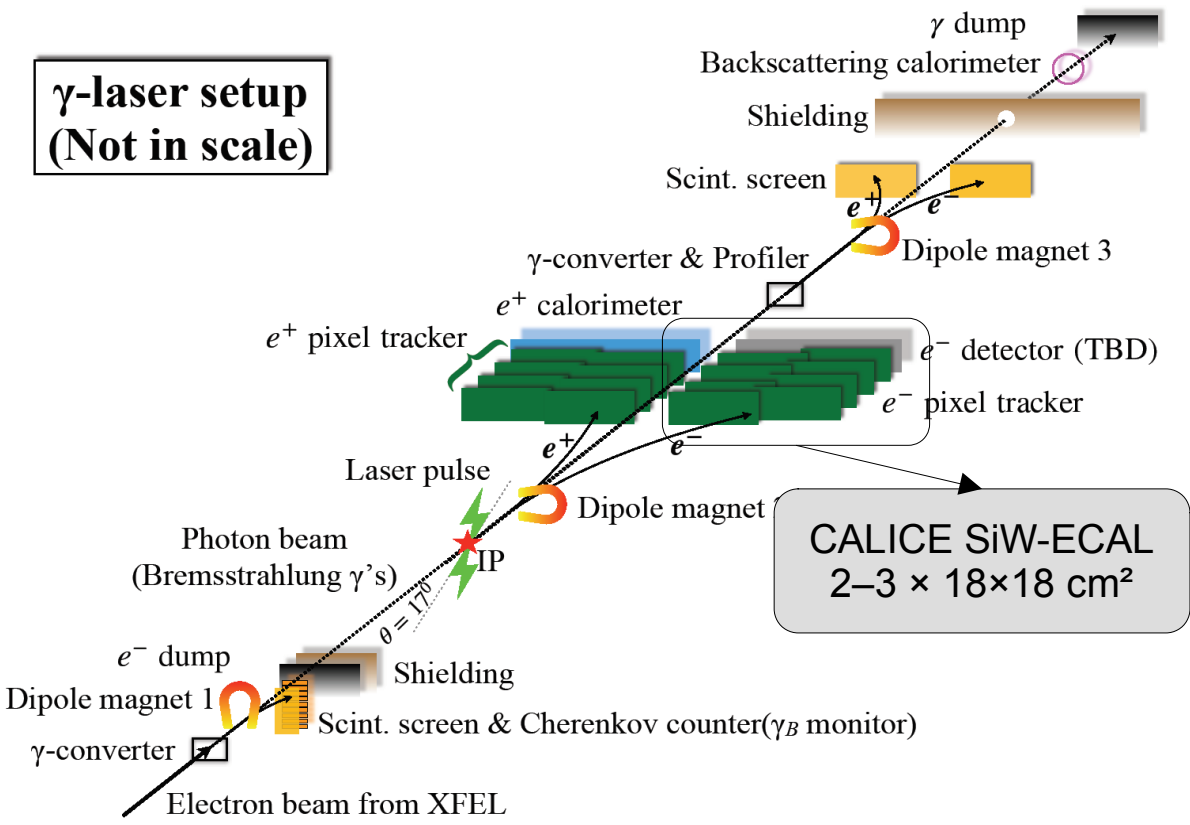
- **XFEL beam 10 Hz,** $1.6\cdot10^9$ e^-, $E_e \leq 17.5$ GeV
- Laser : 40–350 TW, 30 fs, 1 Hz
  → $1.5\cdot10^{20}$ W /cm³
- ≥ 2025 at DESY/XFEL

ECAL's:

- 5×5 mm² cells, 20 X_0, 12? layers, 20 %/√E
- Si+W or GaAs+W → FCAL and/or CALICE

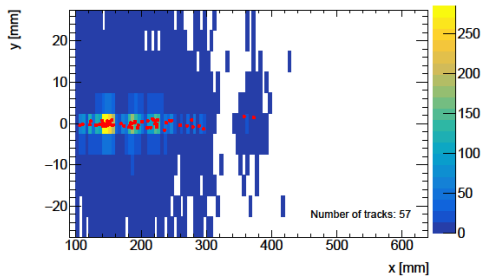
Q? Optimal sampling for Ee ≤ 17.5 GeV ?

- ⊃ Hit counting, shower separations



Overlap of showers

$E(x, z) \rightarrow$ Small R_M



SiW-ECAL for circular EW/Higgs Factories

Running conditions

Linear e+e- (ILC, HL-ILC, …)

- 250 GeV (ZH), 365 GeV (tt), 500 GeV (ZHH) + [1000 GeV], $\mathscr{L}$ ~ cst.
- Power pulsing : 5 [10–15]Hz × 1 [2] ms

Circular e+e- (CEPC, FCC-ee) :

- 90GeV × 10^7 fb × $5{\cdot}10^{36}$ cm^{-2} s^{-1} (qq × 20,000 ILC @ 250GeV)
- 150 GeV (WW) + 250 GeV (ZH)+ 365 GeV (tt)
  ~10^4 fb × $5{\cdot}10^{35}$ cm^{-2} s^{-1} (qq × 5–10 ILC @ 250)

Paradigme Change: *Continuum hypothesis*

– ASIC, Power/Cooling, DAQ, *Granularity, Precisions (E, t),* New ideas…

HL-ILC:

– $\mathscr{L}$ × 4 (6)
– $N_{bunches}$ × 2 : τ_{Train} : 1 → 2 ms
– f_{rep} ×2 (3): 5 → 15 Hz

Dominated by ACQ time:
P(~25µW/ch) × 6

HL-CLIC:

– $\mathscr{L}$ × 2
– $N_{bunches}$ → : τ_{Train} : 176 ns
– f_{rep} ×2 : 50 → 100 Hz

Dominated by Set-up & Conversion time: P (~82µW/ch) ×2

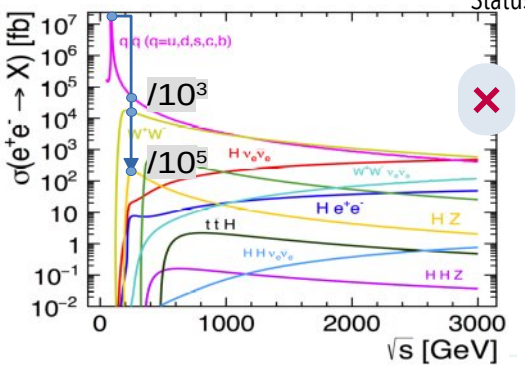
FCC-ee parameters		Z	W⁺W⁻	ZH	ttbar
√s	GeV	91.2	160	240	350-365
Luminosity / IP	10^{34} cm^{-2} s^{-1}	230	28	8.5	1.7
Bunch spacing	ns	19.6	163	994	3000
"Physics" cross section	pb	35,000	10	0.2	0.5
Total cross section (Z)	pb	40,000	30	10	8
Event rate	Hz	92,000	8.4	1	0.1
"Pile up" parameter [μ]	10^{-6}	1,800	1	1	1

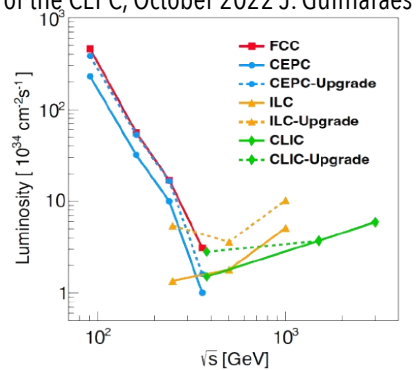
https://indico.cern.ch/event/1064327/contributions/4893208/
Mogens Dam @ FCC Week, 10/06/2022

	Higgs	W	Z	ttbar
Bunch number	249	1297	11951	35
Bunch spacing [ns]	636	257	23 (10% gap)	4524
Bunch population [10^{10}]	14	13.5	14	20
Bunch number	415	2162	19918	58
Bunch spacing [ns]	385	154	15 (10% gap)	2640
Bunch population [10^{10}]	14	13.5	14	20

Snowmass2021 White Paper AF3-CEPC, arXiv:2203.09451

Status of the CEPC, October 2022 J. Guimarães da Costa





Detector Parameters: scaling rules

- Cell lateral size
  - Shower separation (EM~2×cell size)
  - Cell time resolution (1 cm/c ~ 30 ps)
    - Time performance for showers
      - » ParticleID, easier reconstruction
- Longitudinal segmentation
  - sampling fraction
    - E resolution (ECAL ~15%/√E)
  - shower separation/start
- ECAL inner radius; Barrel Z_{Start}
- ECAL–HCAL distance
- Barrel–Endcap distance
- Dead-zones sizes (from Mechanics, Cooling)

Number of cells ↗ ⇒ Cost ↗ (1/size²)
Cell density ↗ ⇒ Power consumption ↗

Time resolution ↘ ⇒ Power ↗

threshold, passive vs active cooling
dead-zones ↗

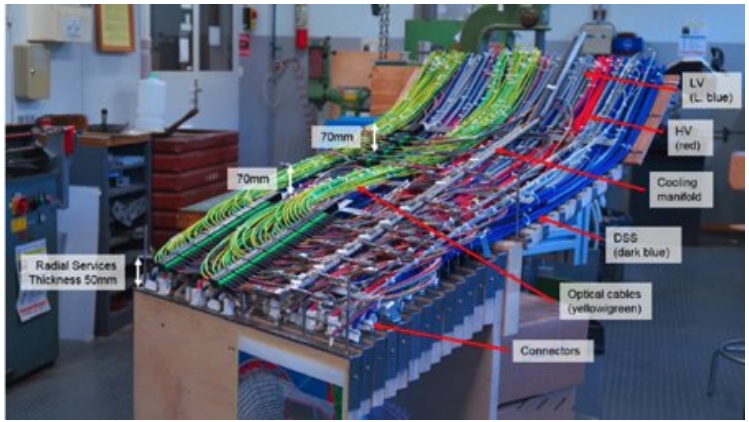
BEING FULLY RE-EVALUATED (→ ILD, CLD)
for EW region with realistic ASIC hypothesis

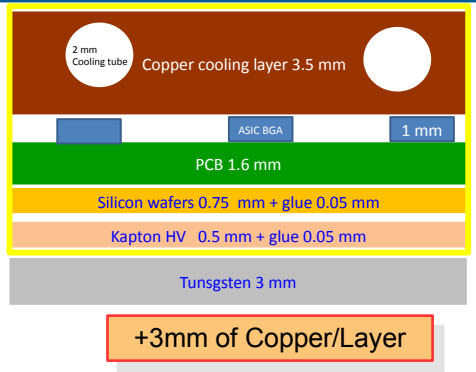
Inner Radius ↗ ⇒ Tracking performance ↗
Cost ↗² (⊃ Magnet, Iron)

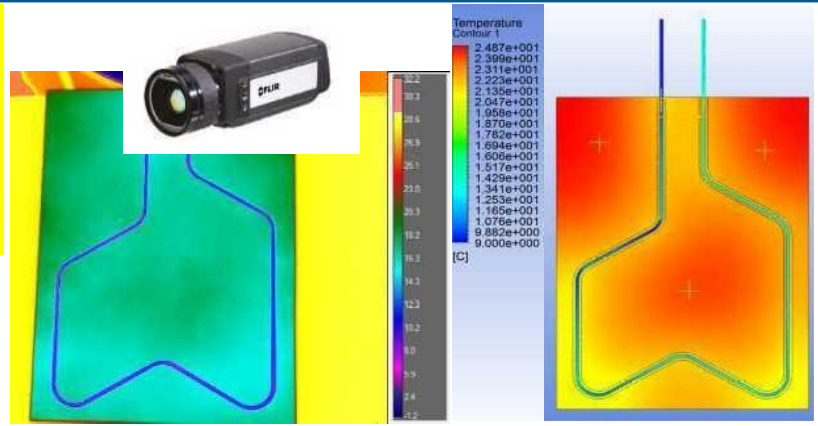
Gaps ↗ ⇒ PFlow performances ↘
↳ ⊃ *Active cooling*

Review of physical implication (from TeV): see Linear collider detector requirements and CLD, F. Simon @ FCC-Now (nov 2020)
Physics Requirement studies @ 250 GeV: see Higgs measurements and others, M. Ruan @ CEPC WS, (nov 2018)

Services: integration & cooling

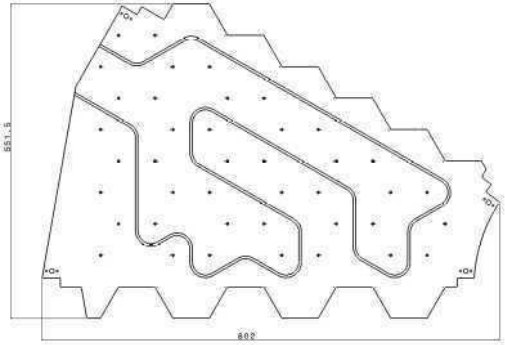


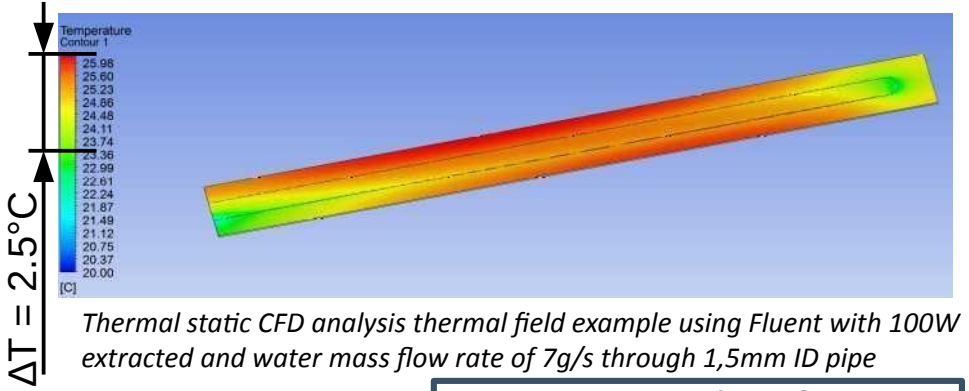




Pipe insertion on a cooling prototype

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling



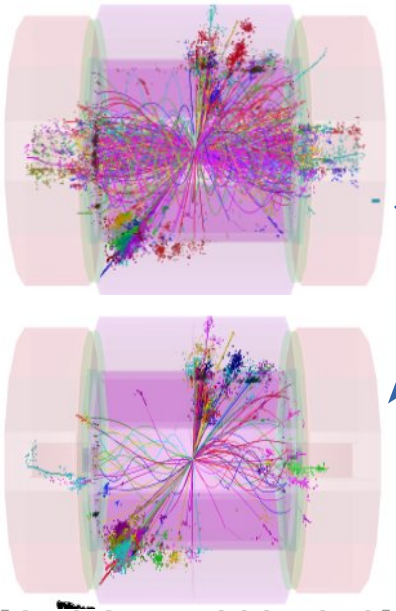


Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

= 2× cont. operation of a SLAB

Timing in calorimeters: 0.1–1 ns range

Cleaning of Events

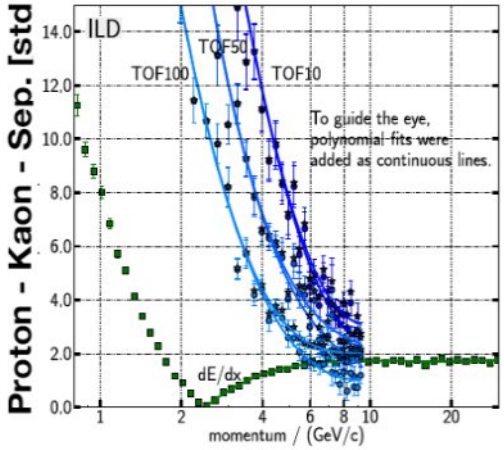


[CLIC CDR: 1202.5940]

adapted from L. Emberger

Particle ID by Time-of-Flight

- Complementary to dE/dx
  - here with 100ps on 10 ECAL hits

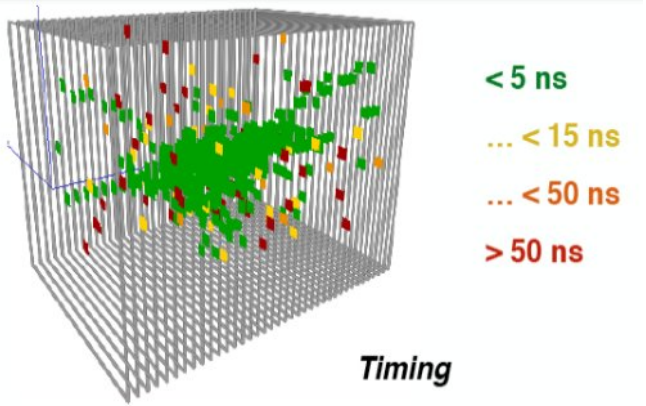


S. Dharani, U. Einhaus, J. List

See Cluster timing and leakage in time at the CEPC baseline Calorimeter (Yuzhi Che)

Ease Particle Flow:

- Identify primers in showers
- Help against confusion
  better separation of showers
- Cleaning of late neutrons & back scattering.
- Requires 4D clustering

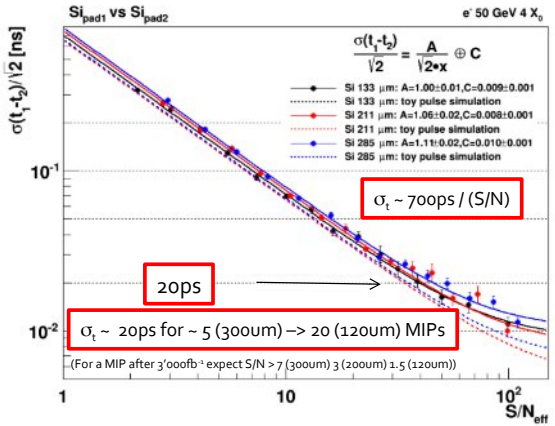


Ch. Graf

Timing Studies

2015 CMS HGCAL CERN timing test beam

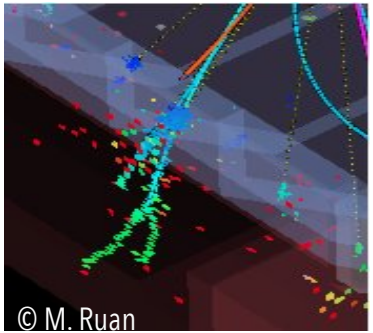
- Time resolution vs S/N ratio

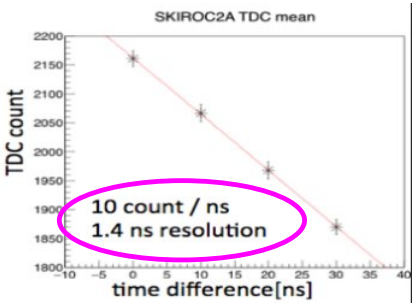


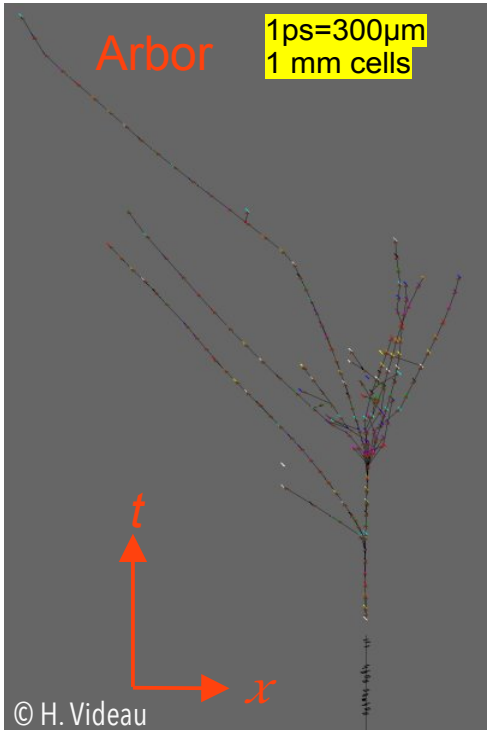
Transparent cells => no timing
Solid cells = > timing information ~50ps

CALICE / ILD

- Bulk Timing







See Cluster timing and leakage in time at the CEPC baseline Calorimeter (Yuzhi Che)

Detector optimisation for Higgs Factories

Continuous running ≠ Pulsed runnning

- Power × 100 !

Low energy (90 GeV)

- Lower energy – less focused jets
  - Lower granularity needed (1–2 cm OK ?)
  - Lower dynamic range
- Other criterions ? Tagging

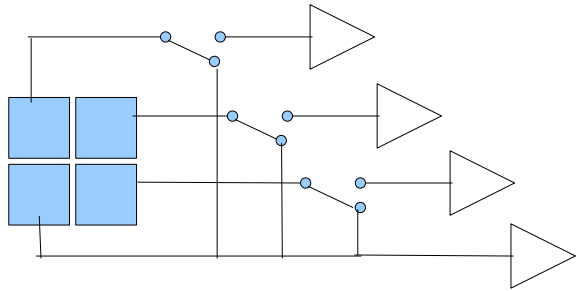
… but not so for the rest (≥ ~250 GeV)

Reduce the number of layers + thicker sensors

- See “Small ILD” model
- 6’’×500µm wafers ➡ 8’’ × 725 µm (resolution $1/\sqrt[5]{d}$)

One size fit all ?

- Have a dynamic granularity ?



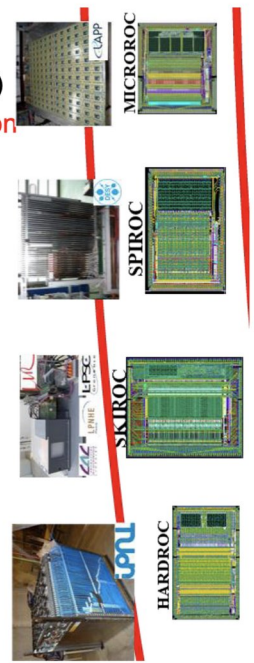
- Have a semi-digital readout ?
  - Hit counting for low energy
  - E measurement for high energies

Use full simulations to estimate fluxes :
- Occupancy, Power, Data …
- … for various hypothesis ($\mathcal{L}$, Granularity, ASIC technology, DAQ scheme, ...)

New ASIC:

DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - ⇒ allows common DAQ and facilitates combined testbeam
- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch
  - Allows better granularity or LAr operation
  - Extend to LAr (cryogenic operation) and MCPs (PID)
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts
- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL



CdLT : future chips DRDI 10 jul 23 8

Low Power

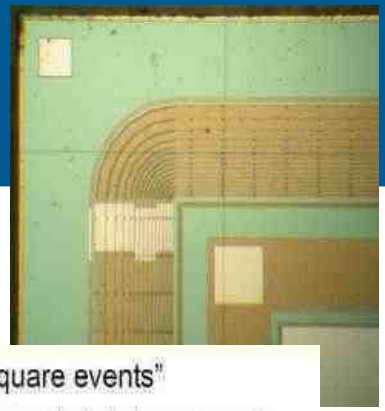
- Timing ?

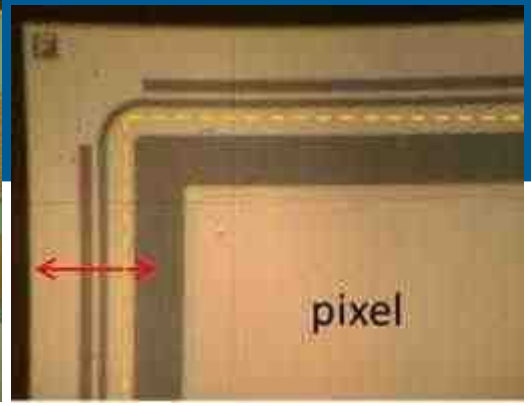
Low occupancy

- Self-trigger
- Less memory
  - if continuous readout

Optimized dynamic range (silicon)

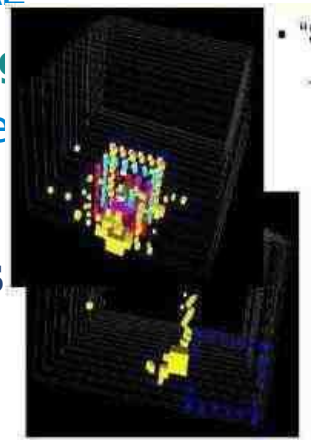
Silicon Sensors



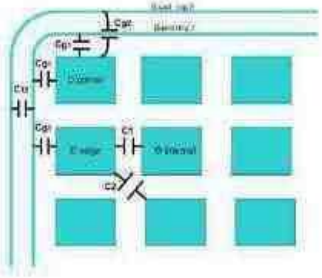


Cost driver

- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction (**CALIIMAX proj**
- Decoupling of Guard Ring (Square Eve
- new design of ILD detector

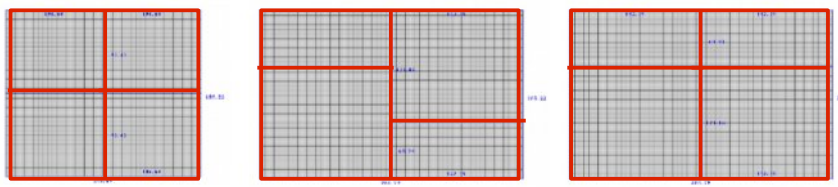


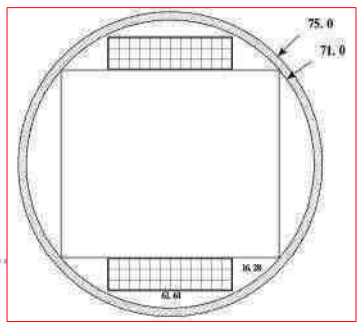
- "Square events"
  - cross talk between guard rings and pixels



Command Sensors (@ Hamamats

- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8'' in 186mm alveola
  320 → 550, 650 → 725 µm ?





'quantum unit' of ILD dimensions (here 6'' wafer)

Conclusions

SiW-ECAL technological prototypes

- **2022:** Heterogeneous 15 layers
  - 1st full calorimeter working [DESY22, CERN22]
    - Shower seen, Detailled simulation ready
    - Analysis on-going ➡ resolutions, ...
  - Numerous emerging issues
    - gluing, HV filtering at high energy
- **2024:** Uniform 15 layers
  - ➡ New VFE boards
    - Cleaner PS & Clock distributions; more uniform
  - Gluing being revisited
  - Material available.
  - To be tested in 2024
    - ➡ Provide reference sample for GEANT4
    - ➡ With funding ➡ “full” LUXE

SiW-ECAL design for HET factories

- **2023–26**: Power budget & performances to be re visited
  - Occupancy, power, data fluxes (on-going)
    - ➡ Granularity; Passive or Active cooling
    - ➡ new ASIC attributes
  - 2024–26: PFA & Physics performances

2025–26: Blue-print for a SiW-ECAL detector for the next ee collider

➡ planning for a pilote module @ T_0 collider-8y -5y (1 Mch, 1/60th of real detector)

semi-industrial, quality, ASICs, …