Caractérisation des puces sur wafer pour le trajectomètre ITk de l'expérience ATLAS

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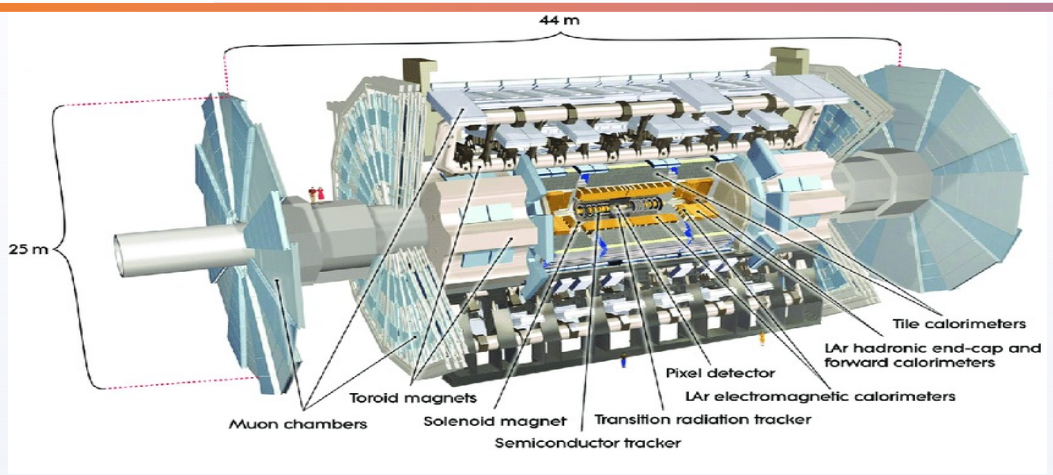
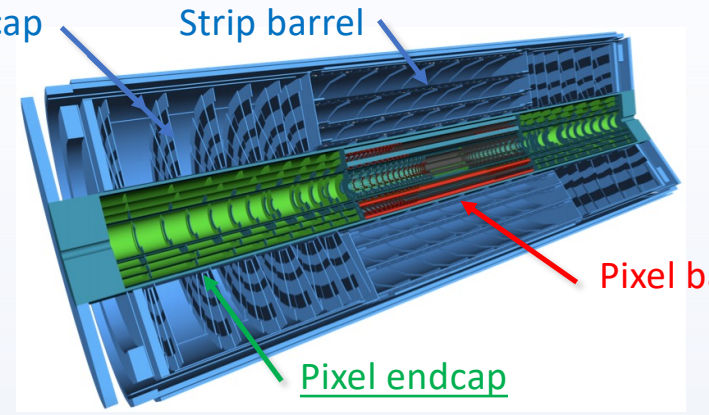
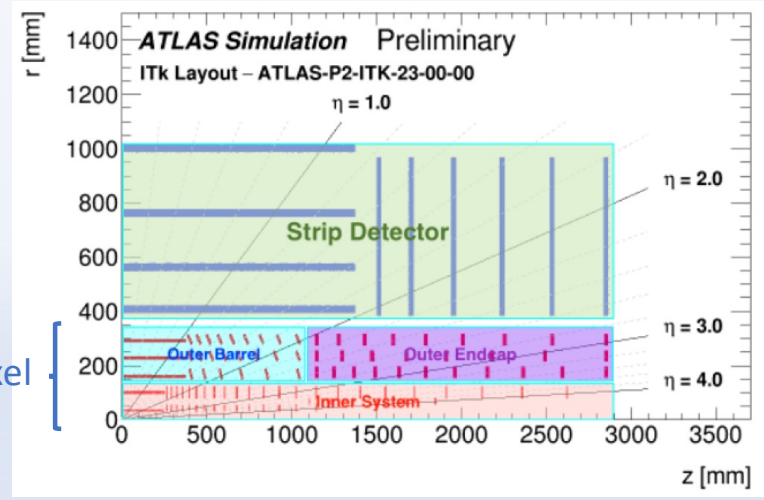
Abdenour Lounis, Ali Slimani

ATLAS Inner Tracker for HL-LHC



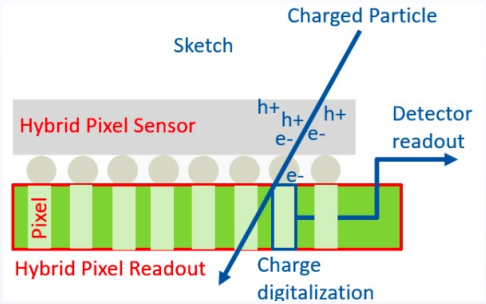


- High Luminosity LHC upgrade : increased luminosity, data rate and radiation damage
- Replacement of current ATLAS Inner Detector ➛ ITk
  - 5 layers of pixel detectors
    - Active area 12.7 m^2
    - ∽ 10000 hybrid modules, ∽30000 electronic readout chips
    - Also 3D sensors
  - 4 layers of strip detectors

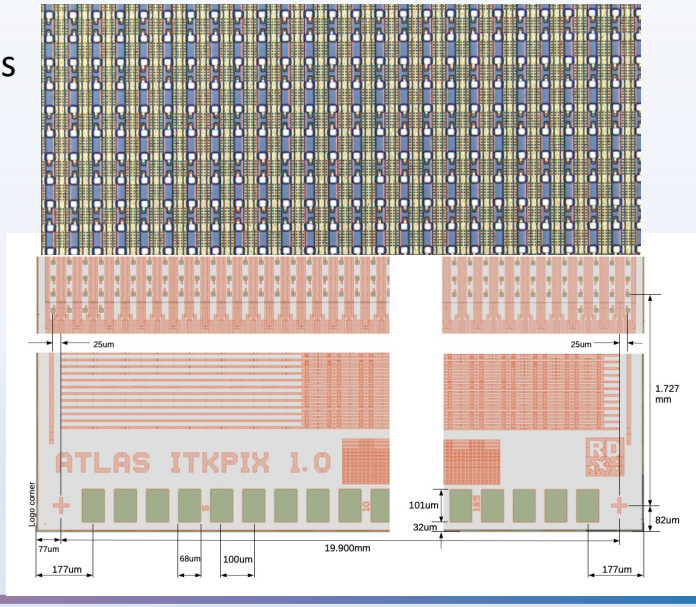


ITk Hybrid modules

- Composed of sensor bump-bonded to readout chip
  - Sensor:
    - 50 µm × 50 µm n-on-p pixels
    - 100 µm / 150 µm thickness
  - ITkPix FE chip developed by RD53 collaboration :
    - 65 nm TSMC technology, 2 × 2 cm^2, 400 × 384 pixels, 198 wirebond pads



	Pixel	Chip bottom
Analog	signal amplification, detection threshold, amplitude measurement	mux to check internal chip potentials and currents, supply voltage/current generators for other chip modules, supply voltage regulators for serial powering
Digital	signal digitization, storage for <500 LHC bunch crossings	communication, A/D and D/A conversion of chip internal signals, debug muxes and temperature and radiation sensors, supply voltage regulators
Digital communication: command received via differential 160 Mbit Rx line, data sent by up to four differential 1.28Gbit Tx lines		



ITkPix Wafer probing

- Wafer probing aims at testing the front-end ITkPix chips before dicing to select those to bump-bond to sensors ➛ first stage of module production !!
- Task shared among several ITk institutes:

UNIVERSITÄT BONN · IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis · University of Glasgow · BERKELEY LAB Lawrence Berkeley National Laboratory · 香港科技大學 THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

⇨ Equipped with a semi-automatic probe station

⇨ The testing procedure has been developped by Bonn University

⇨ Measurement qualification is in progress on the other institutes

Test routine

M. Standke (Bonn Univ.)

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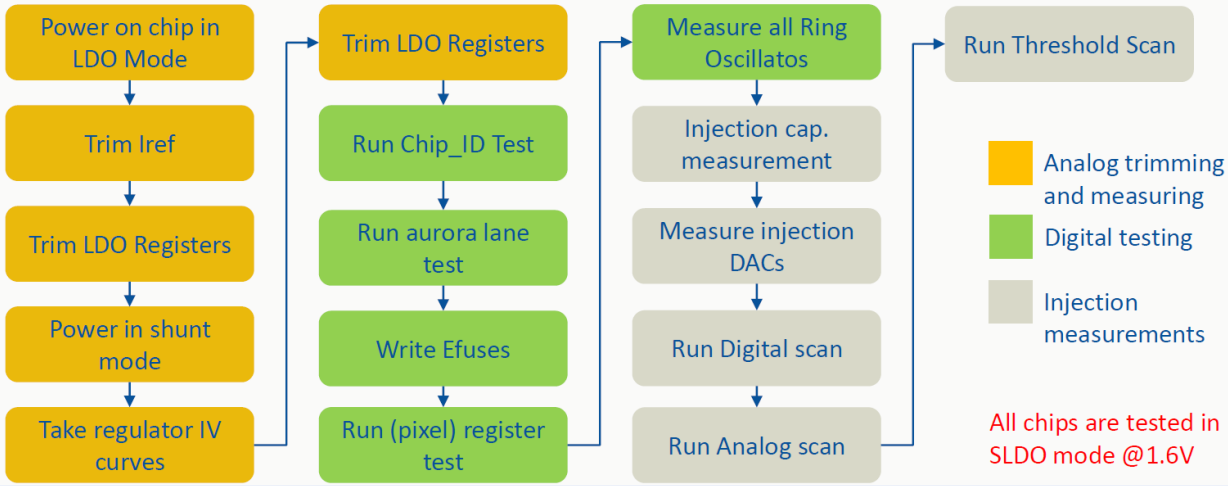
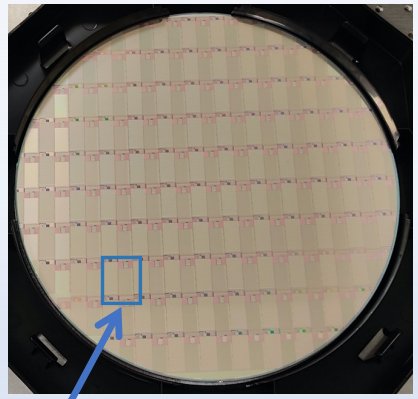
WAFER PROBING ROUTINE



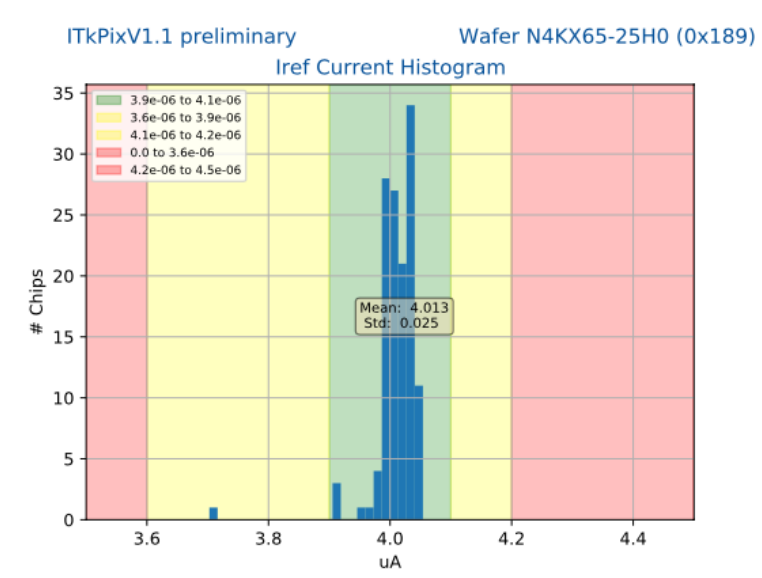
- Test time = 20^{min}/chip = 48^{h}/wafer
  - ↳ will be reduced to 24^{h} for ITKPixV2
- 1.28 Gbit/s
- Room temperature (at IJCLab we could test at cold temperatures if required)



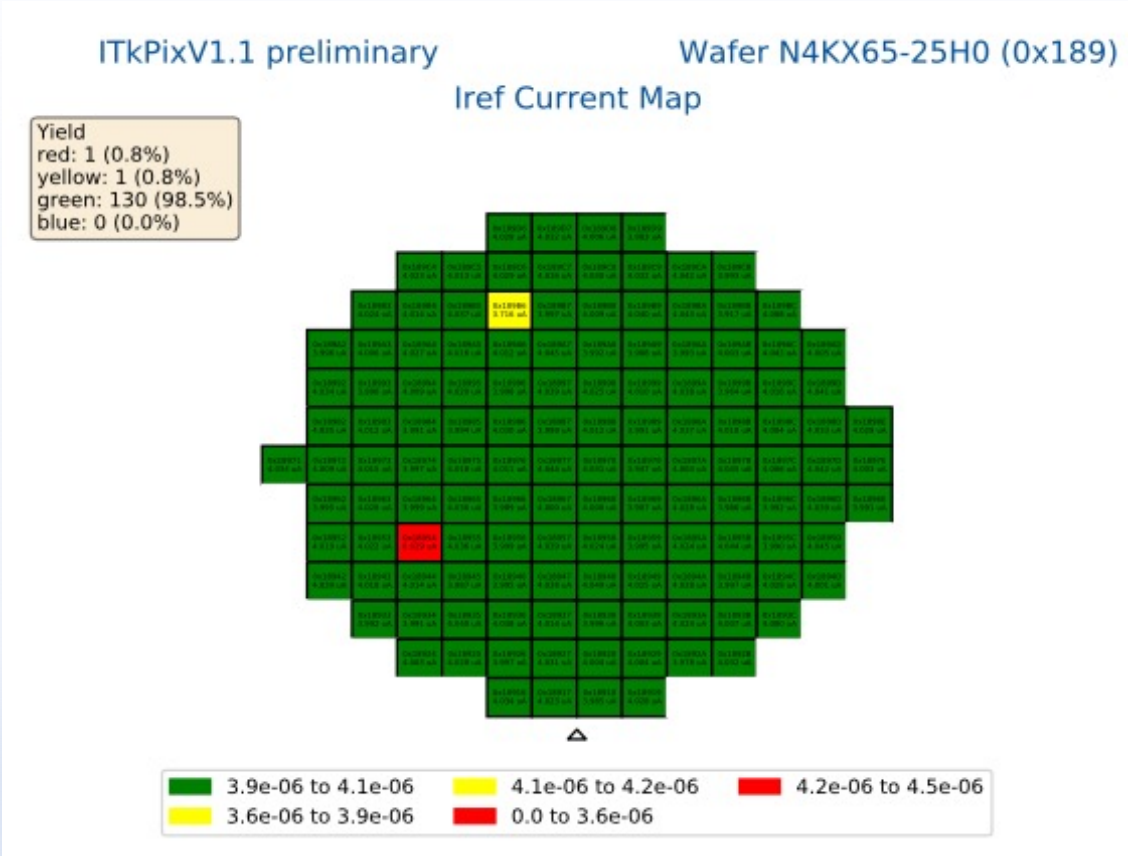
132 chips on a 30-cm wafer

- For each function a **PASS** / **NO PASS** criterium is defined
- The performance of each chip is determined as the **_AND_** of selected relevant tests
- If **PASS** then the chip is selected for bump-bonding to sensors

Measurement example: Iref



COLOR	DEFINITION	APPLICATION
	Fully functional, all tests in wafer probing passed in highest classification	Used to build detector
	Semi functional, at least one of the tests was passed in yellow classification	Used for Lab testing and DAQ development
	Non-functional, at least one tests did not pass	Not Used



M. Standke (Bonn Univ.)

Wafer yield map

Yield = **_AND_** of all relevant tests

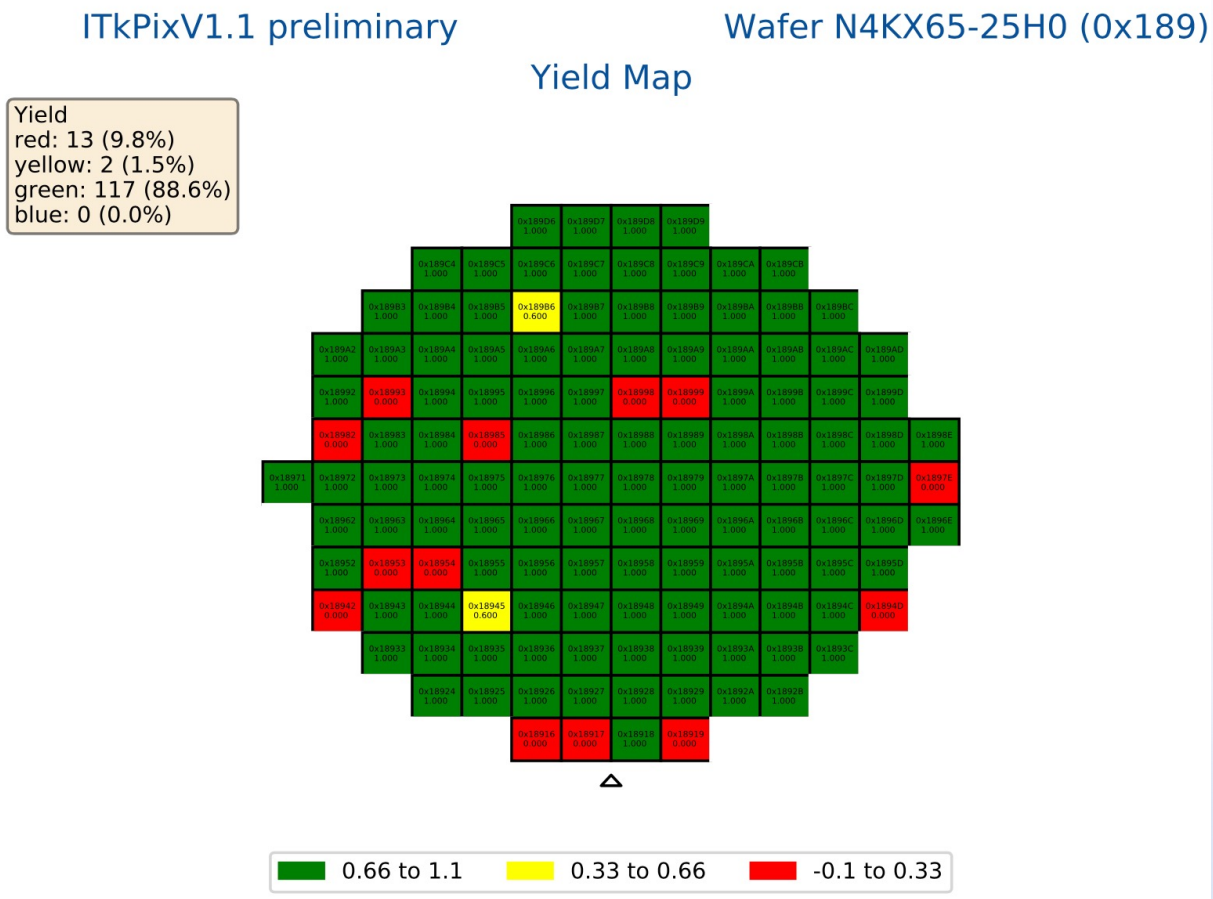
⇨ If all green = **PASS**

⇨ If at least one not green:

= **NO PASS**

or

↳ **Test/Development**



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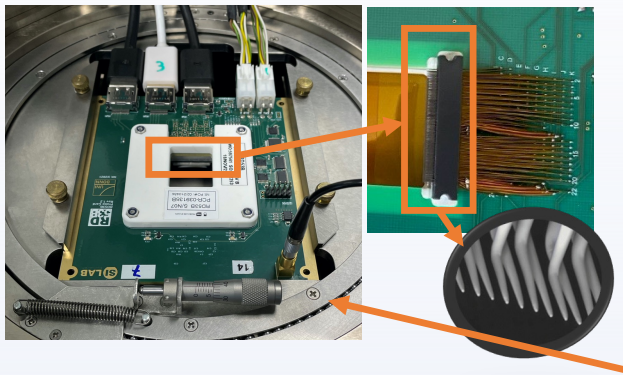
Probing setup @ IJCLab

RD53 probe card with probe « comb »

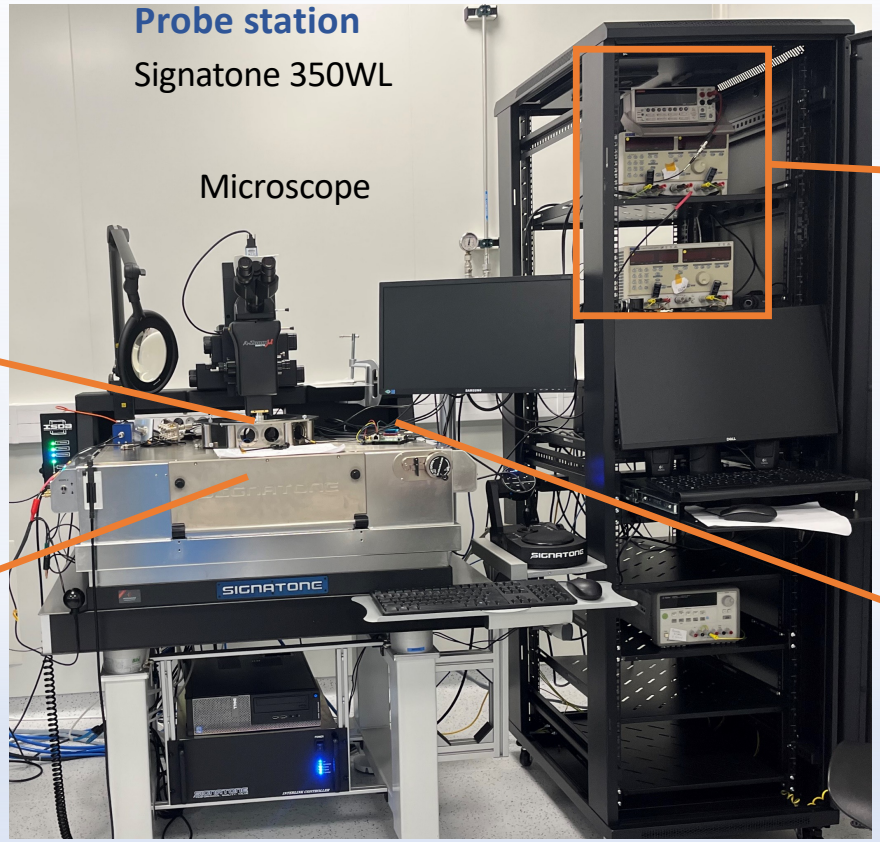


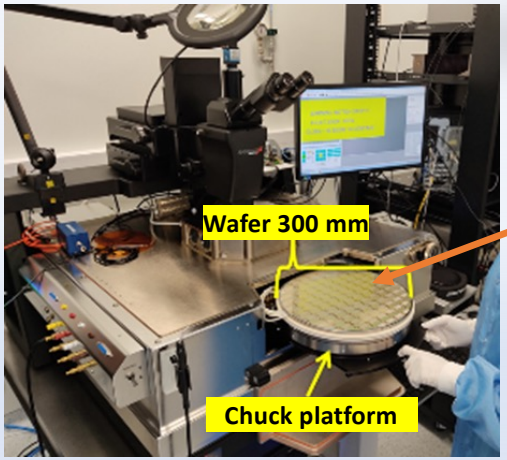
Salle blanche “Pixels” (ISO 7) at PSI Platform

Probe station

Signatone 350WL

Microscope





Measurement Keithley 2400

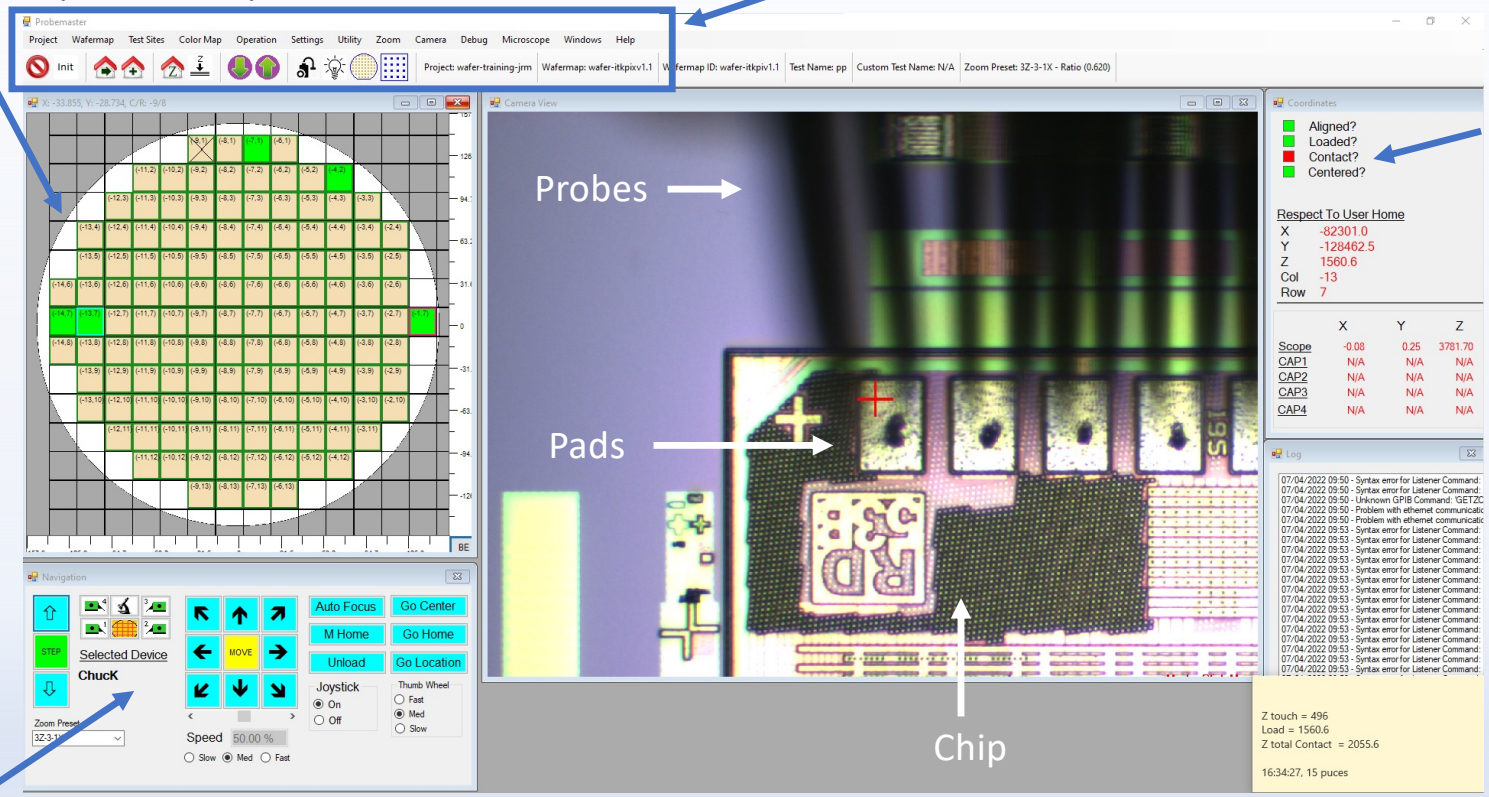
Power supplies TTi QL355

BDAQ53 board

Probing in action

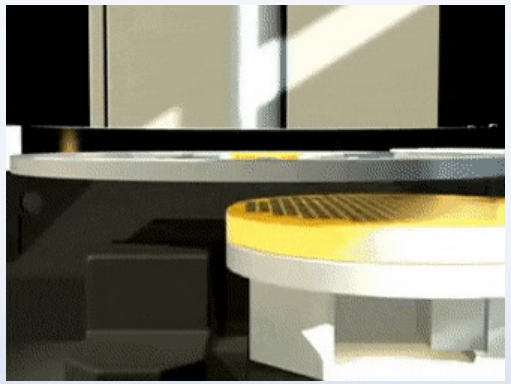
Wafer map (exact chip size)

Menu : wafer alignement, test and probe contact configuration



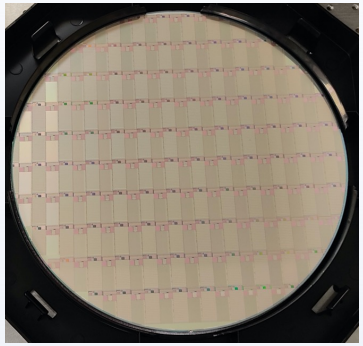
Status

Automated chuck movement to put chip pads under probes

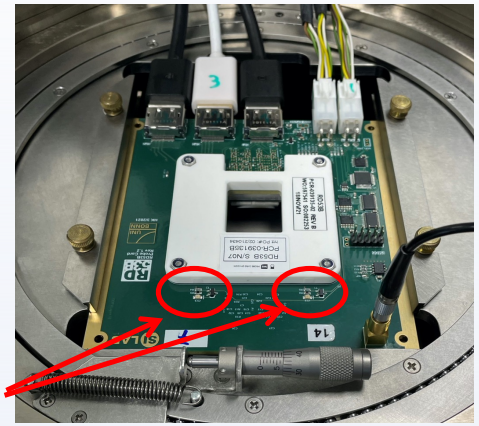


Chuck / microscope movement operation

Test running



- Electrical contact on wafer
  - Contact strength “just” to make good electrical contact



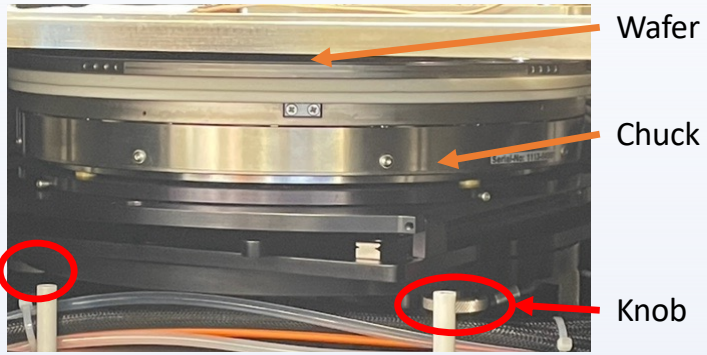
- Probe card with sense edges on the right/left ⇒ LED switches on when contact with wafer
  - Adjust contact distance (+10–15 µm) and card planarity

- BDAQ53 to drive tests
  - Analog trimming
  - Analog measurements
  - Digital testing
  - Injection measurements

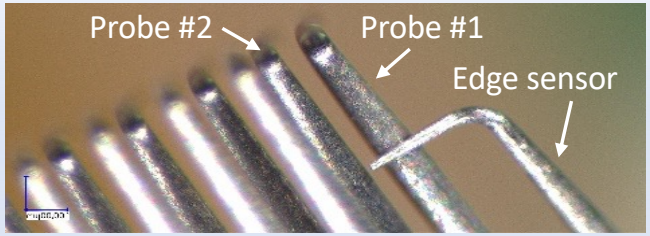
- Python scripts
  - Communication with all devices : BDAQ, Keithley, TTi
  - Send test commands to BDAQ
  - Drive probe station movements (X,Y,Z)
  - Data acquisition
  - Data analysis

Test tricks

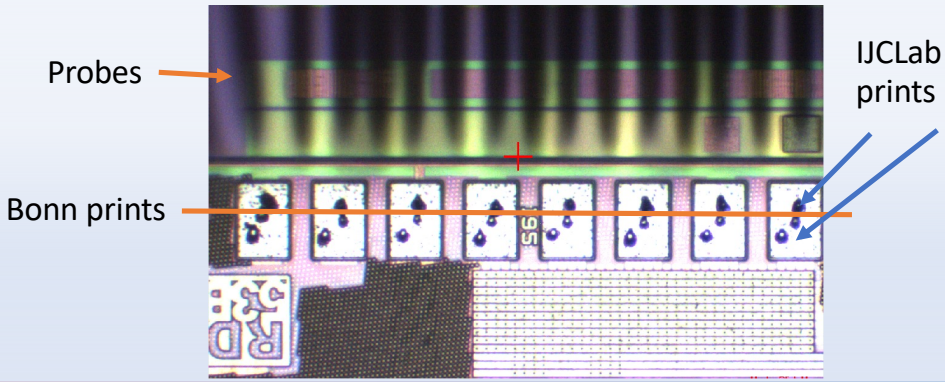
- **Planarity adjustement** : Triangular-shape basis with one fixed point at the back and two front knobs, without any scale or reference… just feeling !!



- **Edge sensor sticks to neighbor probe** → contact LED always OFF → probes crush on wafer (aarrgghh !!)

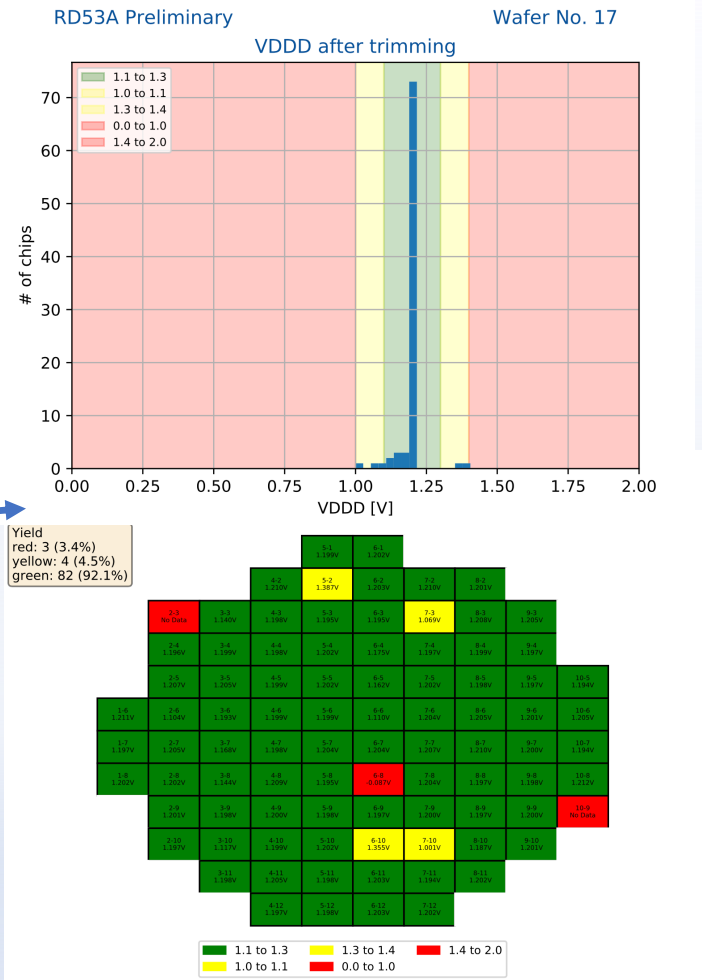


- **Touch strength** = Contact LED ON + x µm surtouch to absorb height difference on probe comb / wafer planarity
  - Too strong is BAD : damages pad layer
  - Too light is BAD : bad electrical contact
  - On an already touched region is BAD : damaged layer → bad electrical contact → bad repeatibility
  - IJCLab's print is bigger than Bonn's → upward movement too fast → chuck wiggles → implementation of "soft touch" functionality (important for wire-bonding)



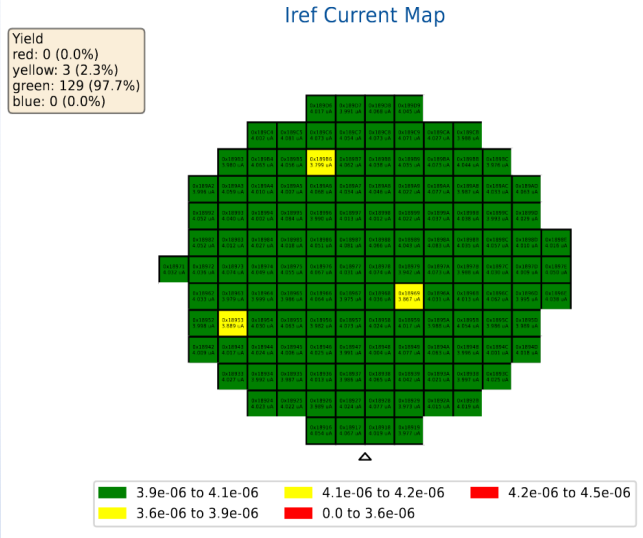
Waferprobing at IJCLab

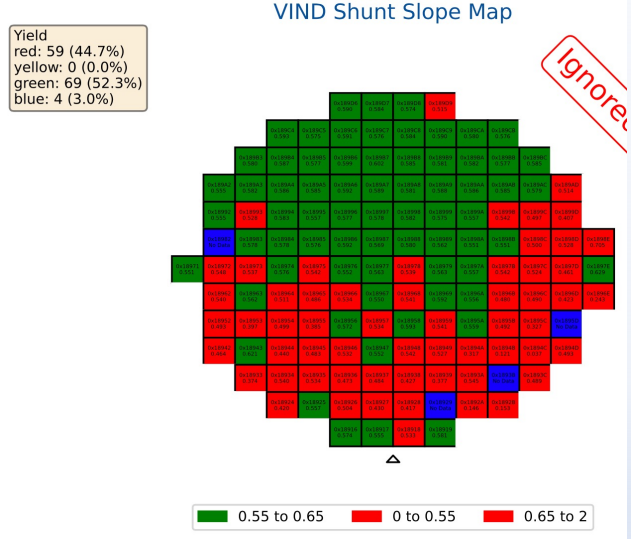
- April 2021 : ITk collaboration asks for contribution on wafer probing
  - ➢ Setup the probe station : calibration, driving, test configuration
  - ➢ Setup the instrumentation, cabling for BDAQ and probe card
  - ➢ Learn test operation : wafer handling, wafer & probe card alignment, chuck planarity
  - ➢ Installation & test of acquisition Python software
  - ➢ Test an RD53A wafer
- 2022 – Site qualification : 48^{h} test of ITkPixV1 wafer already tested in Bonn
  - ➢ Update of acquisition software (RD53A → RD53B)
  - ➢ Refine test operation : planarity, contact strength
  - ➢ Result comparison with Bonn

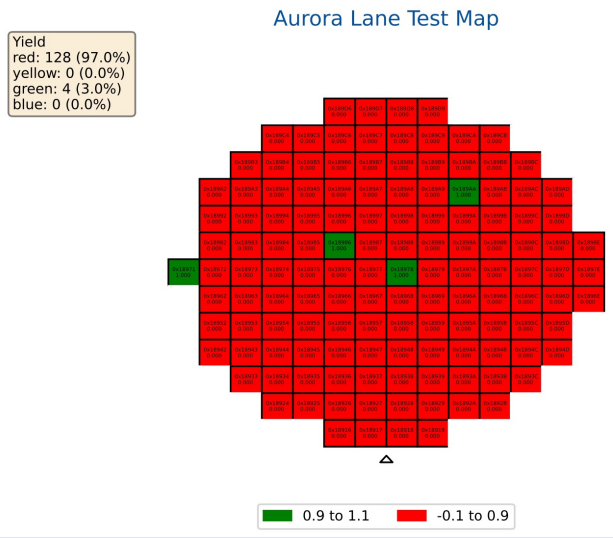


48h test ITkPixV1

- Some results similar to those from Bonn (Iref, VDD_), but some parameters are wrong (Vin_ , Aurora Lane, global Register Test)





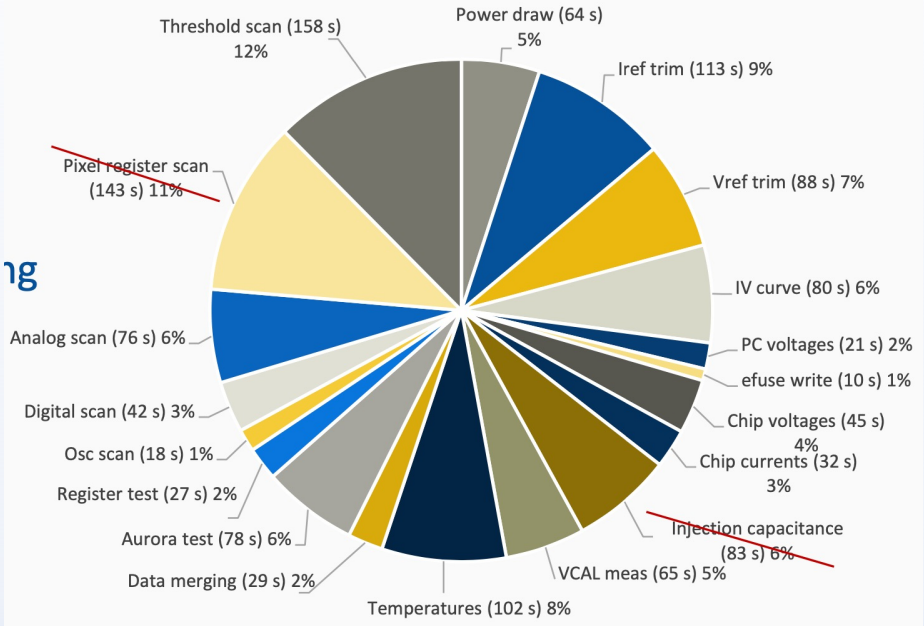


Actual status

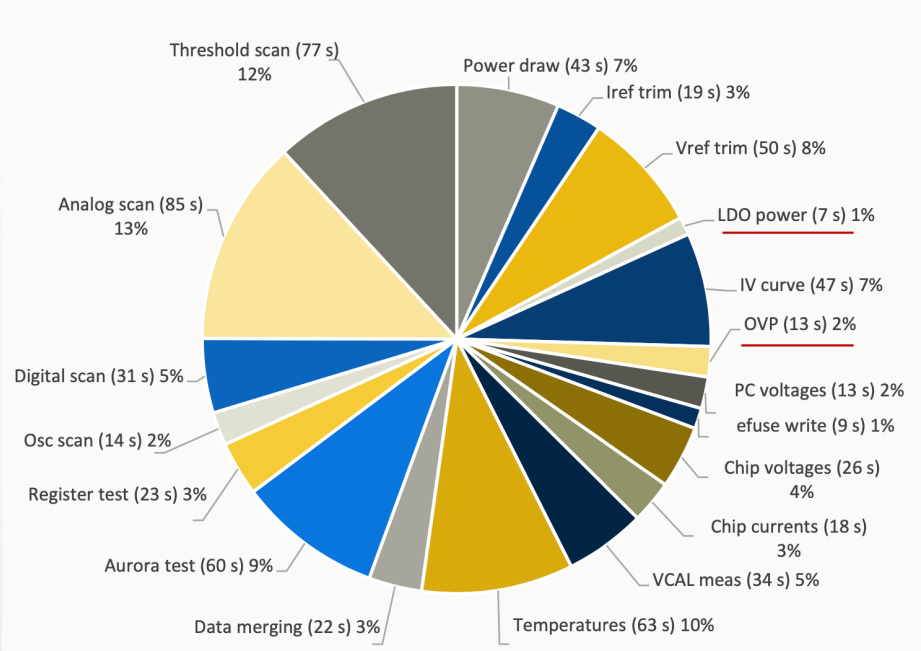
- Since 48^{h}–test, a lot of debugging mini–tests in series of a few chips :
  - ⇨ North – South difference : improvement on chuck planarity **OK**
  - ⇨ V_{in} drop : improved power supply sense cabling **OK** / check multimeter **ONGOING**
  - ⇨ Aurora Lane / register : results seem random **ONGOING**
- Once debug is done, qualification test with “virgin” ITkPixV1 wafer
- ITkPixV2 mechanical dummy and engineering already received
  - ↳ Need to upgrade software before testing: reduction of test duration 48^{h} → 24^{h}

ITkPixV2 : Test duration reduced

ITkPixV1



ITkPixV2



K. Mauer / M. Mucha (Bonn Univ.)

Test time = 48^{h}/wafer (20^{min}/chip)

3 wafer per week max.

Scan optimisation:

- few measurements removed
- Optimised sleep times
- Data analysis while acquisition

Test time = 24^{h}/wafer

5 wafer per week max.

Waferprobing planning

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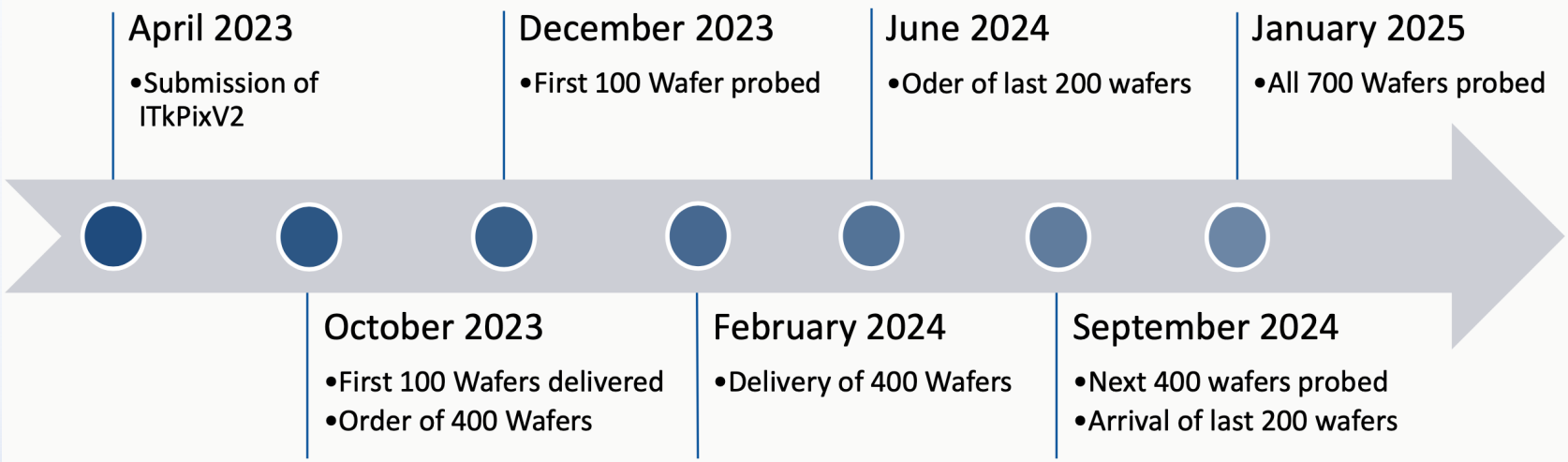
PROBING SCHEDULE: BEST CASE SCENARIO



Conclusions

- IJCLab contributes to wafer probing of front–end chips ITkPix
- We have learnt from scratch how to do this test with a semi–automatic probe station
- IJCLab qualification is almost achieved
- Tight schedule for testing ITkPixV2 wafers: finished in Jan 2025 if…
  - 3–4 probing sites during production
  - 4–5 wafers per week