future ASICs at OMEGA

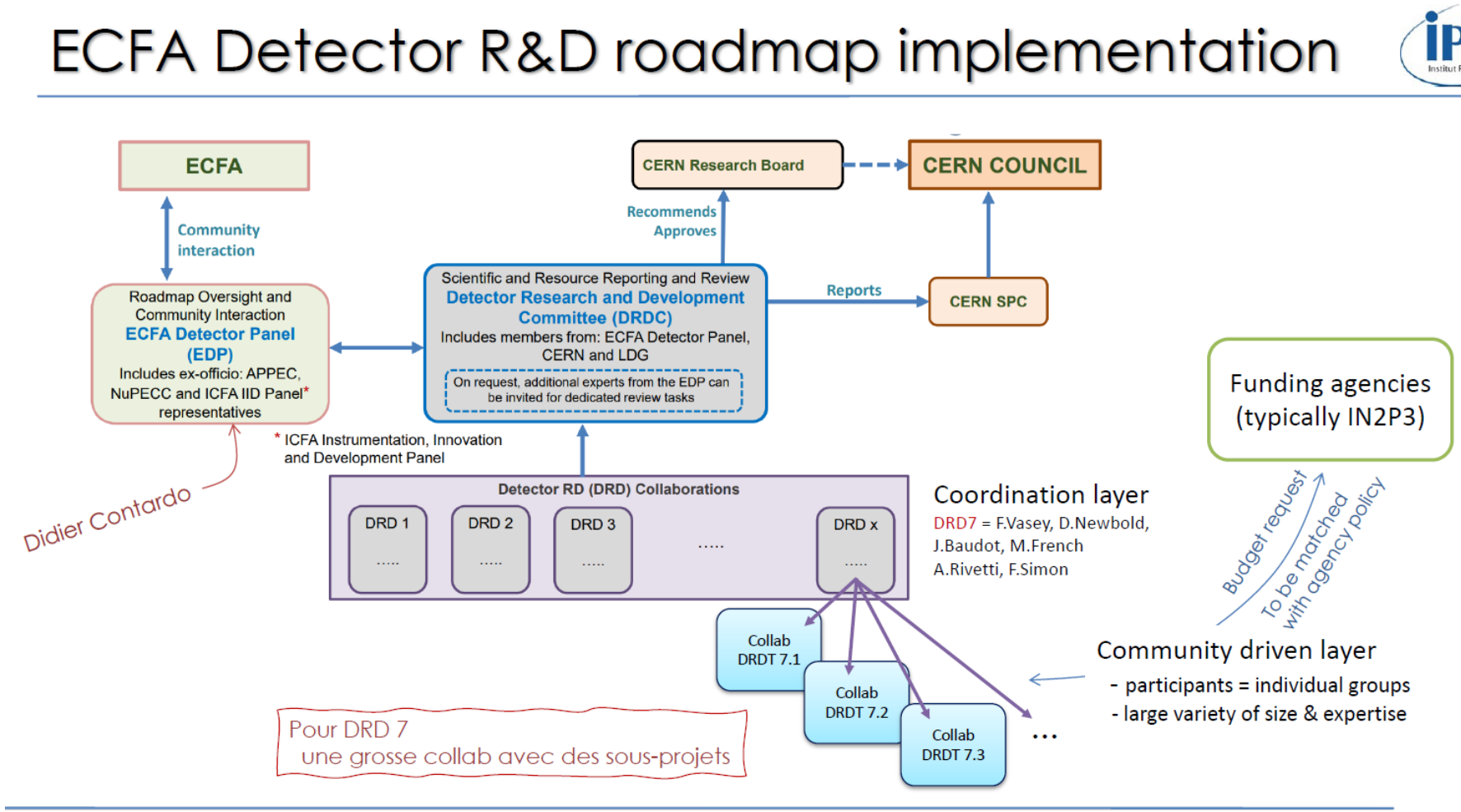
GDR DI2I Nantes 10 jul 23

Ch. de LA TAILLE

Organization for Micro-Electronics desiGn and Applications

ECFA roadmap [from J. Baudot]

- DRD1 : gas detectors
- DRD2 : liquid detectors
- DRD3 : semiconductors
- DRD4 : photon detectors
- DRD5 : quantum
- DRD6 : calorimetry
- DRD7 : electronics



DRD6 (calorimetry) readout schemes

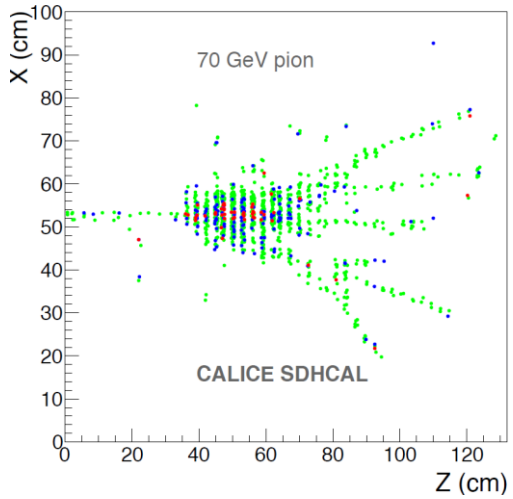
Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Trends for calorimeter readout

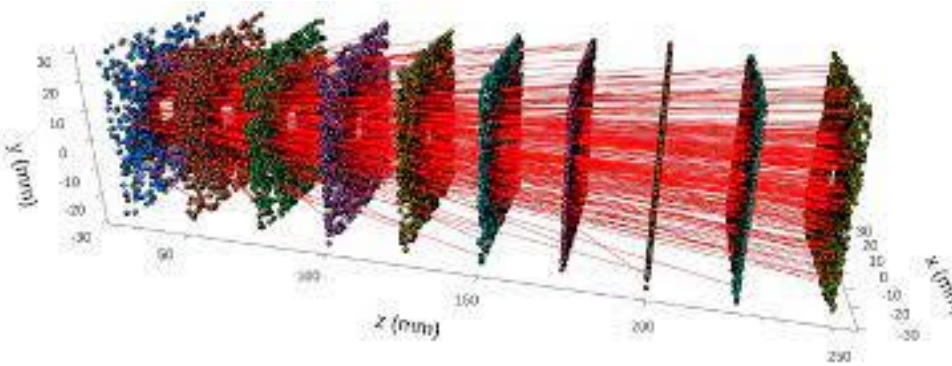
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added



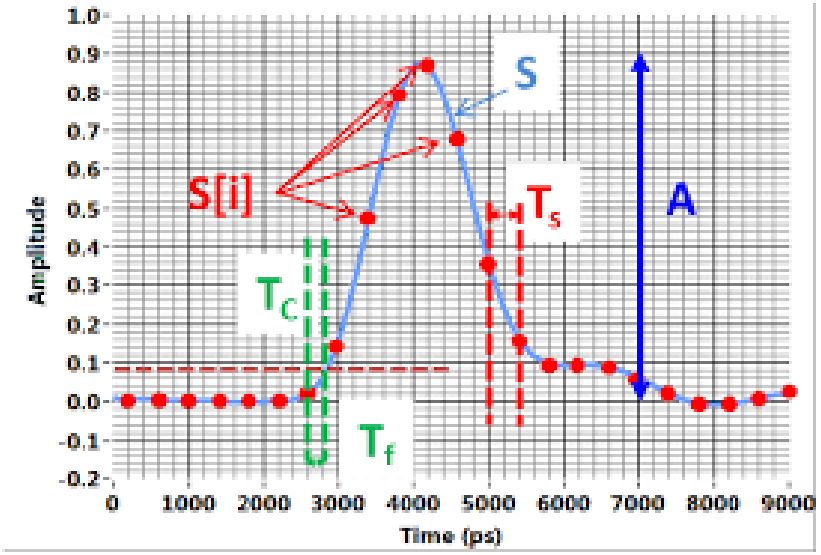
- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

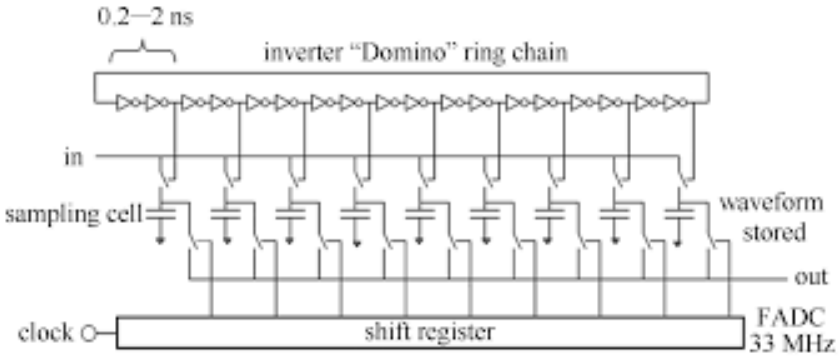


Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SAMPIC…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization



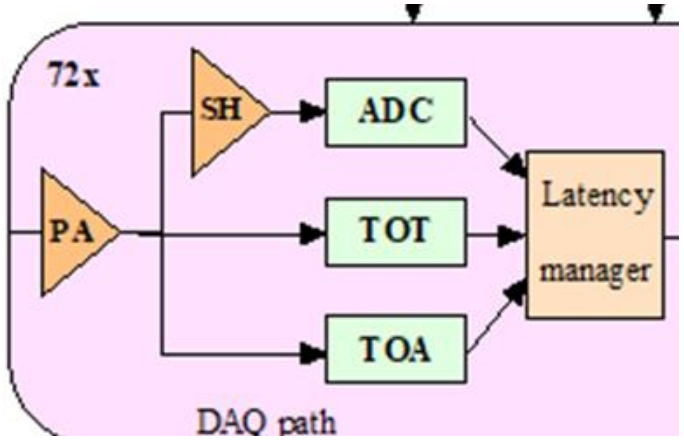


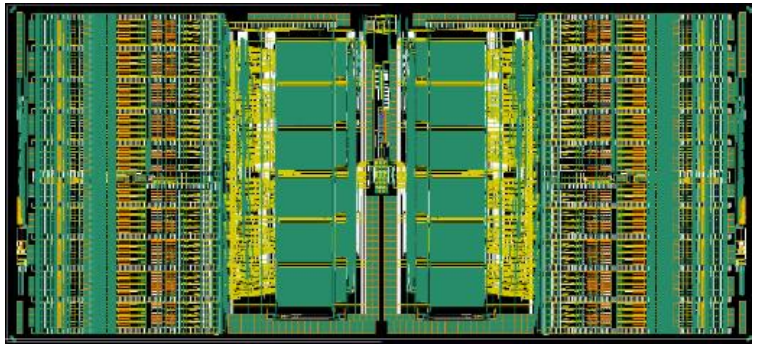
Embedded ASICs

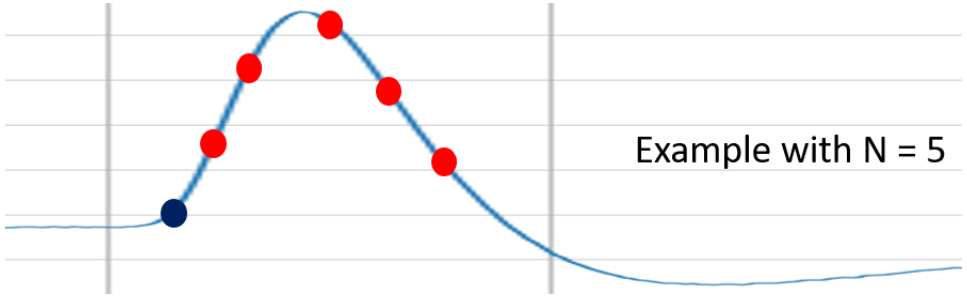
- Pioneered with CALICE R&D (SKIROC, SPIROC..)

- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)

- Difficulties
  - Analog/digital couplings





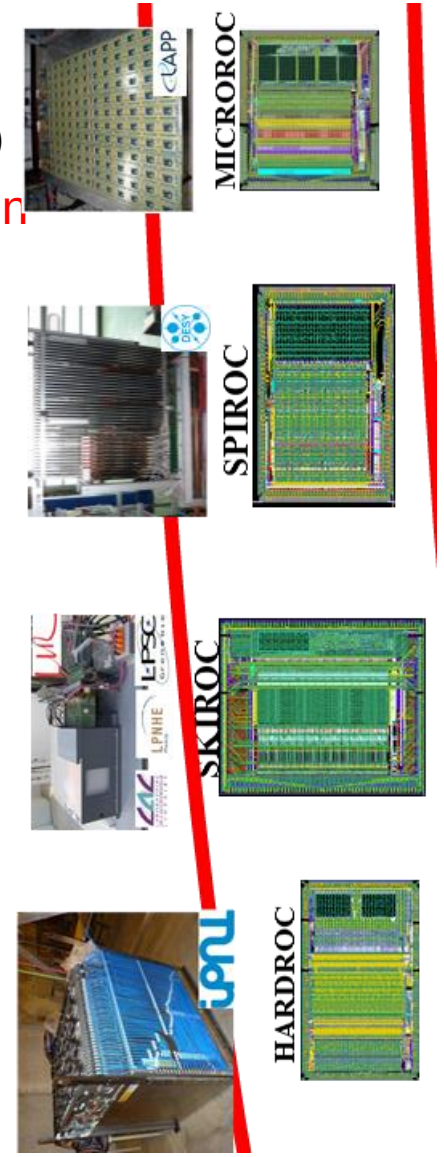


DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch
  - Allows better granularity or LAr operation
  - Extend to LAr (cryogenic operation) and MCPs (PID)
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Several improvements foreseen in the VFE and digitization parts

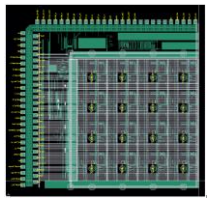
- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL

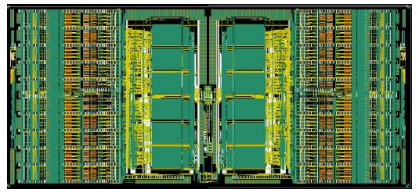


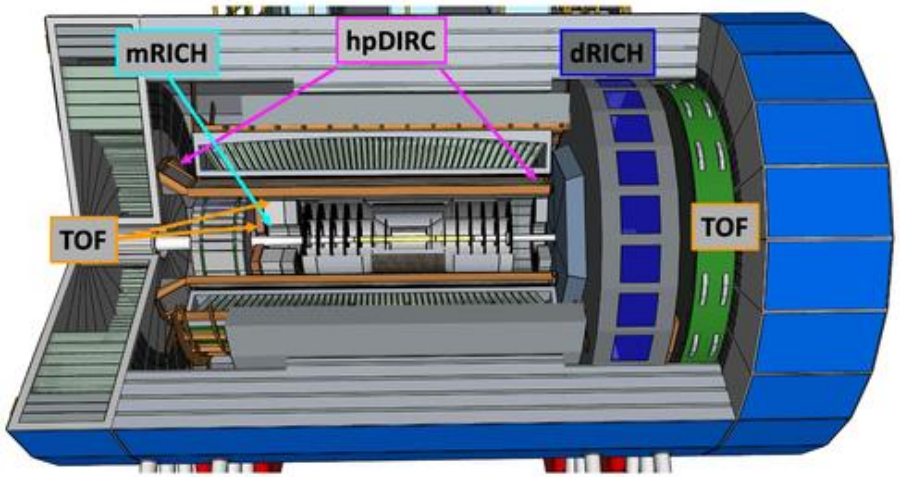
Chips for EIC : electron-ion collider at BNL

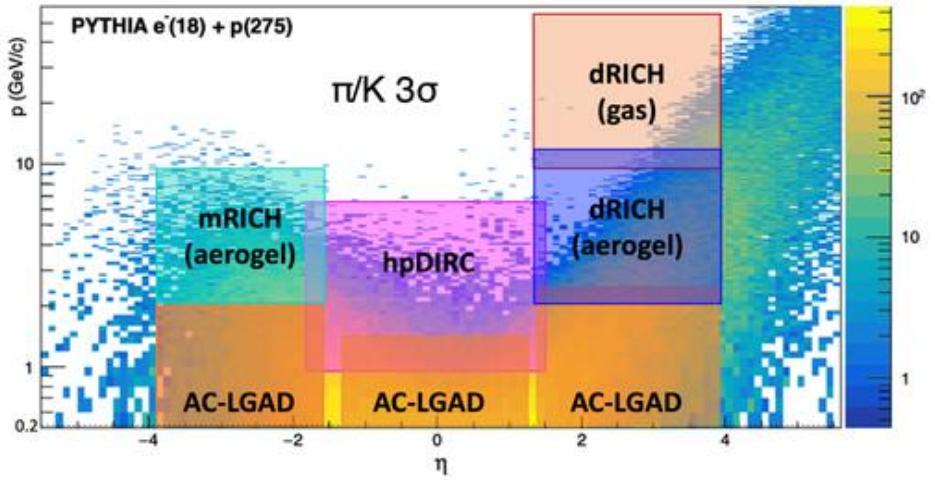
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - HGCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA





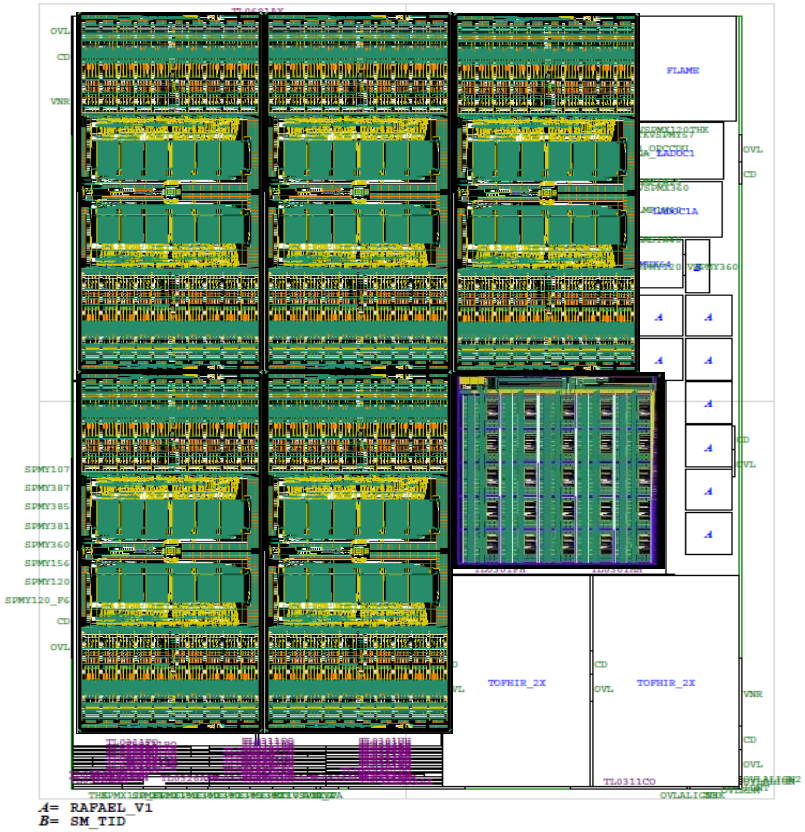




Next OMEGA chips

- Large chips, large detectors need engineering runs

- Chips for calorimetry and timing : EIC, DRD1-4-6
  - HGCROC4 (EIC & DRD6)
    - Dynamic gain switching
    - New digital « à la HKROC »
  - HKROC SiPM (EIC & DRD4-6)
    - New conveyor, new digital
  - EICROC (AC-LGAD & HRPPD EIC) : 16-32 x 4-8 -> 32 x 32
    - Fix digital noise, reduce ADC power
  - SPACIROC4 ?
    - 300 MHz photon counting and charge integration for EUSO

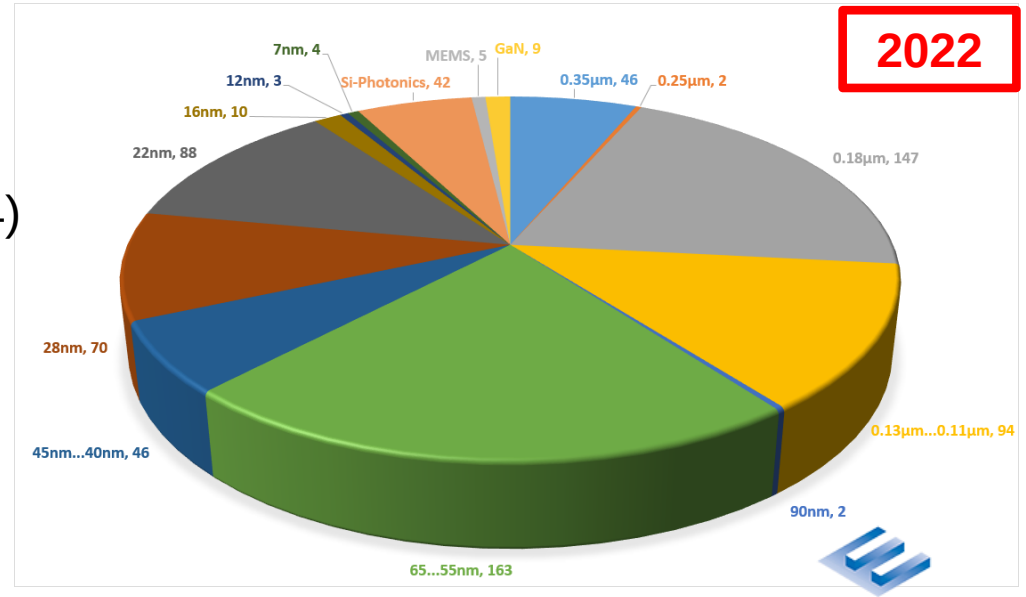


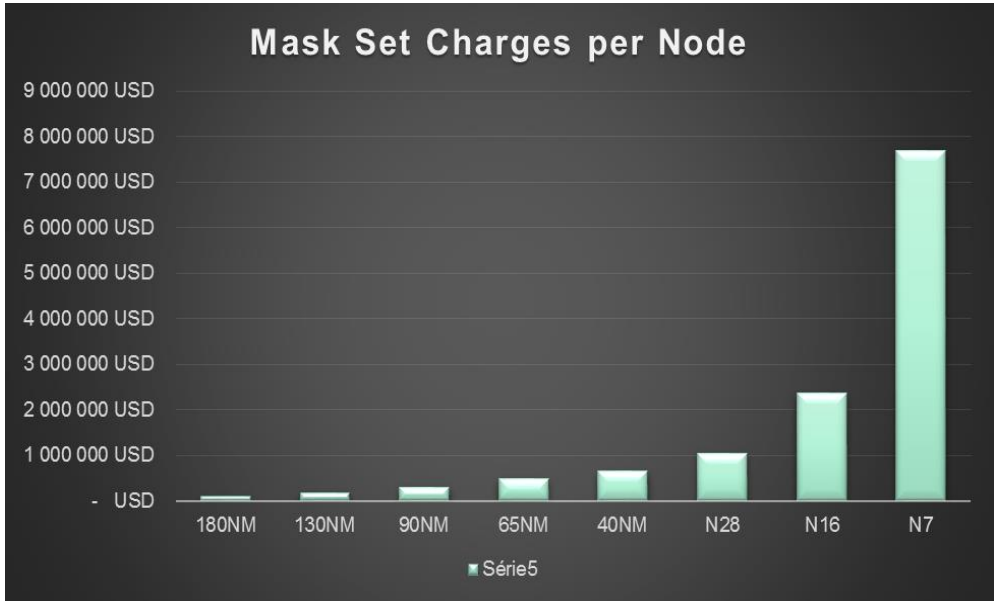
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





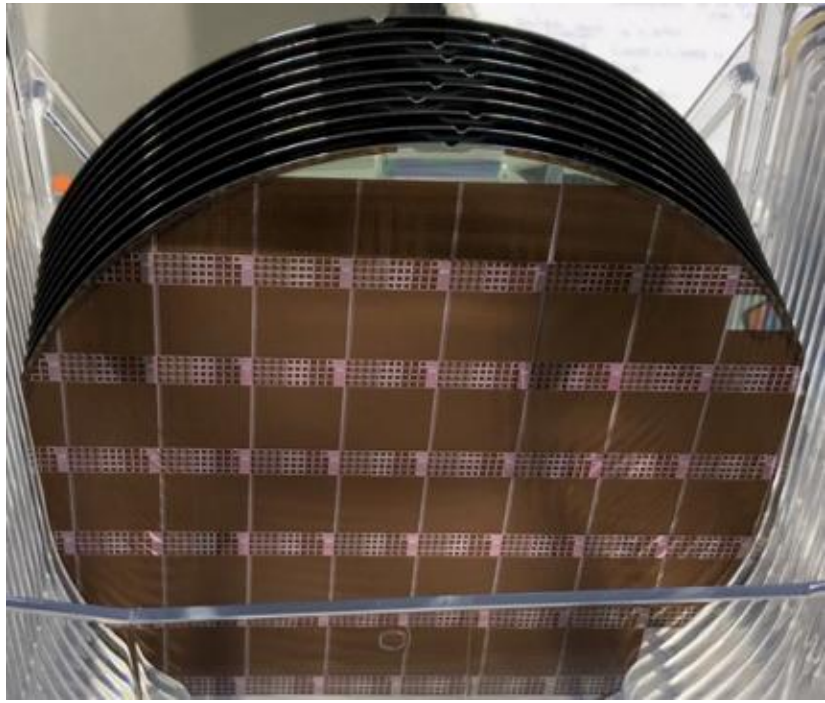
c4. Interface with other DRDs

DRAFT, under discussion

- R&D in electronics is not carried out in isolation
  - Many engineers will be active in both DRD-specific projects and DRD7 generic R&D
  - DRD-specific projects will take care of
    - Determination of system parameters and specifications
    - Planning and costing of prototype development and production
    - Production, verification, and integration of ASICs and other project-specific components
    - Testing and operation of large-scale prototypes
  - DRD7 projects will
    - Review system specifications and design as requested, possibly also on a rolling basis during the course of the project, and including analysis of engineering effort and specialised skills requirements
    - Provision access to tools and vendors
    - Develop and provision common IP, components, and subsystems, encompassing hardware, firmware and software
    - Develop common, generic, complete components or systems, when too big or too complex to be designed in one single DRD
    - Provision specialised or large-scale facilities for electronic development and testing

conclusion

- Importance of joint optimization detector/readout electronics

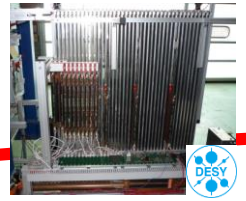


- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)
- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O
- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing
- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

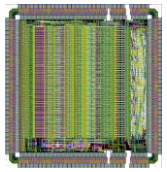
backup

ASICs produced and installed on detectors

Omega

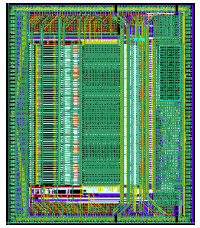


MAROC3

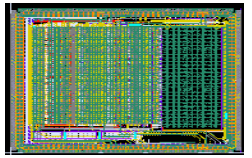


2006

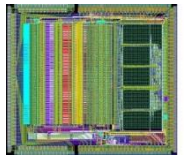
SKIROC



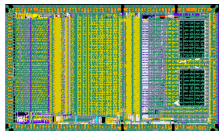
SPIROC



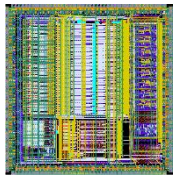
MICROROC



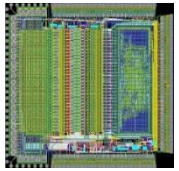
HARDROC



SPACIROC



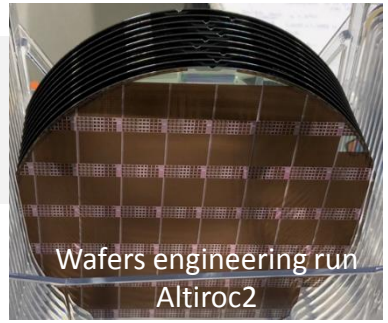
PETIROC



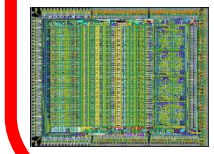
9 engineering runs in 9 years :

AMS SiGe 0,35um 2014, 2016, 2018

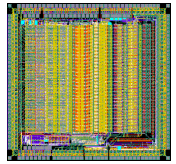
TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



TRIROC

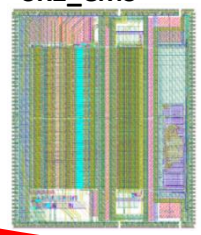


CITIROC

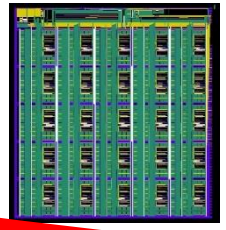


CATIROC

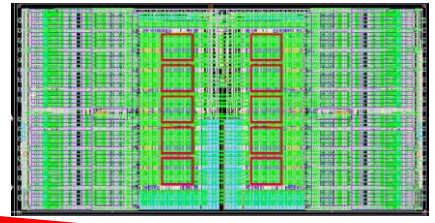
SK2_CMS



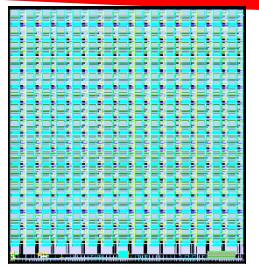
ALTIROC1



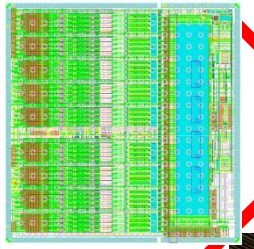
HGCROC



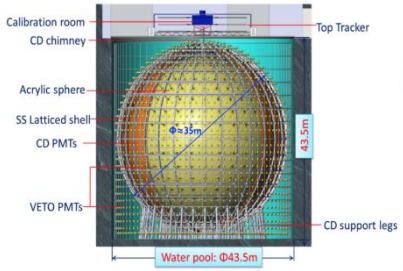
ALTIROC2

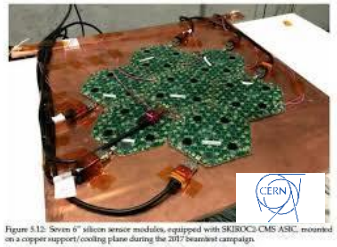


HKROC

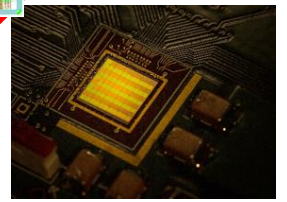


2023



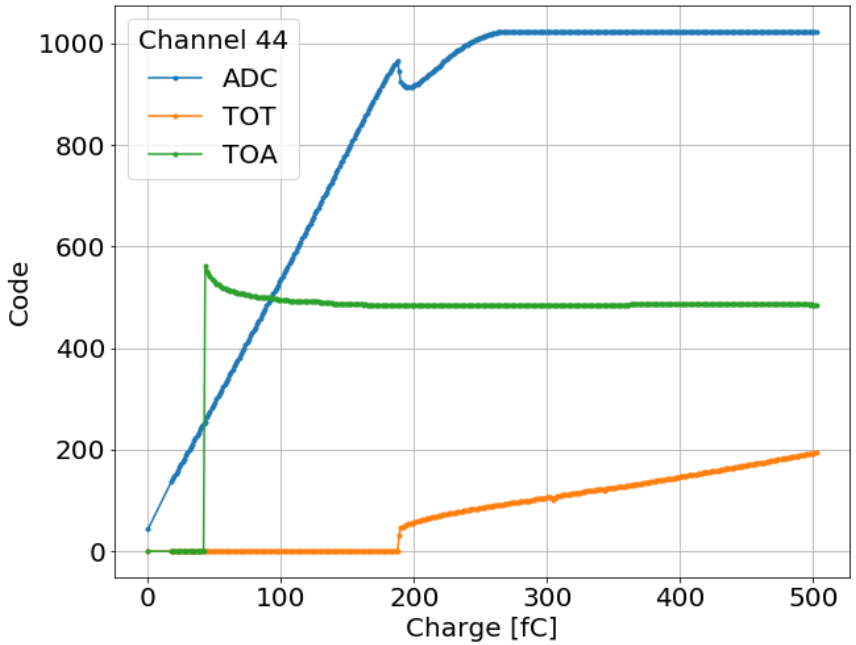


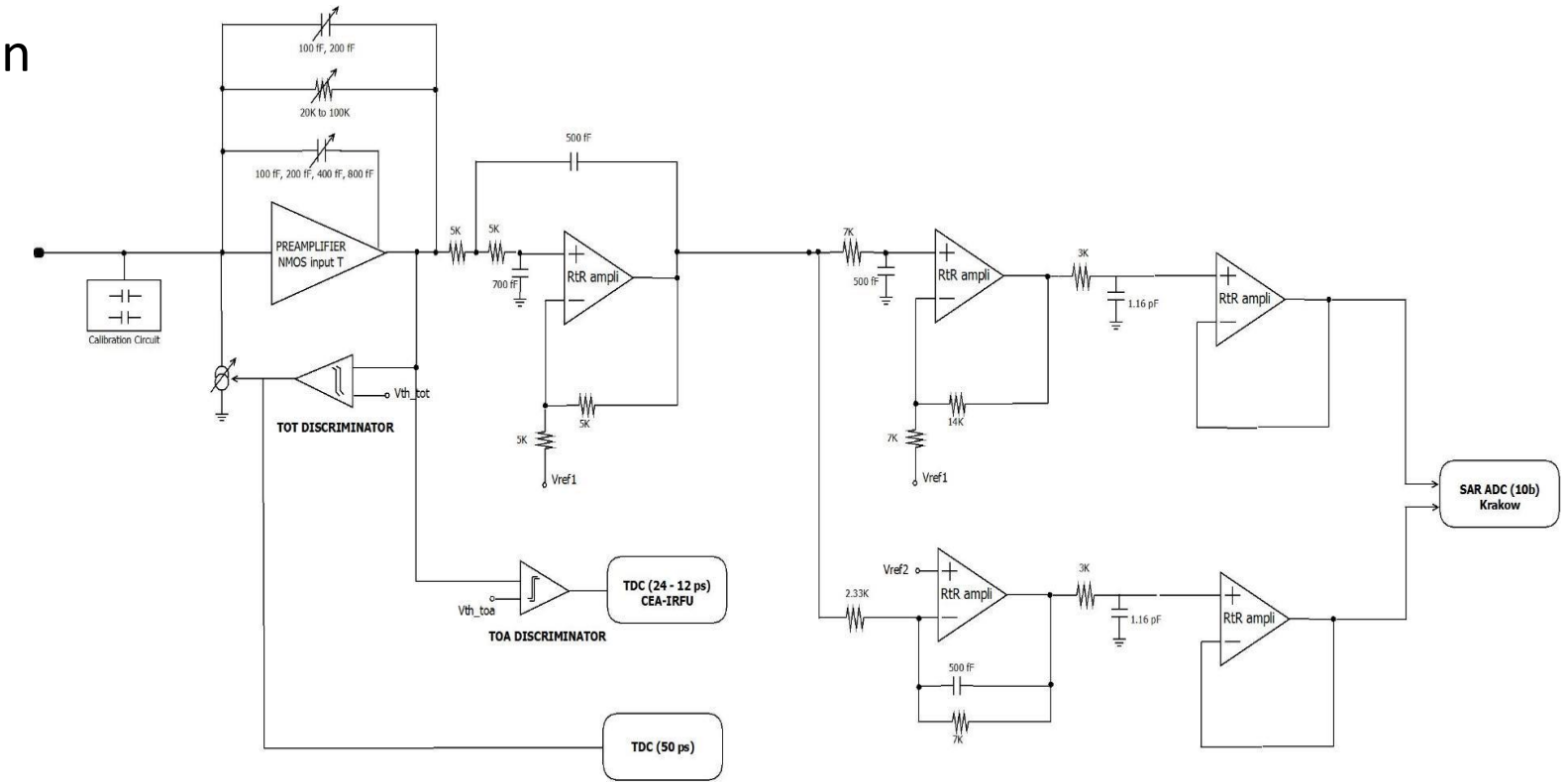
CALICE 29 mar



HGCROC : ADC and TOT

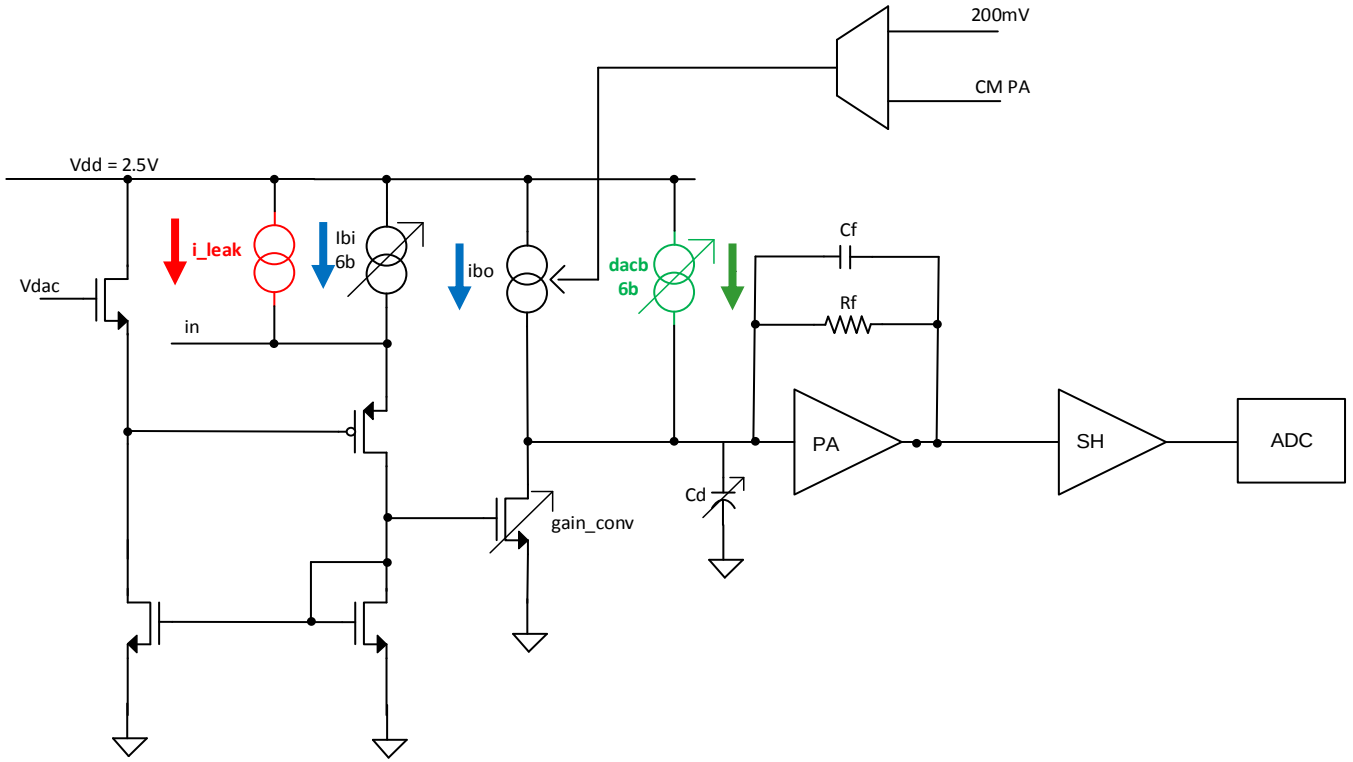
- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- 200 ns dead time
- Not well adapted to SiPM version

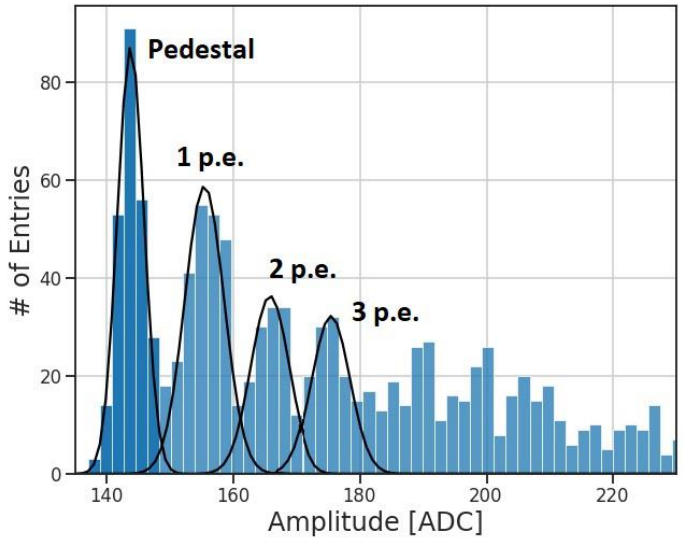


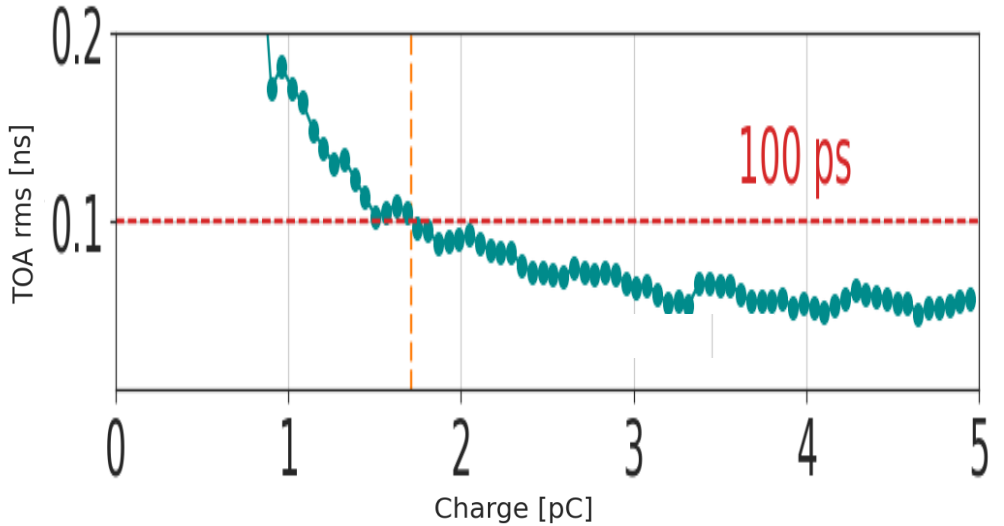


H2GCROC: the current conveyor

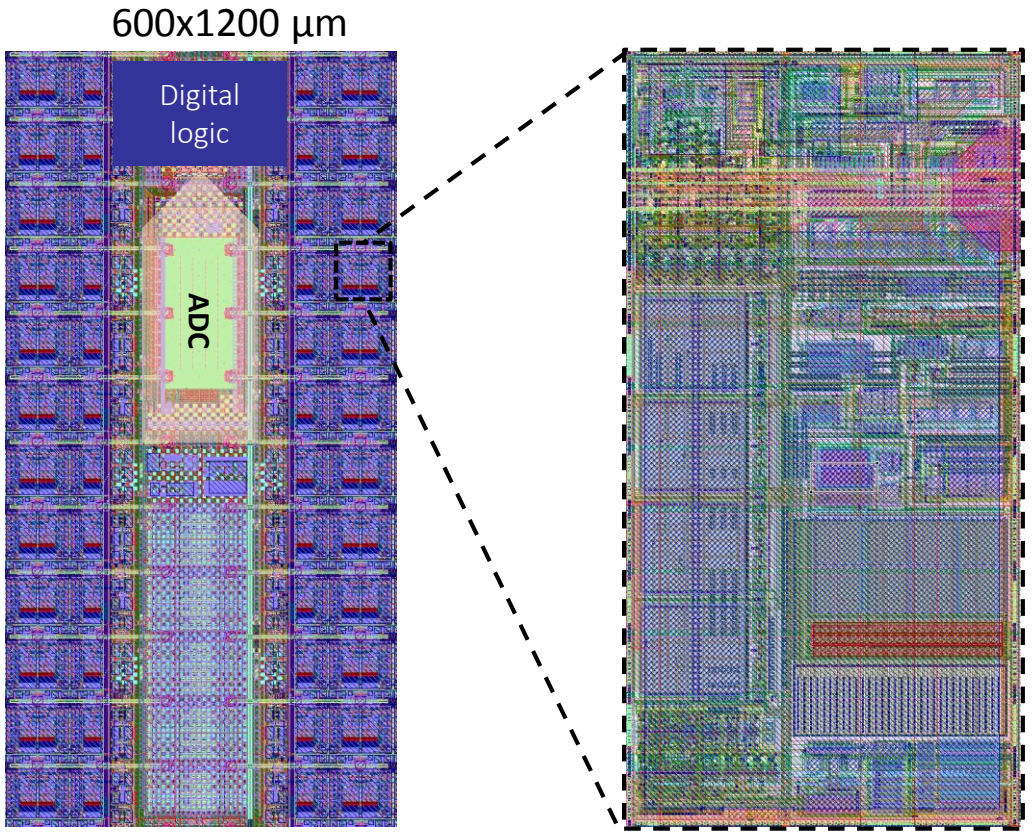
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**
- **Not enough gain for good SPTR**







Dynamic gain switching : Pixel matrix architecture [SLAC]

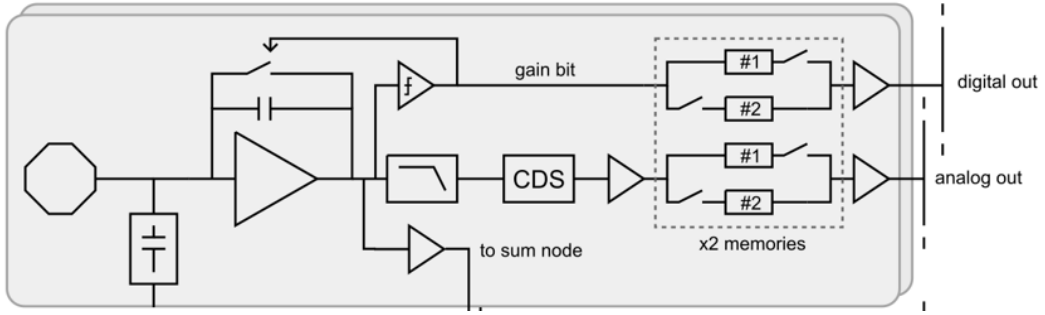


Cluster

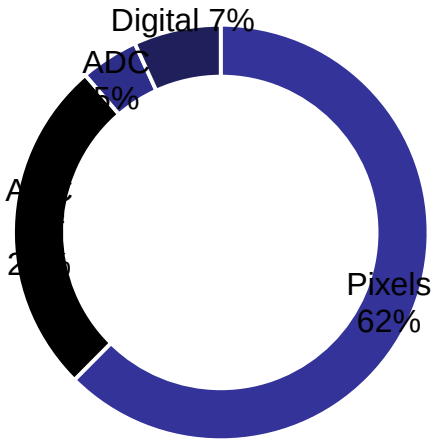
- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

Pixel

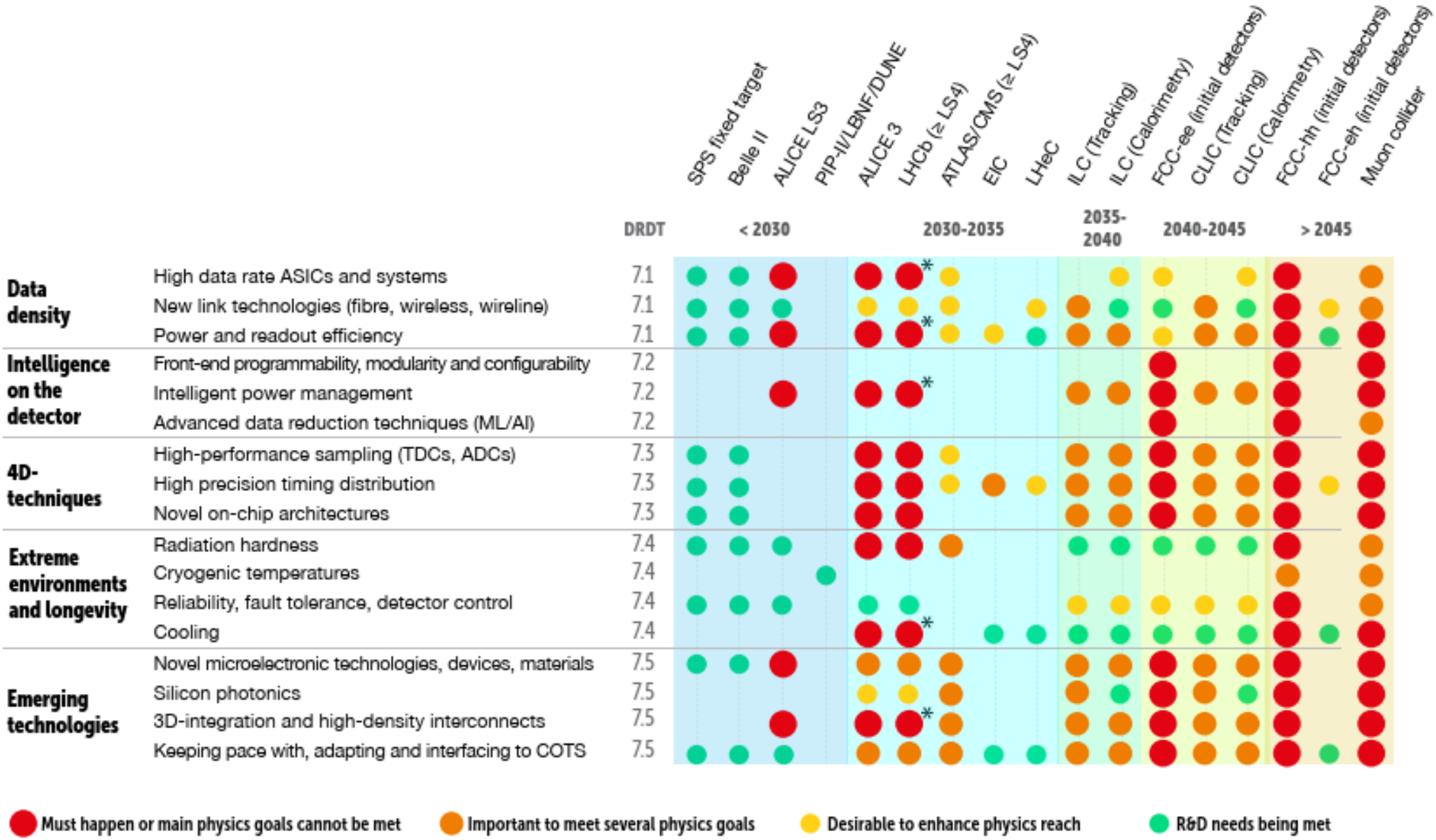
- Operates at 100 kHz – 1 MHz
- Si sensor: 100x100 µm^2
- ASIC: 50x100 µm^2



Pixel analog front-end block diagram



Power consumption of different blocks in matrix
(power density: 0.94 W/cm^2)


SPS fixed target
Belle II
ALICE LS3
PIP-II/LBNF/DUNE
ALICE 3
LHCb (≥ LS4)
ATLAS/CMS (≥ LS4)
EIC
LHeC
ILC (Tracking)
ILC (Calorimetry)
FCC-ee (initial detectors)
CLIC (Tracking)
CLIC (Calorimetry)
FCC-hh (initial detectors)
FCC-eh (initial detectors)
Muon collider
DRDT
< 2030
2030-2035
2035-2040
2040-2045
> 2045
Data density
High data rate ASICs and systems 7.1
New link technologies (fibre, wireless, wireline) 7.1
Power and readout efficiency 7.1
Intelligence on the detector
Front-end programmability, modularity and configurability 7.2
Intelligent power management 7.2
Advanced data reduction techniques (ML/AI) 7.2
4D-techniques
High-performance sampling (TDCs, ADCs) 7.3
High precision timing distribution 7.3
Novel on-chip architectures 7.3
Extreme environments and longevity
Radiation hardness 7.4
Cryogenic temperatures 7.4
Reliability, fault tolerance, detector control 7.4
Cooling 7.4
Emerging technologies
Novel microelectronic technologies, devices, materials 7.5
Silicon photonics 7.5
3D-integration and high-density interconnects 7.5
Keeping pace with, adapting and interfacing to COTS 7.5
Must happen or main physics goals cannot be met
Important to meet several physics goals
Desirable to enhance physics reach
R&D needs being met