OMEGA ROC CHIPs

On behalf of the Omega laboratory

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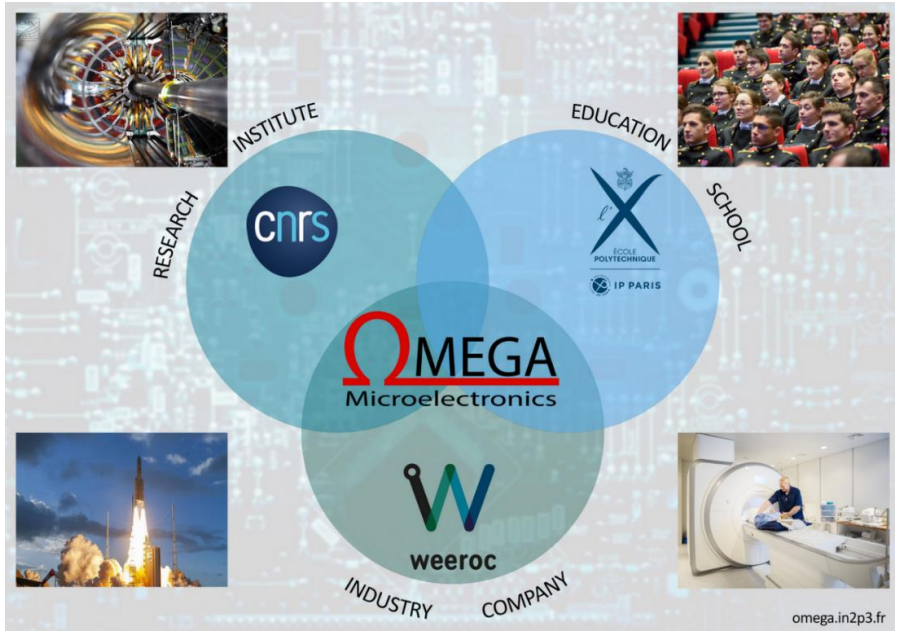
Ecole Polytechnique – CNRS

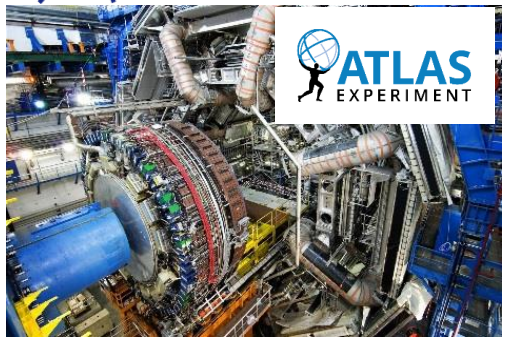
Organization for Micro-Electronics desiGn and Applications

OMEGA Microelectronics Laboratory

- National Micro-electronics design center to address readout electronics needs for instrumentation in Particle and Astroparticle Physics: **10 CNRS staff engineers**, highly specialized in low noise, rad-hard, high speed mixed-signal readout ASICs **+ 2 CDD engineers** + **3 PHD students**

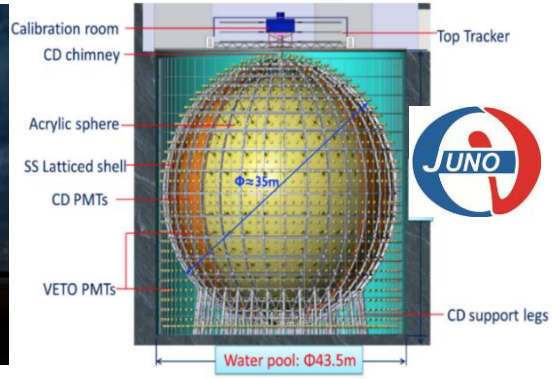


CERN SLAC NATIONAL ACCELERATOR LABORATORY BROOKHAVEN NATIONAL LABORATORY SMU IFAE



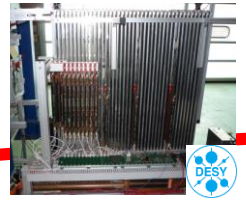
Institute of High Energy Physics
Chinese Academy of Sciences
Fermilab
Imperial College London
DESY
irfu
saclay
NASA

KEK cnes

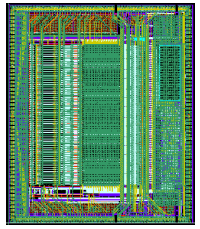


ASICs produced and installed on detectors since 2006

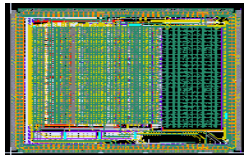
Omega



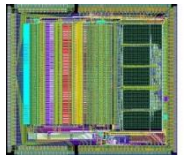
SKIROC



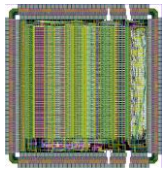
SPIROC



MICROROC

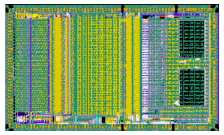


MAROC3

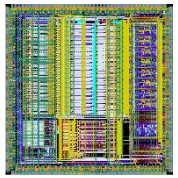


2006

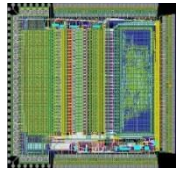
HARDROC



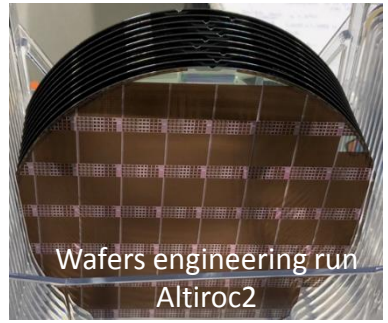
SPACIROC



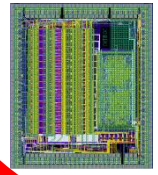
PETIROC



2016
SiGe 350 nm → CMOS 130nm

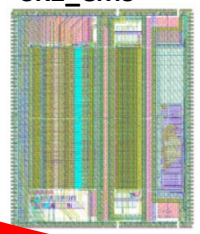


CATIROC

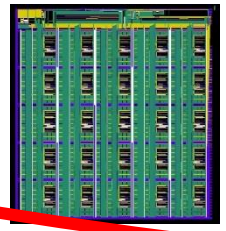


2016

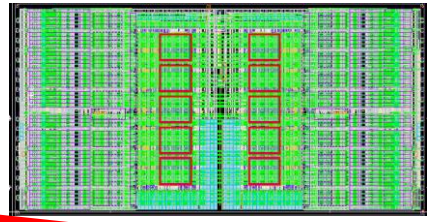
SK2_CMS



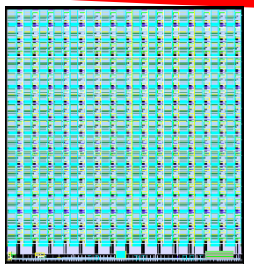
ALTIROC1



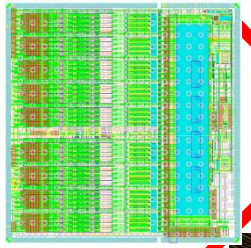
HGCROC



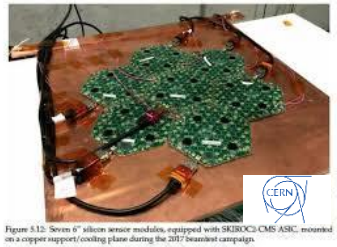
ALTIROC2

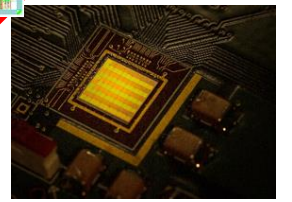


HKROC



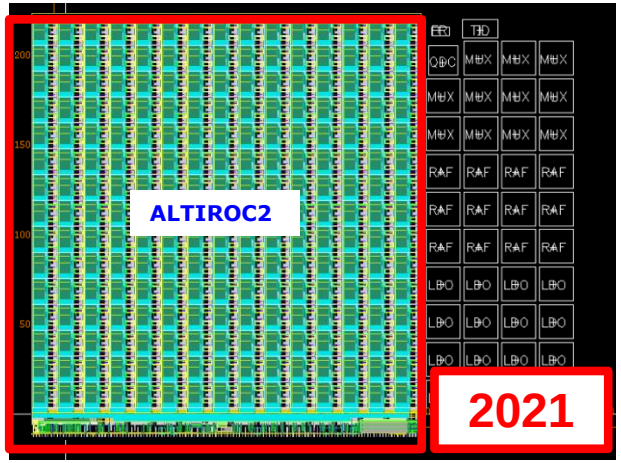
2023

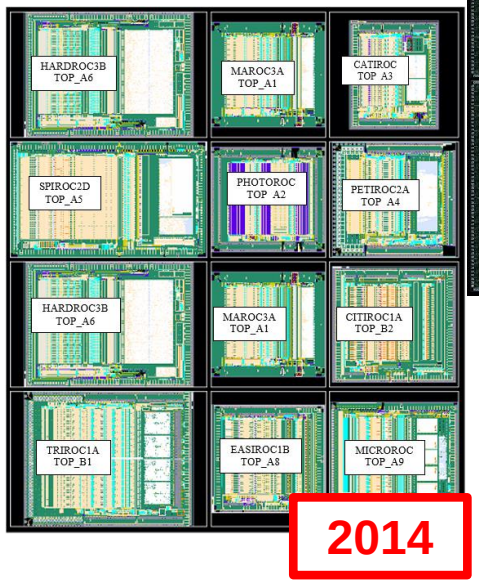


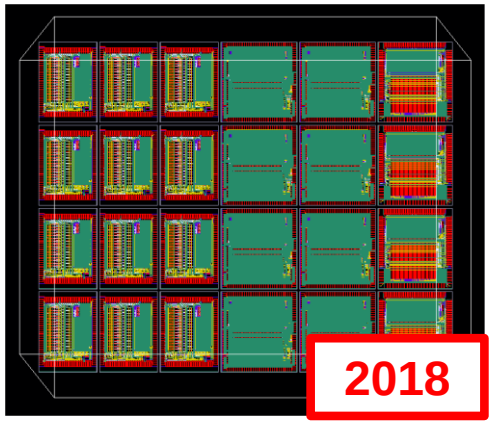


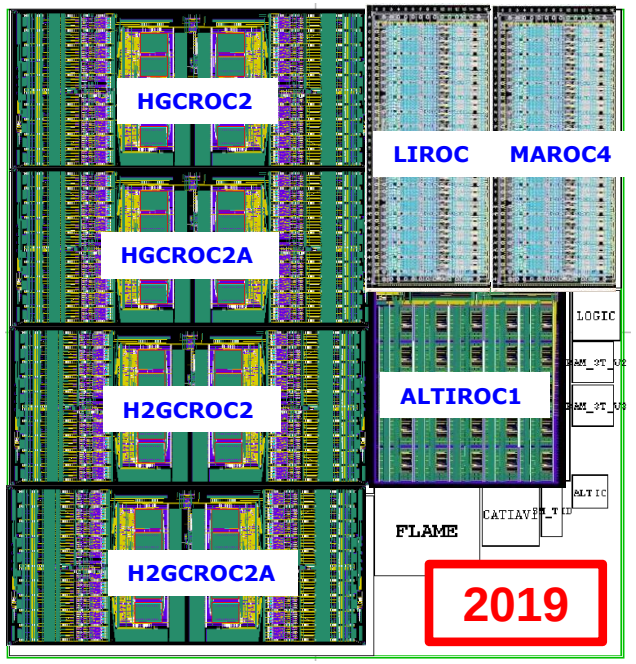
OMEGA Engineering runs

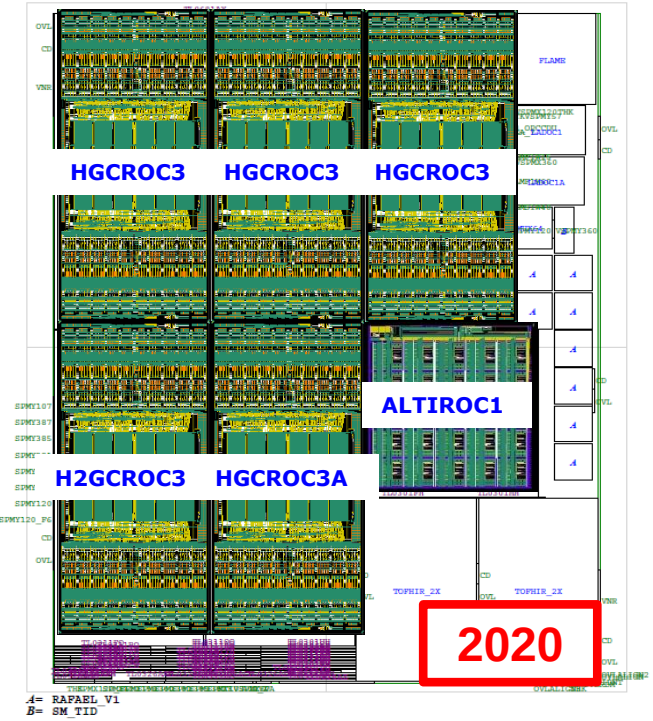
- **9 engineering runs** in **10 years** !
  - **AMS SiGe 0,35um** 2014, 2016, 2018
  - **TSMc 130nm** : 2019, 2020, 2021, 2022, 2x 2023.
  - 6-24 wafers 8'' and 12'' : thousands of ASICs built and used
  - Cost : 200-300 k€, shared between projects : very efficient !







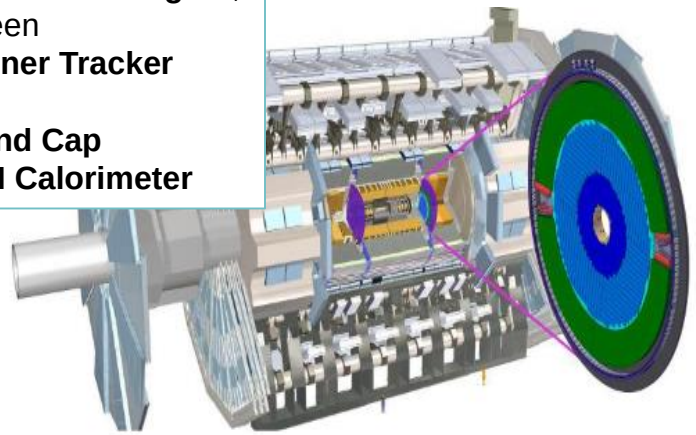




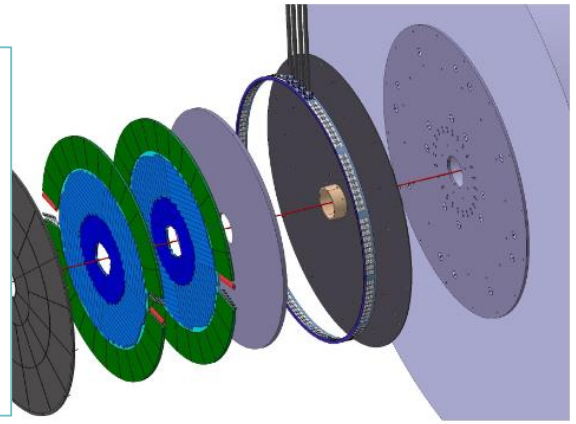
ATLAS HGTD (Timing detector): ALTIROC

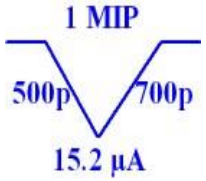
For the **High-Luminosity phase of LHC**, the ATLAS experiment proposed the addition of a **High Granularity Timing Detector (HGTD)** to mitigate the effects of the increased **pile-up**.

In the **forward region**, between the **Inner Tracker** and the **End Cap of EM Calorimeter**

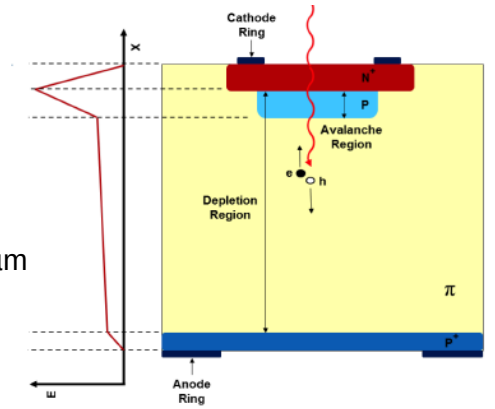


2 disks
2 layers/disk
Equipped with Low Gain Avalanche Diodes (**LGAD**)

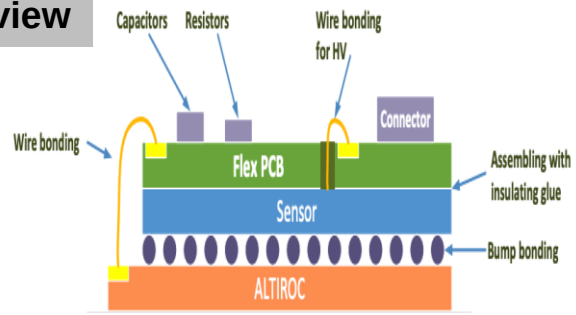




LGAD sensor
1.3 x 1.3 mm^2
Thickness = 50 µm
Cd = 4 pF

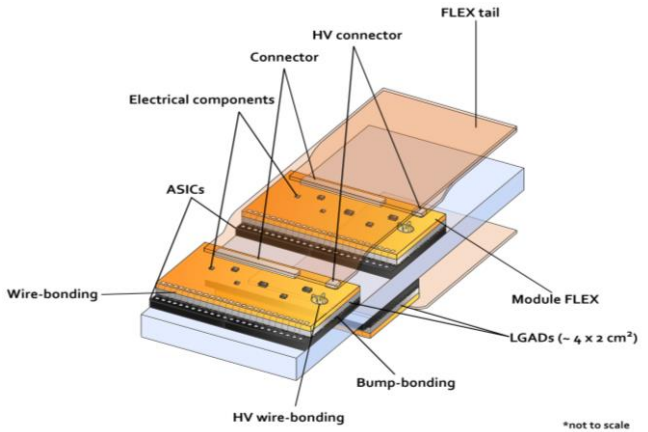


Module: side view



Very challenging ASIC requirements Major requirements	
Time measurement precision **Electronics jitter:**	**35 ps/ hit for Q = 10 fC** **70 ps for Q = 4 fC** **25 ps for Q = 10 fC** **65 ps for Q = 4 fC**
Minimum threshold	**2 fC**
Noise	**< 0.5 fC**
Crosstalk	**< 2%**
Charge dynamic	up to 100 fC
ASIC power dissipation Analog very front-end TDC Digital	< 1.2 W < 2 mW 0,5 mW at 10 % occupancy < 2 mW

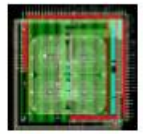
Module: top view



(2×4 cm²; 15×30 channels)
2 ASICs+2 sensors/module

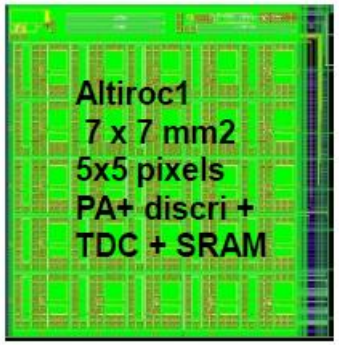
ALTIROC GENEALOGY

2016



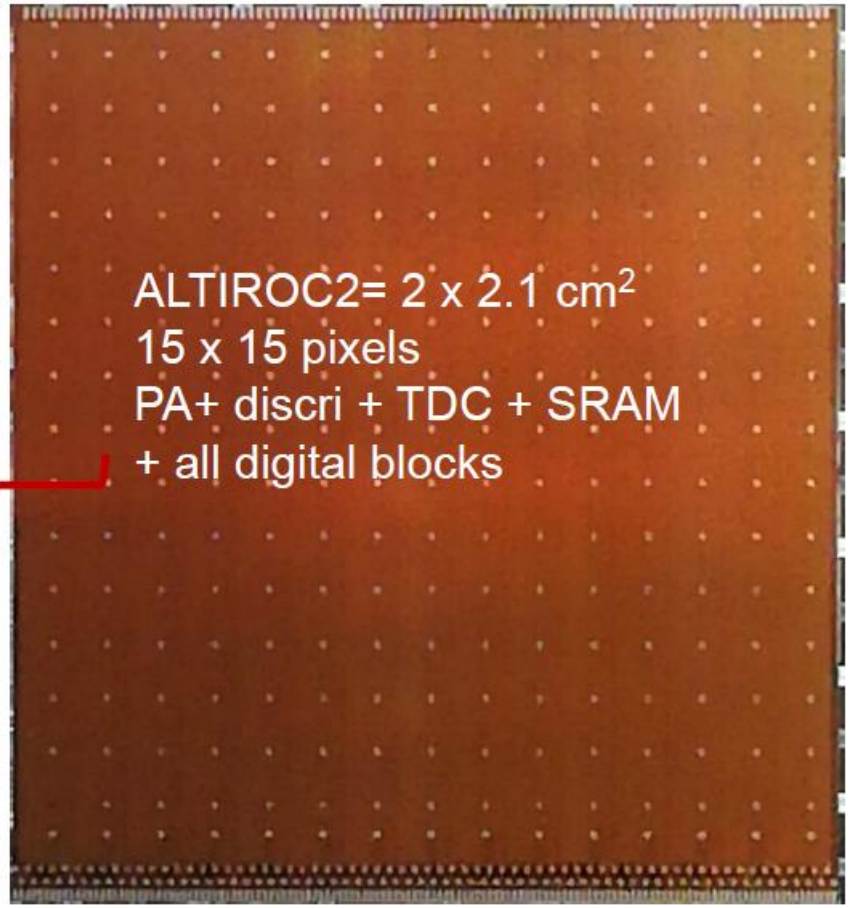
Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

2017



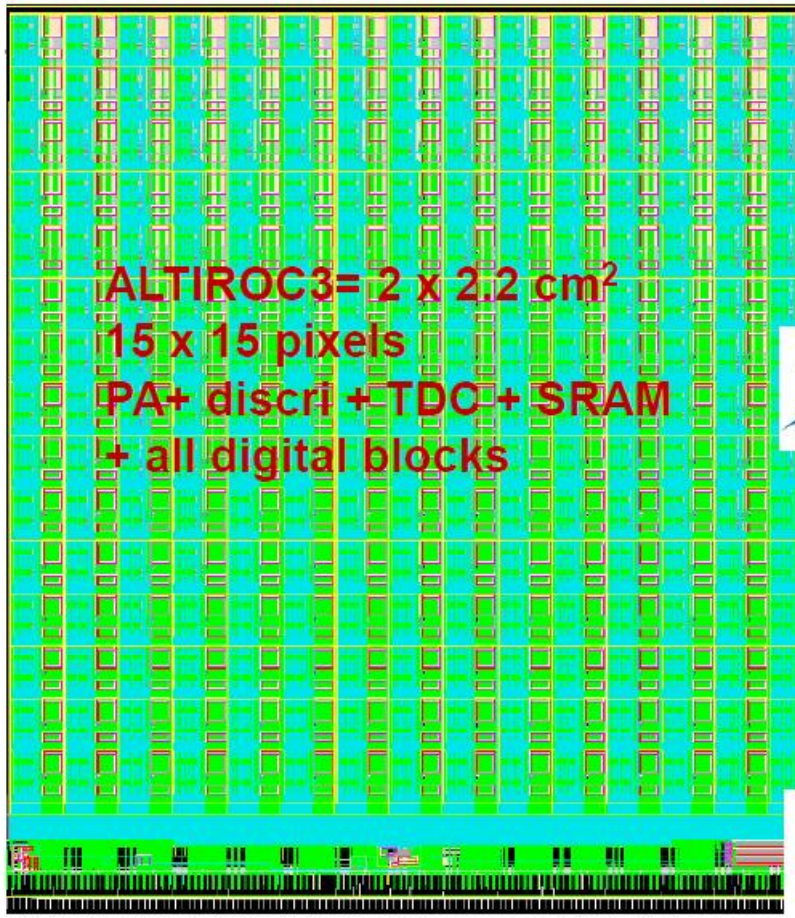
Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

2019



ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

2022



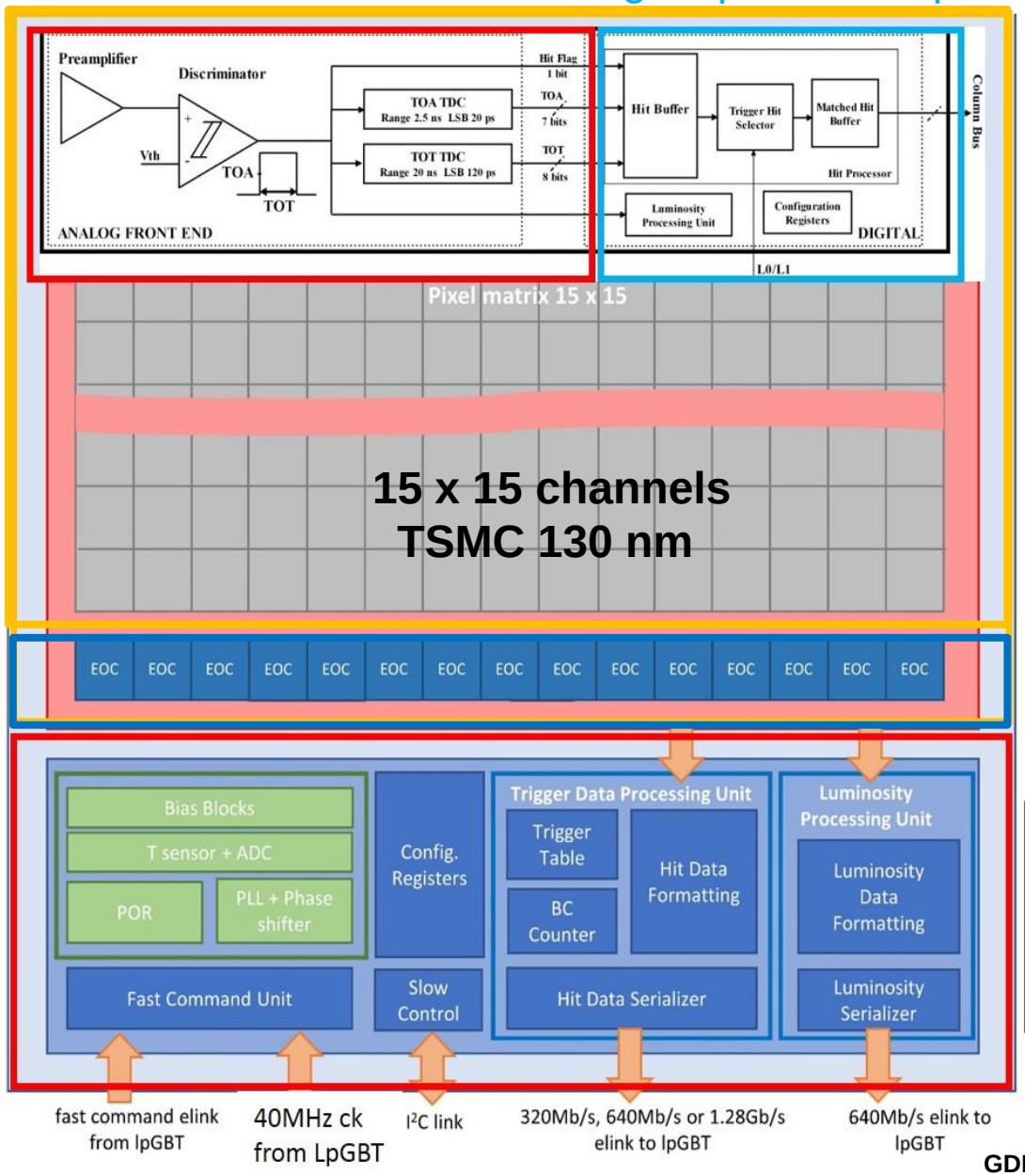
ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

ASIC design coordinator:
Nathalie Seguin-Moreau

ALTIROC 2 and 3 architecture

Analog front-end pixel

Digital part of the pixel



Matrix

EOC

Periphery

ALTIROC2&3 pixel integrates :

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- **Analog Front End pixel:Analog FE performance crucial**
  - **1 GHz preamplifier** followed by a high-speed **discriminator**.
  - **Two TDC** (Time to Digital Converter) to provide Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
    - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
    - TOT TDC: bin of 120 ps (8 bits), range of 20 ns
- **Digital part of the pixel**
  - One SRAM (Hit buffer) with a latency of 38.4 µs
  - Zero suppress logic (Trigger Hit Selector and Matched Hit Buffer)
  - Luminosity processing unit

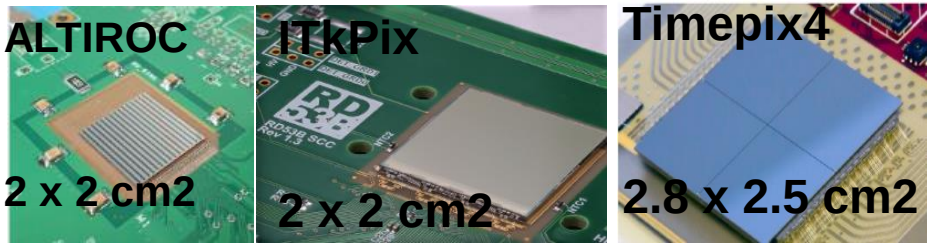
EOC: readout of columns + data transfer to trigger data and luminosity data processing units

ALTIROC2 Periphery

- **Analog periphery**: Bias, DAC for threshold, temp sensor, PLL, Phase Shifter, clocks receivers, data transmitters (up to 1.28 Gb/s)
- **Digital periphery:**
  - 320 Mbit/s fast commands decoder
  - Trigger Processing unit: Modified in Altiroc3: Reads time data from pixel matrix and packs data into frames before serializing them
- Hit data transmission: Average data to be transmitted depends on radial position: 320 Mb/s, 640 Mb/s, **1.28 Gb/s**
- Slow Control: I2C link, 1024 * 8-bit registers (Triplication + auto correction)

Main challenges: technical difficulties

Altiroc looks “similar “ to pixels ASIC such as ITK and Timepix ASIC but



Minimum Charge Qmin/ Detector capacitance Cd

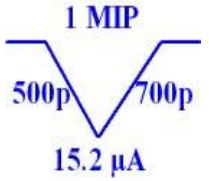
- **Altiroc: Qmin/Cd ~ 500 µV** with **Cd ~4 pF** (1300 x 1300 µm2) and Vth min= **2 fC**
- ITK (no time measurement) , **Timepix4**: Qmin/C > 2 mV with Cd ~ **50 fF** (50 x 50 µm^2) and Vth min = 0.1 – **0.2 fC**

Preamp BW

- Altiroc: **1 GHz**
- Timepix4: ~ 20 MHz

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Cd: detector capacitance
$t_{10\_90\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

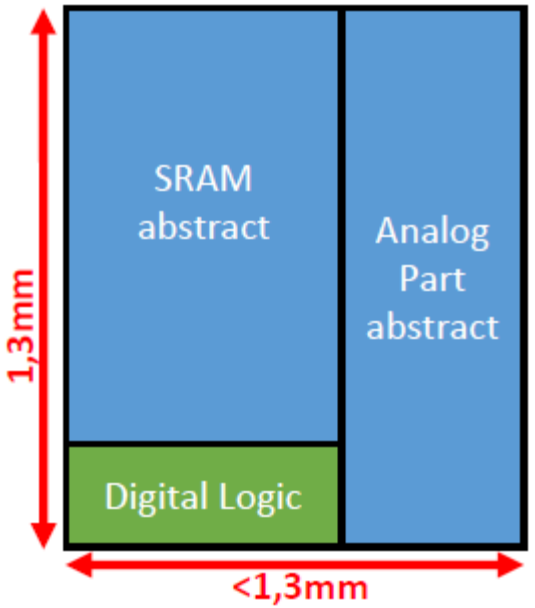


TDC bin

- Altiroc: **20 ps**
- Timepix4: **200 ps**

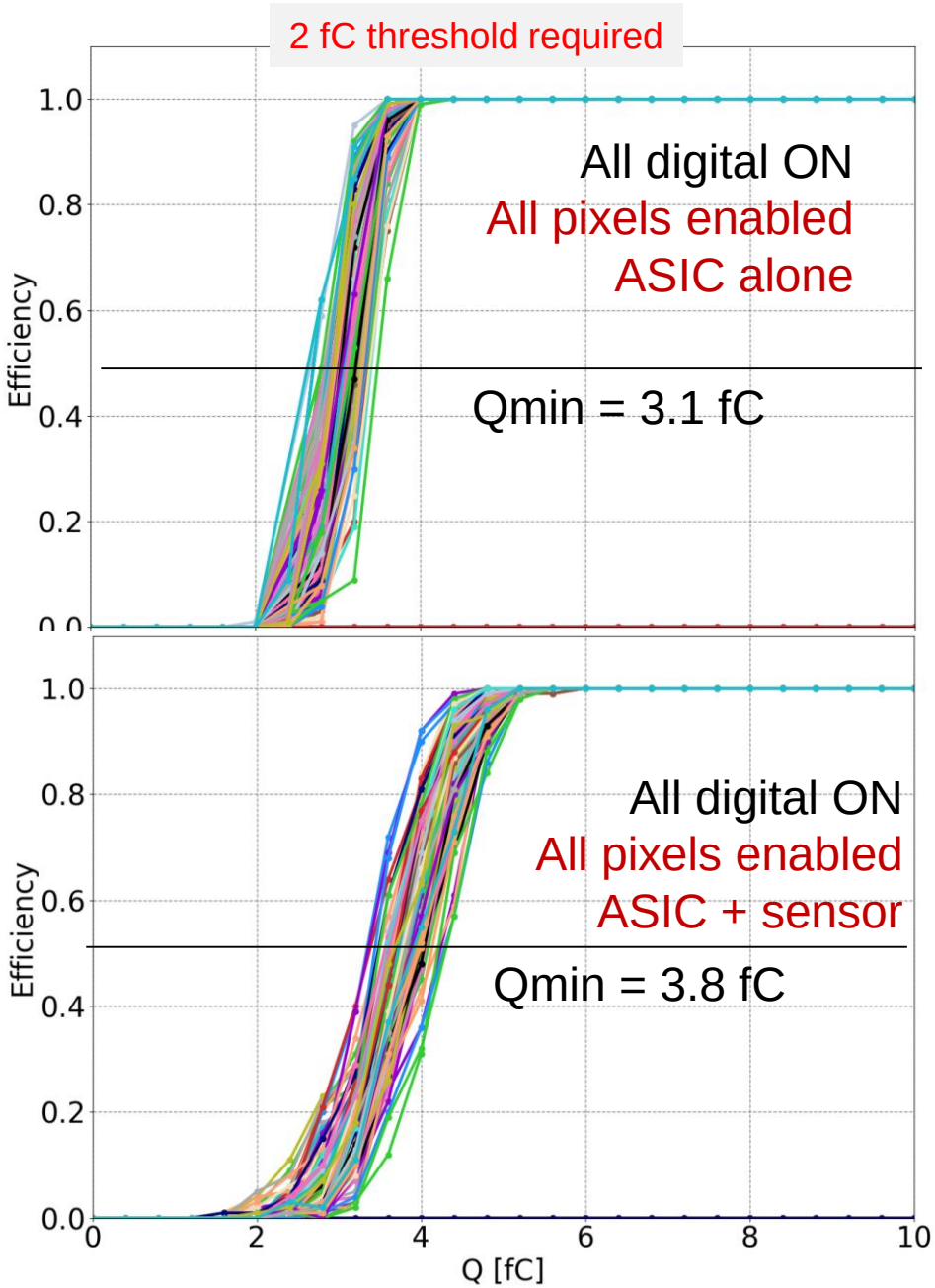
Power dissipation and technology

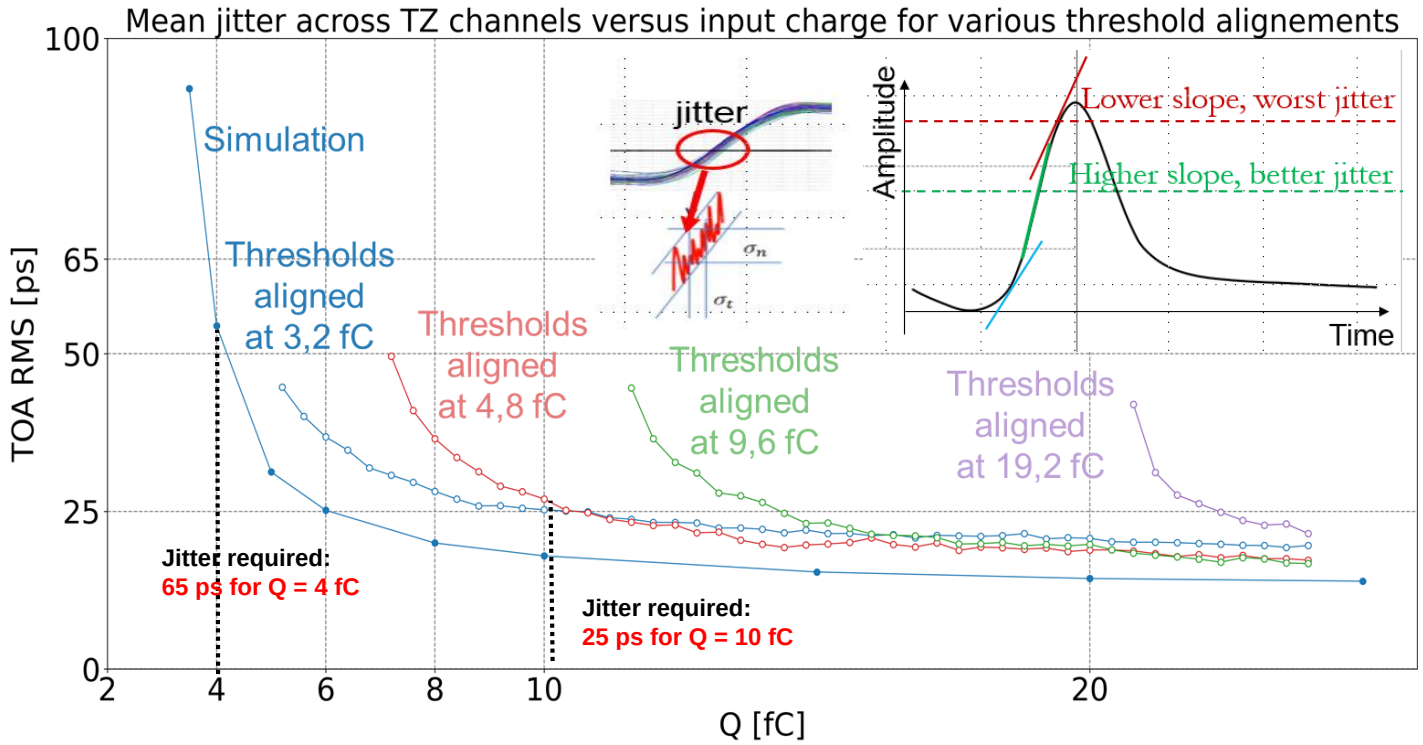
- Altiroc: **300 mW/cm2** + techno CMOS **130 nm**
- Timepix4: 600 mW/cm2 + techno CMOS 65 nm
- ITK: < 1 W/cm2 + techno CMOS 65 nm



Altiroc2 pixel: SRAM Latency of 38.4 µs to cope with 0.8 MHz readout bandwidth

ALTIROC2 Performances





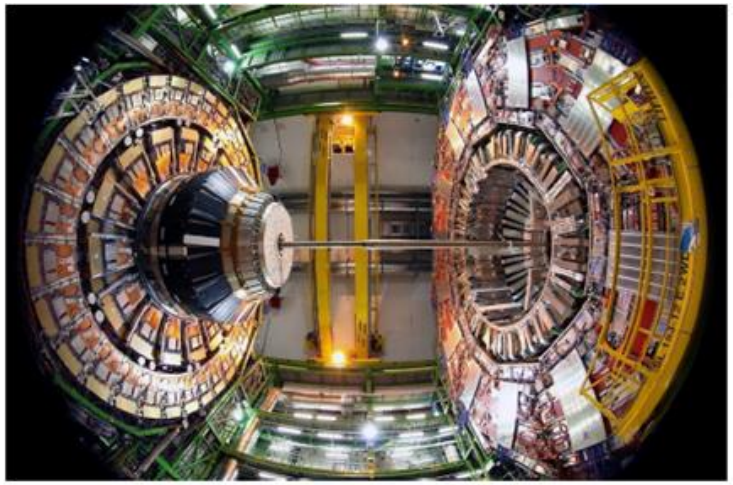
$$\sigma_{analog\ FE} = \frac{Noise}{dV/dt} = \frac{e_n C_d \sqrt{t_d}}{Q_{in}}$$

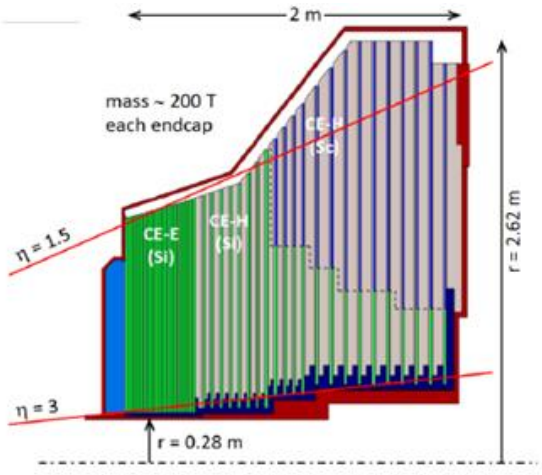
ALTIROC3 is currently under test and the performances are very encouraging !!!!

HGCROC: ASIC for the CMS High Granularity Calorimeter

Full system maintained at -30°C

- ~ 640 m² of silicon sensors, **6.1M** Si **channels**
- ~ 370 m² of scintillators, **240k** SiPM + scint-tile **channels**
- **Active Elements**
  - Electromagnetic calorimeter (CE-E): Si, Cu/CuW/Pb a
  - Hadronic calorimeter (CE-H): Si & scintillator, steel ab



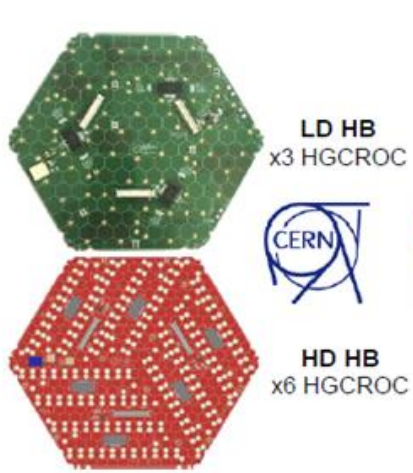


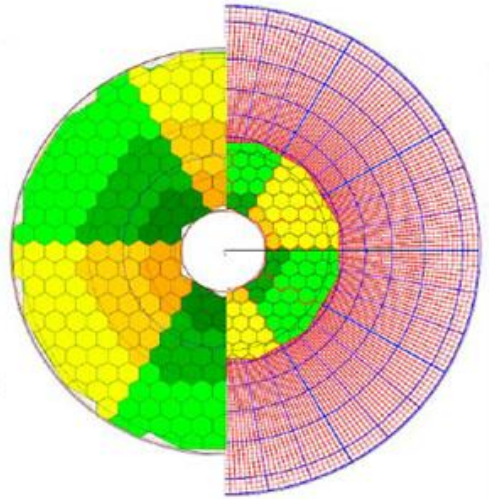
Silicon-only layer (in CE-E) showing "cassettes" and different sensor thicknesses

Mixed layer (in CE-H) with silicon at high η and scintillator+SiPM at low η

- **New Front-end electronics**
  - **Two versions**: Silicon and SiPM
  - **Rad.tolerant** (200 Mrad, 1.10^{16} neq / cm²)
  - Power consumption: **15 mW** per channel
  - Noise: **0.4 fC**
  - Charge: **0.2 fC** to 10 pC (**Cdet= 47 pF**)
  - Pileup mitigation: Fast shaping (peak < 25ns),
  - **Precise timing capability**

(100 ps at 10 MIPs (15–30 fC) and a floor below 25 ps)



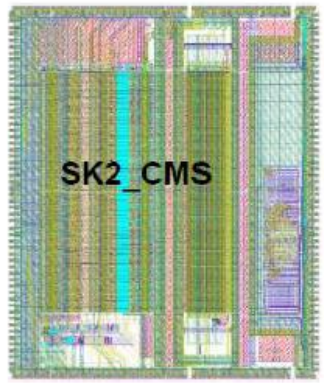


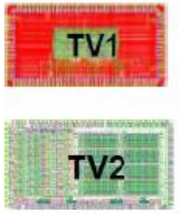
The HGCROC for CMS high granularity calorimeter
D. Thienpont
XII Front-end Electronics workshop. 12–16 juin 2023 Torino

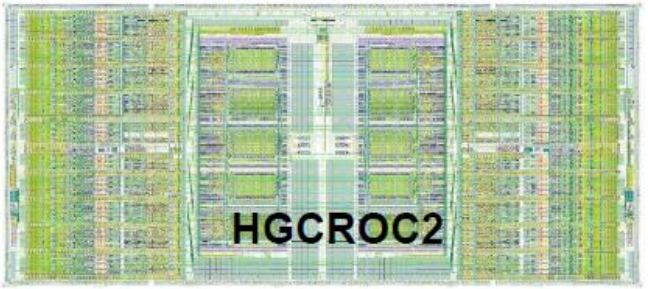
Development history

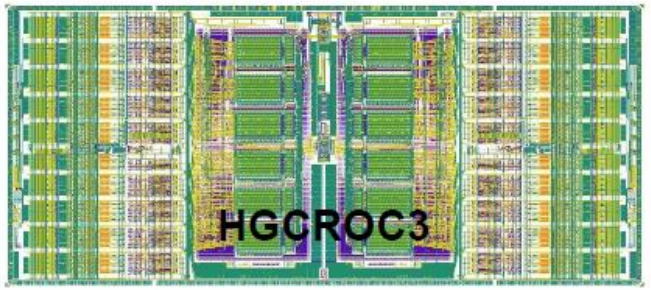
- **Jan 16: SKIROC2_CMS[TWEPP 2016]**
  - SiGe350 nm 7x9 mm²
  - Dedicated to test beam and analog architecture (TOT)
- **May 16: 1sttest vehicle TV1**
  - CMOS 130 nm 2x1 mm²
  - Dedicated to preamplifier studies
- **Dec 16: 2ndtest vehicle TV2[TWEPP 2017]**
  - CMOS 130 nm 4x2 mm²
  - Dedicated to technical proposal analog channel study
- **July 17: HGCROCv1[TWEPP 2018]**
  - CMOS 130 nm 5x7 mm²
  - Wire bonds
  - All analog and mixed blocks; large part of digital blocks
- **Feb 19: HGCROC2 [CHEF 2019, IEEE 2020, TIPP 2021]**
  - CMOS 130 nm 15x6 mm²
  - Bump bonds
  - Silicon and SiPMversions (for both 2 and 2A)
  - Final size, packaging and I/Os
- **Dec 20: HGCROC3[TWEPP 2021, IEEE 2021]**
  - CMOS 130 nm 15x6 mm²
  - Bump bonds
  - Silicon and SiPMversions
- **June 23: HGCROC3b**
  - CMOS 130 nm 15x6 mm²
  - Pre-production

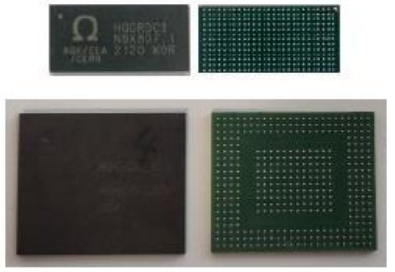
ASIC design coordinator:
Christophe de La Taille
Damien Thienpont











High Density (HD) and Low Density (LD) packages

HGCROC3 and H2GCROC architecture

A 72 channels ASIC for charge and time measurements

Measurements

•**Charge**
- – **ADC** (AGH): **peak measurement**, **10 bits @ 40 MHz**, dynamic range defined by preamplifier gain
- – TDC (IRFU): **TOT** (Time over Threshold), **12 bits** (LSB = **50ps**)
- – ADC: 0.2 fC resolution. TOT: 2.5 fC resolution

•**Time**
- – TDC (IRFU): **TOA** (Time of Arrival), **10 bits** (LSB = **25ps**)

Two data flows

• **DAQ path**
- – 512 depth **DRAM** (CERN), circular buffer
- – Store the ADC, TOT and TOA data
- – 2 DAQ 1.28 Gbps links

•**Trigger path**
- – Sum of 4 (9) channels, linearization, compression over 7 bits
- – 4 Trigger 1.28 Gbps links

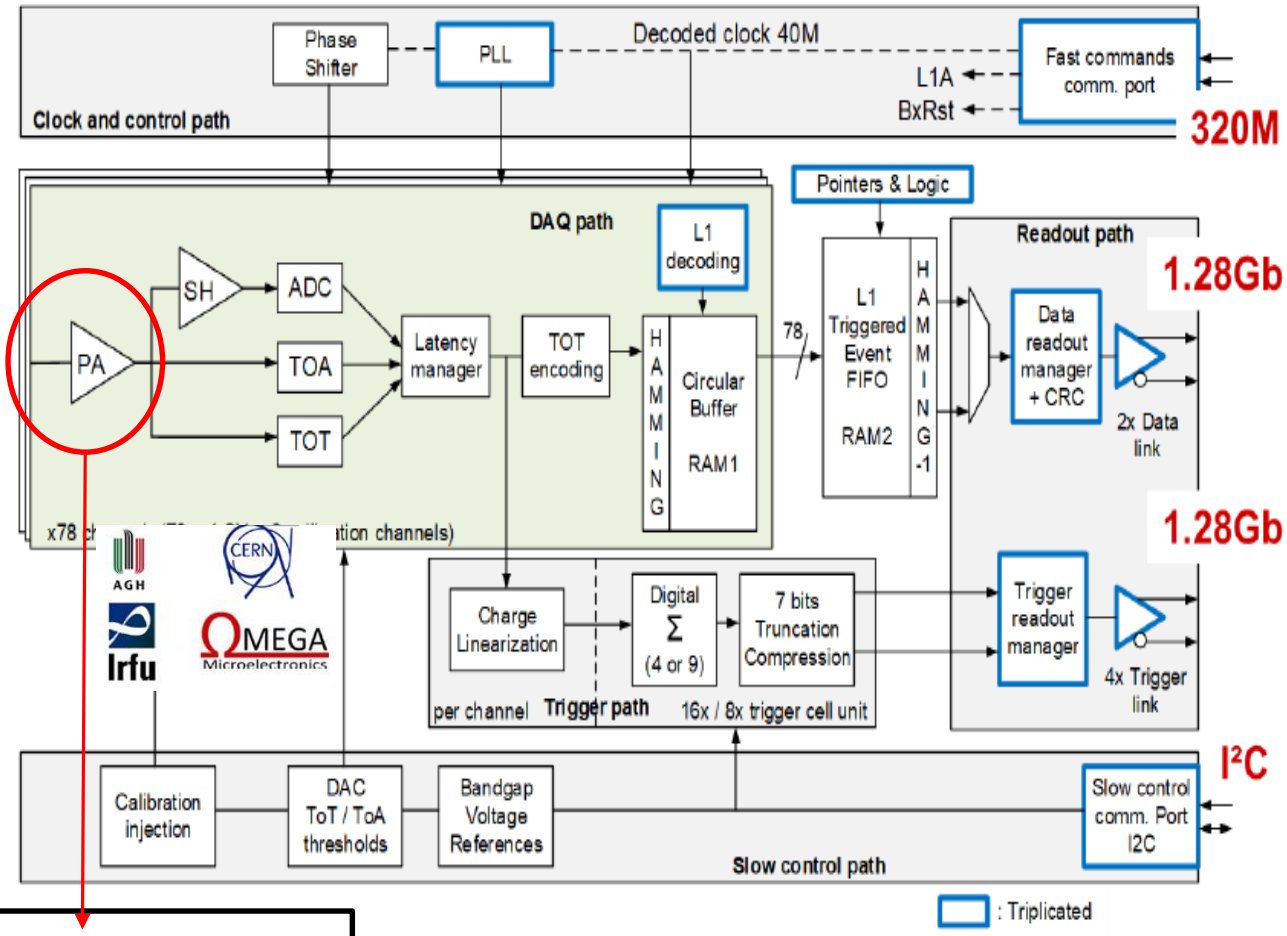
Control

• Fast commands
- – 320 MHz clock and 320 MHz commands
- – A 40 MHz extracted, 5 implemented fast commands

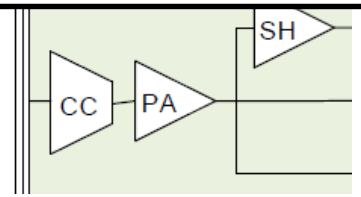
• I2C protocol for slow control

Ancillary blocks

• Bandgap (CERN)
• 10-bits DAC for reference setting
• 11-bits Calibration DAC for characterization and calibration
• PLL (IRFU)
• Adjustable phase for mixed domain



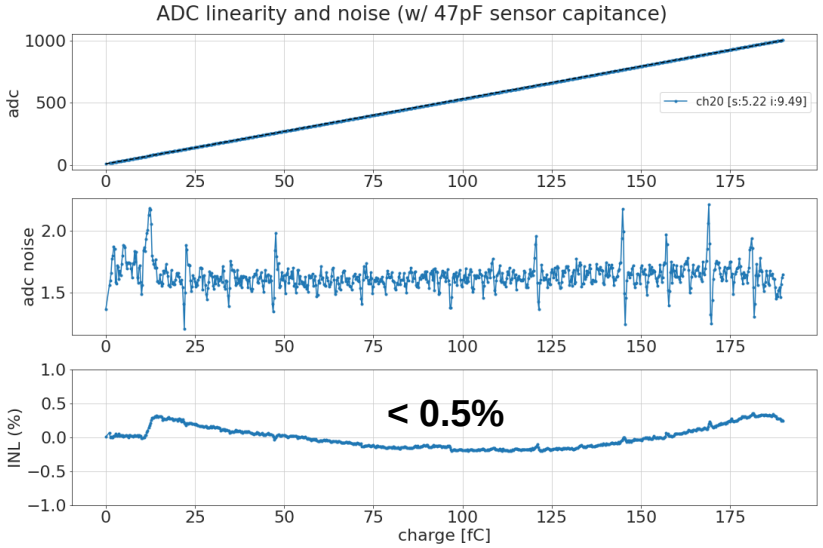
H2GCROC: SiPM version

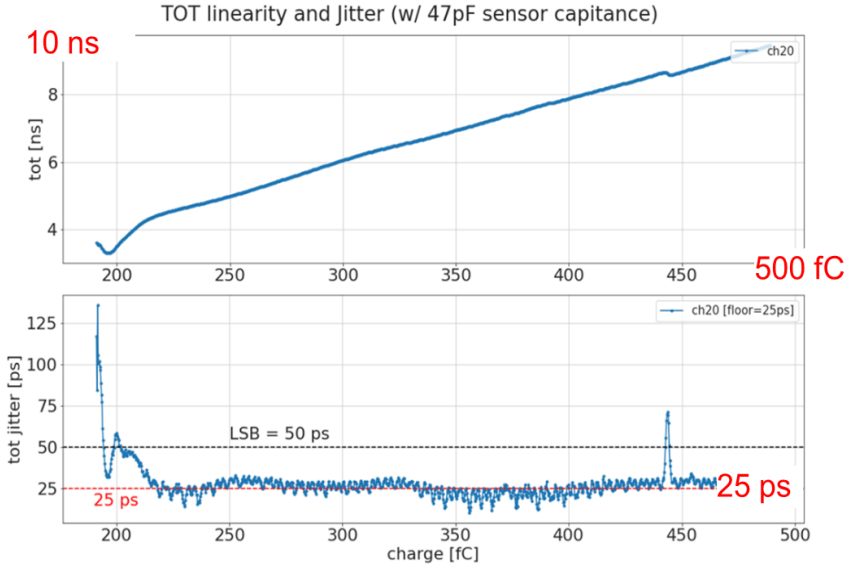


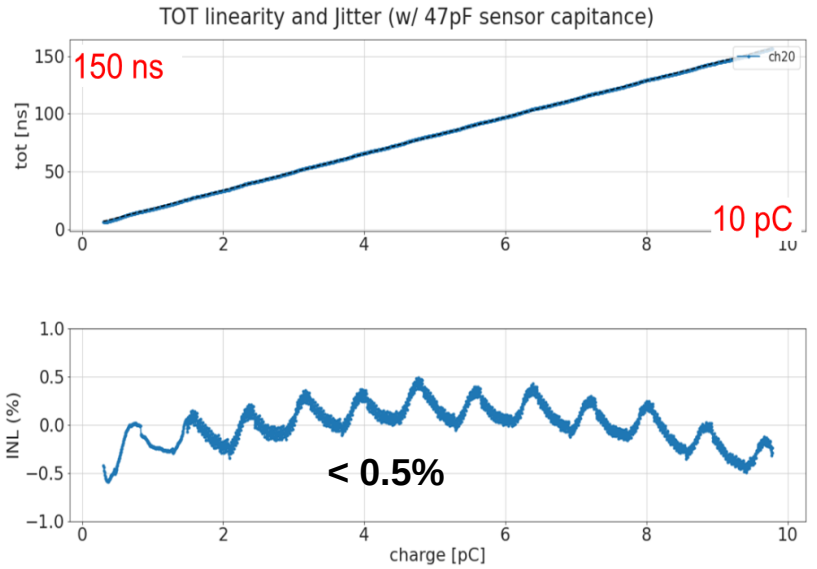
Current Conveyor based on KLAUS chip from Heidelberg UNI
Attenuates the current at the input with 4 bits.
Gain: 0,025 to 0,375 (step 0,025)

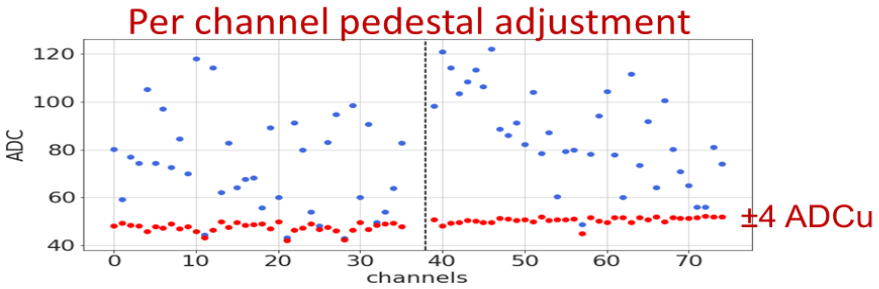
HGCROC Performances

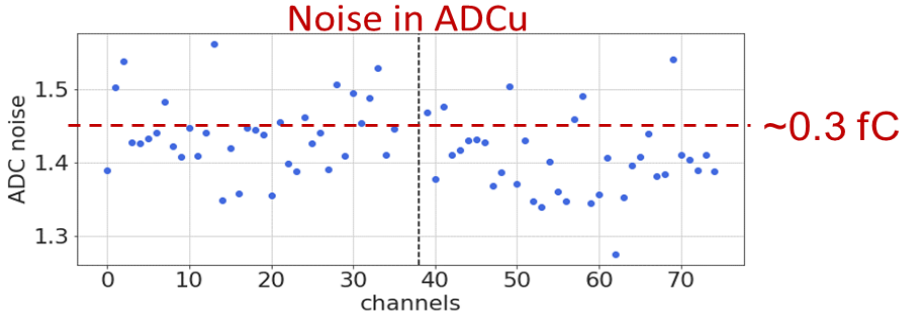
HGCROC for HGCAL has been extensively measured and reaches good performance

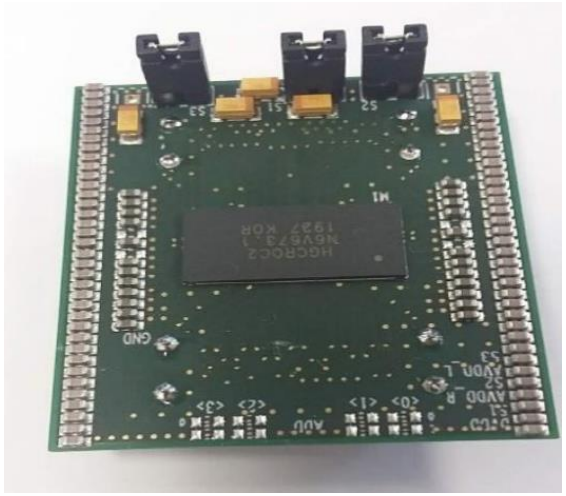


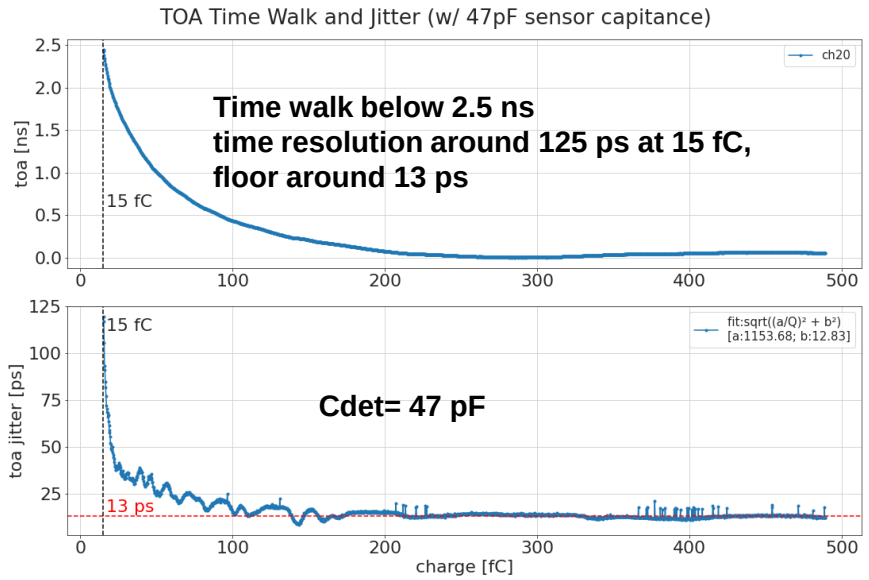












HKROC to readout photomultiplier tubes for large neutrino experiments

Hyperk R&D started in September 2020 (OMEGA_LLR-CEA):

Design of a front-end board for the charge and the time measurements (“Digitizer”) for the Hyper-Kamiokande experiment:

- Omega developed the ASIC **HKROC in TSMC 130 nm** node
- 3 solutions in competition (QTC-Japan, Discrete-Italy, HKROC-France)

Omega expertise in ASIC for Cerenkov detectors

CATIROC ASIC in JUNO experiment in China

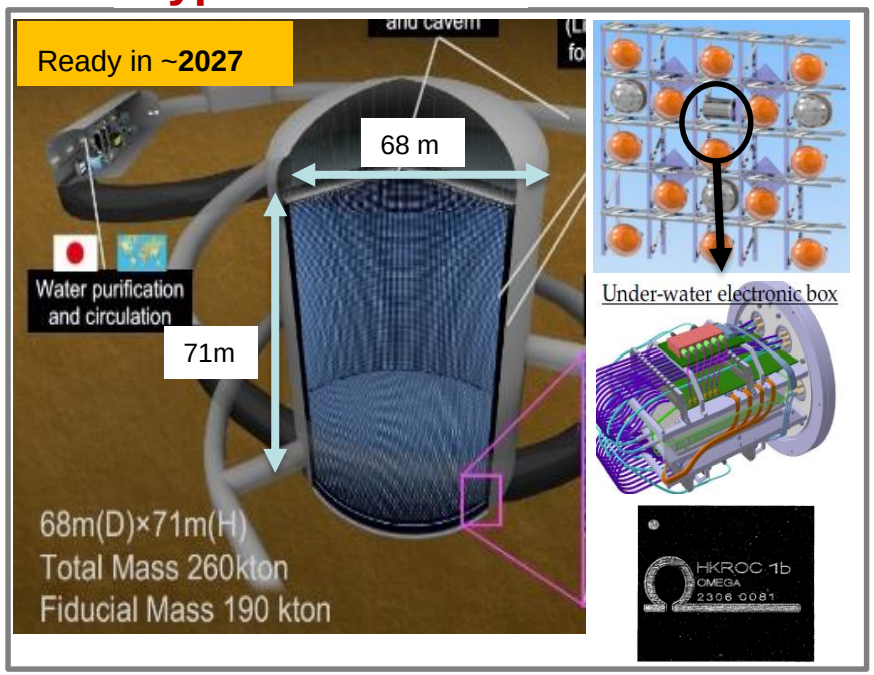
Based on HGCROC, was developed in 3 months. HKROC is versatile, low-power and fully integrated solution for large neutrino experiments

ASIC requirements:

- Autotriggering detection **1/6 of p.e**. (0.33 pC)
- Charge measurement up to **1250 p.e.** (2500 pC)

  with a linearity **< 1%** and a resolution of 0.2 pC up to 20 pC
- Time measurement at **300 ps** at **1 p.e.** (2 pC)
- Hit rate up to **1 MHz**

Hyperkamiokande **20,000 20” PMTs**

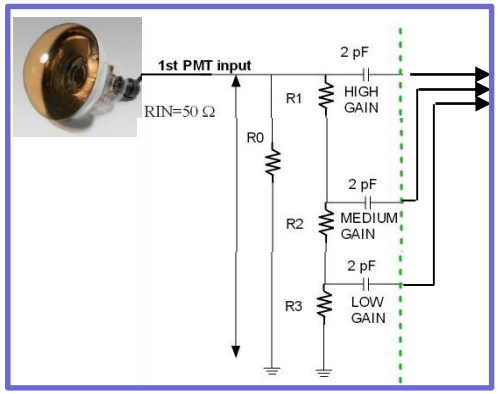


HKROC overview

HKROC 36 channels asic submitted in **August 2021** in **TSMC 130 nm** technology

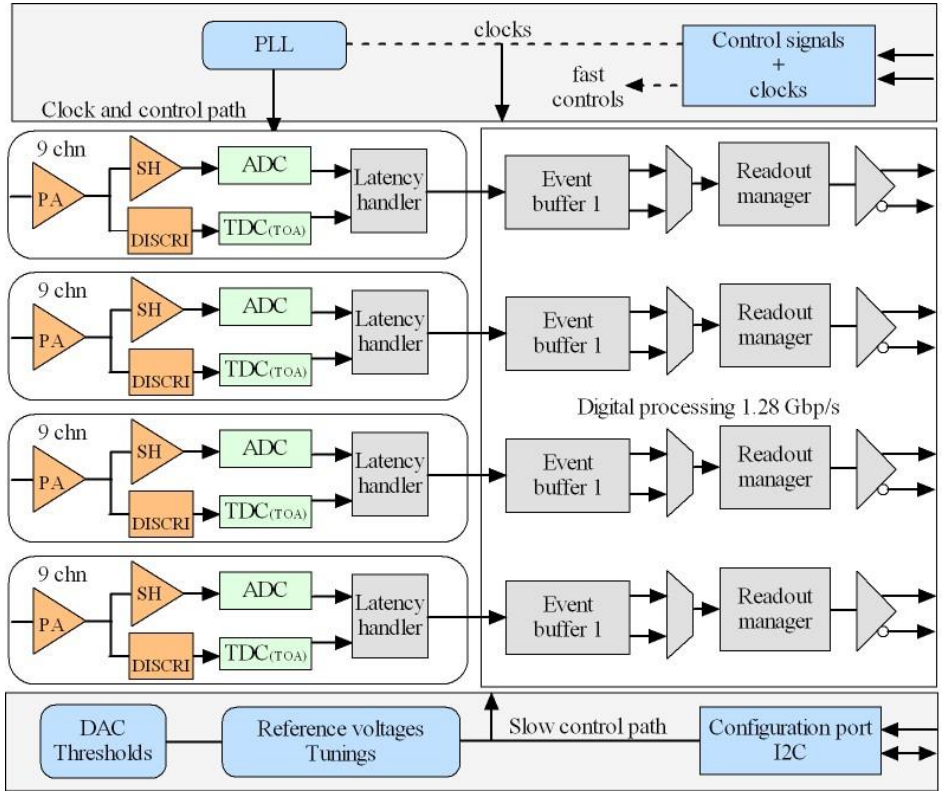
ASIC design coordinator:
Dulucq Frederic
Selma Conforti

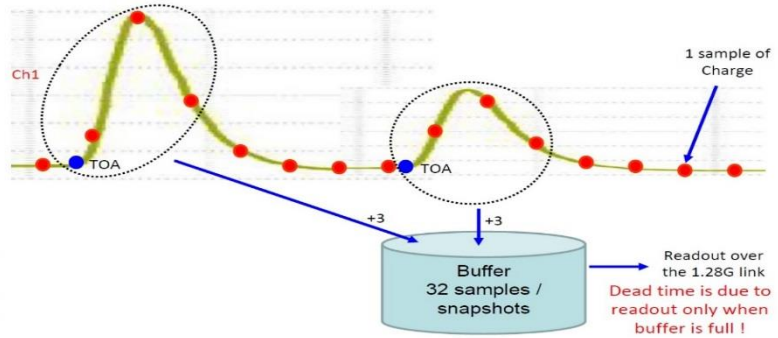
- **36 independent channels** working in **triggerless mode**. Input signal amplified and auto-triggered.
- A **digital part** to manage all the system, the conversion and the read-out
- **A waveform digitizer**: it is able to reconstruct the full shape of the charge provides a high precision Time of Arrival (ToA)
- **Transmits the data** by 4 high speed differential links at **1.28 Gbps**



10-bit TDC
(designed by
the CEA IRFU group in Saclay)

10-bit SAR ADC
(designed by AGH in Krakow)



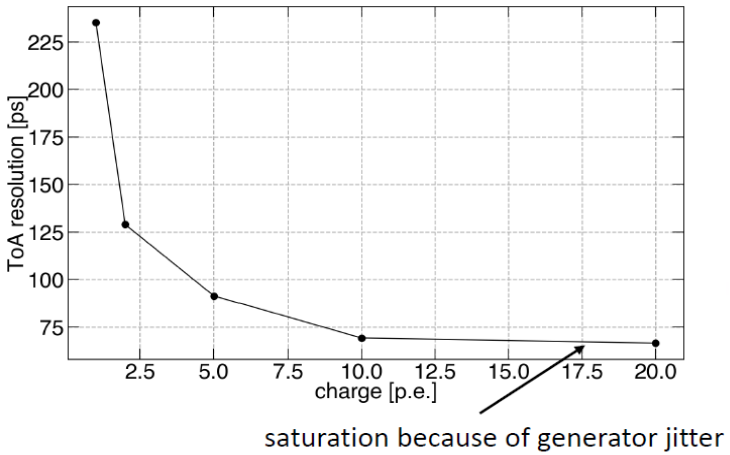


HKROC performances

Extensively measured (by LLR-OMEGA-CEA) and **reaches good performances!**

200 ps rms @ 1 p.e [300 ps required]

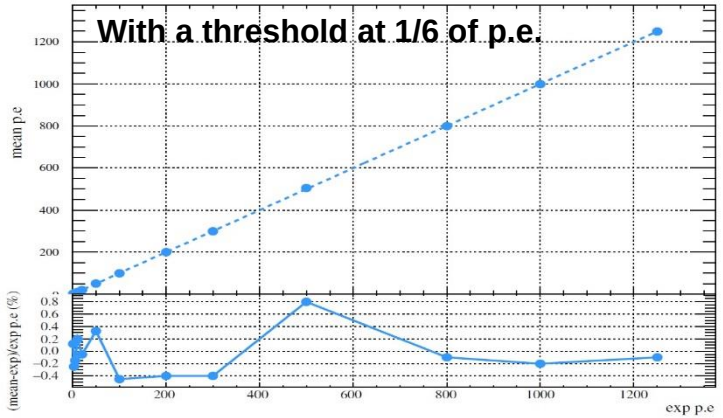
With a threshold at **1/6 of p.e.**



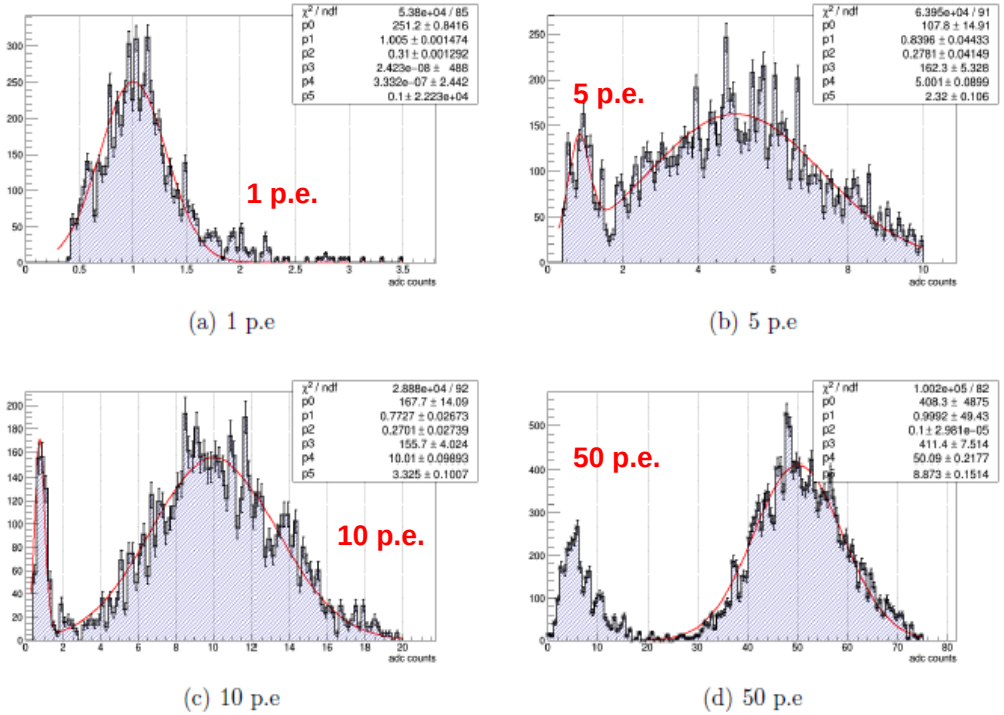
Charge linearity < ±1%

from 1 to 1250 p.e. (2500 pC)

With a threshold at 1/6 of p.e.



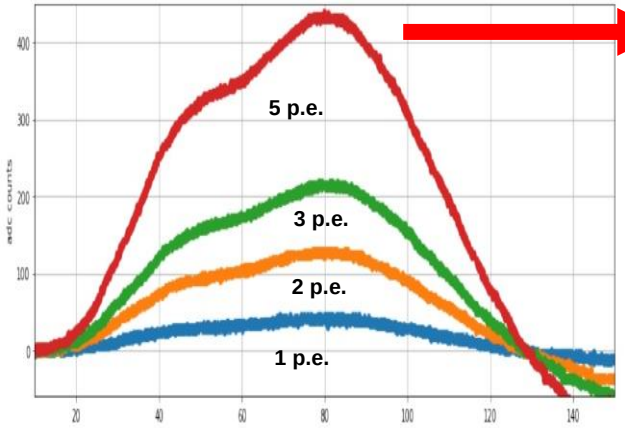
Charge measurements with a **20" Hamamatsu R12860**



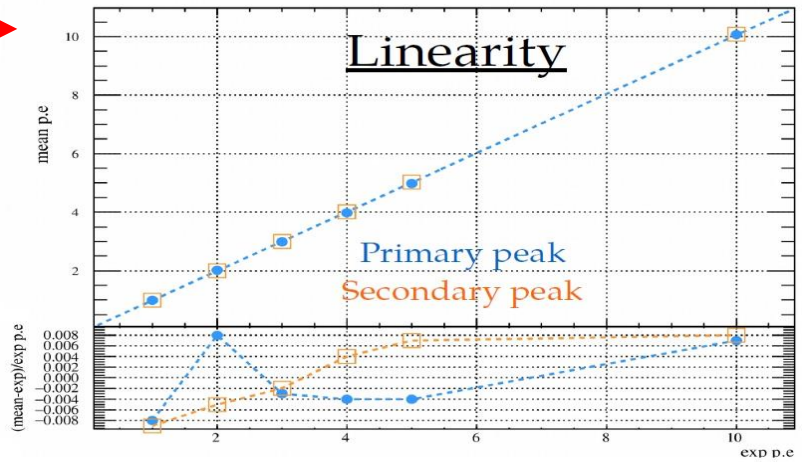
(a) 1 p.e (b) 5 p.e

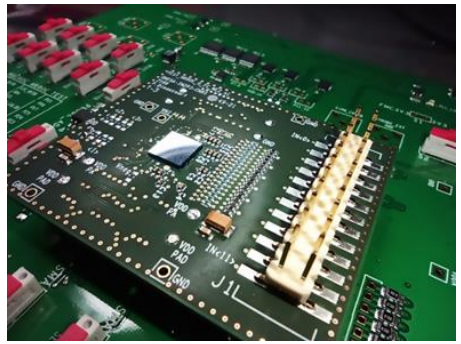
(c) 10 p.e (d) 50 p.e

ASIC is tested with 2 signals separated by Δt = 30 ns



Good linearity, even for pile-up event
Appling charge reconstruction of the two peaks





Summary

- **15 ASICs** for **timing detectors**, **calorimeters** and **spatial projects** under OMEGA responsibility produced and **installed on detectors** in **15 years**
  - **Lot of versatility** integrated in ASICs **to adapt their use for various detectors**
  - **New ASIC design usually derived from a previous one, design "re-use"**

- **ALTIROC**, **HGCROC** and **HKROC are complex and state of the art ASICs**
  - **ALTIROC** : Analog **30%** (derived from Petiroc) and Digital **70 %** (Digital on Top)
    - **First 225 channels full matrix LGAD readout chip with 1 GHz preamplifier with 4 pF detector capacitance**
    - ASIC with a mix of requirements specific to calorimetry and to pixel ASICs for trackers = new territory in HEP
    - Electronics jitter **~25 ps** for **MIP=10 fC,** 4 mW/ch
  - **HGCROC**: derived from **SKIROC chip (CALICE), State of the art performance**,
    - **Noise < 0.4 fC**, ADC and TDC **linearity < 1 %,** Time walk < 2.5 ns, 15 mW /ch
    - **Time resolution ~125 ps** for **15 fC** (Cdet= **47 pF**), floor **13 ps**, **min TOA thereshold 25 fC**
  - **HKROC**: **derived from HGCROC chip**, designed in **only 3 months**, extensive characterization in 6 months
    - **Triggerless, waveform digitizer**
    - Time resolution **150 ps** for **1 pe,** Charge measurement up **to 2500 fC**

- **Complexity of the latest ROC chips => Design and tests at system level performed in strong collaboration with other labs**
- A lot of digital to process data internally ant output them at 1.28 Gbps but Front End and floor plan are crucial ensure the performance with the detector

BACKUP

HGTD time precision

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

$$\sigma_{elec}^2 = \sigma_{time\ walk}^2 + \sigma_{analog\ front-end}^2 + \sigma_{TDC}^2$$

$$\sigma_{analog\ FE} = \frac{Noise}{dV/dt} = \frac{e_n C_d \sqrt{t_d}}{Q_{in}}$$

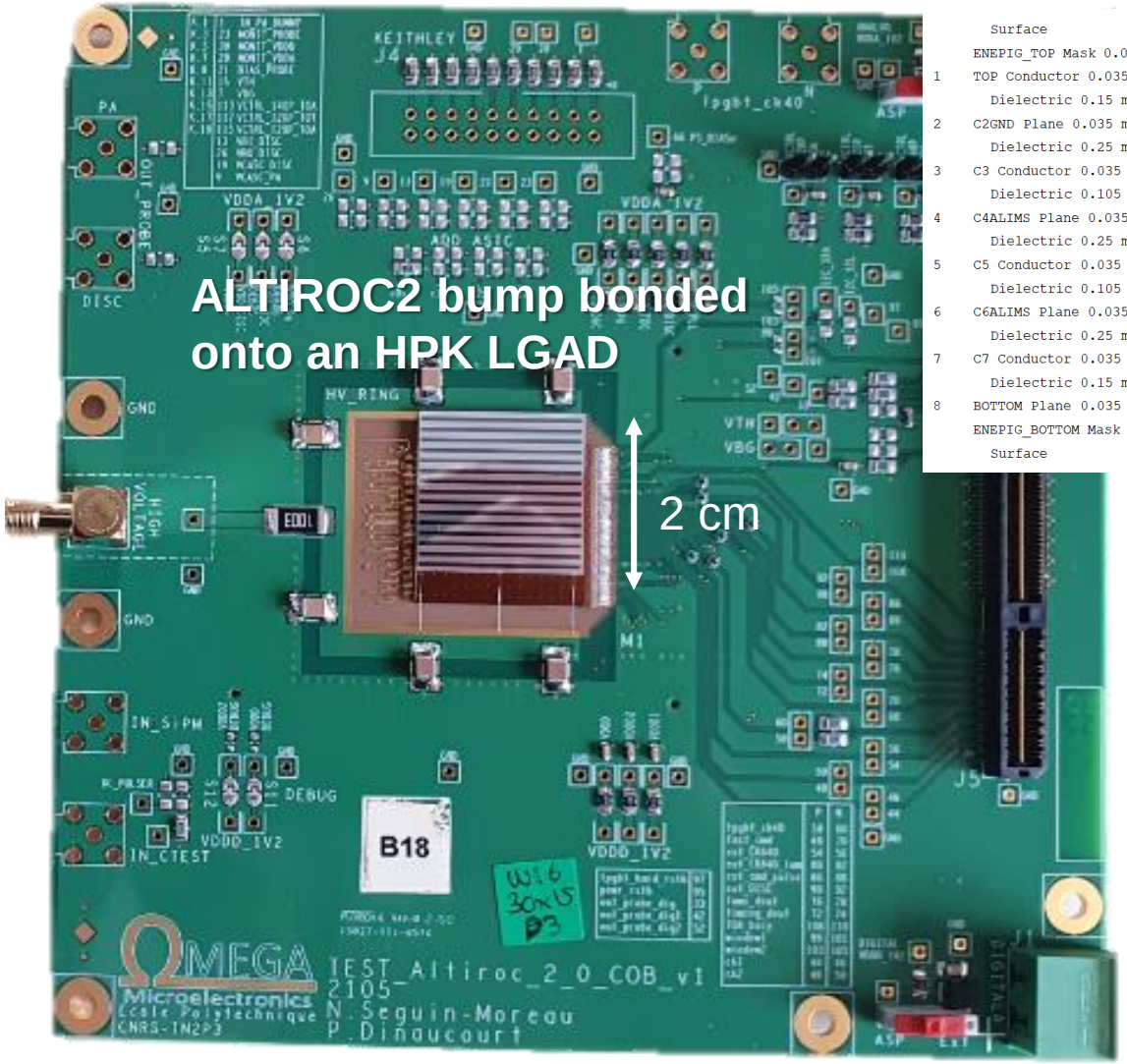
Criteria		Max.	Conditions
Total hit jitter	initial :	35 ps	at 10 fC
	final :	70 ps	at 4 fC
↳ Landau jitter		25 ps	for un-irradiated LGAD
↳ Clock jitter		15 ps	
↳ Electronic jitter		20 ps	
↳ Time walk jitter		10 ps	
↳ Front-end jitter		10 ps	
↳ TDC jitter		10 ps	

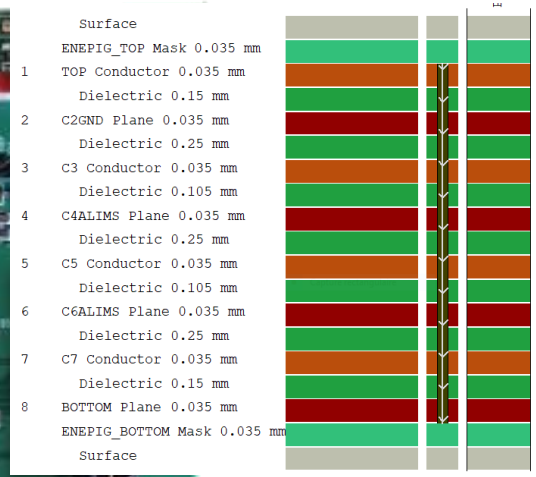
C_d: Sensor capacitance (around 4 pF expected)
t_d: LGAD drift time (600 ps)
Q_{in}: MIP collected charge (10 fC at the start of the detector lifetime, 4 fC at the end and after 200 MRad)
e_n: Noise spectral density of the input transistor

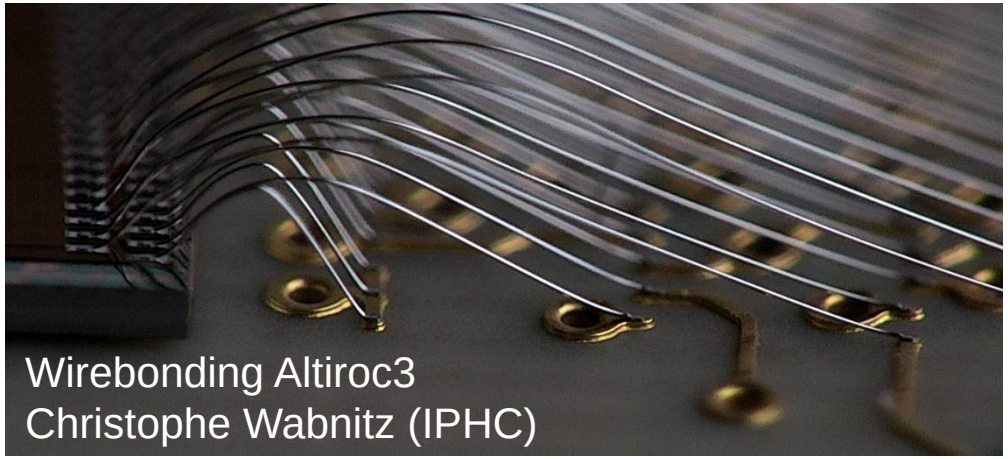
Testbench for ALTIROC2

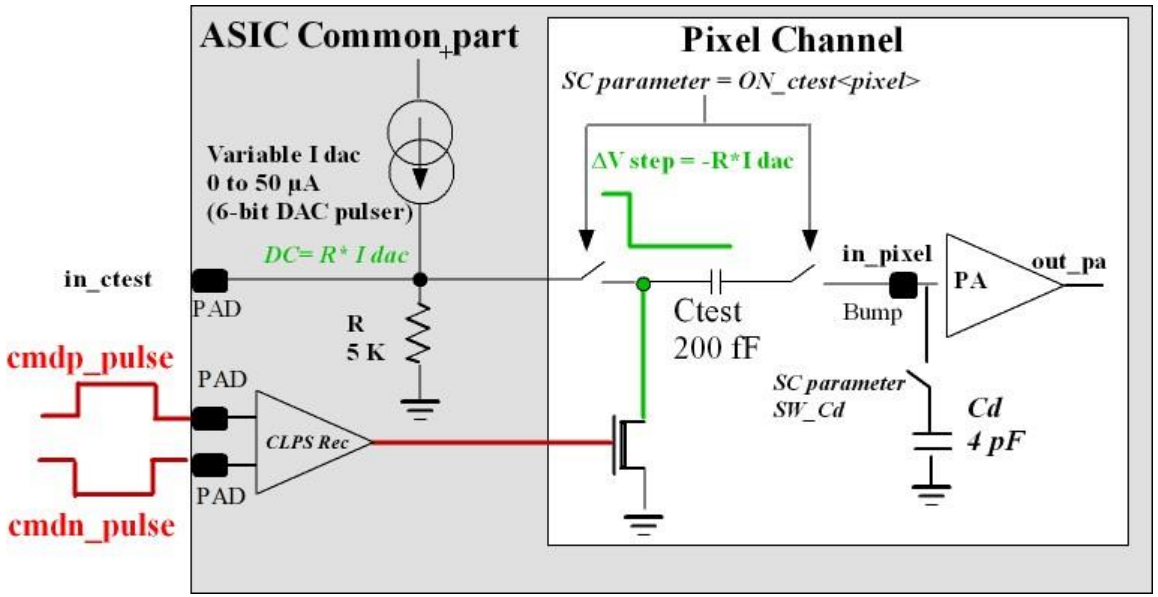
- Setup = ASIC board (ASIC alone or bump bonded onto sensor) + interface board + FPGA board

- **Front-end calibration :** charge injection (0 up to 50 fC) using **ASIC internal calibration pulser**, controlled by the FPGA, synchronous to 40 MHz clock, ASIC alone: Cd=3,5 pF can be set by SC to mimic sensor capacitor



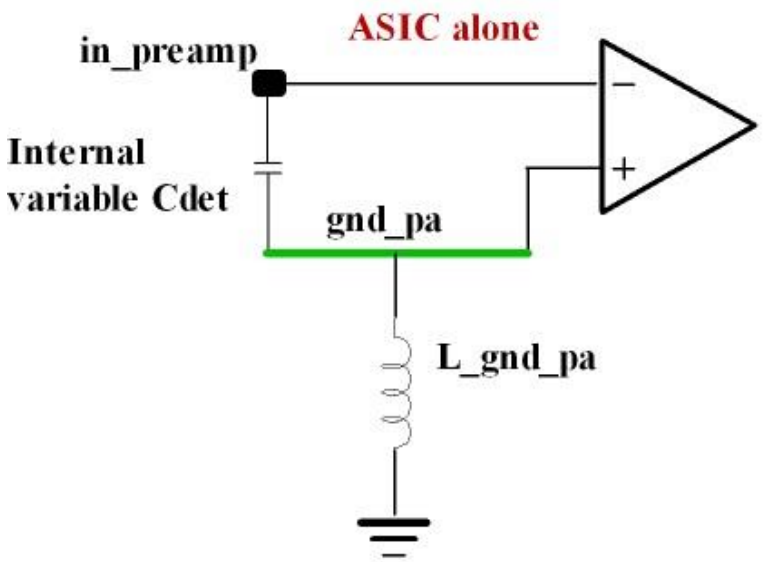


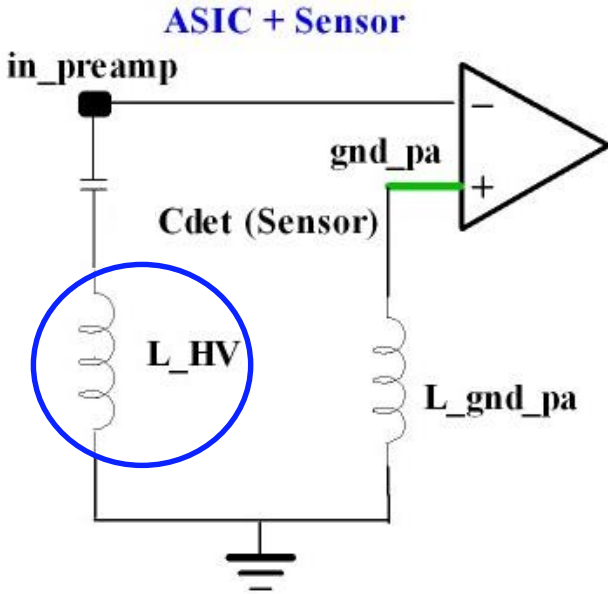


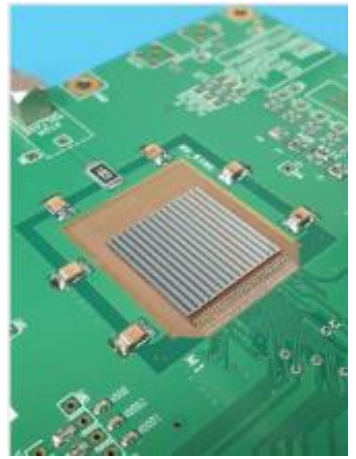


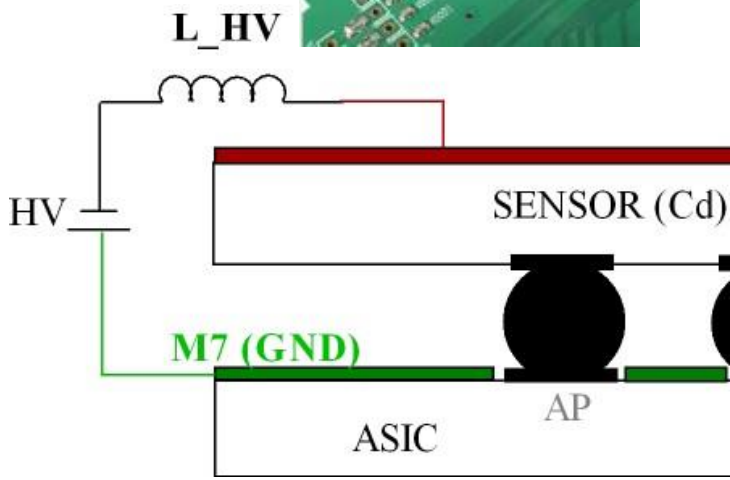
Sensor effect on noise

One channel









Noise on analog gnd amplified x1
"common mode"

ASIC alone = favourable situation

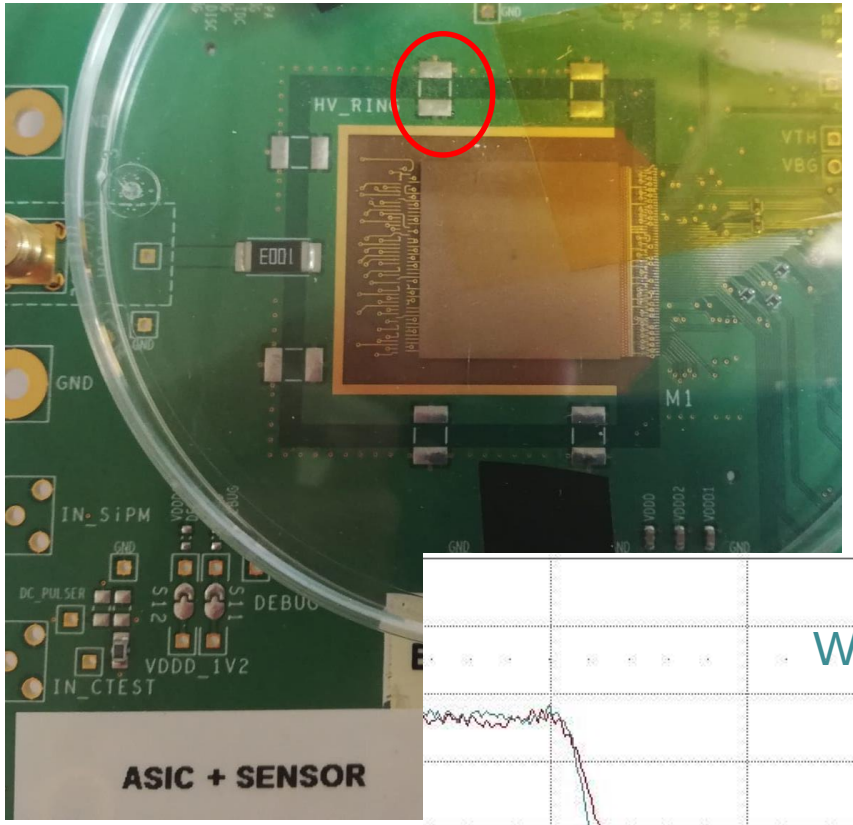
Can this parasitic inductance be hidden from the preamplifier ?

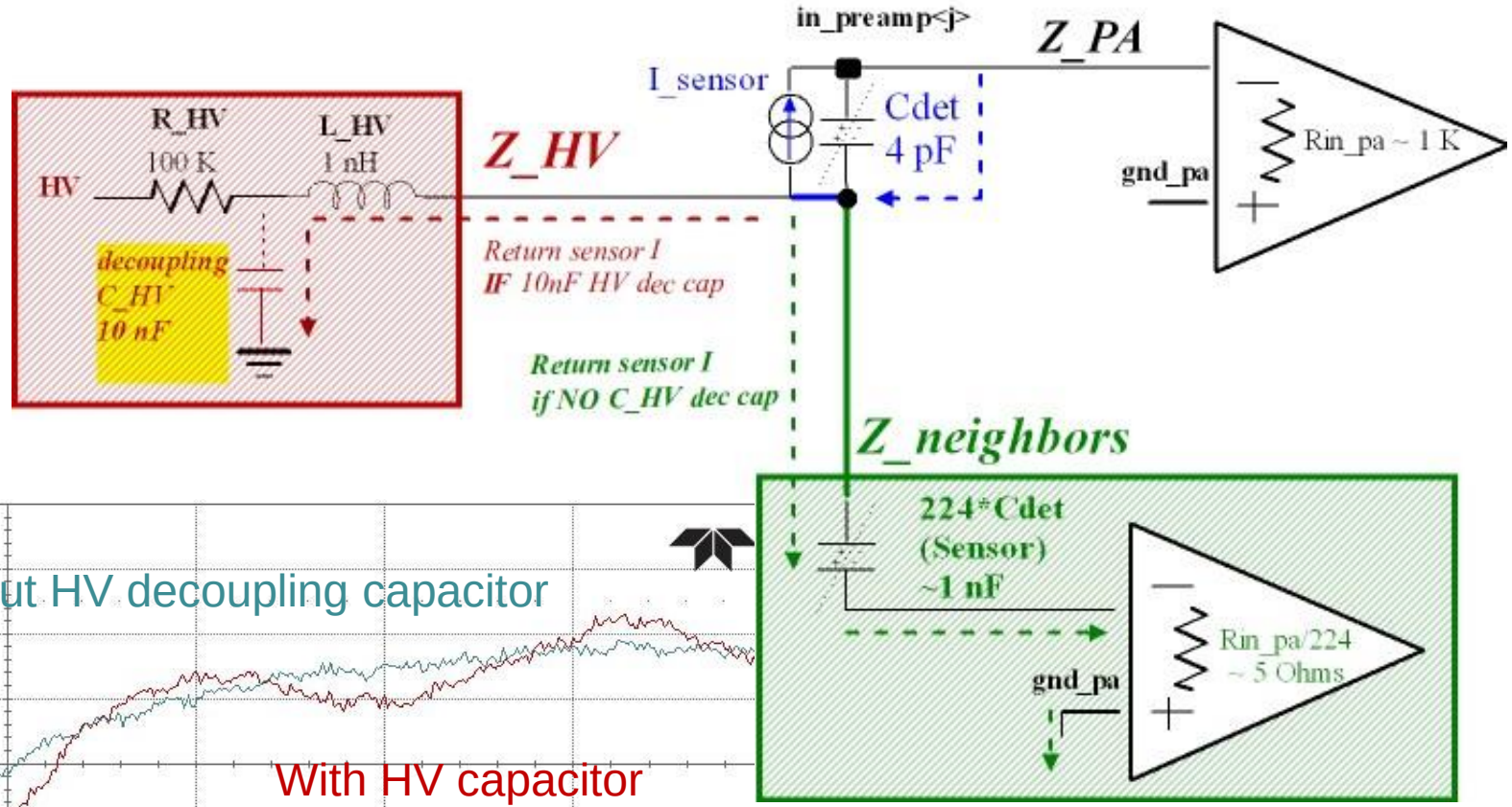
Noise on gnd_pa amplified x20
"differential mode"

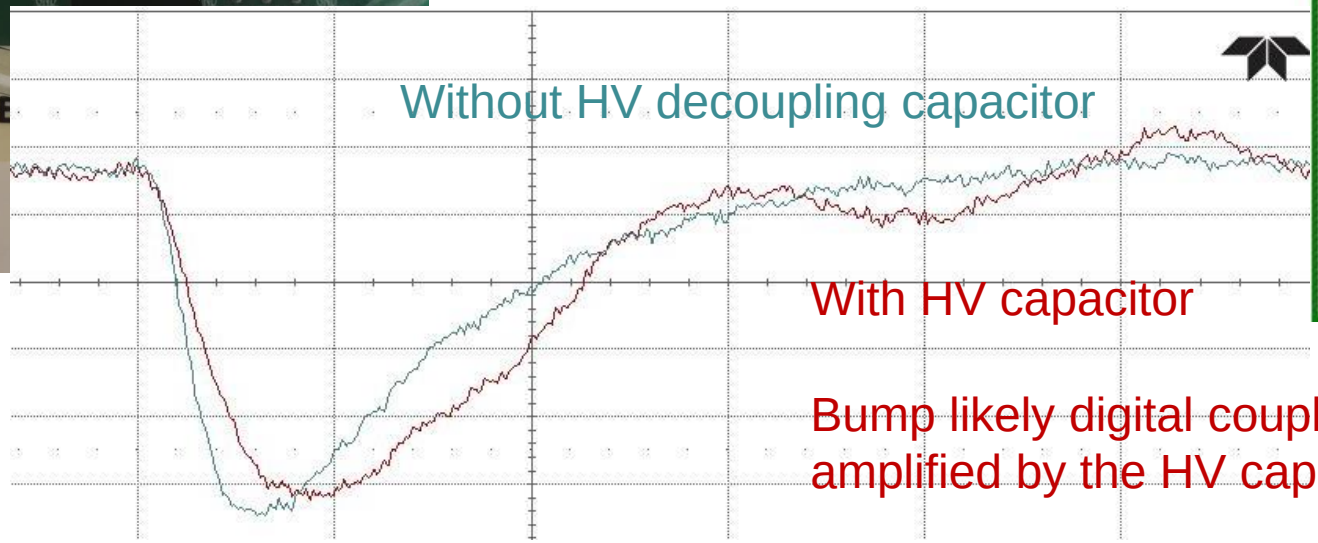
Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero : when the sensor is connected !

Effect of HV decoupling : where is the AC current flowing back to ground ?

10 nF HV decoupling capacitor adds 50% more noise on a TZ output.







Bump likely digital coupling inside the asic amplified by the HV capacitor

Optimal HV impedance is very different for 5x5 and 15x15 sensor

- **HV resistance :**
  - varied from 0 to 1kOhm
  - Effect on gnd_pa noise amplification
    - Goes from 20 to 1
    - ~1 for R>100 Ohm
  - Current return ensured by the 224 spectator channels
    - Was not the case with smaller sensor

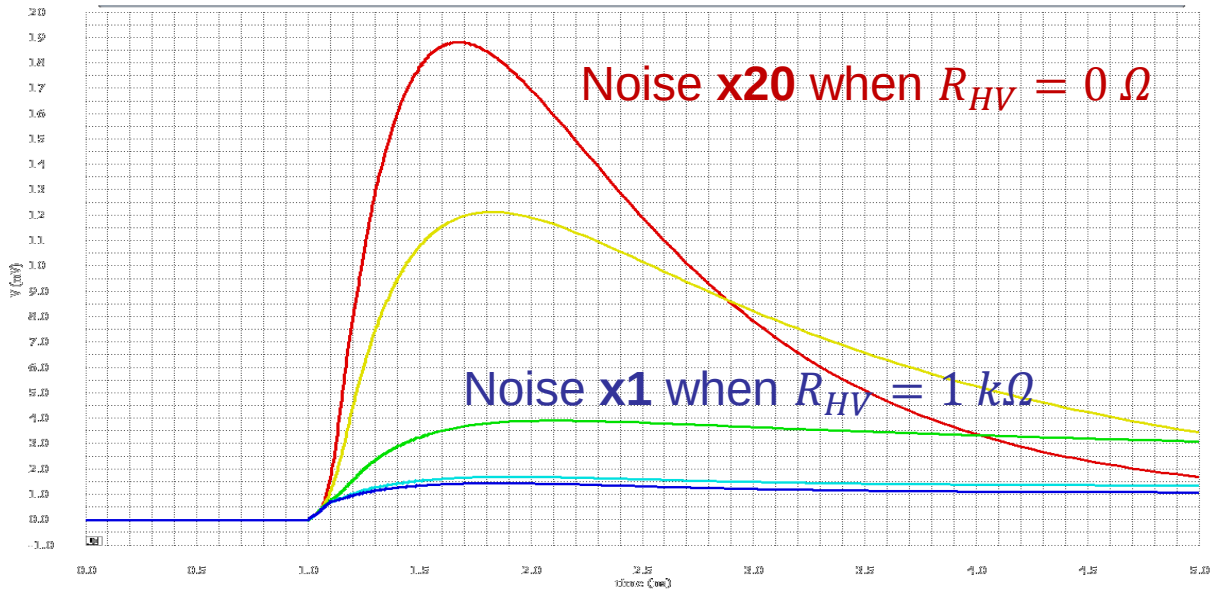
- **HV parasitic inductance :**
  - Effect of 10 nH in HV

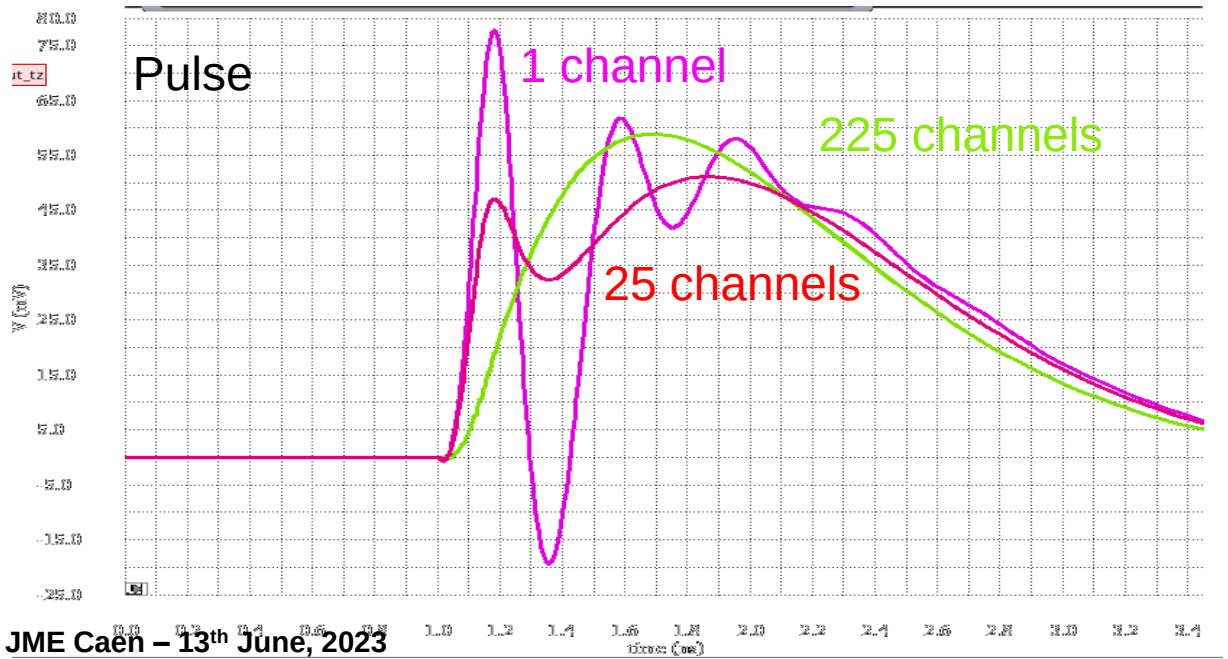
  1 channel, 25 channels, 225 channels

  = Altiroc0/Altiroc1/Altiroc2

Altiroc2 doesn't suffer from HV parasitic inductance !

Noise amplified by PA as signal





ALTIROC STATUS

ALTIROC2 : first 225 channels full matrix LGAD readout chip with 1 GHz preamplifier with 4 pF detector capacitance : new territory in HEP !

- **Design done by engineers spread in 6 labs**
  - **Analog 30 %** of the chip
    - Analog performance and **Floorplan crucial** to guarantee analog performance at system level
    - 2.5 FTE: **Omega** (1.8 FTE) , Clermont (0.7 FTE) , SLAC (< 0.1 FTE for TDC) , SMU (< 0.1 FTE for Phase shifter)
  - **Digital 70 %** of the chip
    - **Clock Domain Crossing, timings, SEE robustness**
    - 5 FTE: Clermont (2.2 FTE) , Chips (2 FTE) , IFAE (0.8 FTE)
  - Assembly done **Full Digital on Top** + UVM verification

ALTIROC Performances

- **Analog performance demonstrated with ALTIROC2 are encouraging !**
  - Jitter (ASIC+sensor) ~ 25 ps at 10 fC with calibration pulse (→ required ~ 20 ps)
  - Vth (ASIC+sensor) can be set at ~3 fC (→ required 4 fC)
  - First assembled module has given similar performances than full ASIC testboard
  - Digital coupling observed

ALTIROC2: Performance of an LGAD readout ASIC for ATLAS HGTD picosecond MIP timing detector
Maxime Morenas
JINST 18 (2023) C01070
In: Topical Workshop on Electronics for Particle Physics 2022 (TWEPP 2022), Bergen, Norway, 19 - 23 Sep 2022, pp.C01070 DOI 10.1088/1748-0221/18/01/C01070

- **ALTIROC3 is currently under test with improvements**
  - ALTIROC ASIC: 225-channel ASIC: Foundry TSMC 130 nm, submission through CERN/IMEC. Delivery of 12-inch wafers, FAB 12 for rad hardness (120 ASICs/wafer).
  - 1086 working ASICs required for hybridization and module assembly for pre-production and 21708 working ASICs are required for production. The expected ASIC yield is 80 %

	Working ASICs	Needed ASICs
Pre production HGTD-ALTIROC-A (5%)	1086	1358
Production HGTD-ALTIROC-B	21708	27135

HGCROC for HGCAL has been extensively measured and reaches good performance

- < 1% linearity for charge measurement over the full dynamic
- Noise level as expected < 0.4 fC with Cd= 65 pF
- Timing (Time walk and jitter) as expected: TW < 1.4 ns, jitter~ 1.8 ns/Q(fC) and 13 ps floor

HGCROC3 irradiation tolerant

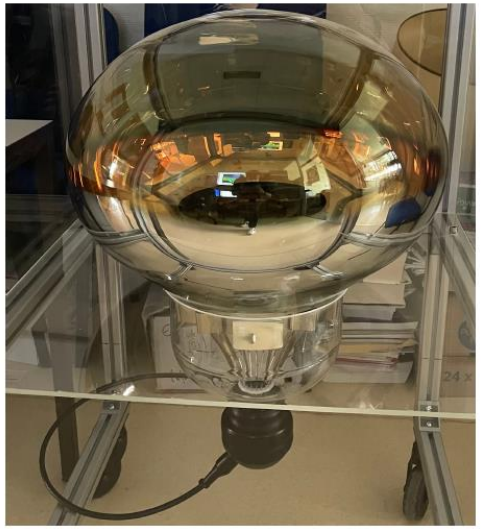
– Still working properly up to ~ 400 Mrad

	CE-E Silicon	CE-H Silicon	CE-H Scintillator	Total
HGCROC	60 324	31 596	8 496	100 416
Motherboards	5 004	2 556	384	7 944
Bidirectional data/control links	5 004	2 556	384	7 944
Trigger links	4 020	2 556	768	7 344

- 2 robots: LLR and OMEGA
- Pick and placing features work
- DAQ and analysis software work
- ~ 450 HD-ROCv3 have been tested
- ~ 300 LDROCv3 have been tested

Preliminary tests list:
- Power consumption
- Write/read fuse number
- Write/read the 8 bits of the 800 SC registers
- Measure the 2*64 probe_dc values
- Measure the 10bits DACs and 12 bits calibration
- Measure the 6 bits channel wise tuning dacs : 78 x 6 bits x 3 dacs
  - Adjust the pedestals, TOA/TOT thresholds channel wise
- Check the fast commands and links
- Check rms to detect bad or unconnected channels
- Make a phase scan to check shifter OK
- Run the DRAM tests
- Check ADC linearity with test pulse injection : 10 points* 72 channels * 100 meas.
- Set threshold to ~10 fC measure TOA and TOT vs Qinj (DAQ and TRIG paths)
- **Specific tests for the SiPM version**
  - 2V5 power consumption
  - Input DC level adjustment (Input DAC)
  - Conveyor gain (DACb adjustment)

HKROC + PMT



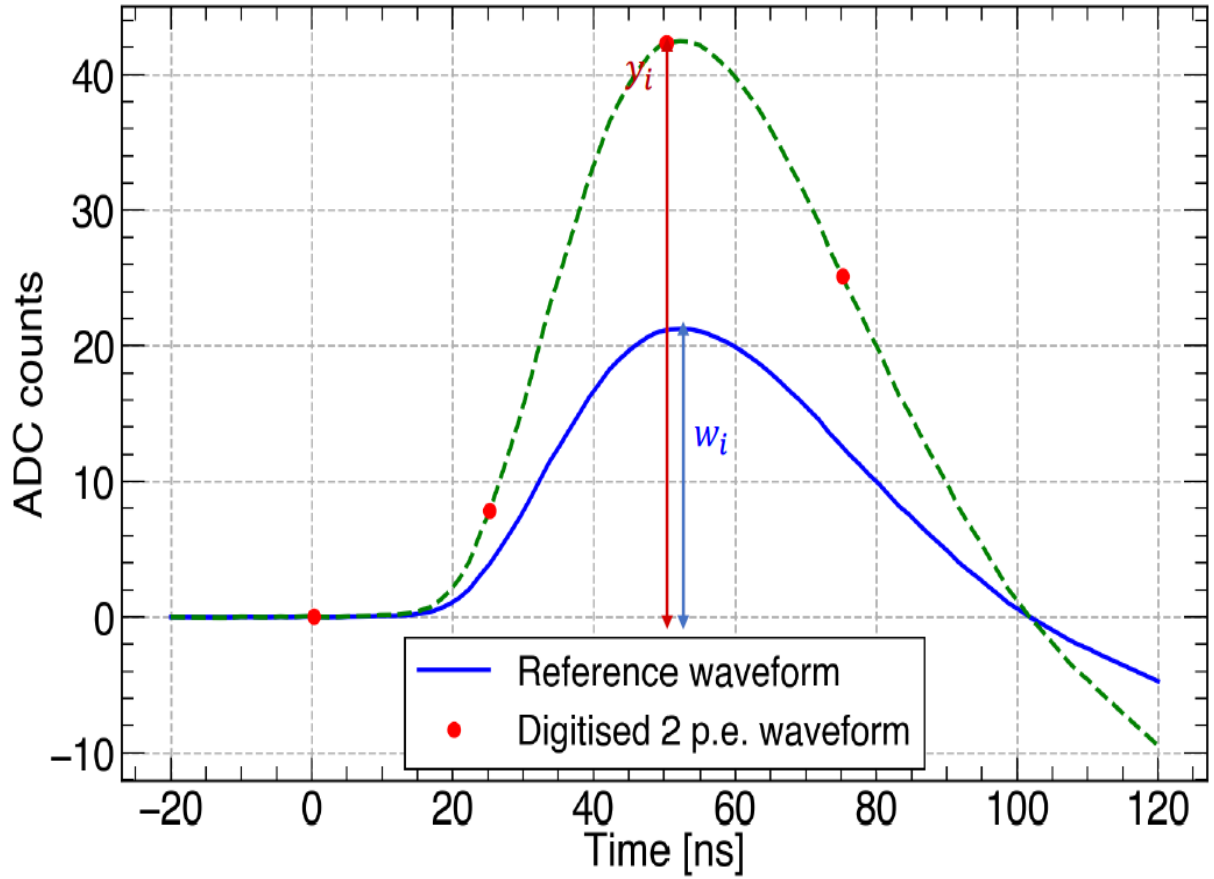
The PMT support is covered by a black sheet, and is itself installed into a black-room to minimize the external light contamination.

For this measurement, the PMT was illuminated by a 402 nm PILAS laser of 100 ps pulse width with a 500 kHz rate.

Reconstruction method

Calibrate each channel of the digitizer with one charge – build a **reference waveform**

$$\chi^2(q)$$



Charge reconstruction

Reconstruction method

$$\chi^2(q) = \sum_{i=1}^{N} \left(\frac{y_i - q w_i}{\sigma_i} \right)^2$$

$$q = \frac{\sum_{i=1}^{N} \frac{y_i w_i}{\sigma_i^2}}{\sum_{i=1}^{N} \frac{w_i}{\sigma_i^2}}$$

- HKROC is waveform digitizer working @ 40 MHz
- Number of charge sampling points from 1 to 7
- Charge reconstruction algorithm in FPGA
- 5 % resources of a modern XILINX FPGA