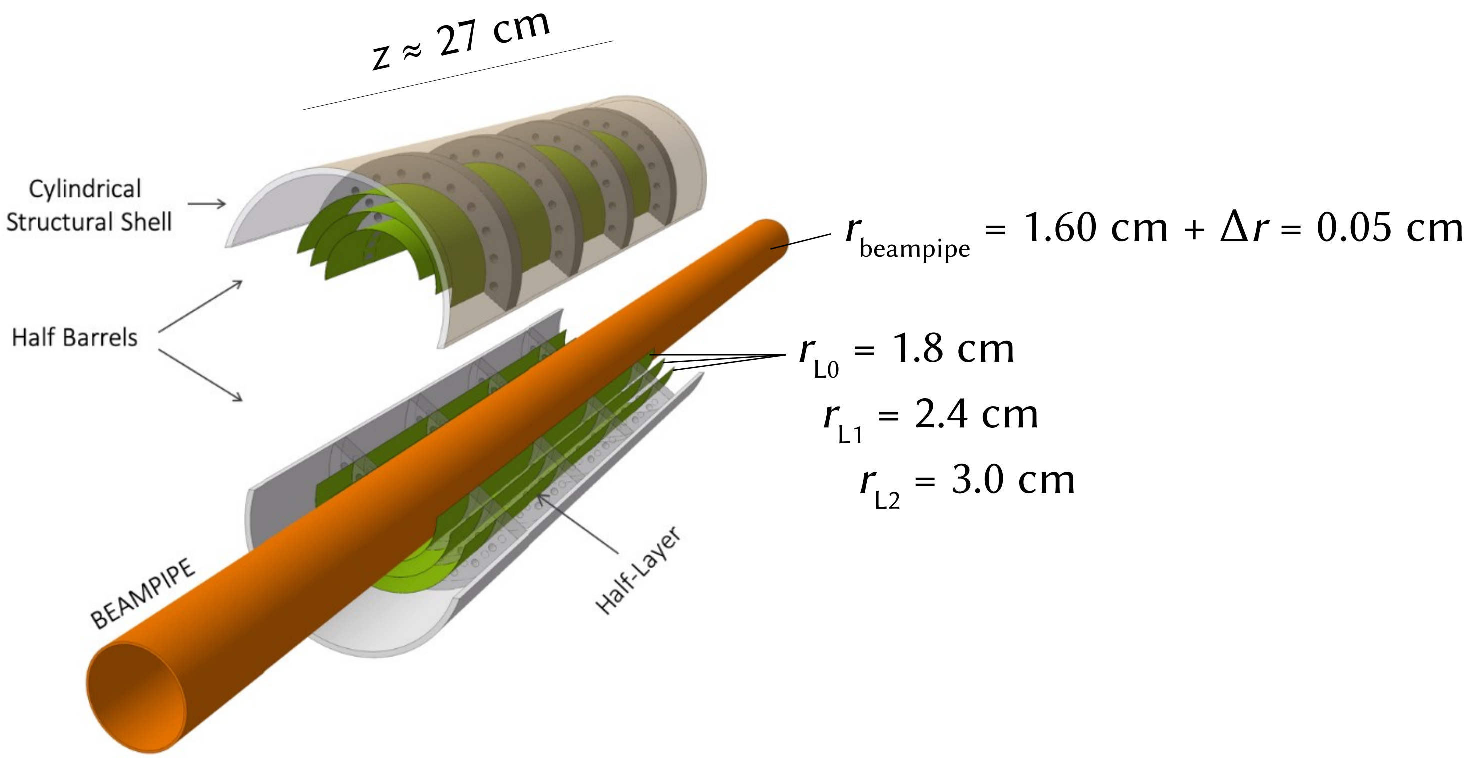
Antonin MAIRE (IPHC Strasbourg), for the ALICE team
Tuesday, 27 June 2023 – **Scientific Council IPHC**

Upgrade of the internal tracker of ALICE₂ :
ITS3 for run 4 at LHC (2029-2032)



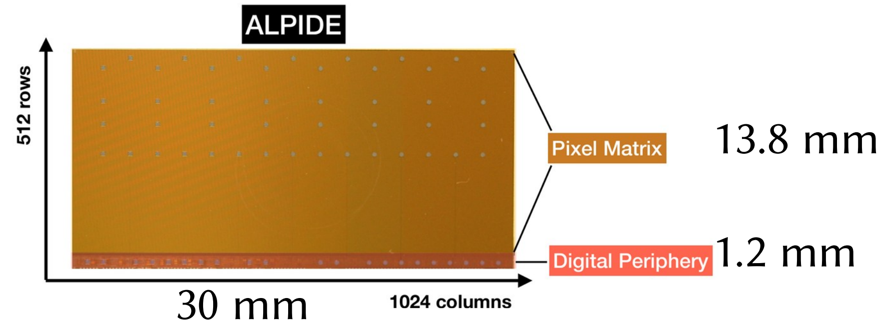
Plan

+ Conseil Scientifique IN2P3 : Council evaluation 27 Oct 2022 (+Indico.in2p3/28308)
+ Key Decision Point 2 at IN2P3 : 23 May 2023

Back to main TOC

Part A – Context & scientific objectives

I.2 – Background : ITS2+MFT, MAPS-based detectors for Run 3

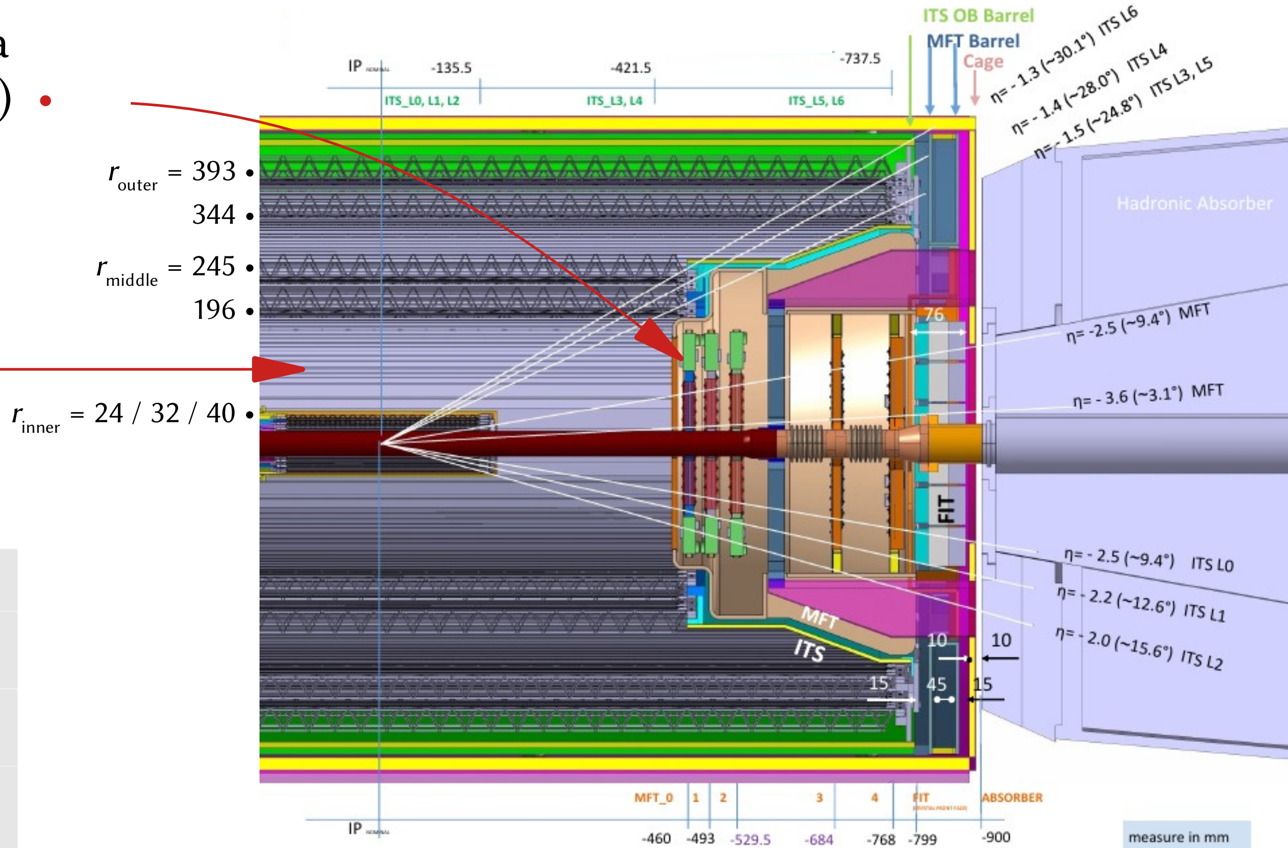


MFT

5 double-sided vertical discs
896 ALPIDE chips
0.47 x10⁹ pixels
= 0.37 m² of active area
(3.7% of ITS2 area)

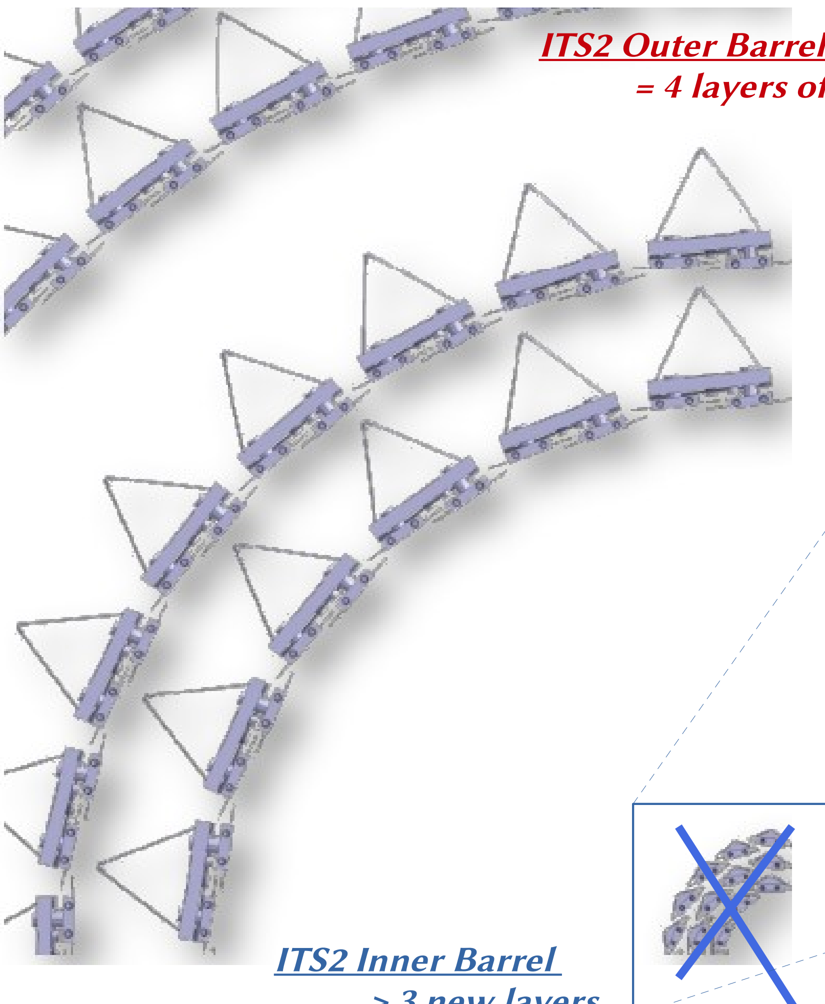
ITS2

7 layers as barrel structure
24120 ALPIDE chips,
12,6 x10⁹ pixels
= 9.99 m² of active area



	L0,L1,L2	L3+L4	L5+L6
Layers	*Inner*	Middle	Outer
Chips	432	6048	17640
Active surface	0.18 m²	2.50 m²	7.30 m²
Fraction	1.8%	25%	73%

II.1 – ITS3 detector : the idea in one glimpse



ITS2 Outer Barrel
= 4 layers of ITS2 kept !

ITS2 Inner Barrel
≥ 3 new layers

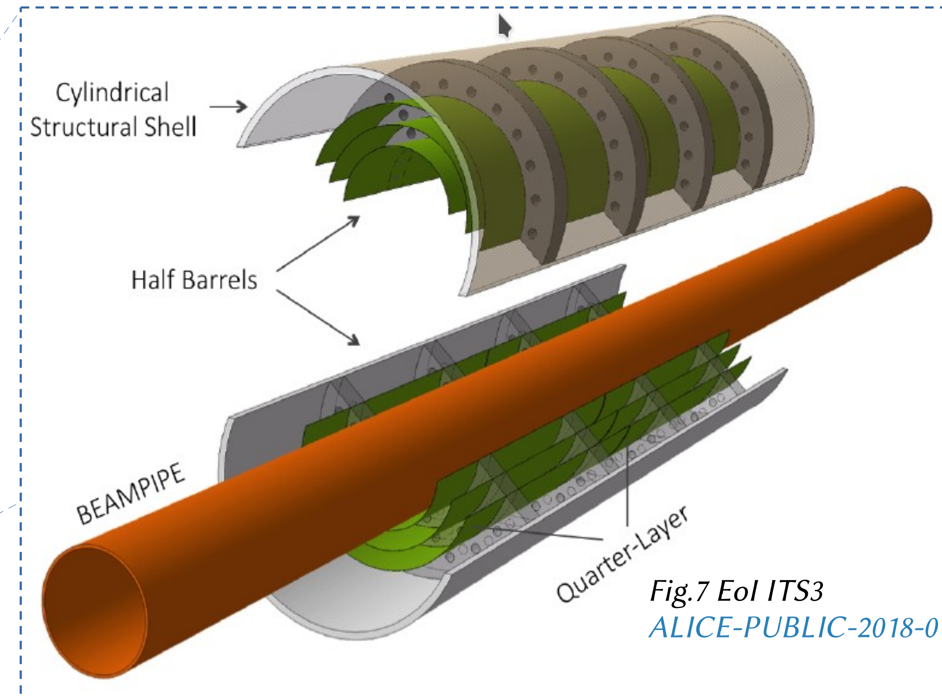


Fig.7 EoI ITS3
ALICE-PUBLIC-2018-013

II.2 – ITS3 detector : some key figures

ITS3 :
curled and lightweight wafer-scaled
CMOS active silicon sensor
Active surface 0.12 m²

r_0 = 1.8 cm

r_1 = 2.4 cm

r_2 = 3.0 cm

Fig.5.8 TDR ITS2
CERN-LHCC-2013-024

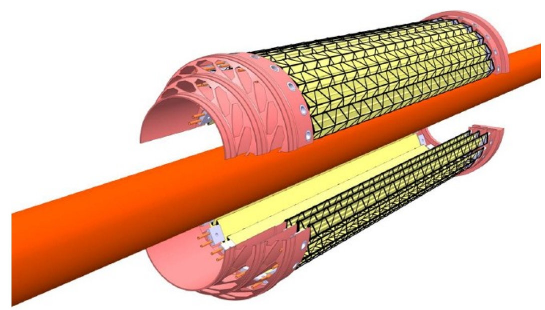
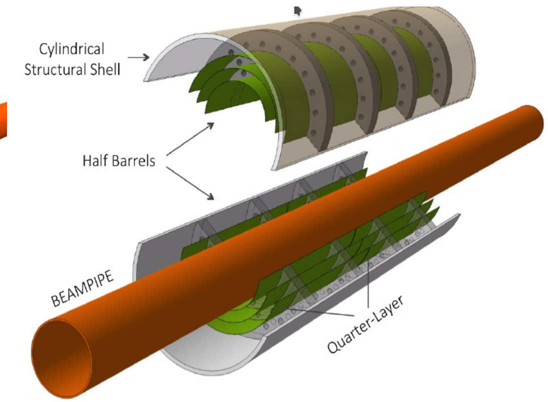


Fig.7 EoI ITS3
ALICE-PUBLIC-2018-013



2. NEW keys	ITS2 IB	**ITS3**
Technology	180 nm	65 nm
Chips	432	6
Pixel size	27 x 29 µm²	≈ 20 x 20 µm²
Material /layer	0.35 % x/X°	≈ 0.05 % x/X°
r_{L0}	2.24-2.67 cm	1.80-3.00 cm
$r_{\text{Beryllium pipe}}$	1.82+0.08 cm	1.6+0.05 cm

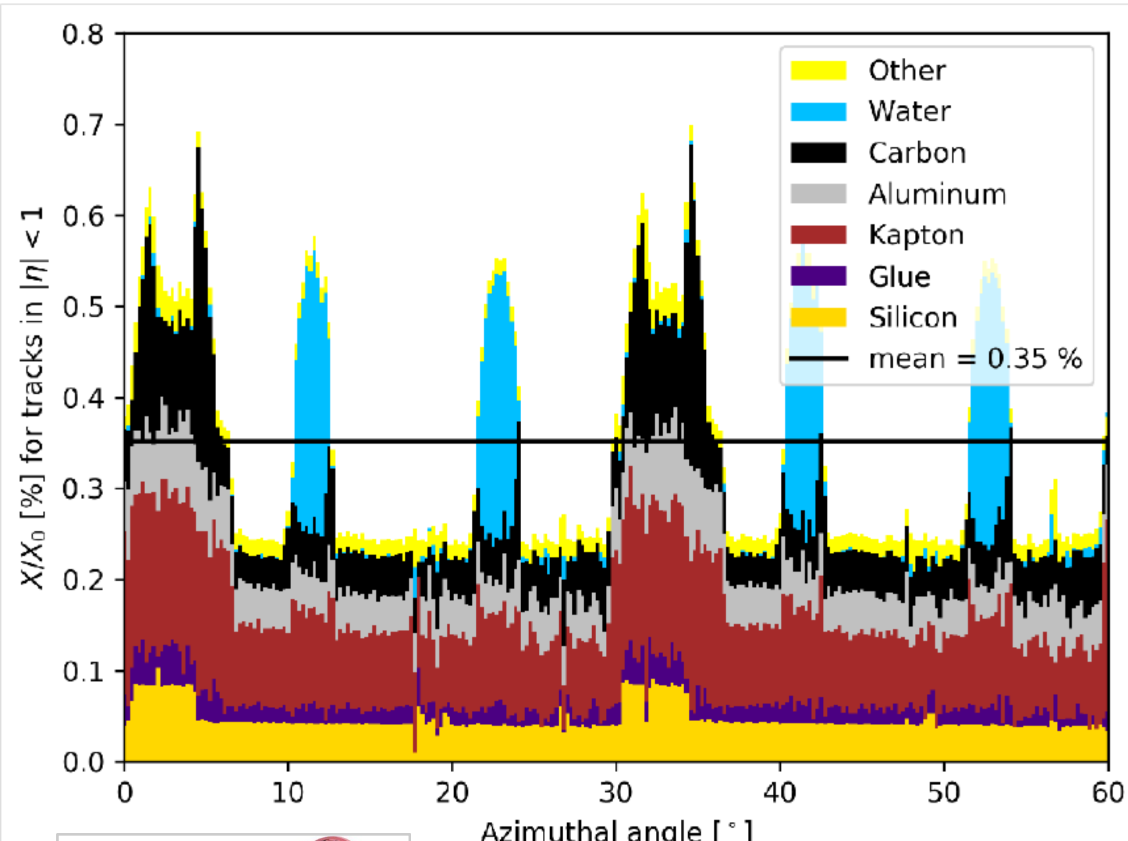
1. (≈ preserved) keys :

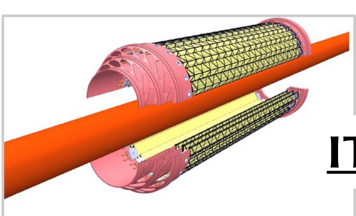
- |η| < 2.2
- spatial resolution/layer ≈ 5 µm
- time resolution ≤ 2-5 µs
- Radiation hardness : NIEL: >3x10^{12} 1-MeV n_{eq}.cm^{-2} // TID: >0.3 Mrad

III.1 – ITS3 project : characteristics and keywords

1./ Can we get closer to IP ?

2./ Can we get lighter in terms of material budget ?





ITS2 IB situation

Starting point : ITS2 Inner Barrel one layer

Statements :

- Si = 1/7 of the overall material budget
- Irregularities = from support + cooling…

1. Get rid of cooling ?

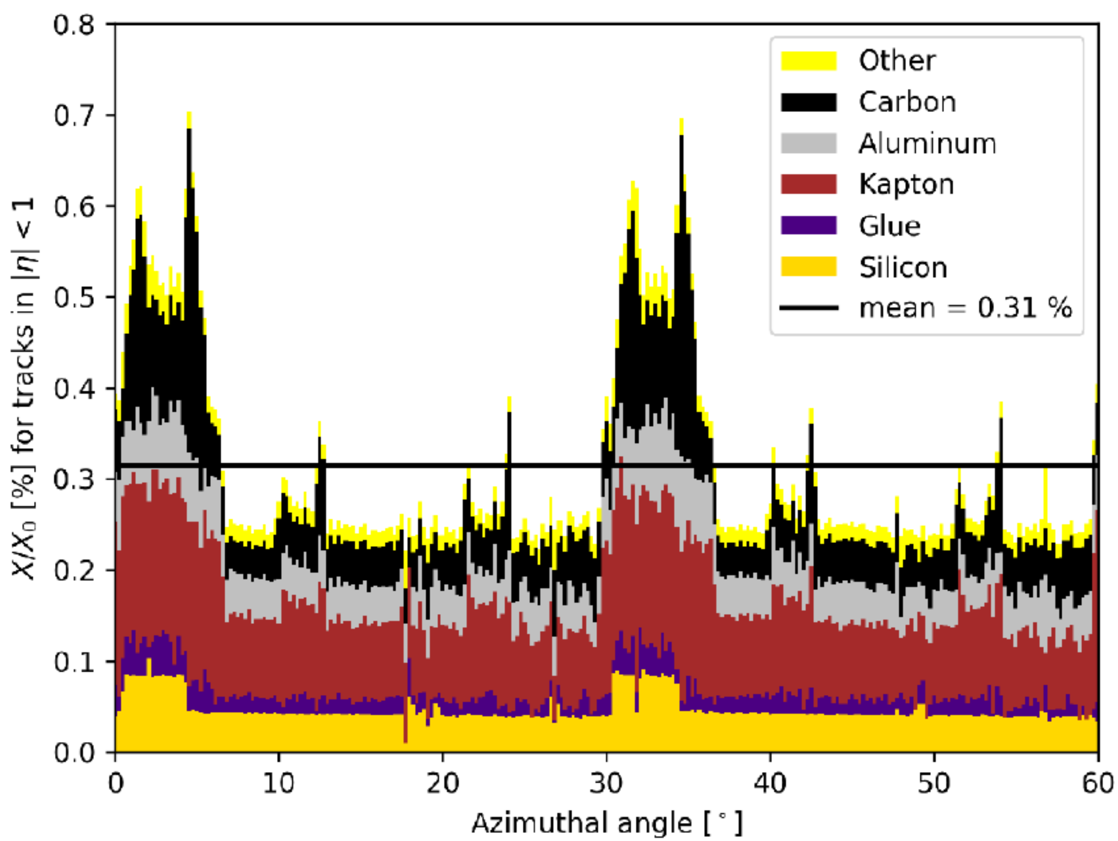
2. Remove the Flexible Printed Circuit (power+data transfer) ?

3. Shift the mechanical support to outside acceptance ?

III.2 – ITS3 project : characteristics and keywords

1./ Can we get closer to IP ?

2./ Can we get lighter in terms of material budget ?



Starting point : ITS2 Inner Barrel one layer
Statements :

- Si = 1/7 of the overall material budget
- Irregularities = from support + cooling…

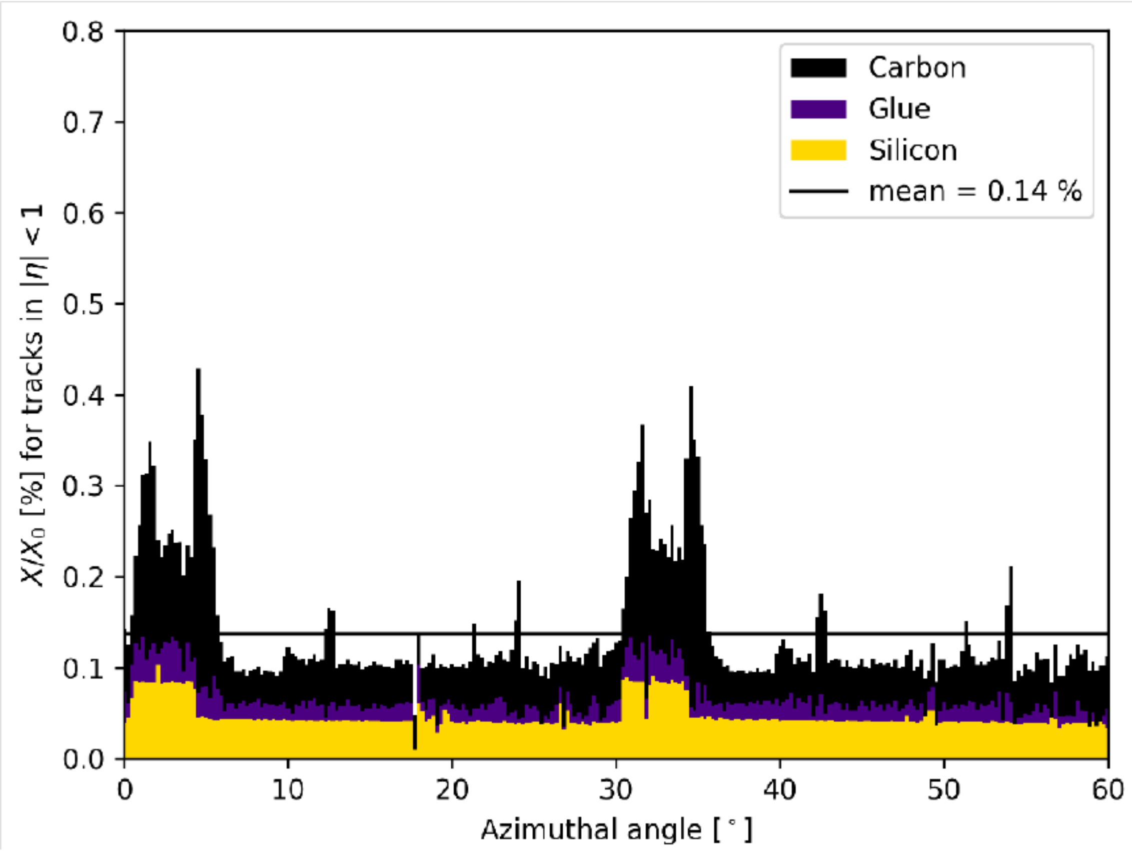
1. Get rid of cooling ?
→ Possible if reduction of power consumption i.e. < 20 mW/cm² on the pixel matrix

2. Remove the Flexible Printed Circuit (power+data transfer) ?

3. Shift the mechanical support to outside acceptance ?

III.3 – ITS3 project : characteristics and keywords

1./ Can we get closer to IP ? **2./ Can we get lighter in terms of material budget ?**



Starting point : ITS2 Inner Barrel one layer

Statements :

- Si = 1/7 of the overall material budget
- Irregularities = from support + cooling…

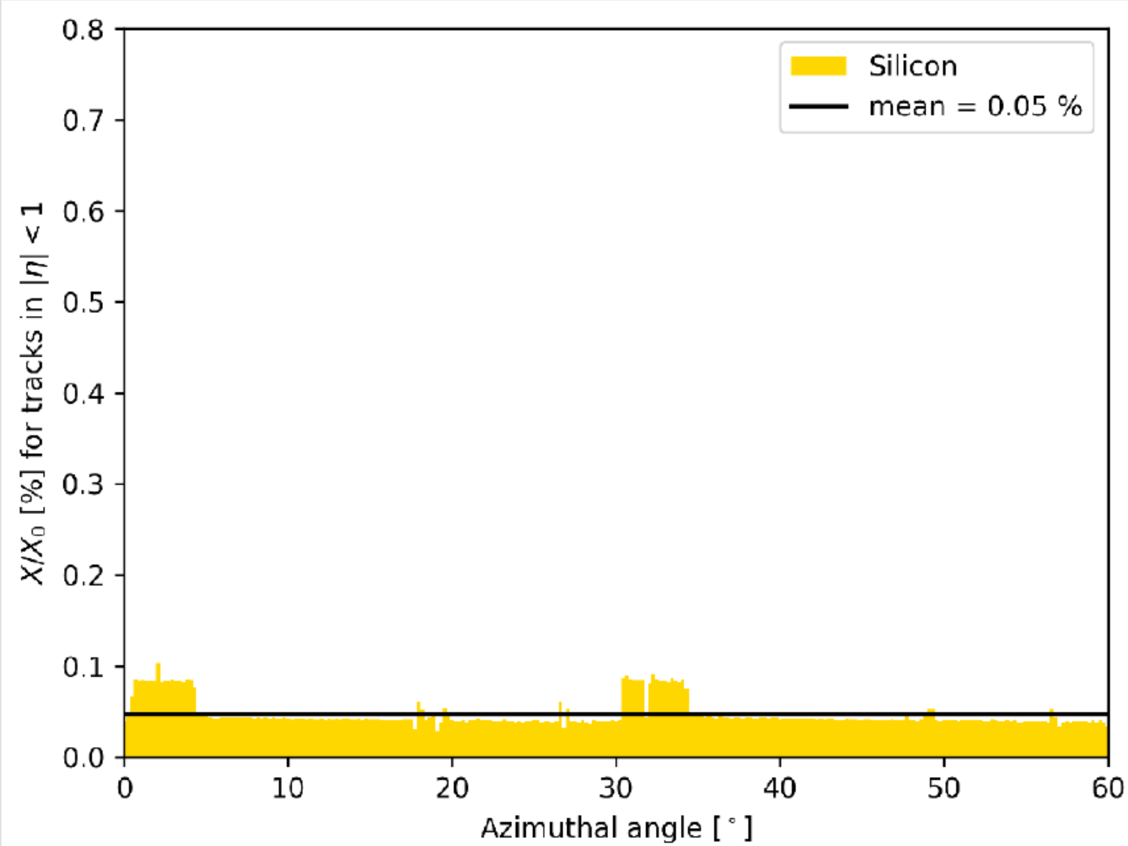
1. Get rid of cooling ?
⟶ Possible if reduction of power consumption i.e. < 20 mW/cm² on the pixel matrix

2. Remove the Flexible Printed Circuit (power+data transfer) ?
⟶ integrate it on the metal layers of the chip itself

3. Shift the mechanical support to outside acceptance ?

III.4 – ITS3 project : characteristics and keywords

1./ Can we get closer to IP ? **2./ Can we get lighter in terms of material budget ?**



Starting point : ITS2 Inner Barrel one layer
Statements :

- Si = 1/7 of the overall material budget
- Irregularities = from support + cooling...

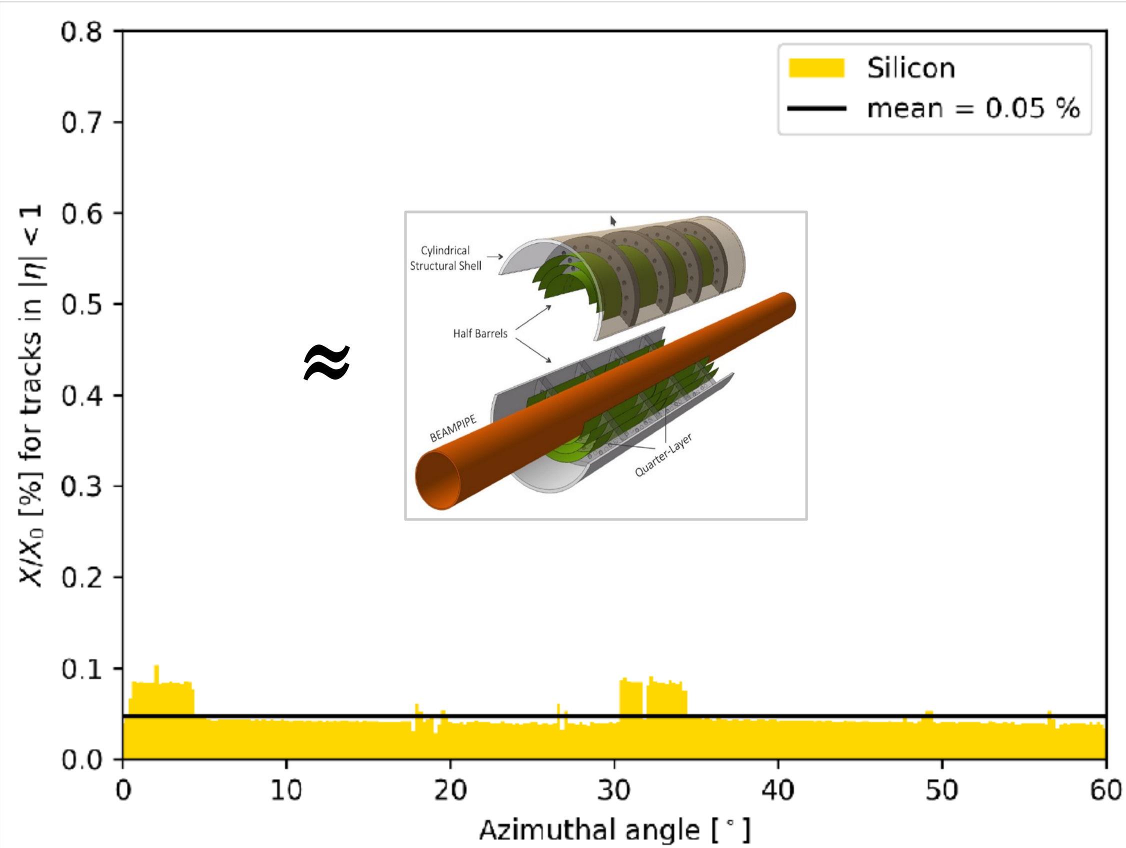
1. Get rid of cooling ?
⟶ Possible if reduction of power consumption i.e. < 20 mW/cm² on the pixel matrix

2. Remove the Flexible Printed Circuit (power+data transfer) ?
⟶ integrate it on the metal layers of the chip itself

3. Shift the mechanical support to outside acceptance ?
⟶ thinned silicon [≤ 50 µm] ⟶ bending
Gain extra stiffness with curled sensor

III.4 – ITS3 project : characteristics and keywords

1./ Can we get closer to IP ? **2./ Can we get lighter in terms of material budget ?**



Starting point : ITS2 Inner Barrel one layer
Statements :

- Si = 1/7 of the overall material budget
- Irregularities = from support + cooling…

1. Get rid of cooling ?
→ Possible if reduction of power consumption i.e. < 20 mW/cm² on the pixel matrix

2. Remove the Flexible Printed Circuit (power+data transfer) ?
→ integrate it on the metal layers of the chip itself

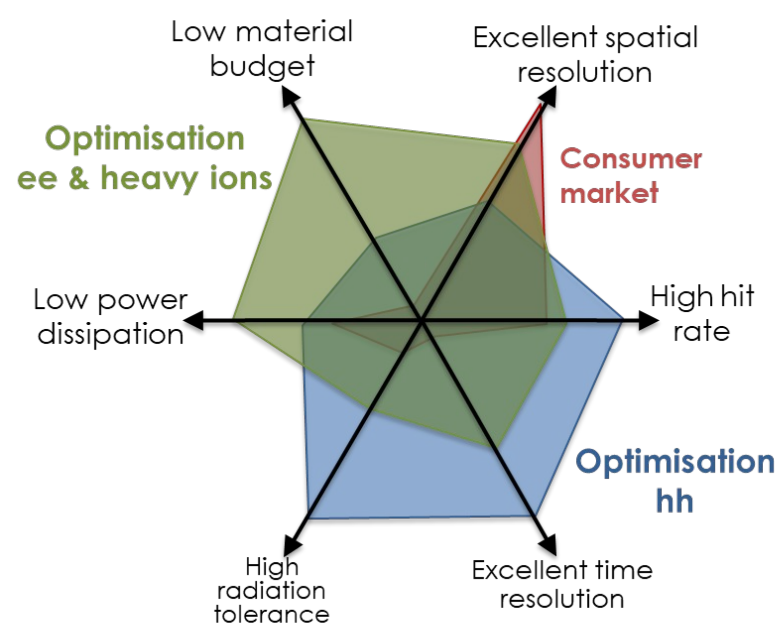
3. Shift the mechanical support to outside acceptance ?
→ thinned slicon [≤ 50 µm] → bending
Gain extra stiffness with curled sensor

IV.1 – “3rd” reason to commit : (e^+e^-) Higgs factories

A. Conclusion 1 out of 4 (*2021 ECFA roadmap*) :

”Develop cost-effective detectors matching the precision physics potential of a next-decade Higgs factory with beyond state-of-the-art performance, optimised granularity, resolution and timing, and with ultimate compactness and minimised material budgets”

B. Overlap of specifications : eA, pA, AA // e^+e^- !



Courtesy J. Baudot

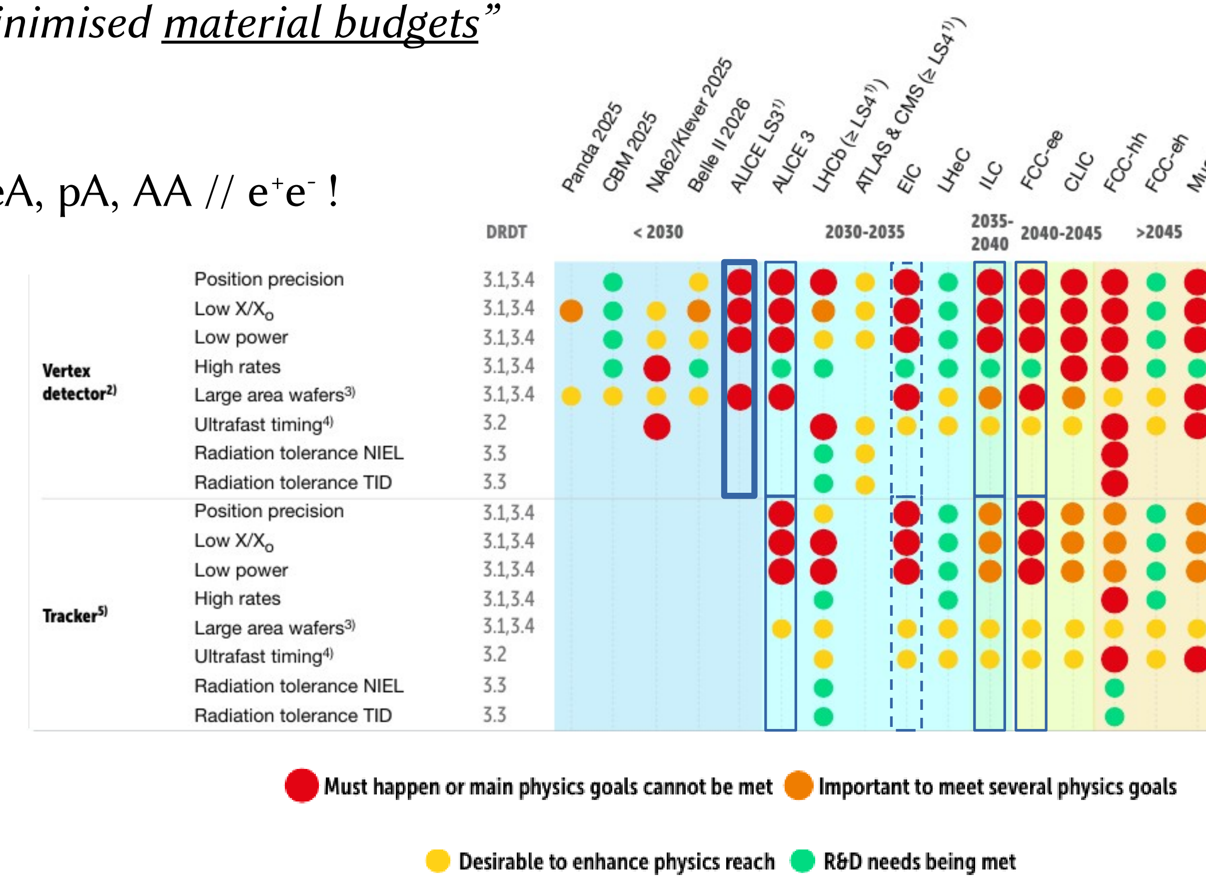


Fig. 3.1, 2021 ECFA roadmap

Back to main TOC

Part B – Breakdown structure

Product Breakdown Structure & *Work* Breakdown Structure

I.1 – ITS3 project : global milestones

4 Engineering Runs **(ER)**, all in 65-nm technology, "*no production phase, only R&D*" :

1. **MLR1** tape out (2020-12) :

. Objective (validated): detection efficiency in 65-nm technology (>99%) vs. 180-nm ALPIDE
. Flag : "generic R&D" (i.e. WP1.2 MAPS CERN, within the CERN EP R&D)
. Technology node : 65 nm
. pixel pitches : 10, 15, 20, 25 μm

→ 54 different prototypes of sensors = (analog and/or digital sub-blocks),
among which 3 prototypes, each with variants :

- APTS (CERN)
- DPTS (CERN)
- CE65 (IPHC)

all of (very) small surfaces of 1.5x1.5 mm^2
(from 6x6 to not more than 64x32 matrix, *i.e.* "*chiplets*"
e.g. to be compared with ALPIDE having 512x1024 pixels)

Main goals:
- Learn technology features of 65-nm node
- Characterize charge collection (cluster, timing, ...) and detection eff. (>99%)
- Validate radiation hardness

I.1 – ITS3 project : global milestones

4 Engineering Runs **(ER)**, all in 65-nm technology, "*no production phase, only R&D*" :

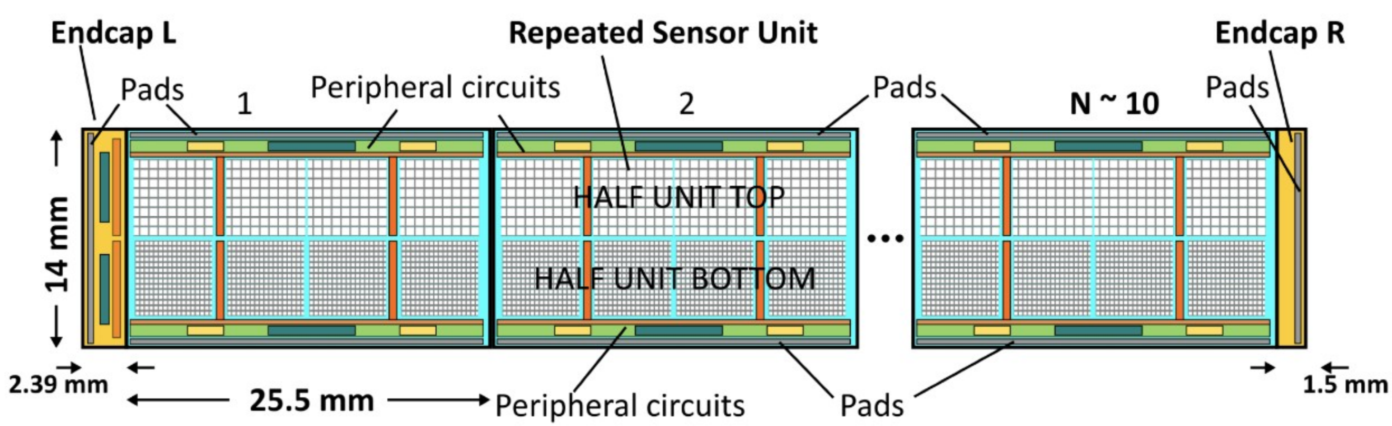
1. **MLR1** tape out (2020-12) : ...
2. **ER1** tape out (2022-11) :

. Objective : *stitching* 1D (+ assess yields by the foundry)
. Flag : "generic R&D"
. Technology node : 65 nm,
. pixel pitches: 18 and 22,5 μm

→ 24 wafers with (51 chiplets, e.g. DPTSv2, CE65v2, ...) + (2 large-sensor variants : MOSt and **MOSs**)

MOSs = 1.4 x 25.9 cm², + consists of 10 sub-units ("RSU") of ($r\varphi$ x z) =1.4 x 2.55 cm² each,

repeated along z, stitched "natively" on the wafer, in the close spirit of what ITS3 should look like.



From Mager-ICHEP22

I.1 – ITS3 project : global milestones

4 Engineering Runs **(ER)**, all in 65-nm technology, "*no production phase, only R&D*" :

1. **MLR1** tape out (2020-12) : ...

2. **ER1** tape out (2022-11) : ...

– Technical Design Report, **TDR** (2023-10) for LHCc, relying on 3 "pillars" (*i.e.* proofs expected)

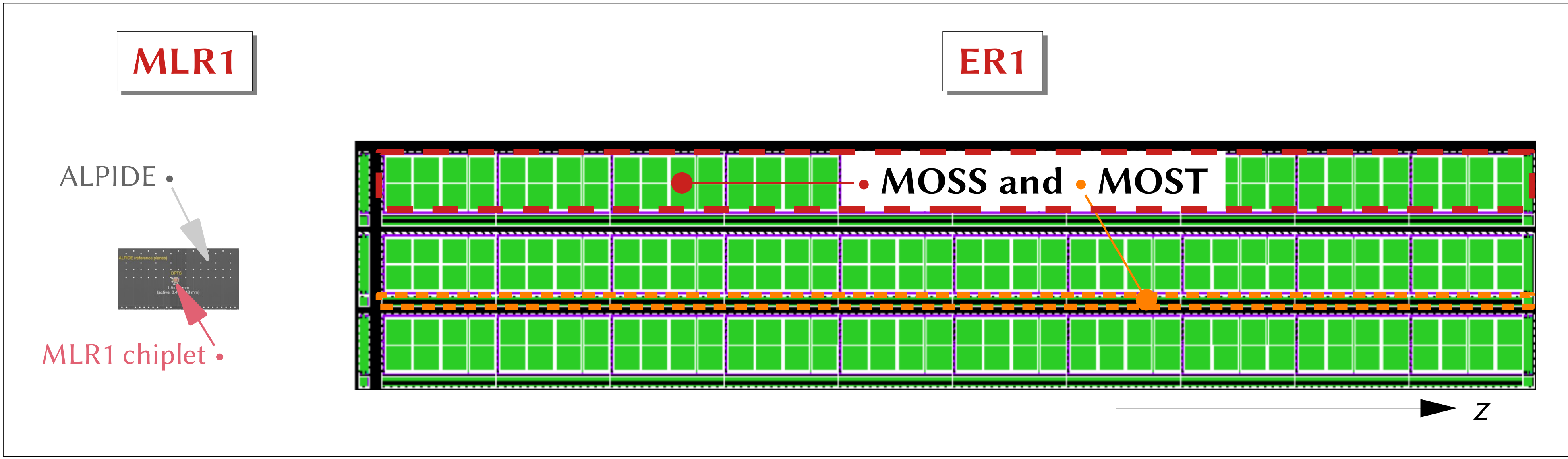
i) bending MAPS **ok!**
ii) 65-nm MAPS **ok!**
iii) stitching **= ER1...**

3. **ER2** tape out (2024-02) : ,

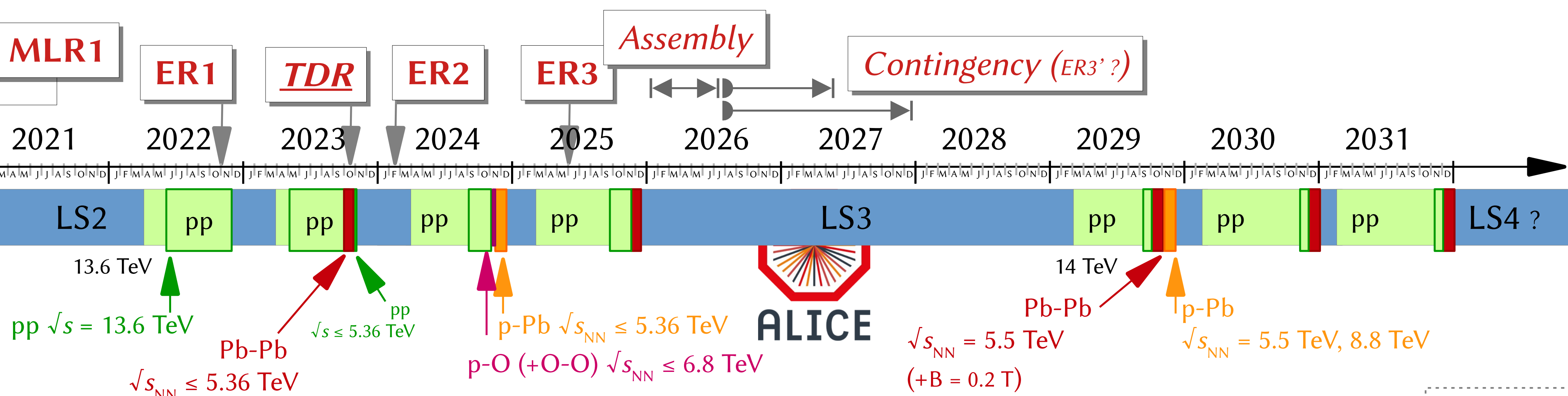
. Objective : full-scale demonstrator, with complete set of functionalities ITS3-like, notably :
. power
. readout
. Flag : "generic R&D" or "ALICE ITS3-specific R&D" ?
. Technology node : 65 nm,
. pixel pitch: likely only one = 18 x 22,5 µm

4. **ER3** tape out (2025-06) : final "production"

I.2 – ITS3 project : global milestones and timeline



(NB : here, relative sizes to scale)



II.1 – ITS3 project : ALICE organisation in work packages

Project Leaders: Magnus MAGER (CERN) and Alex KLUGE (CERN)

ALICE Indico : *https://indico.cern.ch/category/11668/* → *weekly or bi-weekly meeting per WP*

- **WP1 - Physics, Simulation and Reconstruction**
  Fabrizio GROSA (CERN), Andrea ROSSI (INFN Padova)

- **WP2 - Pixel Sensor Design** ≈ CERN+IPHC +NIKHEF
  Gianluca AGLIERI RINELLA (CERN), Walter SNOEYS (CERN)

- **WP3 - Sensor Characterisation and Qualification** = Lots of people... [$\mathcal{O}$(30-50 people)]
  Serhiy SENYUKOV (CNRS IPHC), Miljenko SULJIC (CERN)

- **WP4 - Thinning, Bending, Interconnection** ≈ INFN +IPHC
  Domenico COLELLA (INFN Bari), Giacomo CONTIN (INFN Trieste)

- **WP5 - Mechanics and Cooling** ≈ CERN +Grenoble +St Petersburg + Utrecht
  Massimo ANGELETTI (CERN), Corrado GARGIULO (CERN)

- **WP6 - Readout electronics** ≈ CERN+Grenoble
  Ola GROETTVIK (CERN), Felix REIDT (CERN)

III.1 – ITS3 France : national-level status

©LaChaineMeteo

- Signatories (IN2P3 Sci. Council 2022-10) :
  >39 (physicists + engineers)
- Requested budget to IN2P3 :
  ***O*(600 k€)** for core contribution (*i.e.* ~~*HR salary*~~),
  out of Whole ITS3 core ≈ 6500 kCHF

1. National **Scientific Council at IN2P3** : 2022-10
See Evaluation report 27 Oct 2022 (+Indico.in2p3/28308)
⟶ project approval by IN2P3 (01 March 2023)

IN2P3 scientific responsible : Antonin MAIRE (IPHC)
IN2P3 technical responsible : TbD (IPHC)

2. Key Decision Point 2 (**KDP2**) (23 May 2023)
i.e. define / review ITS3 French perimeter
- deliverables
- budget
- Human Resources

⟶ **Endorsement** of a perimeter (9 June 2023)
(Deputy director for Particle Physics + 3 Lab. Directors)
Debriefing, to be done.

3. Local scientific council IPHC, today...

III.2 – ALICE France : French delivrables for ITS3

1.a Design of the pixel matrix [IPHC]
- analogic level (charge collection + very front-end electronics)
- numeric level (digital treatment + power management)

1.b Qualification and tests of CMOS prototypes submitted to foundry [IPHC]

2.a *middle-end* electronic cards (readout + slow control + powering of ITS3) [LPSC]
- Design of cards
- Production of cards
- (Mechanical + optronic) integration (design + production of mechanical supports)

2.b Mechanical elements for the cooling circuitry [LPSC]

3. Integration and electronic micro-connectics, in view the final installation [IPHC]

4. Assembly of a detector according to a back-up plan (Super ALPIDE) [IPHC]

NB :
- ~~Computing~~
- ~~Tracking and reconstruction algorithms~~ (vertexing, tracking, alignment, simulations)

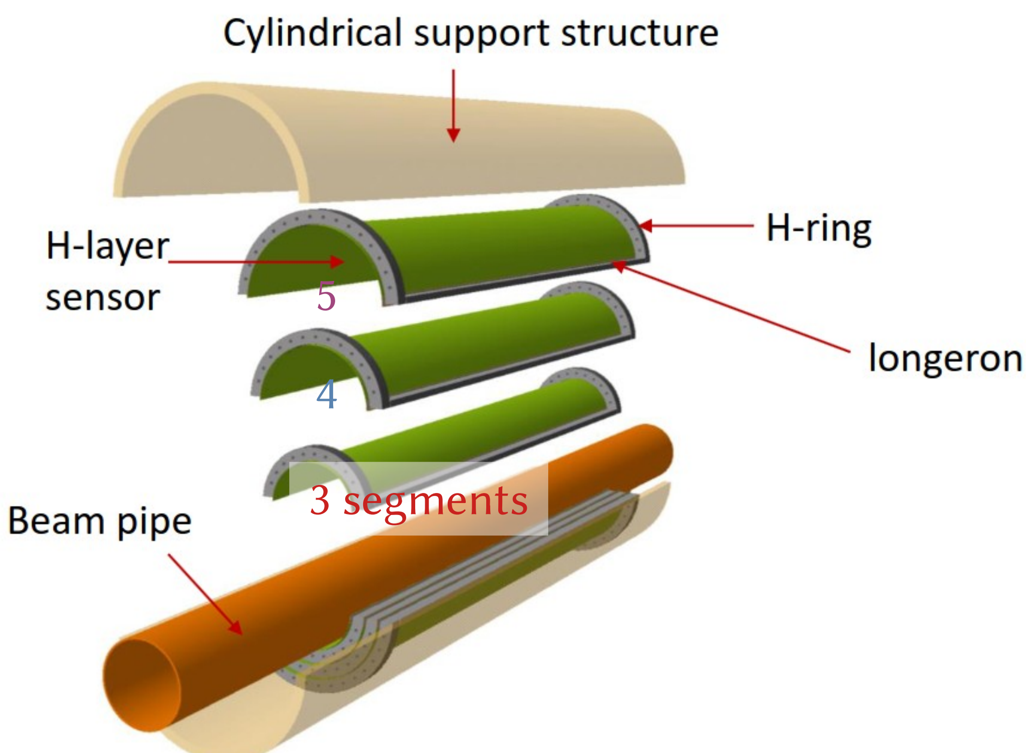
+ link ~~reconstr° ITS2+3~~

= relegated to missions of the 3 ALICE teams [IPHC, IP2I, LPSC],
no French-specific deliverable expected

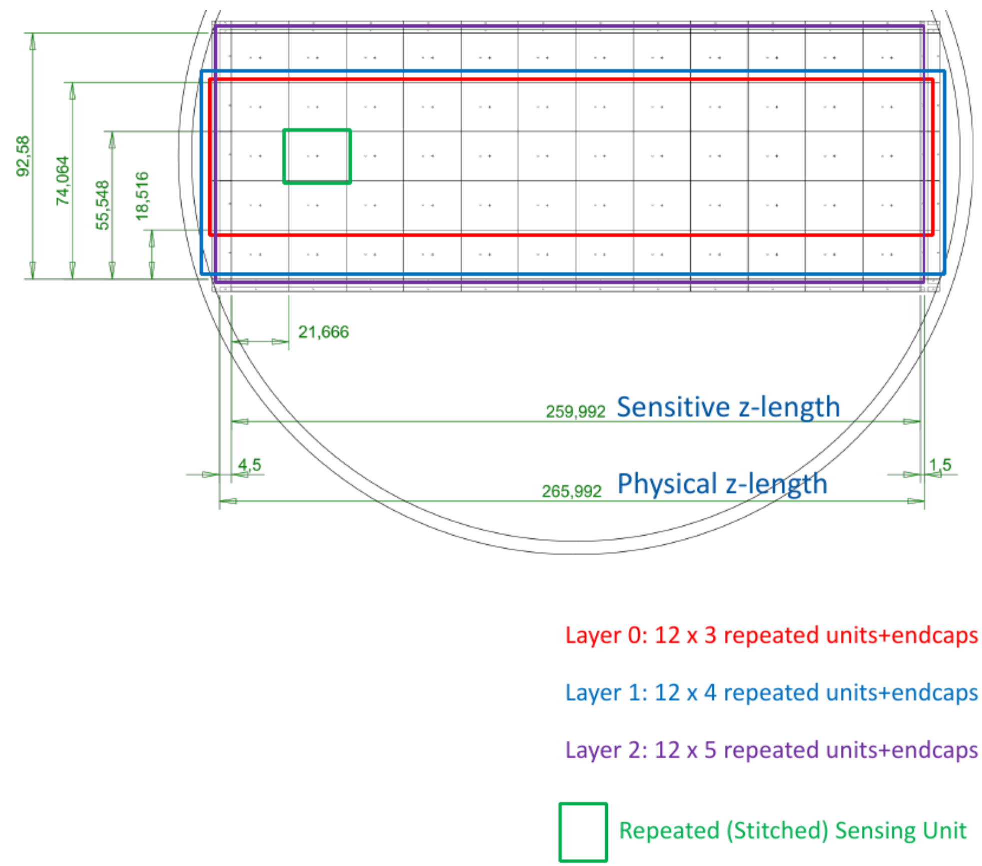
IV.1 – Locate within ITS3 : the logic of "*n*-segments"

Aglieri, WP2 ITS3 plenary 2023-05

Exploded view :
(1 stitched sensor / hemi-cylinder)
x 2 halfs/layer
x (3-4 layers)



30-cm wafer, with 3,4,5 **segments** of 12 RSU



Corrado Gargiulo, WP5 ITS3 Plenary 2023-04

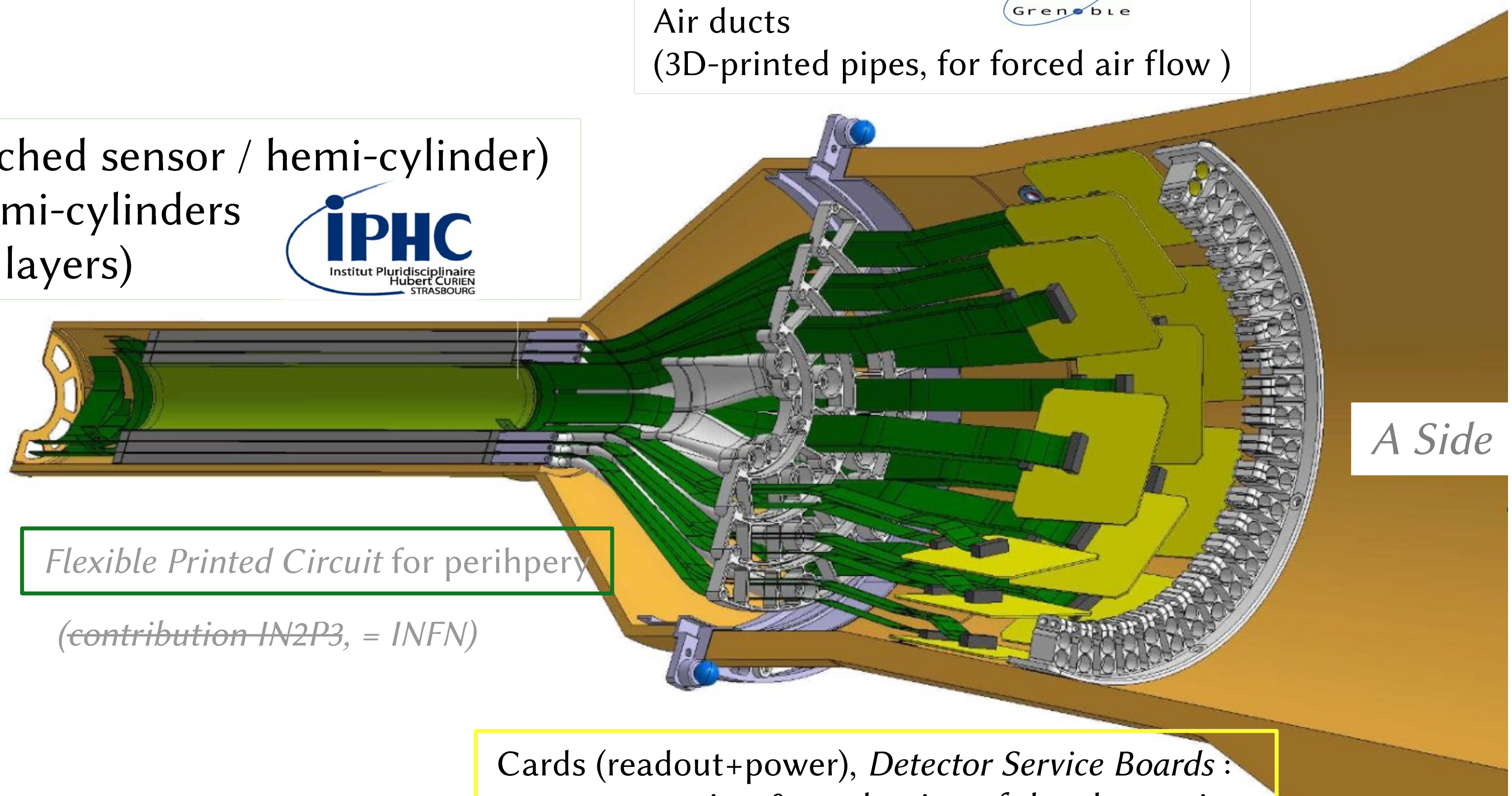
IV.2 – Locate within ITS3 : from pixels to patch panels

French contributions

Air ducts
(3D-printed pipes, for forced air flow)

(1 stitched sensor / hemi-cylinder)
x 2 hemi-cylinders
x (3-4 layers)

C Side



A Side

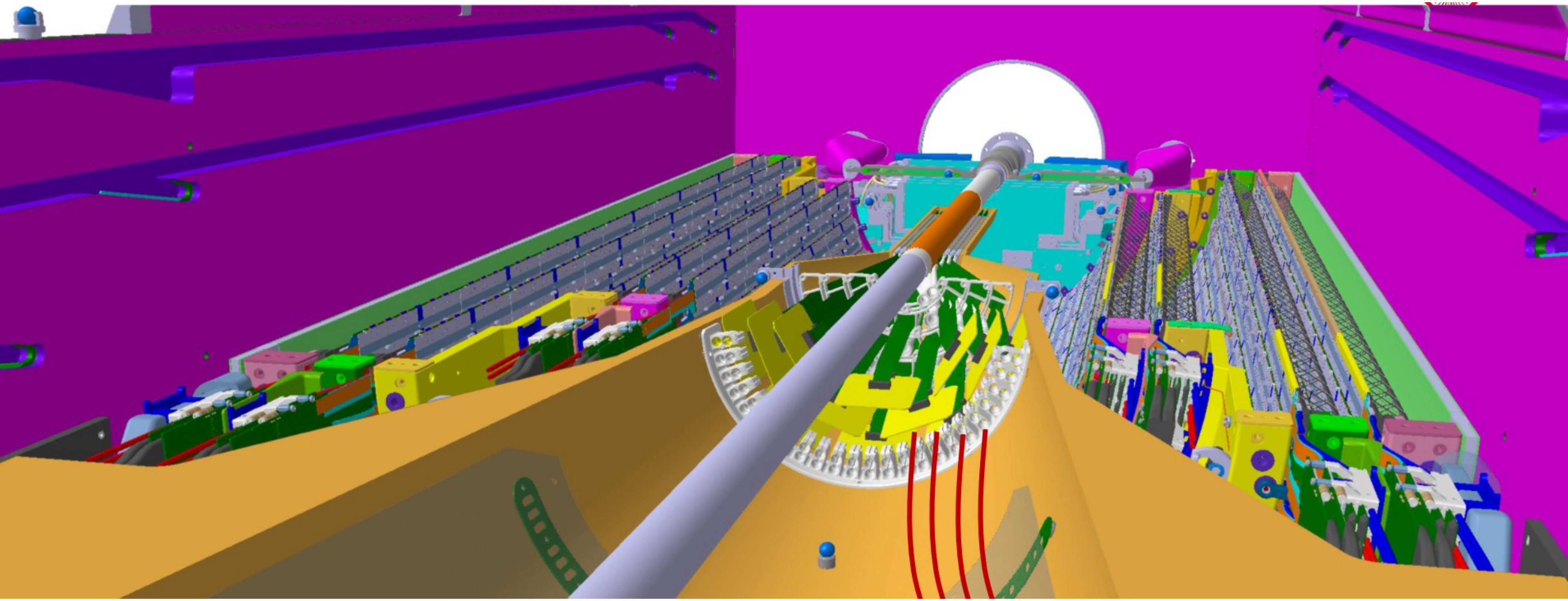
Flexible Printed Circuit for perihpery

(~~contribution IN2P3~~, = INFN)

Cards (readout+power), *Detector Service Boards* :
conception & production of the electronics,
+ mechanical integration

Corrado Gargiulo, WP5 ITS3 Plenary 2023-04

IV.3 – Locate within ITS3 : global view



Corrado Gargiulo, WP5 ITS3 Plenary 2023-04

V.1 – Work breakdown : 1.a CMOS design

What does it imply/mean to design ITS3 CMOS sensor ? *e.g.* ongoing breakdown for ER2

1 Introduction
2 Overview
- 2.1 Concept Overview and Characteristics
  - 2.1.1 General objectives and requirements
  - 2.1.2 FIG: Overall concept diagram of the sensor
  - 2.1.3 General characteristics
  - 2.1.4 Nomenclature
- 2.2 Sensor Connectivity, I/Os and Supplies
  - 2.2.1 FIG: Sensor IOs and supplies
- 2.3 Block Diagram and Floorplan of RSU
  - 2.3.1 FIG: of RSU block diagram
  - 2.3.2 Dimensions of the blocks
- 2.4 Block Diagram and Floorplan of Endcap Left and Endcap Right
  - 2.4.1 FIG: Block diagram of Endcap Left
  - 2.4.2 FIG: Dimensions of Endcap Left

3 Detailed dimensions
- 3.1 Reticle, sensors and wafer stitching plan
  - 3.1.1 FIG: Mechanical baseline figures and table of dimensions

4 Supply Distribution Scheme
- 4.1 Supply distribution scheme
- 4.2 Power domains
- 4.3 Substrate
- 4.4 Local power regulation
- 4.5 Isolation between power domains
- 4.6 Power estimates

5 Pixel Array
- 5.1 Pixel Array Overview
- 5.2 Pixel Size
- 5.3 Pixel Front-End
- 5.4 Analog Biasing
- 5.5 Analog Monitoring (ADC)
- 5.6 Pixel Digital Section
- 5.7 Priority Encoder

6 Slow Control
- 6.1 Configuration, Management, Slow Control for Power Management
- 6.2 Slow Control for Biasing
- 6.3 Slow Control for Readout
- 6.4 Distribution of strobing synchronization
- 6.5 Power On and Power Down, default configuration

7 Readout
- 7.1 Architecture and Performance
- 7.2 Readout memories

8 Stitched Communication Backbone

9 Data collection in Endcap
- 9.1 Phase aligners
- 9.2 Deserializers in Endcap Left
- 9.3 Encoding
- 9.4 High speed serial transmitters

10 Design for Manufacturability and High Yield
- 10.1 Design Rules, Recommended, High Yield, Custom
- 10.2 High yield standard cell for peripheries
- 10.3 High yield compact cells for pixel array
- 10.4 High yield SRAM block

11 Radiation Resistance
- 11.1 TMR
- 11.2 Requirements, acceptable rates, input from experiment

12 Pad rings
- 12.1 I/O pad cells
- 12.2 Supply cells
- 12.3 ESD cells

13 DFT Design for Testability
- Features for testability.

14 Verification of power intent

(Courtesy WP2, Gianluca Aglieri)

(*Red items* = contributed by IPHC)

NB: ER2 et ER3 designer lineup ≈ 50% CERN + 50% IPHC, ≈ 4-5 FTE each

V.1 – Work breakdown : 1.a CMOS design

"(*Red items* = contributed by IPHC)" , that is ?

IPHC/C4π = work on the heart of the pixel matrix
(i.e. ≠ peripheries, ≠ slow control)

Produce the building elements of the matrix

item **A** – **Analogic front-end** within pixels (50/50 CERN+IPHC)

item **B** – **Numeric architecture for pixel readout** within the matrix (≈ 100% IPHC)

+ validation and consolidation *actions*

item **C** - Integration of the matrix in the so-called **Digital On Top** description

item **D** – Analysis of **power** and of the behaviour of power rails

V.2 – Work breakdown : 1.b Tests and qualification

(See later App. D – 65-nm MAPS)

- *[2020-2023]* **MLR1** = 51 *65-nm* chiplets, among which 3 main prototypes:
  ◦ APTS (CERN) ◦ DPTS (CERN) ◦ CE65 (C4π+PICSEL)

  Tests of these chiplets
  - ◦ in their different variants (along 3x4 lithographic processes, 4 pitches, readout architectures, ...),
  - ◦ non-irradiated / **irradiated,** at different levels

  → 1/ Probe testing

  +2/ tests under source (^{55}Fe) in the lab

  +3/ campaigns of 5-10 days under beam

  ≈ 4 campaigns in 2021, 4 in 2022, 4 already in 2023 / (PS, SPS, DESY),
  i.e. intensive...

- *[2023-07 / 2024-08]* Idem to come from MOSs and MOSt by ER1 (≥ 2023-07, 1st tests in view of TDR)
  ◦ **ER1** = MOSs + MOSt + 54 chiplets (ex: MLR1 chiplets in v2 + in v1 pour contrôle)

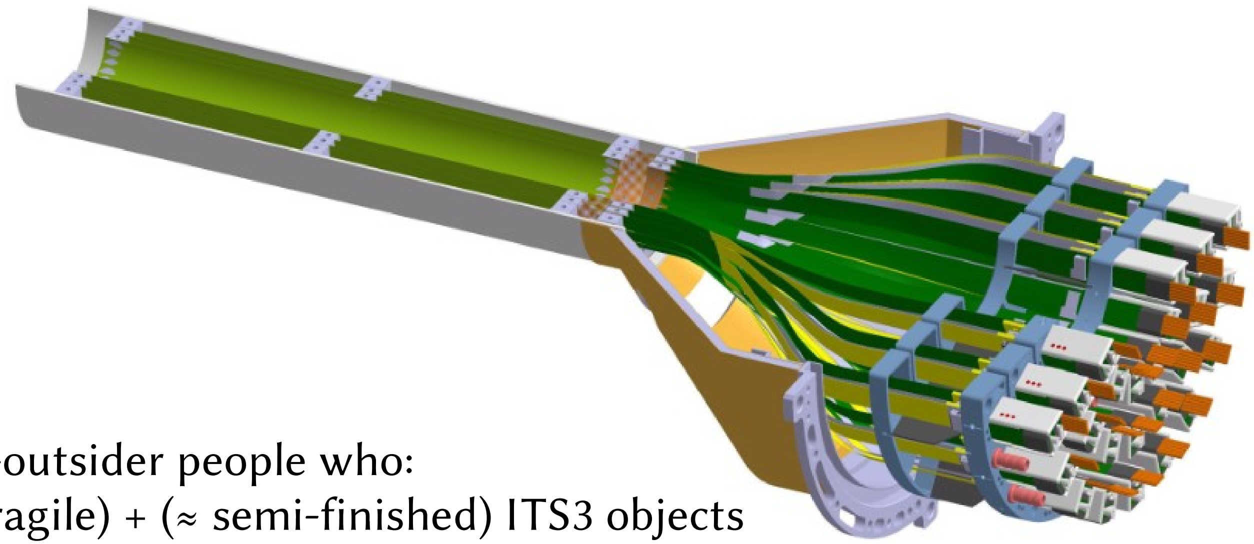
  ...

  3/ [4-6] campaigns dedicated to ER1, already programmed between July and Nov. 2023
  See *PS+SPS schedule*

- *[2023-08 / 2025-12]* Idem for **ER2**, with MOSS2 + only few chiplets

- *[2026-2027]* Idem for **ER3** + **qualification/choice** of sensors to equip ITS3 itself

V.4 – Work breakdown : 3. Integration, installation

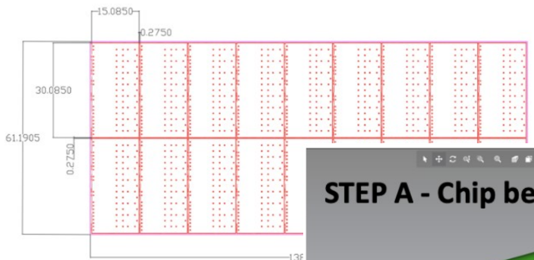


The ITS3 project = need a few WP-outsider people who:
- can/will be able to handle (fragile) + (≈ semi-finished) ITS3 objects
- help establishing the protocols
  - of the sub-part assembly
  - of ground-floor as well as cave installations
- practice assembly, to validate the process / identify difficulties in advance to correct them

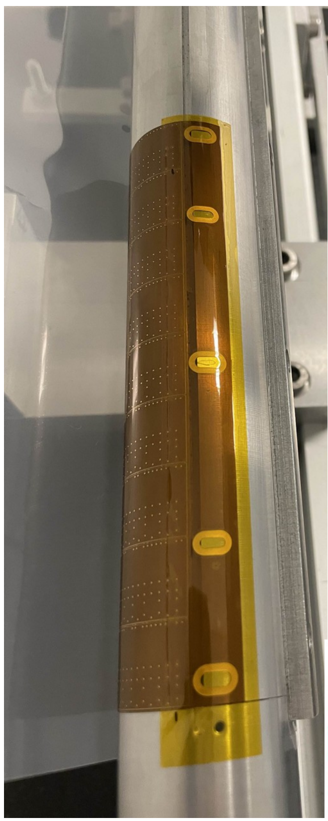
That are, people who move from "plans" to concrete and global implementation.
(manipulation tools, glueing strategy, test cards, ER1 bonding, routing of flex, etc.)

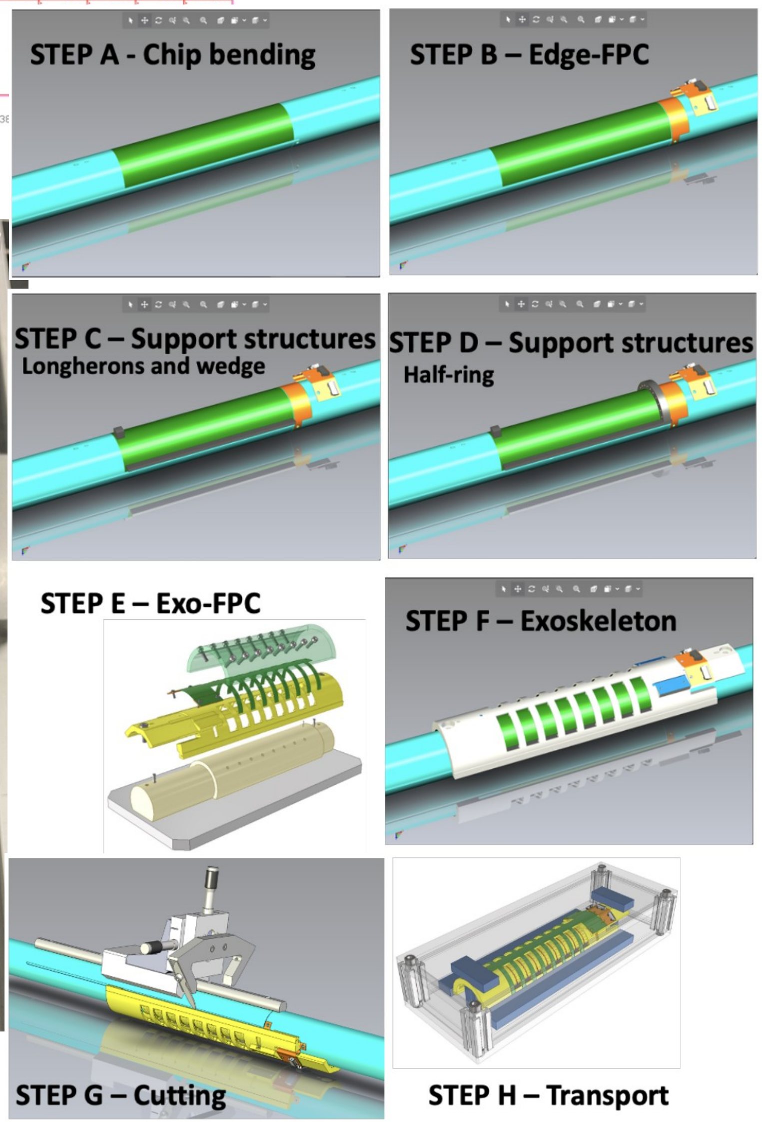
→ "*transversal*" vision between WP3 (tests), WP4 (interconnection, bending), WP5 (mechanics) and WP6 (readout)

V.5 – Work breakdown : 4. SuperALPIDE



A.





Pursue a back-up plan for ITS3 (*ex: if stitching turn out to be severe bottleneck*)

→ Style exercise :

A. [4h] bending over mandrel of 2x9 ALPIDEs
(*"~~diced~~" but "monoblock", i.e.* from a same wafer)
≈ 6 (=2x3^+ cm) x 14 (=9x1,5^+) cm²

B. [0,5+2h] placing + <u>bonding</u> of periph. FPC

C+D. [2+1h] glueing of carbon foams

E. [02h] placing, glueing of exo-FPC

F. [2h] placing, glueing of exo-skeleton

F. [7j] <u>bonding (Exo-FPC+ALPIDEs)</u>

G. [2h] Cutting

H. preparation for transport

<u>NB</u> : B+F = bonding on a *curved* surface…

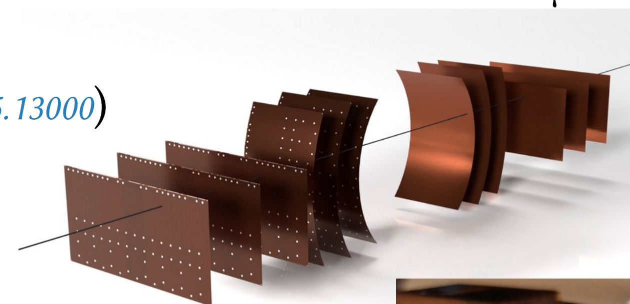
→ Project which is outside-CERN, decentralised (among ITS3 project, only IPHC + INFN Bari = sub-project attached to WP4)

Back to main TOC

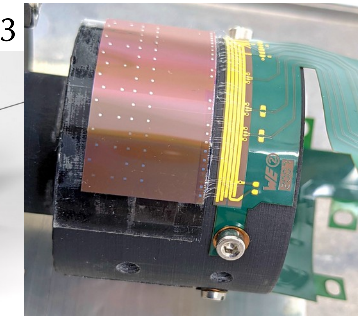
Part C – State of the art

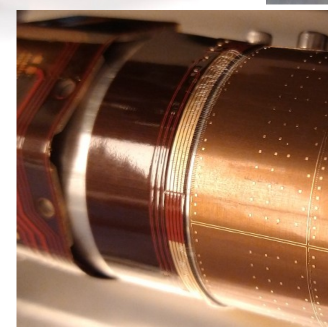
I.1 – ITS3 project : ALICE state of the art 2023-05

A. • Beam tests of ***bent*** ALPIDE chips (*arXiv:2105.13000*)
• Beam tests with µITS3
• Construction of SuperALPIDE, ongoing
(i.e. ITS2 chip 50-µm thick, 180-nm technology)



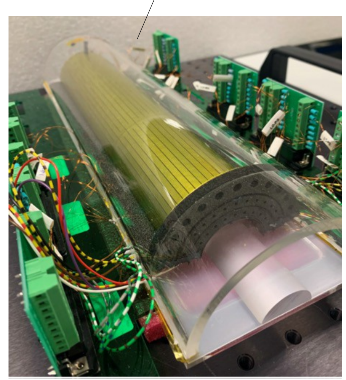
µITS3

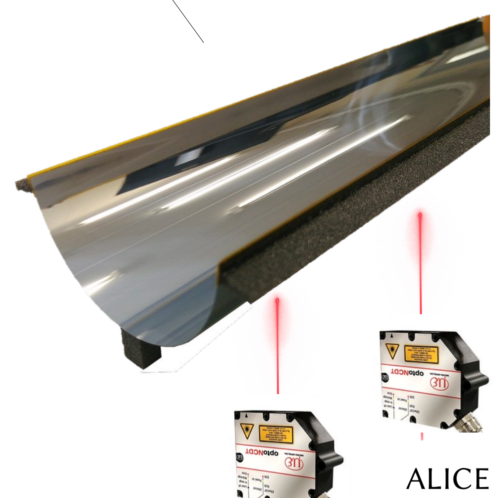




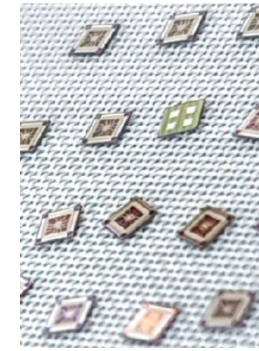
SuperALPIDE

B. Mechanical <u>integration</u> with carbon (foams as rings and longerons) + carbon exoskeleton, <u>cooling</u> tests ($\Delta T < 2\text{-}5$ K) + <u>vibration</u> measurements ($|\Delta d| < 0.5$ µm, at most so far)



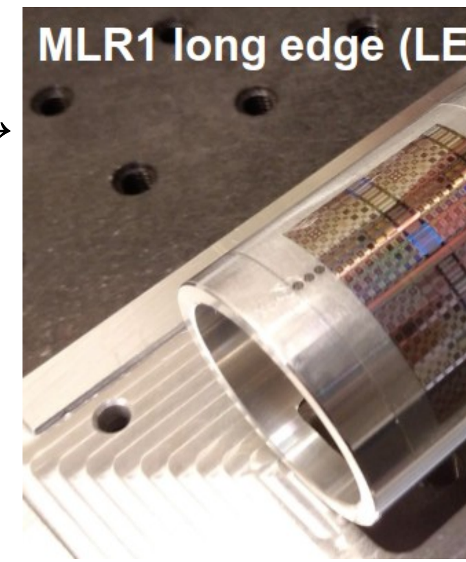


I.1 – ITS3 project : ALICE state of the art 2023-05

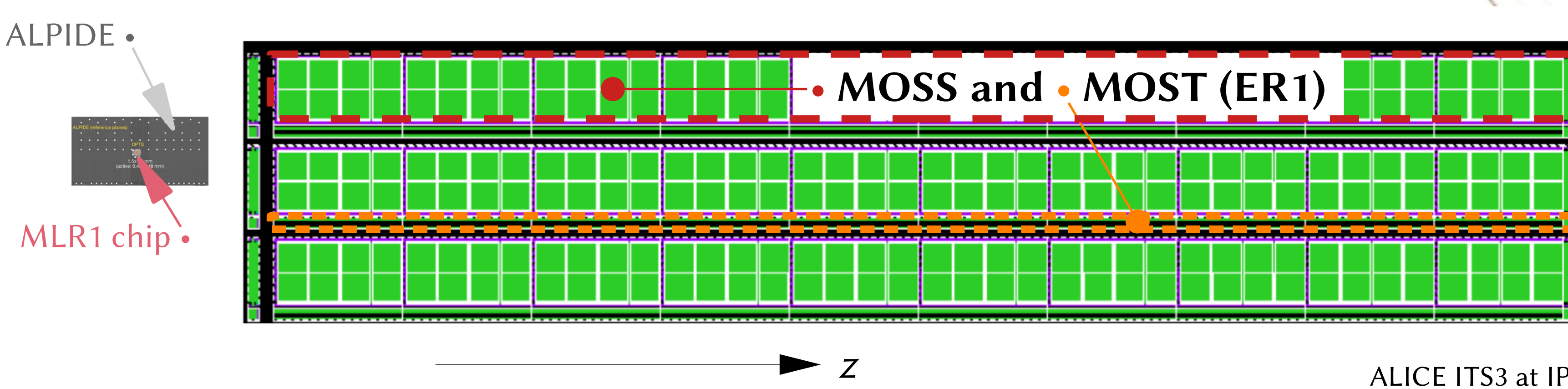


C. from 180-nm CMOS technology to **65-nm** (Tower foundry) :
⟶ 54 different chiplets from **MLR1** run ≈ APTS, DPTS (CERN) + CE65 (IPHC)

i) charge collection, **ok!**
ii) ε **> 99%**
iii) rad hard, **ok!**
iv) performances *after* bending 65-nm chiplets ? ⟶ ***ongoing*** ⟶

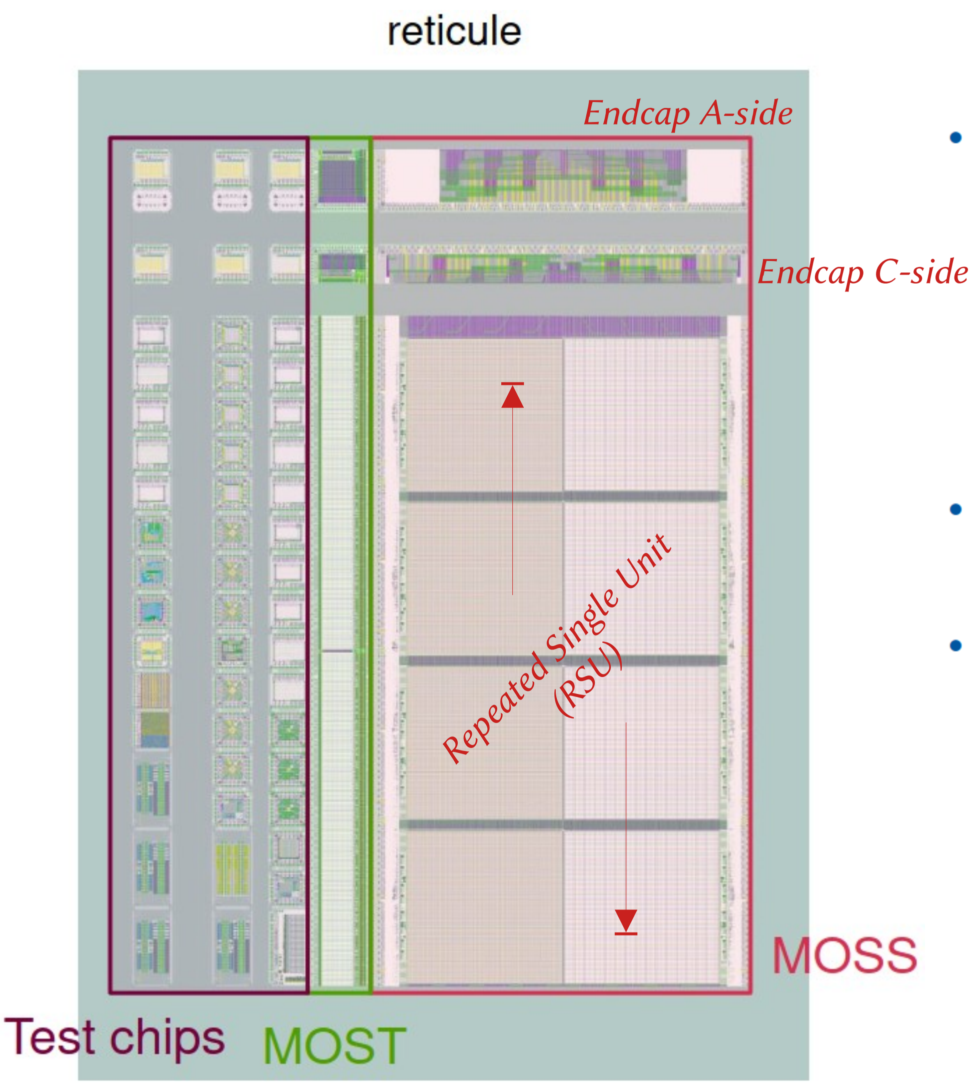


D. 1D **Stitching** *(along z direction)* : wafer-scale “chip” (≈1.4x26 cm²),
thinned (< 40 µm)



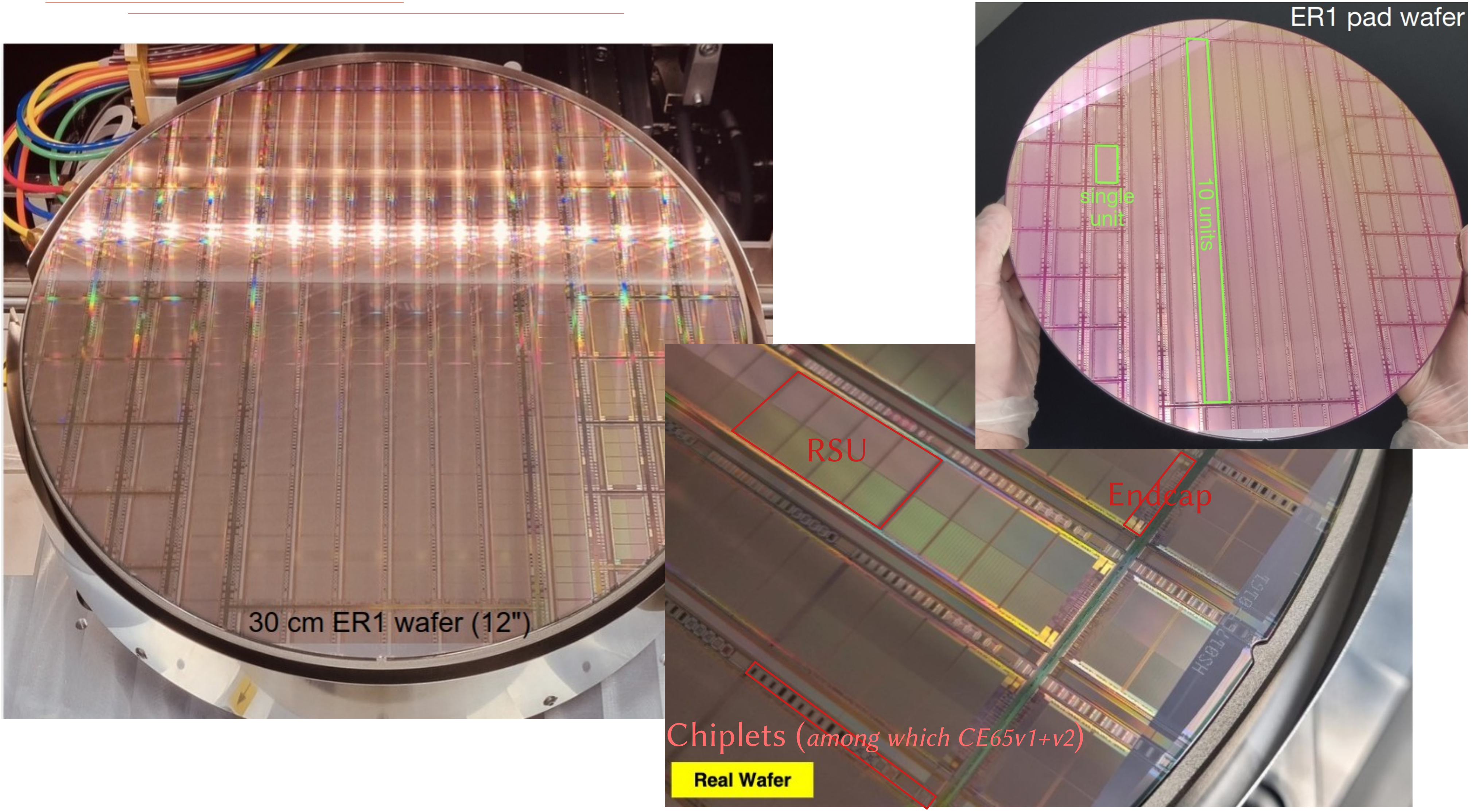
II.1 – Technical status : panel 1.a Design CMOS, ER1 status

WP1.2, CERN, Pedro Leitao, EP R&D day 2023

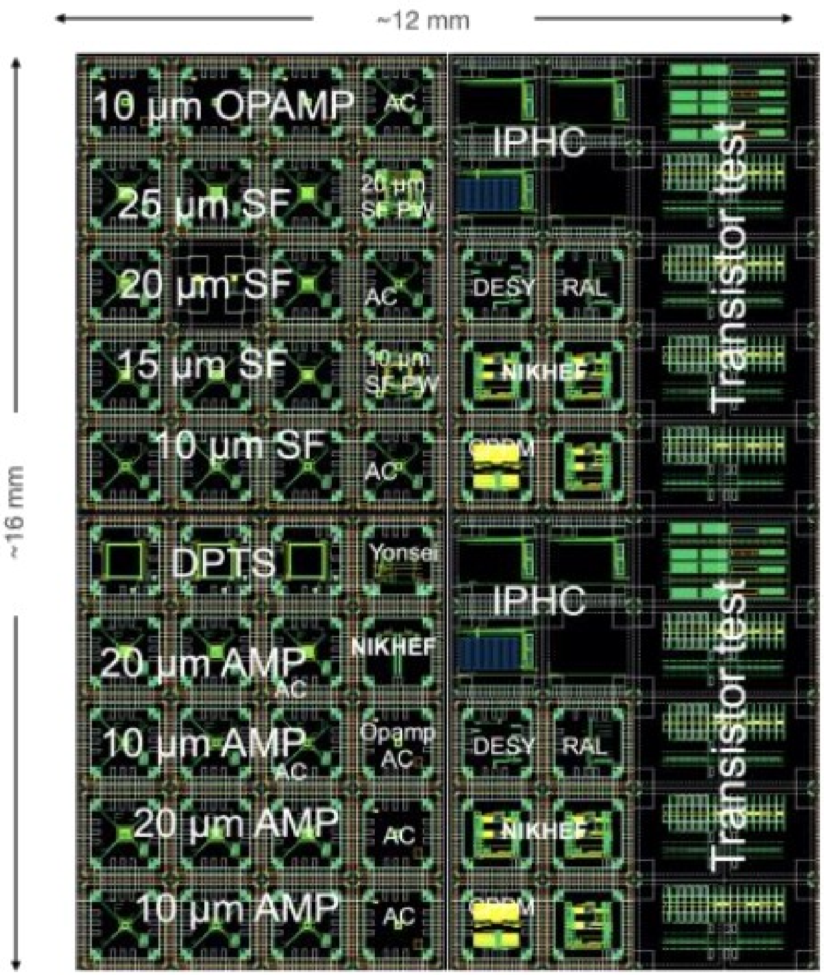


- Features two stitched sensor chips
  - MOSS chip (1.4 x 26 cm, 6x per wafer)
    - Conservative layout (DFM rules), Alpide-like readout scheme with 1/20 power segmentation
  - MOST chip (0.25 x 26 cm, 6x per wafer)
    - High local density with higher power gating granularity to mitigate faults, async hit driven readout
- Features 51/reticule chiplets for prototyping
  - PLL, pixel prototypes, fast serial links, SEU test chips, ...
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC deck
  - Custom DRC/LVS rule deck
  - Custom DFM standard cell library implemented
  - Setup of a legal and contractual framework
  - Develop wafer assembly and signoff methodology

II.1 – Technical status : panel 1.a CMOS design, ER1 status

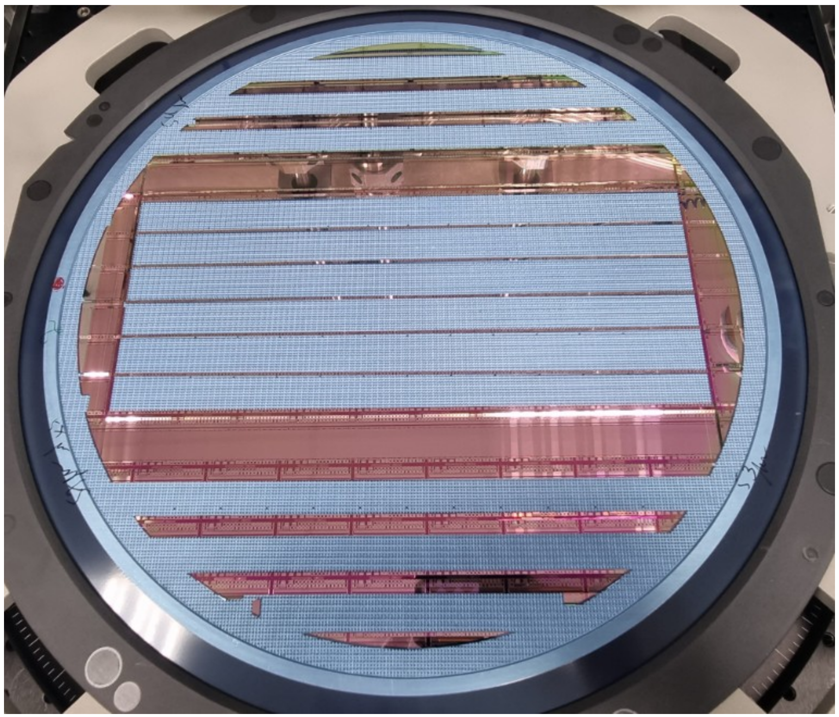


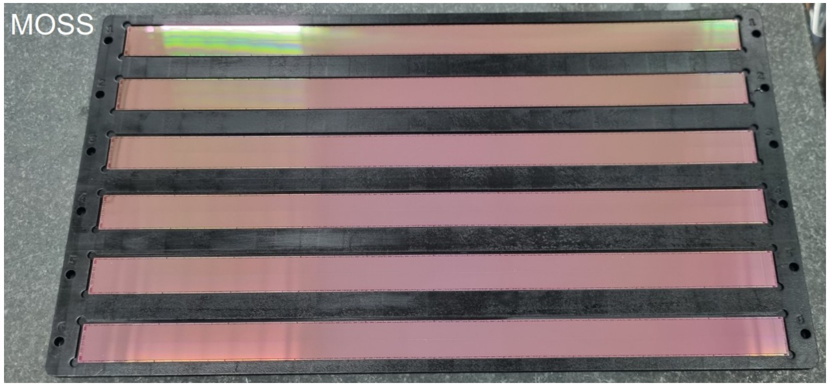
II.2 – Technical status : panel 1.b Test and qualification

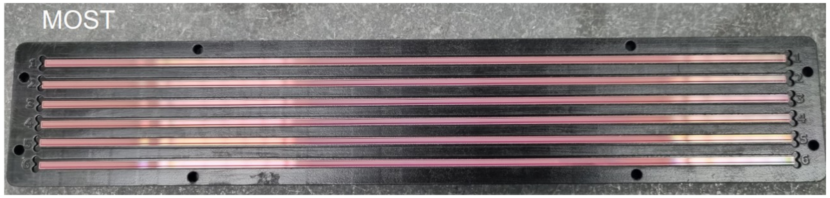


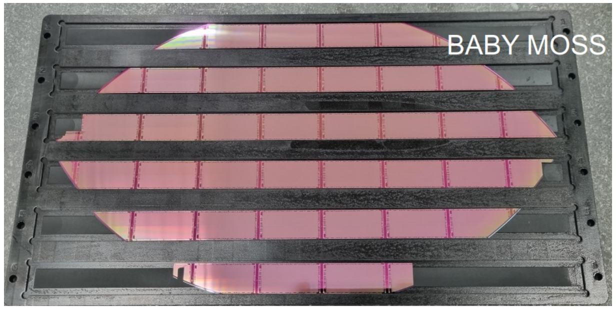
- Characterisation of bent ALPIDE (180 nm), **ok!**
  - ⟶ *arXiv:2105.13000*
- µITS3 under beams, **ok!**
  - ⟶ ongoing draft
- Analysis of MLR1 chiplets (TPSco 65 nm), with their variants, 0 radiation + irradiated ~done!
  - **CE65** v1 (IPHC C4π+PICSEL) **~done**
  - **DPTS** (CERN) **done + ok!**
    - ⟶ *arXiv:2212.08621*
    - process = modified with gaps 2.5 µm
    - pitch 15 µm / pixel matrix 32x32
    - ⟶ AxEff, ok!
    - ⟶ radiation hardness ok! (i.e. 99% with >10^{15} n_{eq} 1-MeV/cm² at 20°C)
    - ⟶ spatial resol° = 4-4.25 µm /
    - ⟶ cluster size ≈ 1-1.2 pixels/cluster
    - ⟶ time resol° ≈ 9 ns
  - **APTS** (CERN) **~done**
    - = investigations on charge collection

II.4 – Technical status : panel 3. Integration









ER1 Dicing and picking,
Mai 2023

NB: ER1 = 24 wafers,
i.e. 24 x6 MOSS, possible = 144 instances
+ 24 x6 MOST, possible

Antoine JUNIQUE (CERN)
+ Marc IMHOFF (IPHC)

II.4 – Technical status : panel 3. Integration

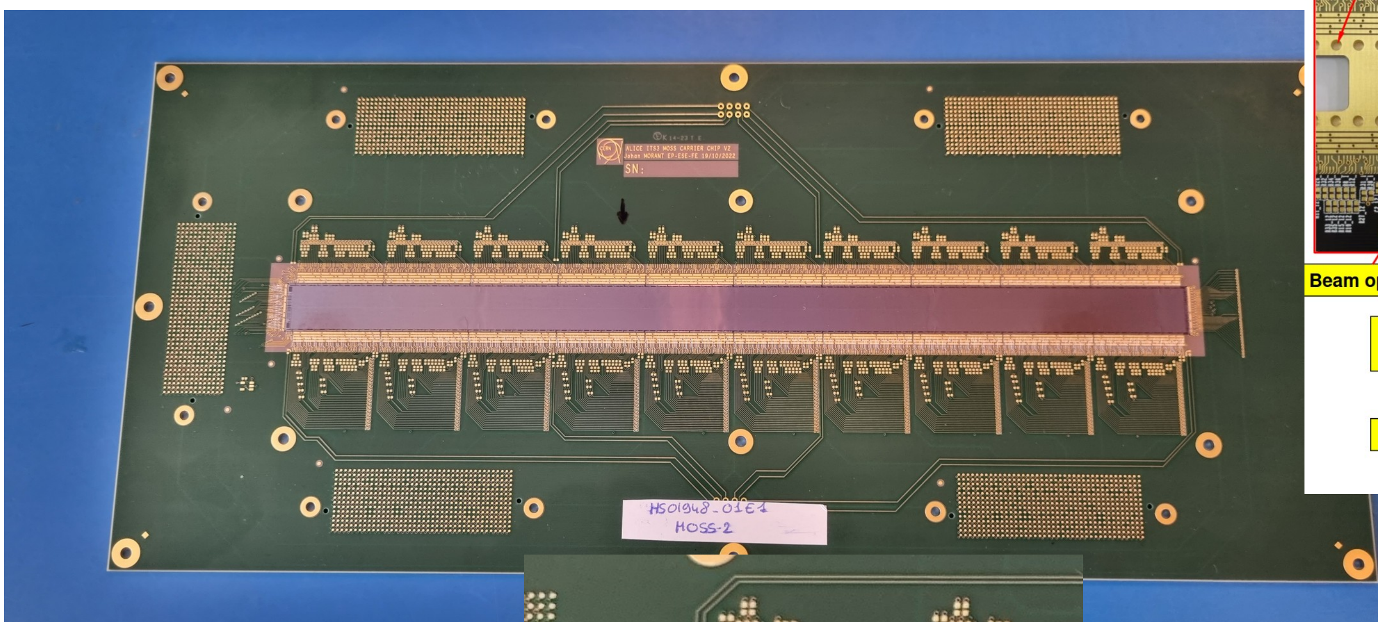
11 May 2023 :

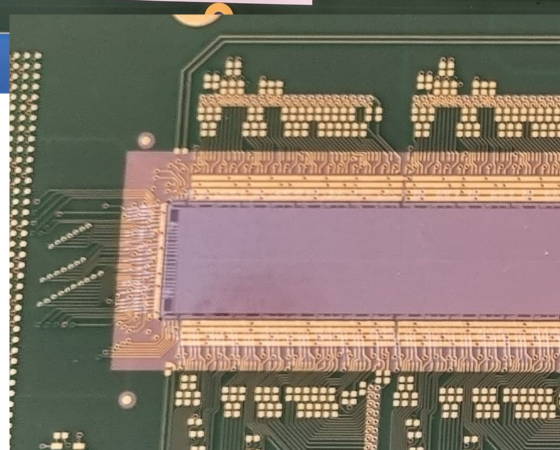
ER1 MOSS pad wafer (glued + bonded) on carrier board,

40 µm thick

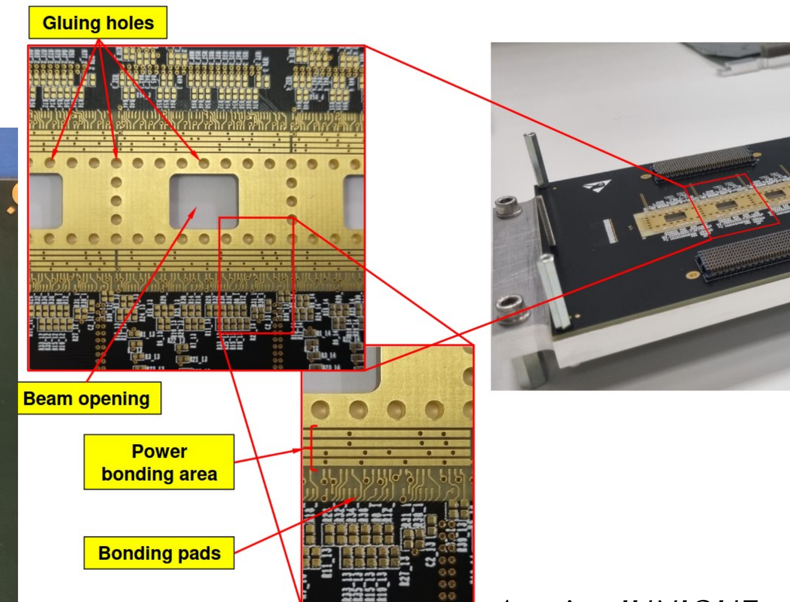
MOSS dimensions ≈ 1,4 x 25,9 cm²

2192 bonds (in 2x16 min...)





Marc IMHOFF
(Priv. com°)



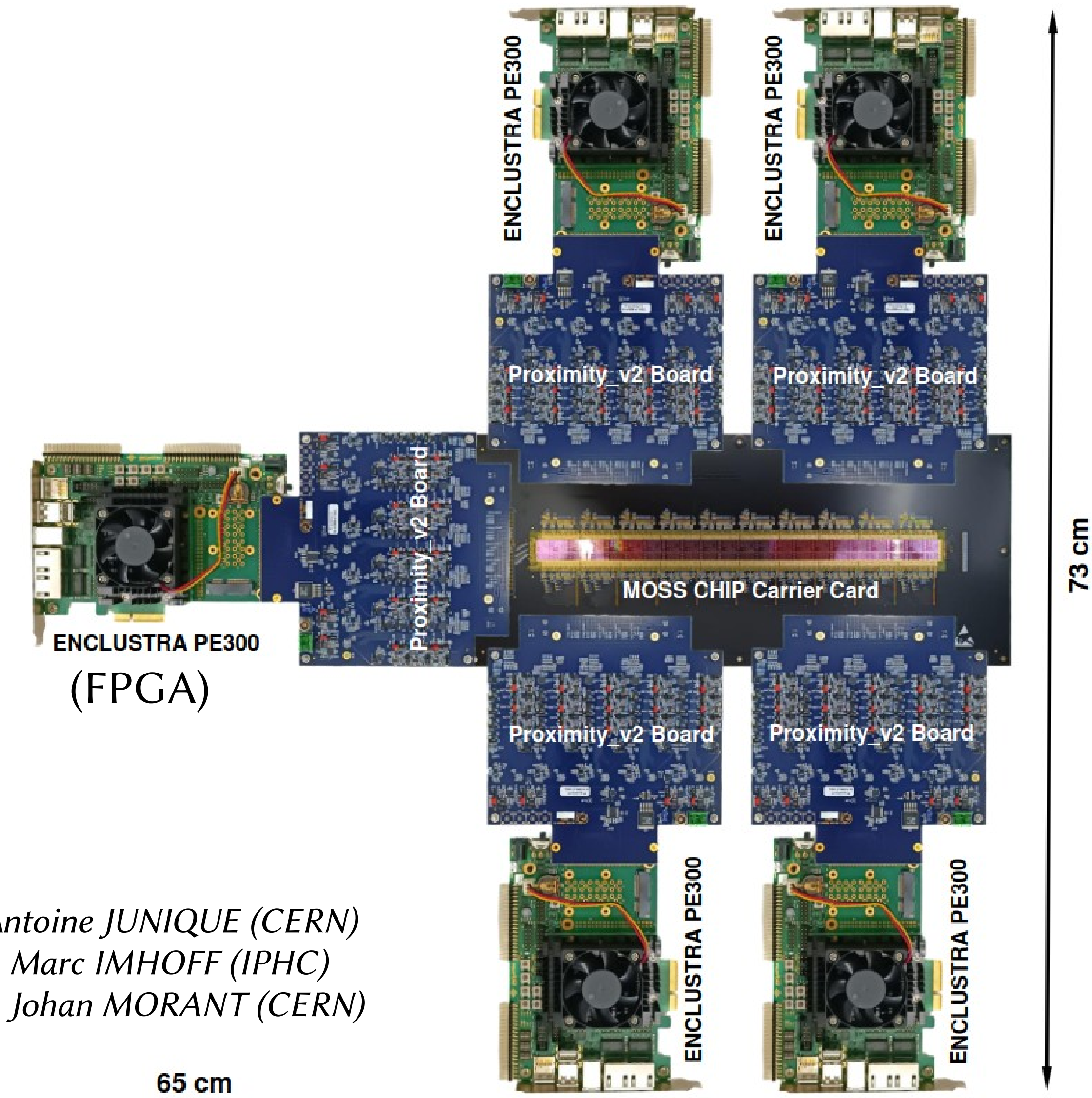
Antoine JUNIQUE,
ITS3 Plenary 2023-04

21 June 2023:

10 out of 12 ER1-MOSS sensors mounted on carrier board,
⟶ ready for test (beams)

II.4 – Technical status : panel 3. Integration

ER1-specific card for (DAQ + Slow Control + Powering) of MOSS ER1



Antoine JUNIQUE (CERN)
+ Marc IMHOFF (IPHC)
+ Johan MORANT (CERN)

Remarks :

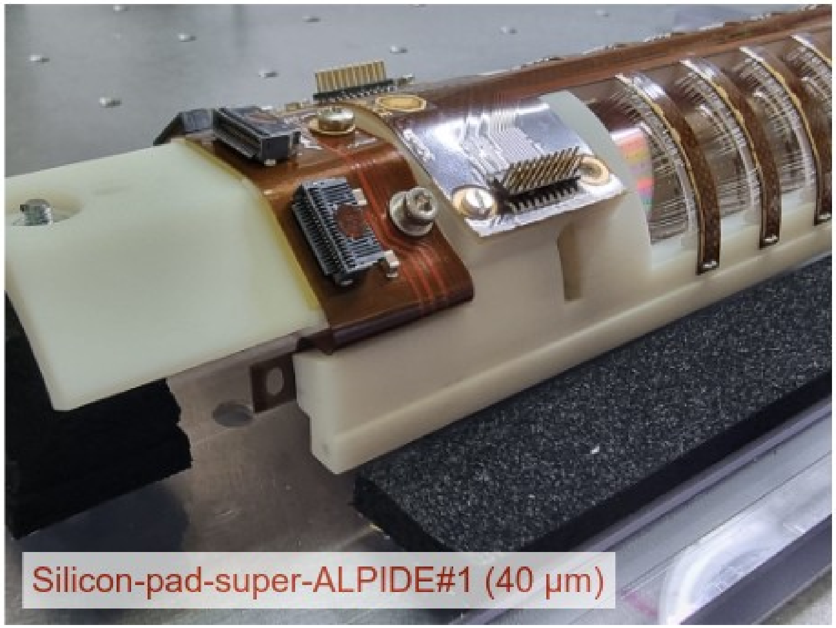
- Carrrier board with MOSS,
  = the part that can interchange
  - 10 mounted, (2023-June-21),
    target: ≥5 with functional MOSS
    (= *tests in view of TDR...*)
  - ∃ possibilities for 50 carrier boards
    (components = available)

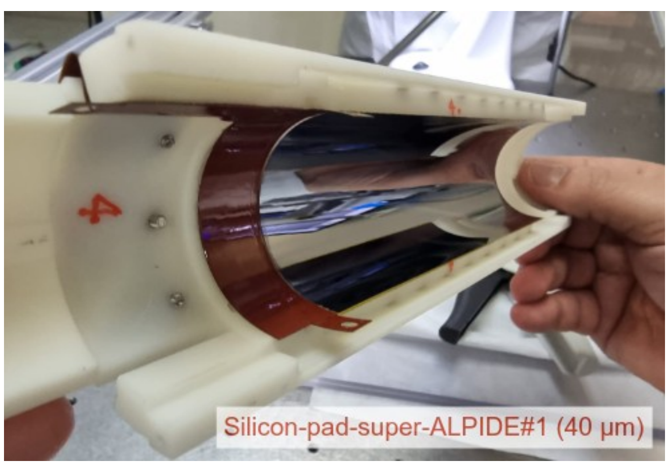
- Proximity board + ENCLUSTRA
  = only few pieces, $O[5]$

Usage :

- tests in labs (sources, probes)
- tests under beam over summer
  (4 beam-test session possible up to Oct. 2023)

II.5 – Technical status : panel 4. SuperALPIDE





r_{Layer}(SuperALPIDE) ≈ [6 cm]/π ≈ 1,91 cm
L_z(2 SuperALPIDE) = 2 x 14 cm
i.e. compatible r_{L0}(ITS3) and $L_{z,L0}$(ITS3)

ok! Bending of *blank* silicon (Bari, IPHC)
ok! + Bonding on "*pad wafers*", thinned to 40 µm thickness
= 2 SuperALPIDE of that kind, already done (Bari) with 710 bonds (with 94% = success)

⟶ *i.e.* proof of mechanical feasibility

ToDo : same achievements but now with *functional* (super)ALPIDEs

Remarks :

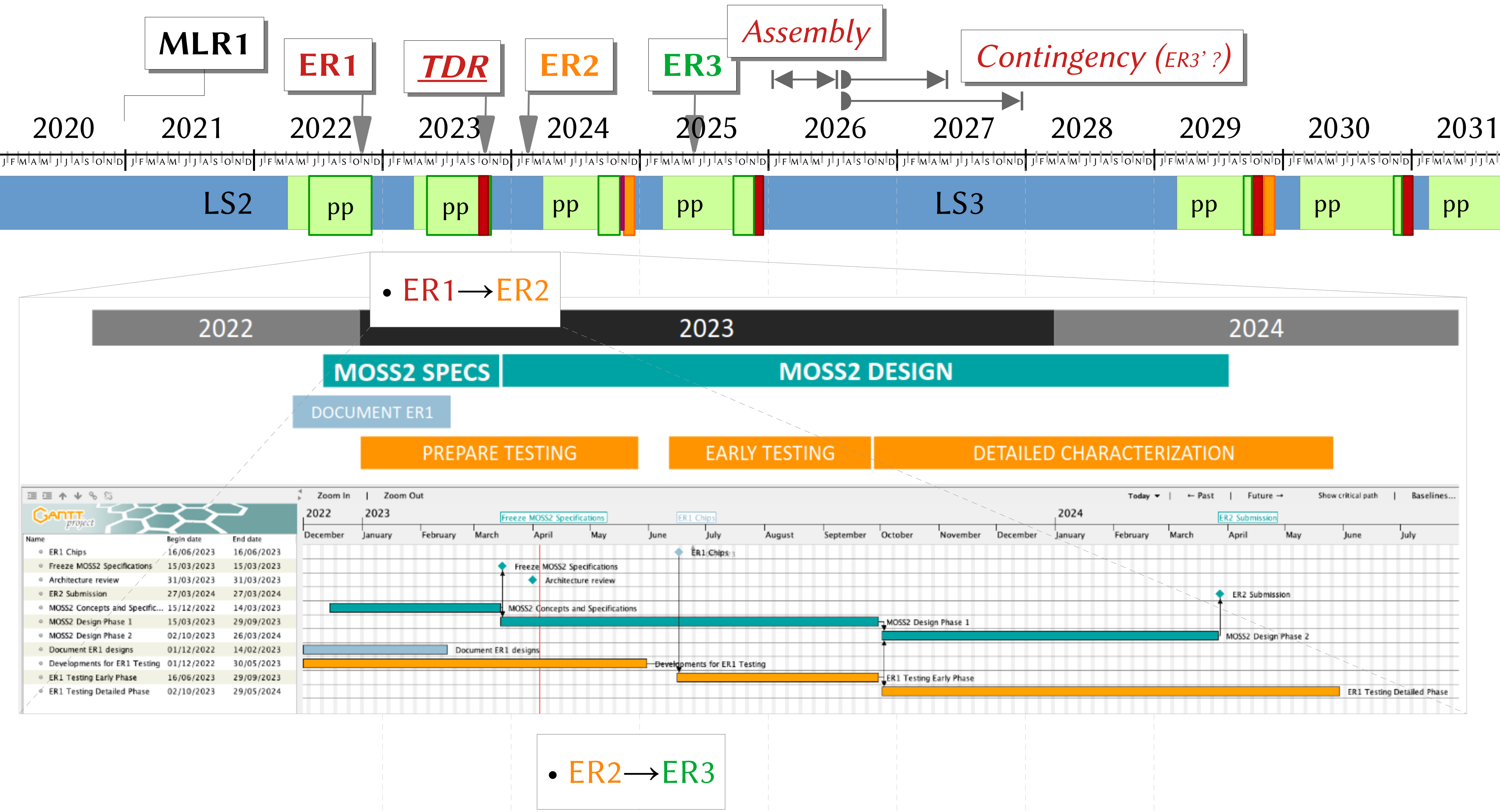
- minimal inter-pad distance ≈100 µm
- mechanical constraints, longest bonds
  - ≈ 4 mm (FPC perihpery)
  - ≈ 15 mm (exo-FPC)

Domenico Collela, WP4 ITS3 plenary 2023-05

Back to main TOC

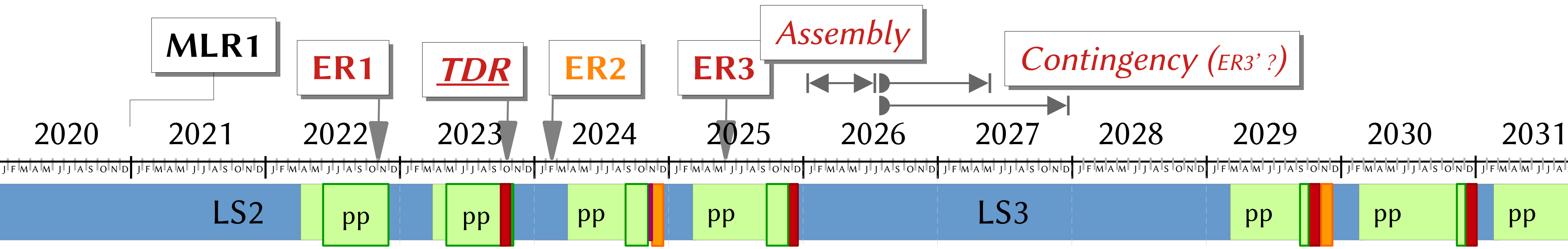
Part D – Calendars & Gantt planning

I.1 – Gantt : 1.a CMOS design of sensor



Name	Begin date	End date
ER1 Chips	16/06/2023	16/06/2023
Freeze MOSS2 Specifications	15/03/2023	15/03/2023
Architecture review	31/03/2023	31/03/2023
ER2 Submission	27/03/2024	27/03/2024
MOSS2 Concepts and Specific...	15/12/2022	14/03/2023
MOSS2 Design Phase 1	15/03/2023	29/09/2023
MOSS2 Design Phase 2	02/10/2023	26/03/2024
Document ER1 designs	01/12/2022	14/02/2023
Developments for ER1 Testing	01/12/2022	30/05/2023
ER1 Testing Early Phase	16/06/2023	29/09/2023
ER1 Testing Detailed Phase	02/10/2023	29/05/2024

I.2 – Gantt : 1.b Tests and qualification of sensors



Tests of ER1 stitched sensors + chiplets

Tests of ER2 stitched sensors + few chiplets

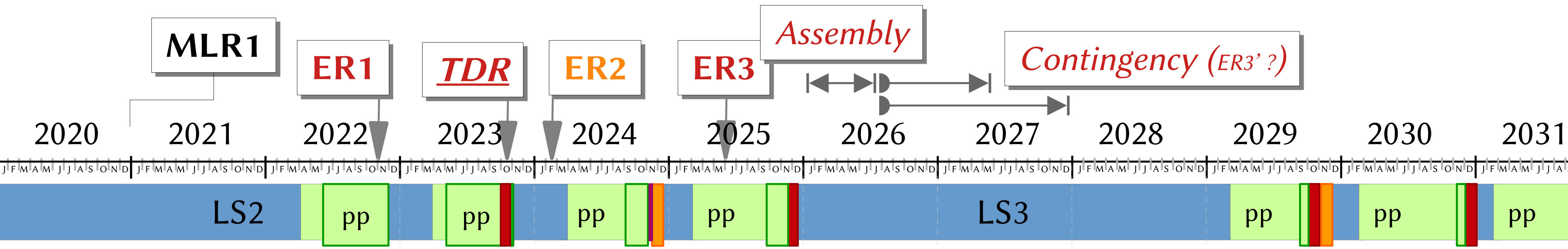
- Qualification of the segments of MOSS3 ER3

Assembly

Delivery / commissioning of ITS3
(at ground-floor *installation*)

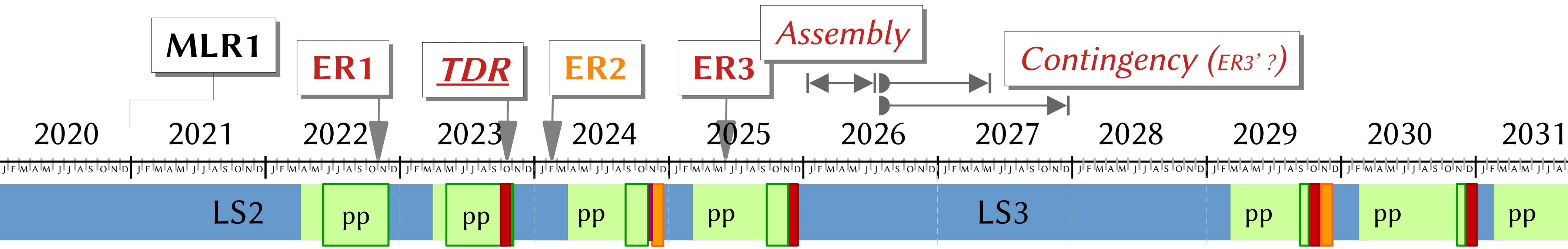
Tests = in synchronisation with ERx returns from foundry
i.e. ≈ (tape-out date + 6-month cycle)

I.3 – Gantt : 3. Integration



- Card (DAQ/power/SlowControl) for ER1 MOSS1
- Mounting on *Carrier Board* for ER1 MOSS1
- Mounting on *Carrier Board* for ER2 MOSS2 (*with Grenoble DSB*)
- Mounting of an ITS3-like prototype with ER2 MOSS2
- Wafer qualification of ER3 MOSS3
- *Assembly* of ITS3 with qualified ER3 MOSS3
- Ground-floor installation / moving of ITS3 to ALICE exp. point
- ITS3 installation down the pit

I.4 – Gantt : 4. “SuperALPIDE”



- Assembly with 2x9 *dummy* ALPIDEs (180nm)
- Assembly with 2x9 *functional* ALPIDEs (180nm)
- *Bending+bonding with babyMOSS2 (65nm) ?*

Back to main TOC

Part E – Human resources

II.1 – IPHC HR costs : 1.a CMOS design for pixel matrix

C4π

RH IPHC :

(4±0.5) FTE/year C4π , 4 years, [2022-2026[(*i.e.* post ER3),
with an overhaul at 2026 horizon, for possible prolongation (*e.g.* if calendar drift)

distributed over 7 permanent-staff engineers :

- analogists (*charge collection, in-pixel electronics of "very front-end"*) :
  Andrei DOROKHOV, Isabelle VALIN
  + one PhD student (Corentin LEMOINE, co-direction CERN+IPHC, based at CERN)

- numericists (*in-matrix digital treatment and power management*) :
  Frédéric MOREL, Xiaochao FANG, Grégory BERTOLONE, Abdelkader HIMMI,
  + one PhD student (for now, Jean SOUDIER, based at IPHC)

Remark : (4-5 FTE) ≈ 50% of the workforce into the ITS3 project on the CMOS design front
+ ≈ 50% left, at CERN

II.2 – IPHC HR costs : 1.b Tests and qualification of sensors

PICSEL

RH IPHC :

(*NB* : ≠ tests CE65v2 ∈ PICSEL/GRAM, *cf.* 0,5 FTE Kimmo)

- **≈ $0^{+0.1}$ ETP C4π, 3 ans, [2024-2026]**
  Test of MOSS1 (1,4 x 26 cm²) ≈ impossible as it is
  ⟶ current probe machine for tests, too small
  i.e. no 30-cm-diameter plate to host 65-nm wafers of such diameter
  ⟶ need a dedicated purchase in the long run (e.g. via CPER ? + Help IN2P3 ?)

- **($0{,}5^{+0{,}2}$) ETP/year PICSEL, 6 years [2021-2026]**
  = responsibility of WP3 - [Test and qualification] (Serhiy SENYUKOV)
  + Tests of CE65 prototypes (laboratory + beam tests)
  + in-house Lab tests on SuperALPIDE
  ⟶ Overhaul of a contribution extension in 2026 (gr. ALICE / gr. PICSEL)

NB : privileged partnership initiated on CE65 sensor tests
with Univ. Tsukuba+KEK, Japan (via FJPPL)

II.3 – IPHC HR costs : 3. Integration

ALICE IPHC

RH IPHC :

0.8 FTE/year ALICE, 6 years, [2023-2028]
= Marc IMHOFF, ∈ "transversal" trinom at CERN
[2 engineers: MI + Antoine JUNIQUE (CERN), + 1 technician : Johan MORANT (CERN)]

In practice : mission of 1 week/month at CERN
with ponctual intensive periods at CERN
(*e.g.* 2 months full time at CERN for mounting ER1-MOSS1 on carrier board)

II.4 – IPHC HR costs : 4. “SuperALPIDE”

C4π

RH IPHC :

0.5 FTE/an C4π, 4 years, [2023-2026]
⟶ activity rather on the R&D side, on *bending* + *bonding* of MAPS,
centred on the achievement of SuperALPIDE
distributed over the 3 persons of the µTechnique pole of the platform :
Franck AGNESE, Olivier CLAUSSE (bending)
+ Christophe WABNITZ (bonding)

⟶ uncertainty linked to the duration of this contribution
= function of real need of SuperALPIDE for ITS3 + R&D progress on bending

Back to main TOC

Partie F – Conclusions

Conclusion : ITS3 triangulation

ITS3 = unprecedented physics roads open for ALICE :
hyper-granular, ultra-light, proximity to beam line.

i.e. “finer, lighter, closer, cooler, (faster?) … better”

Peculiarities of the ITS3 project

- a continuous R&D project : ~R&D only, no real construction phase per se.
- small surface to be equipped
- tightly bound logic of design, making (mechanic design + sensor designs + physics perf.) closely intertwined

IPHC in ITS3 ⟶

- Expertises in Strasbourg known, identified and recognised within the ALICE Collaboration :
  MAPS design (C4π, PICSEL), integration (the 3 teams) + tracking, data analysis (ALICE-IPHC)
  ⟶ Something to build further upon.
- ITS3 project approached since its early stages (C4π/PICSEL, 2019)
  ⟶ Strategic roles offered, on time and in position to take them
- task share at IN2P3 : a consistent global set, with factorisation of the tasks ≈ [IPHC // LPSC]

ITS3 at IPHC ⟵

- Local synergies among MAPS-based projects at IPHC : 65-nm technology node, stitching, bending, …

Appendices

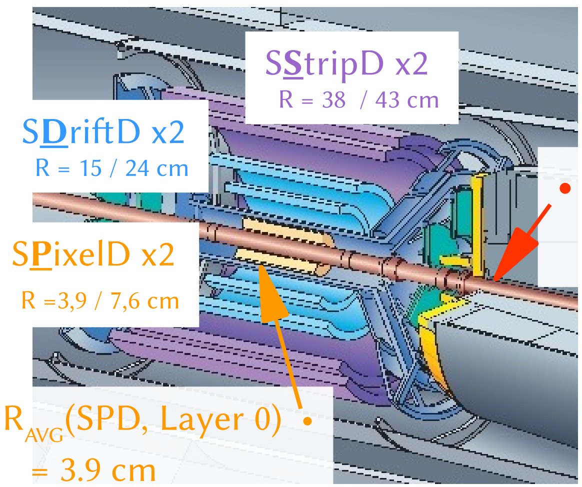
Back to App. TOC

App. A – ITS**2** + MFT

TDR ITS Upgrade
- CERN-LHCC-2013-024

A.1 – ITS2 : from ITS1 to ITS2

ITS Runs 1+2

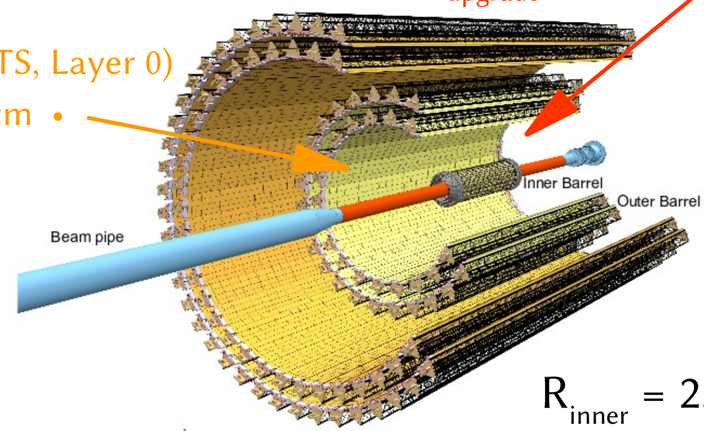


3 technologies : pixels, drifts, strips
6 layers

- x/X_0 (per layer) ≥ 1.1%

→ x/X_0 (ITS1) ~ 7.4%

ITS upgrade Runs 3+4

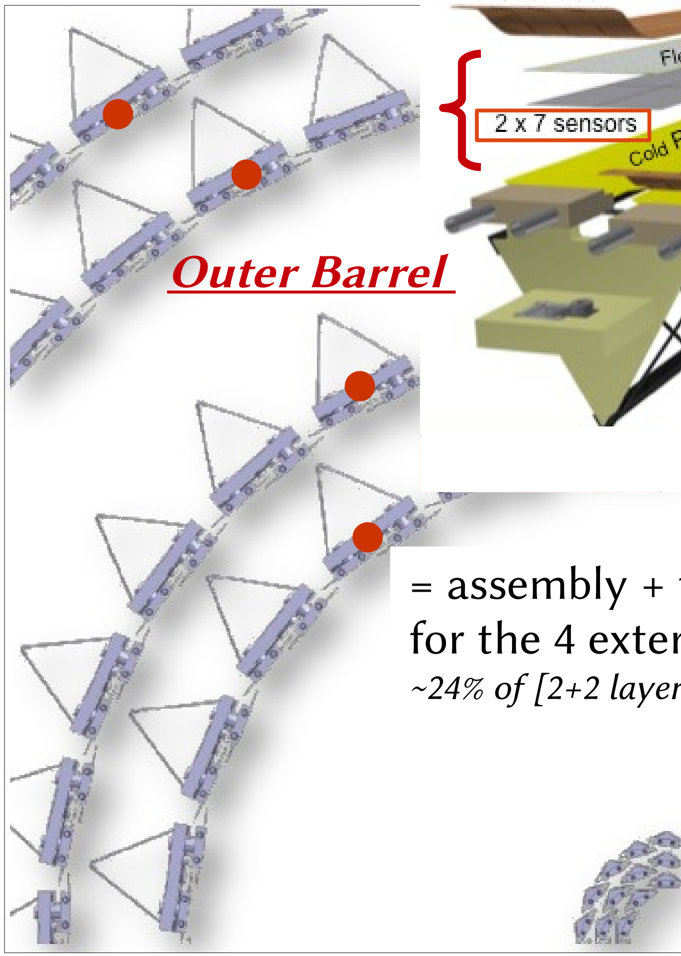


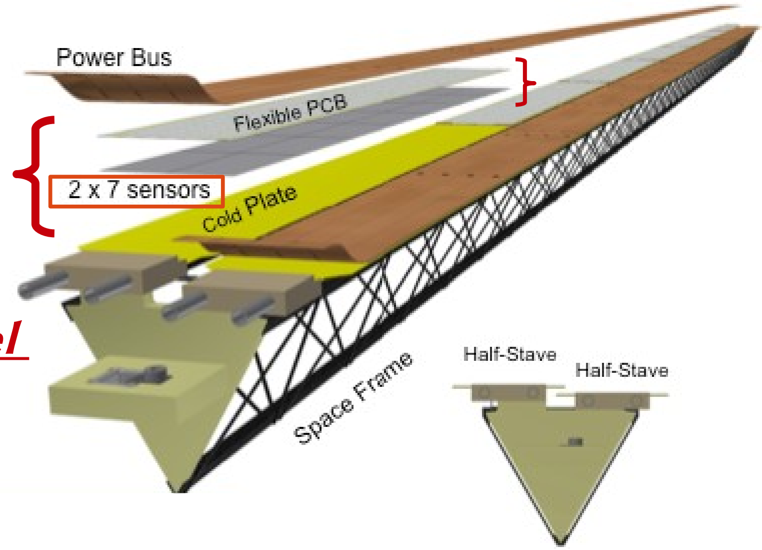
Single technology : CMOS (ALPIDE)
7 layers

- IB, Layer 0,1,2 : x/X_0(per layer) ~0.35%
- OB, Layer 3,4,5,6 : x/X_0(per layer) ~0.85%

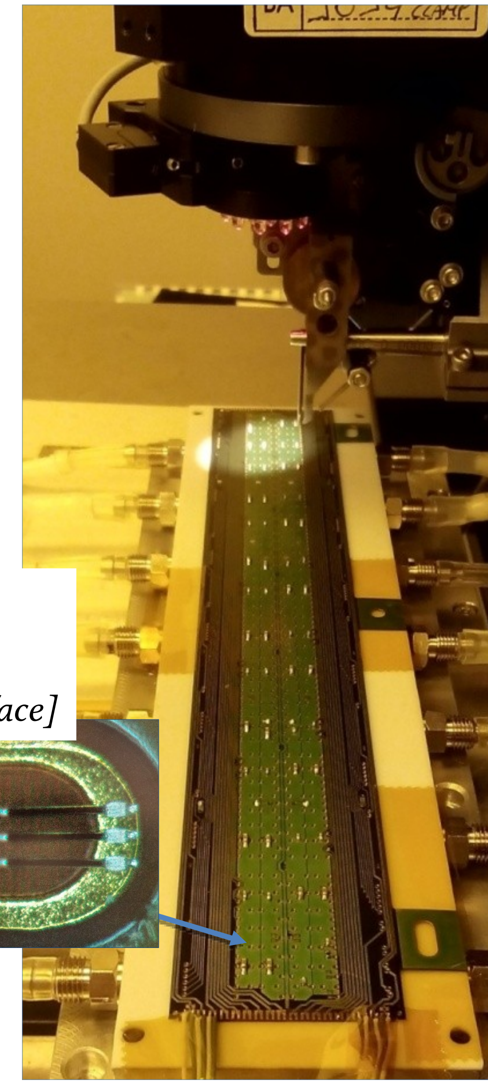
→ x/X_0 (ITS2) ~ 6.9%

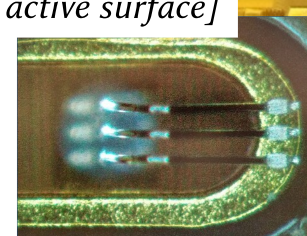
A.2 – ITS2 : instrumentation, assembly ITS2





= assembly + tests of 2x7 CMOS sensors
for the 4 external layers of the ITS2 (out of 7 layers)
~24% of [2+2 layers = 2.3 + 6.9 m² = 25% +73% of the total active surface]





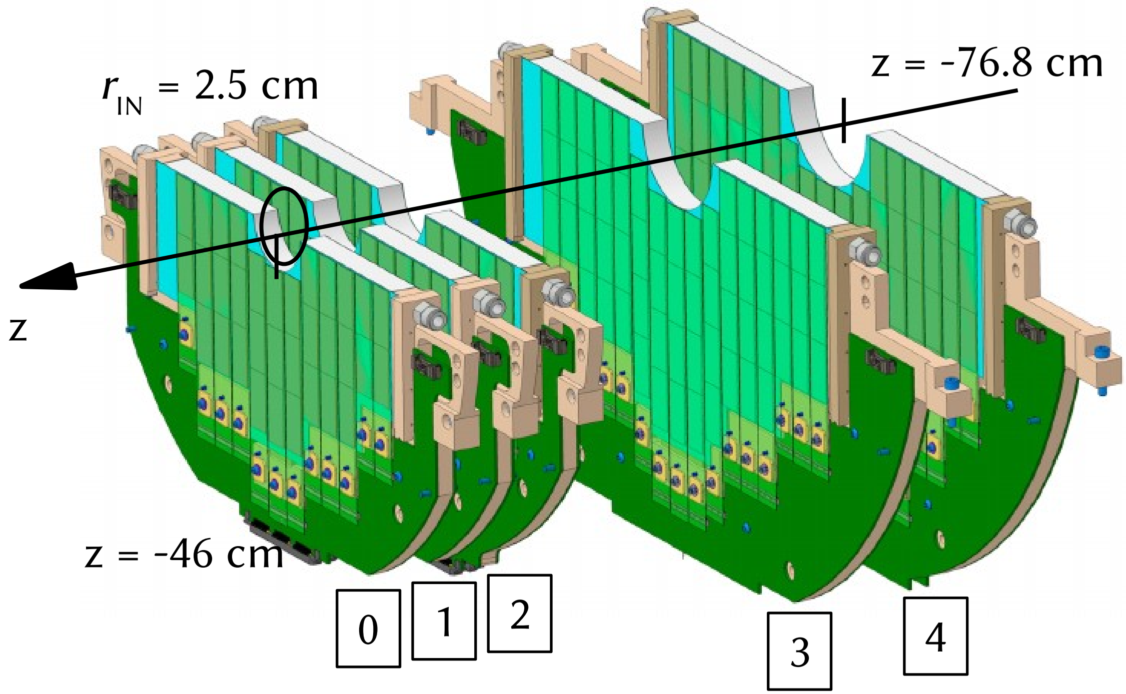
Bonding : YouTube

1. Production of ~585 modules (=25% of the total) (2017-11-2019-05)
2. Commissioning (2019-2021)
3. Data taking (2021-)

A.3 – MFT : layout

MFT = vertexing ahead of μ spectrometer
$-3.6 < \eta < -2.5$

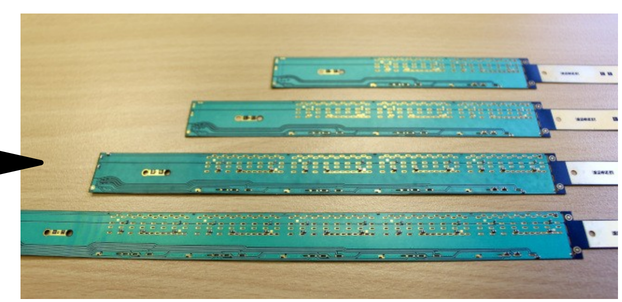
(NB : in front of absorber,
no sensitive magnetic field)



Components :

5 disks split into 2 halves
each disk = 2 sides of detection

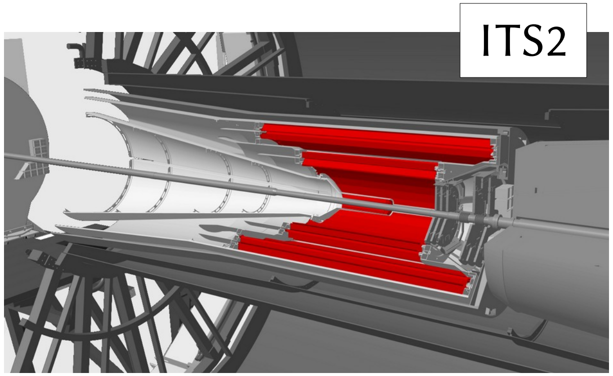
280 ladders out of 920 silicon sensors (2 to 5 chips/ladder) •



0.6 % x/X^0 per disk

NB : MFT doses (700 krad) over 10 years of operation,
~same ballpark as ITS inner layer

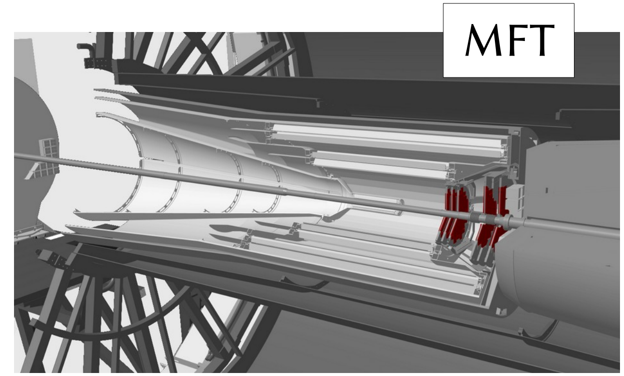
A.4 – ITS2+MFT : ALICE-France MAPS commitments

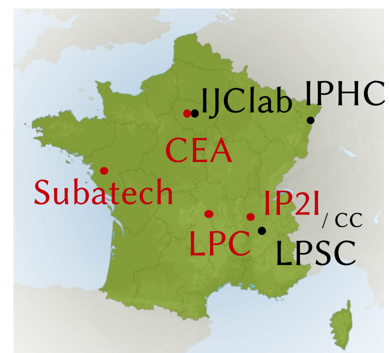


Total cost :
15.4 MCHF

In2p3 :
≈ 800 k€

LPSC : • assembly tool
IPHC : • module assembly
585 modules /~2500
(*2x7 chips glued, bonded on flexible circuit*)
• Coordination WG tracking/simul°/phys perf.





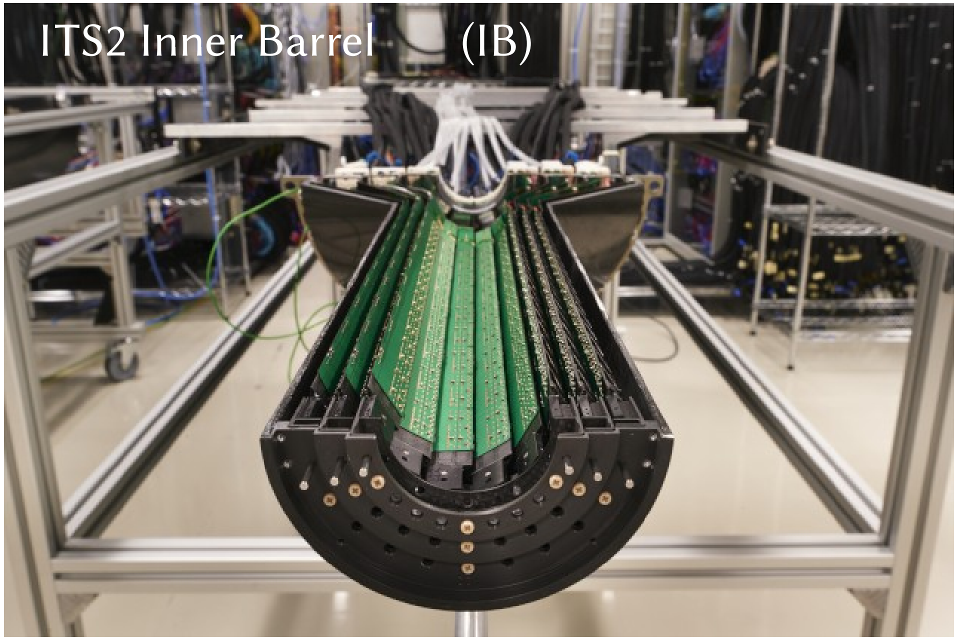
Total cost :
3.35 MCHF

In2p3 :
≈ 1.4 M€

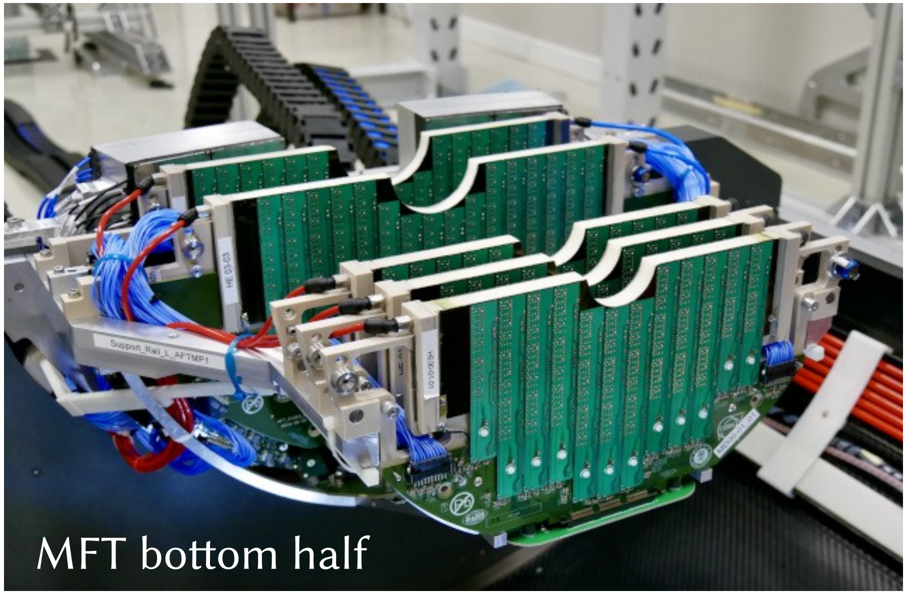
• Project leader
• Full detector construction
→ 8 out of 9 WG led by In2p3/CEA staff
• Coordination WG tracking/simul°/phys perf.

+ Read-out firmware of Common Readout Unit CRU (LPSC)

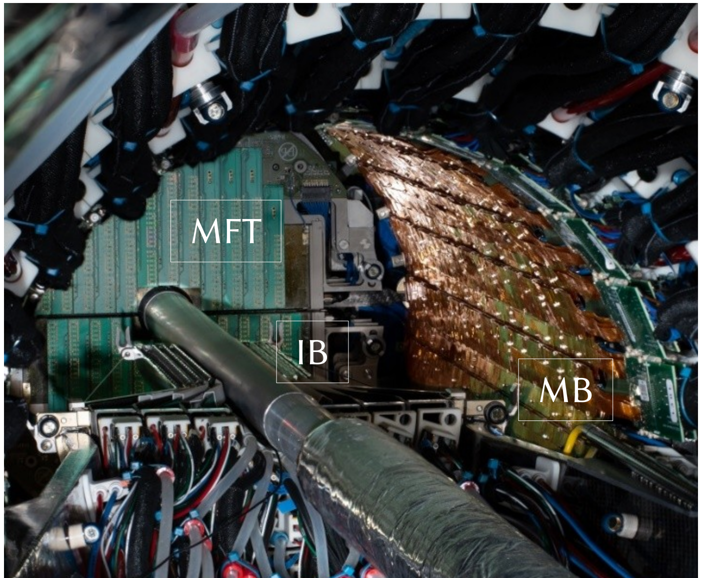
A.5 – ITS2+MFT : pictures



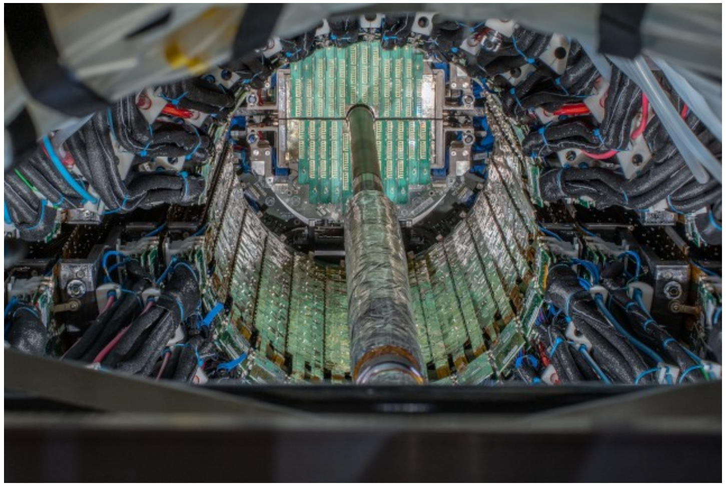
ALICE-PHO-GEN-2021-002



OPEN-PHO-EXP-2020-004



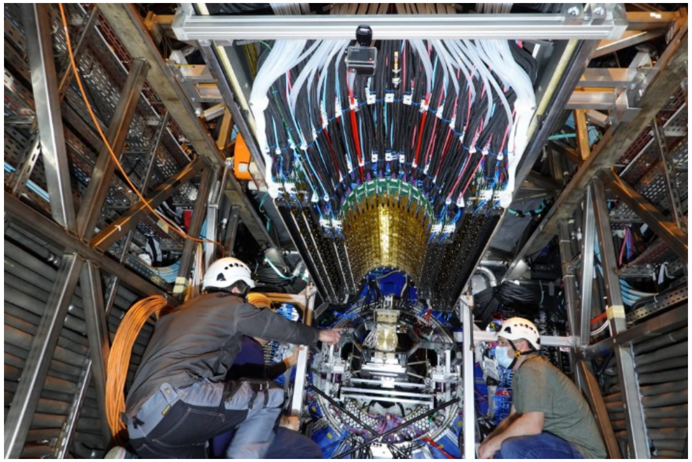
ALICE-PHO-GEN-2021-002



ALICE-PHO-ITS-2021-002

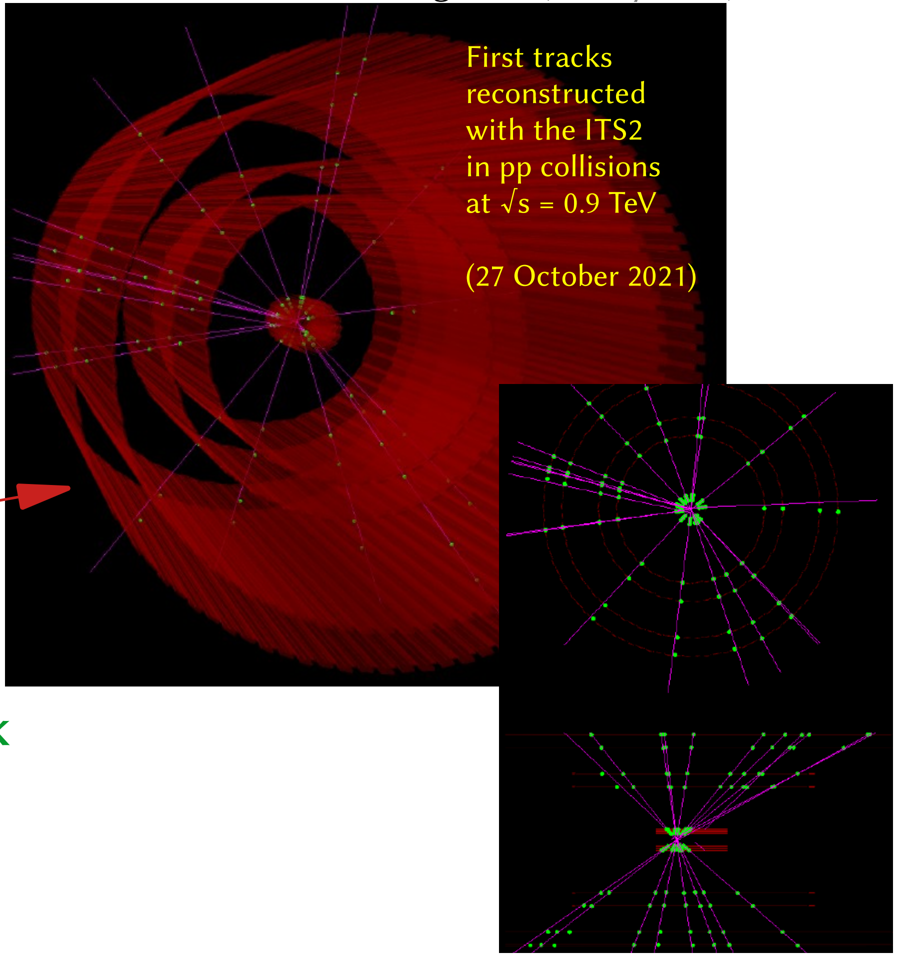
A.6 – ITS2 : installation+commissioning

ITS2 installation at LHC Point 2 (Jan. to May 2021)



- *Global commissioning ALICE* *(≥ July 2021)*
- *LHC pilot beam test* *(18-31 October 2021)*
- *Proton beams at 6,8 TeV* *(25 April 2022)*
- *Stable collisions pp $\sqrt{s}$ = 13,6 TeV* *(July 2022)*

Commisioning ITS2 (≥ May 2021)



Status point

- Power supplies, readout, Detector Control System, Cooling: **OK**
- Reconstruction algorithms + simulations, calibration: **OK**
  - . Acceptance (operational modules): **> 98%**
  - . Detection efficiency **> 99%** on average
- **Alignment:** 1st version + improvements, ongoing

Responsabilities ALICE-IPHC :

a) Coordination of the development/installation of **detector control system** and **cooling** for **ITS2**

b) **Installation** of readout electronics and detector cabling

A.7 – MFT : installation+commissioning

Back to App. TOC

App. B – ALPIDE chip

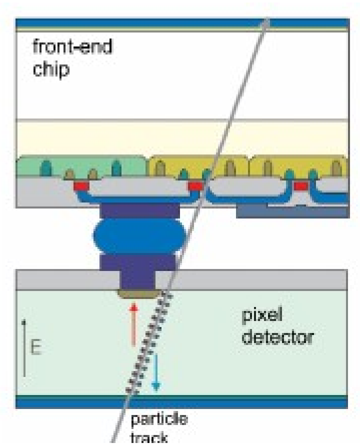
B.1 – Pixel detectors : Monolithic Active vs Hybrid techno.

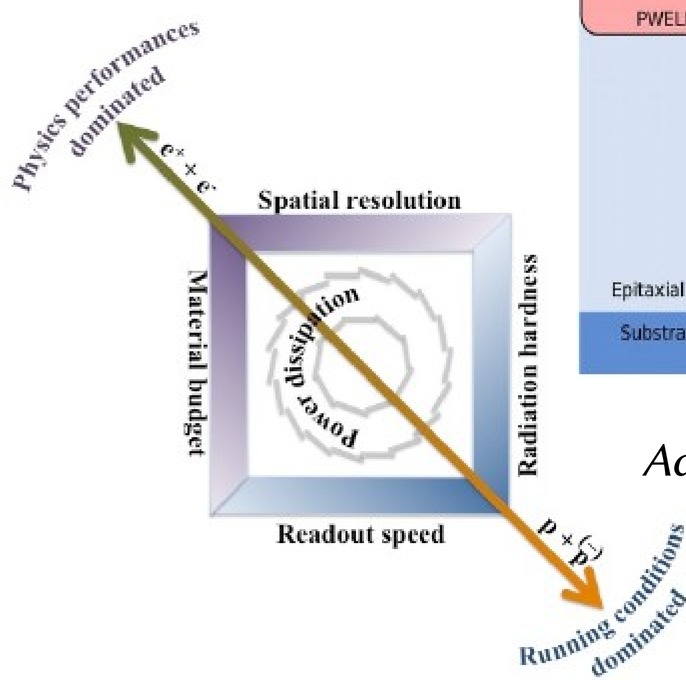
sens. layer ➡ q-collect ➡ ampli ➡ analog treat ➡ A-D conv ➡ digital proc

Hybrid pixel sensor ⟶ **sensor:** [bar] **+FEE** [bar]

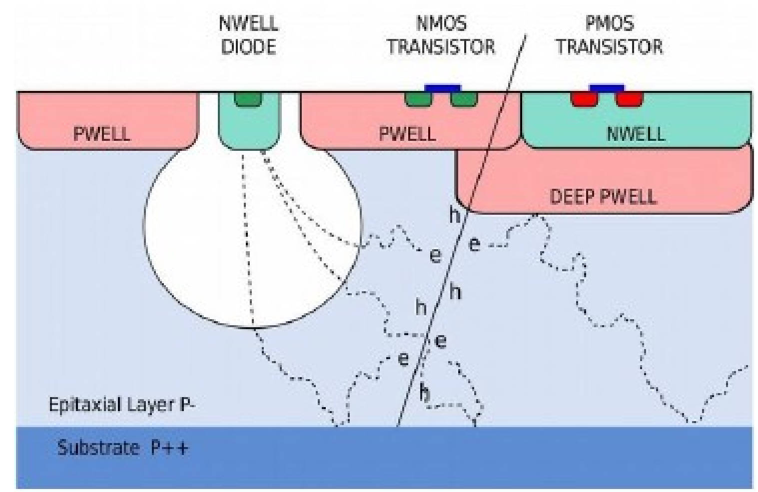
CMOS pixel sensor ⟶ **CPS:** [bar]

<u>Hybrid pixel sensor</u>





<u>CMOS pixel sensor</u>



Advantages :

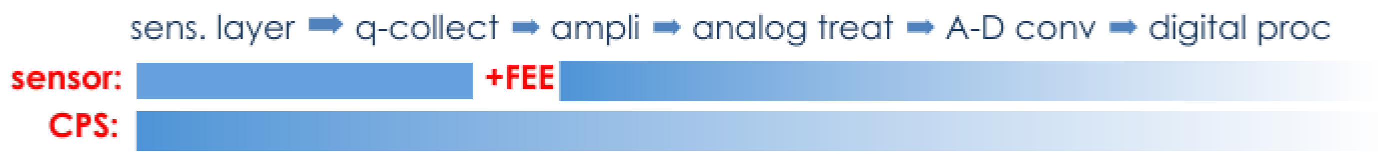
- faster readout
- better radiation-hardness
- ...

Advantages :

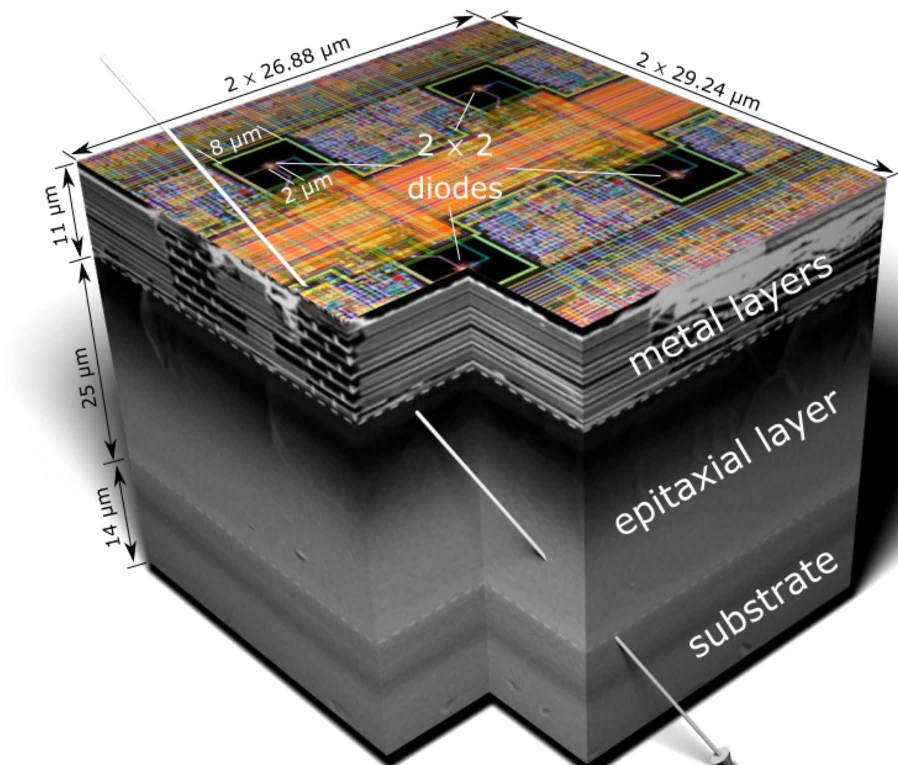
- thinner
- smaller pixel size accessible
- lower power consumption
- cheaper
- ...

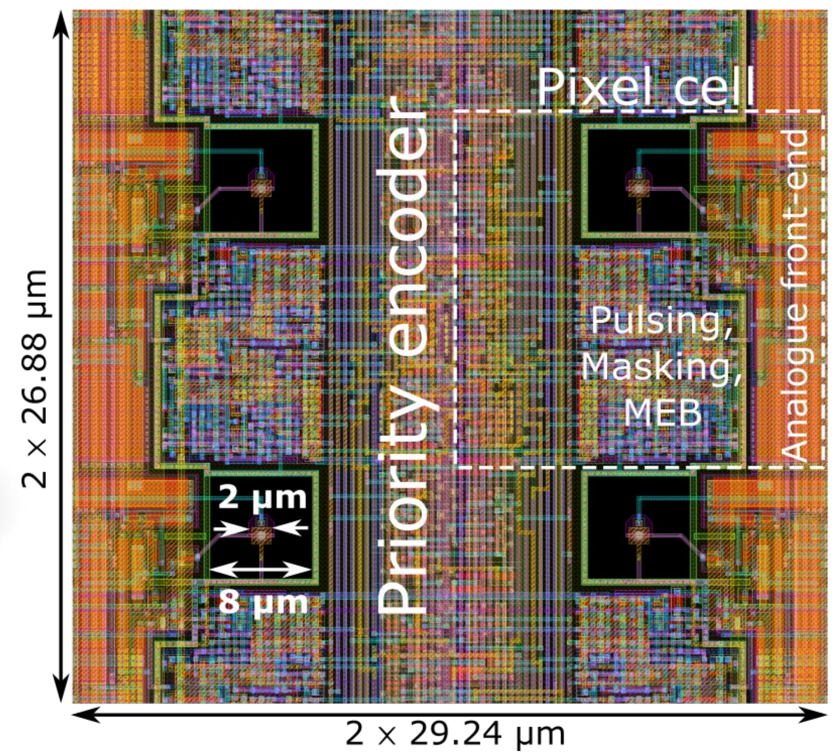
B.1 – Background: MAPS instrumental background

Hybrid pixel sensor ⟶
CMOS pixel sensor ⟶



Ex: sensor using
TowerSemiconductor 180-nm CMOS Imaging Process

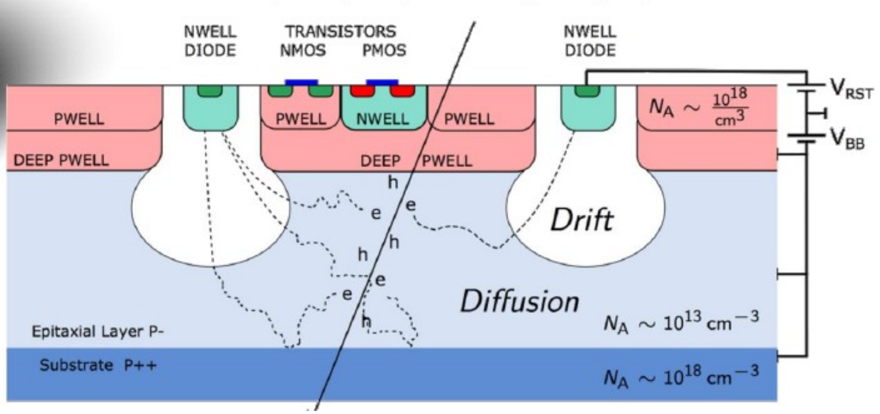




ITS2 ALPIDE – 3D and 2D views of 2x2 pixels
(Here, in the 50-µm-thick version...)

B.2 – ALPIDE : chip characteristics

- **Process:** Tower Semiconductor 180 nm CIS
  - deep p-well to allow CMOS circuitry inside matrix
  - reverse-substrate bias
- **Detection layer:** 25 µm high-resistive (>1 kΩcm) epitaxial layer
- **Thickness:** 100 µm (OB) or 50 µm (IB)



- **Front-end:** (9 transistors, full-custom)
  - continuously active
  - shaping time: < 10 µs
  - power consumption: 40 nW
- **Multiple-event memory:** 3 stages (62 transistors, full-custom)
- **Configuration:** pulsing & masking registers (31 transistors, full-custom)
- **Testing:** analogue and digital test pulse circuitry (17 transistors, full-custom)
- **Readout:** priority encoder, asynchronous, hit-driven

O(200) transistors / pixel (wrt. 3T/4T)

M. Mager, CERN Detector Seminar 2021-09-24

B.3 – ALPIDE : ALPIDE chip

ALICE ITS, arXiv:2105.13000

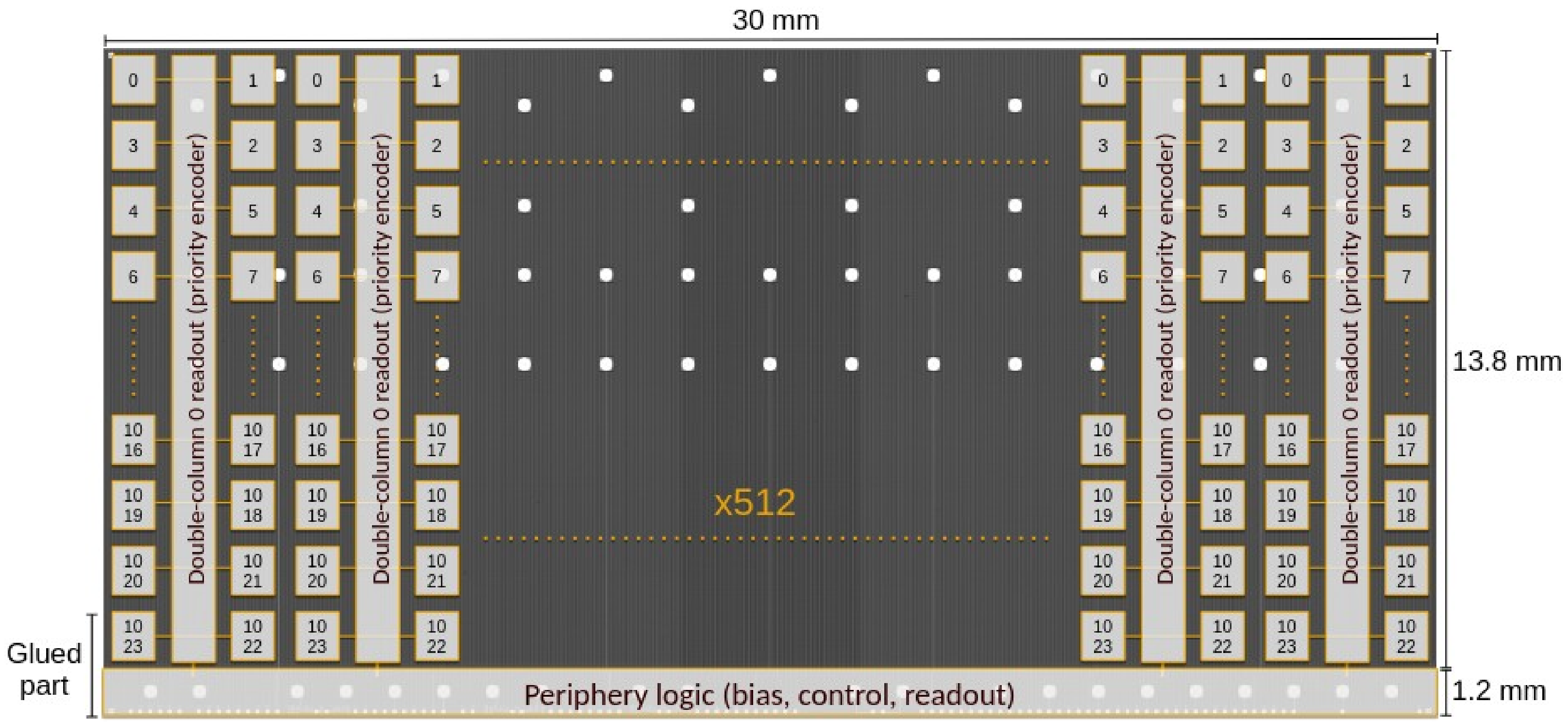
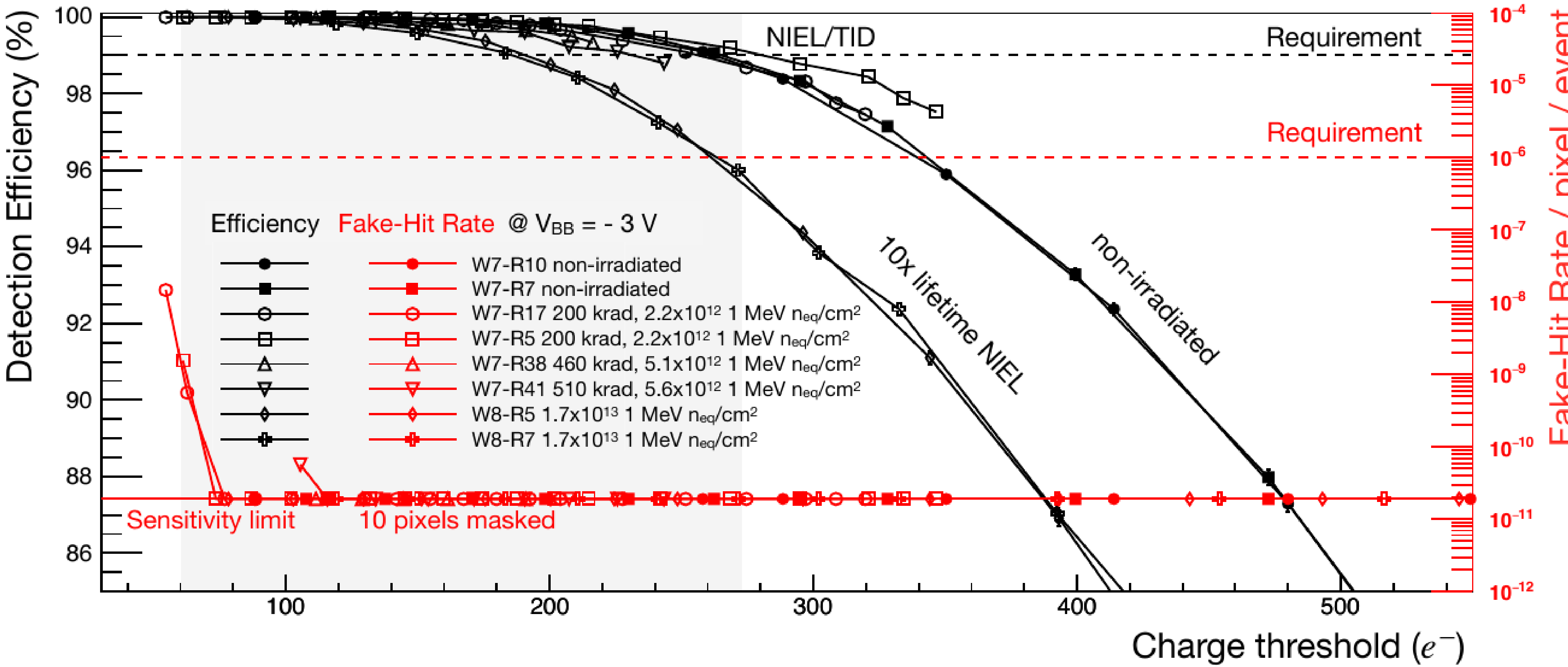


Figure 1: Layout of the ALPIDE pixel matrix. The pixels are organised in double-columns, each featuring a priority encoder circuit which propagates the addresses of the hit pixels to the periphery logic. The aluminum pads providing the electrical interface to the chip are located on the top of the periphery logic.

B.4 – ALPIDE : detection efficiency / Fake Hit Rate



10 pixels masked in 512 x 1024 = 2^{19} = 524 288 pixels/ALPIDE chip

→ 10/524 288 ≈ 2. 10^{-5} level

B.4 – ALPIDE : detection efficiency / Fake Hit Rate

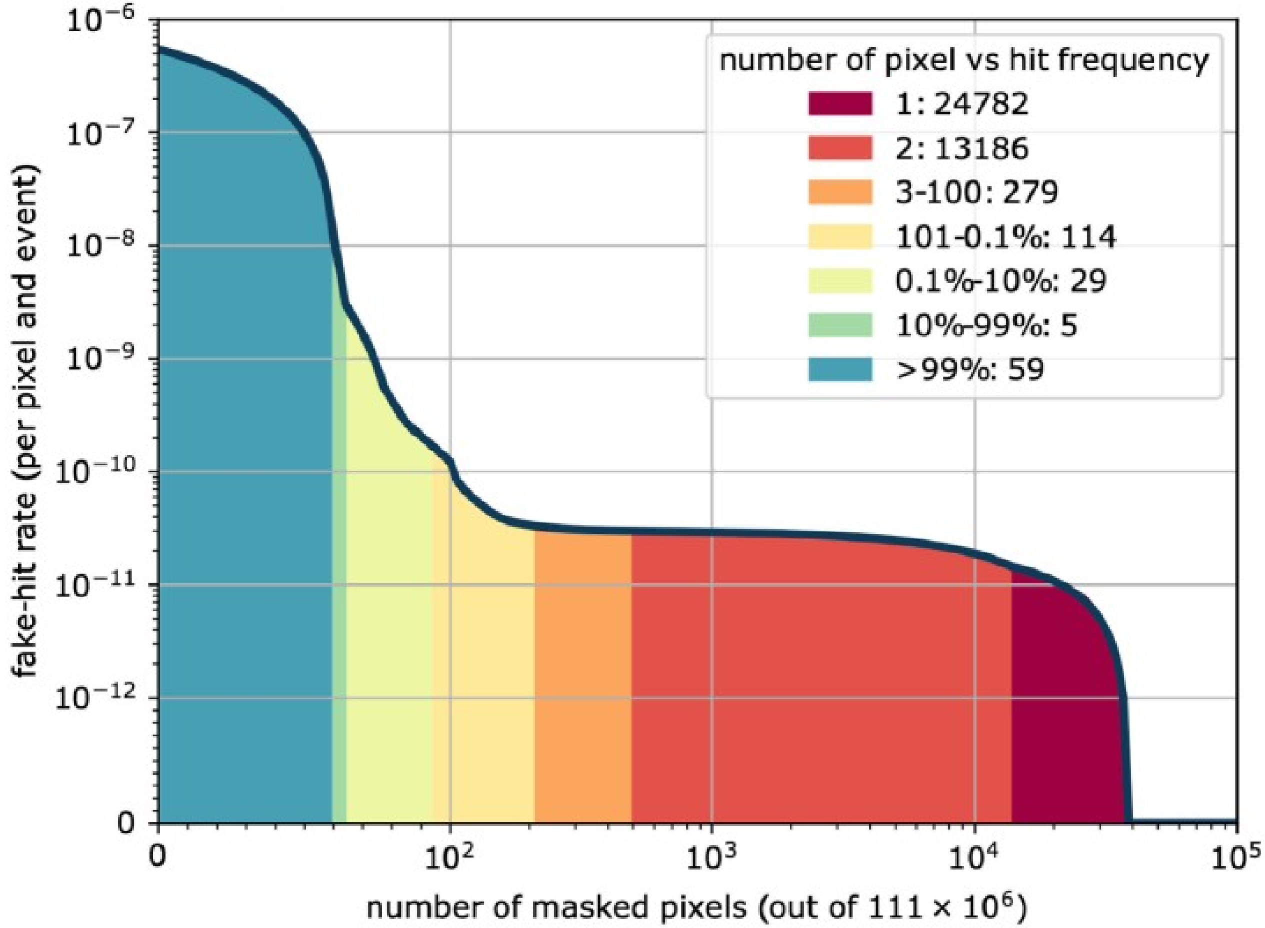


Figure 32: Fake-hit rate of an inner half-barrel as function of the number of masked pixels. Colors indicate how often a pixel fired in 15×10^6 events acquired at a trigger rate of 50 kHz using a charge threshold of 100 e^-, e.g. there were 24782 pixels which fired once in the sample.

B.5 – ALPIDE : spatial resolution / average cluster size

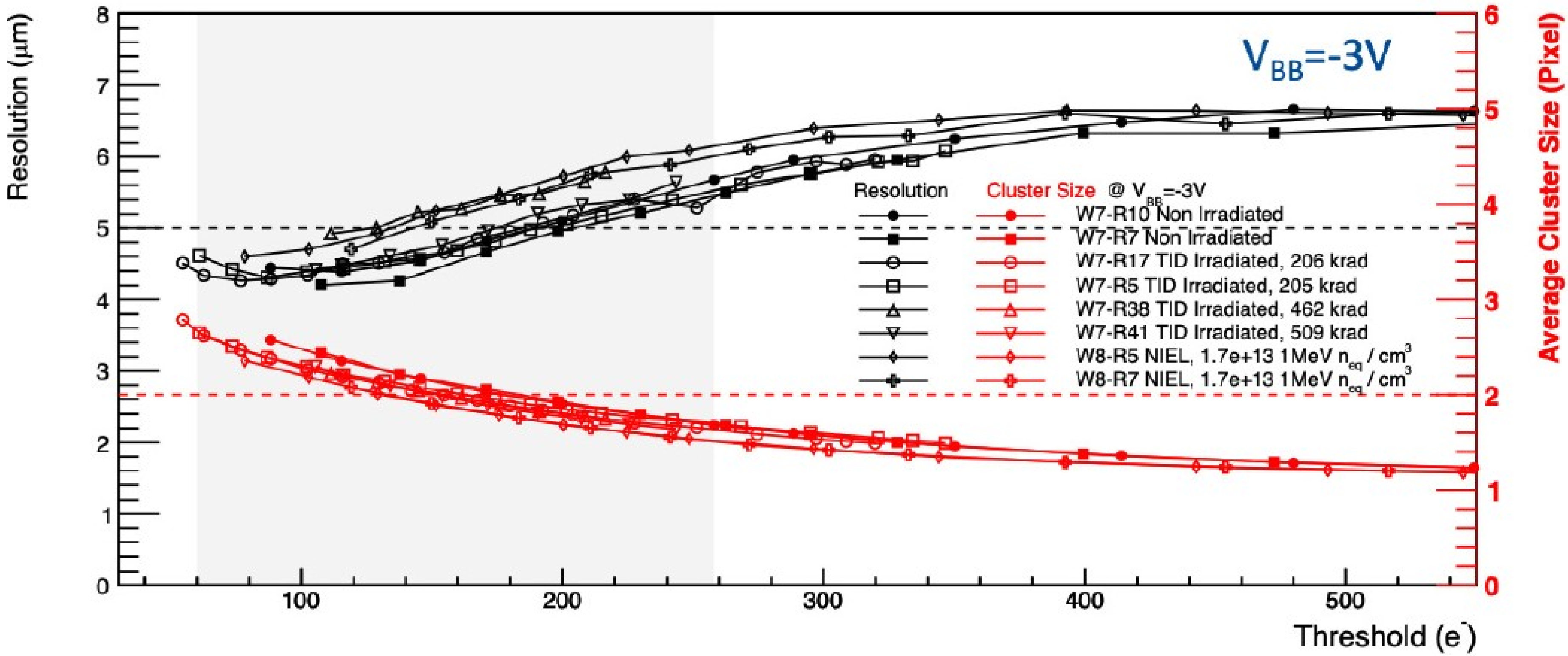
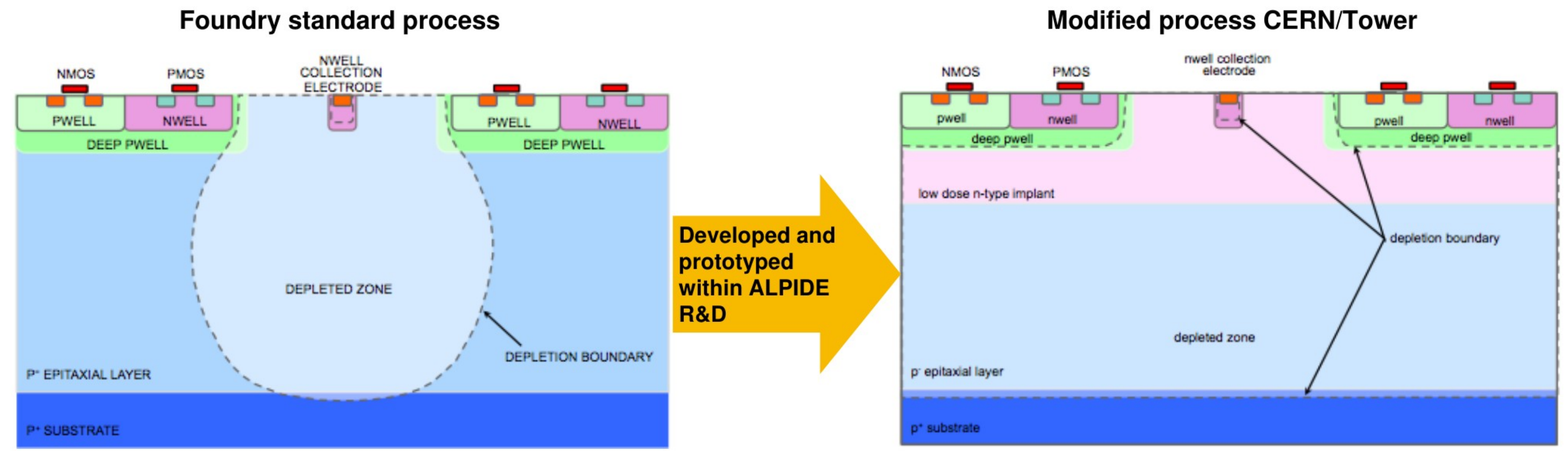


Figure 13: ALPIDE sensor chip hit-position resolution and average cluster size vs global threshold setting. Beam test results (6 GeV/c pions, orthogonal incidence). ALPIDE substrate reverse bias: -3 V.

B.6 – ALPIDE : R&D around ALPIDE chip

process modification, depleted MAPS — ITS2 "side project"

ALICE



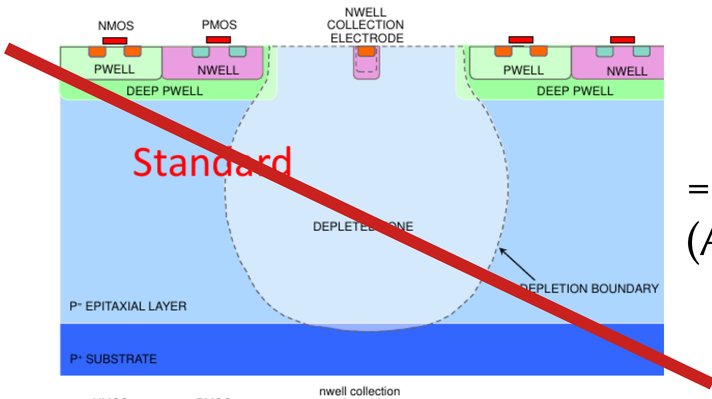
Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2

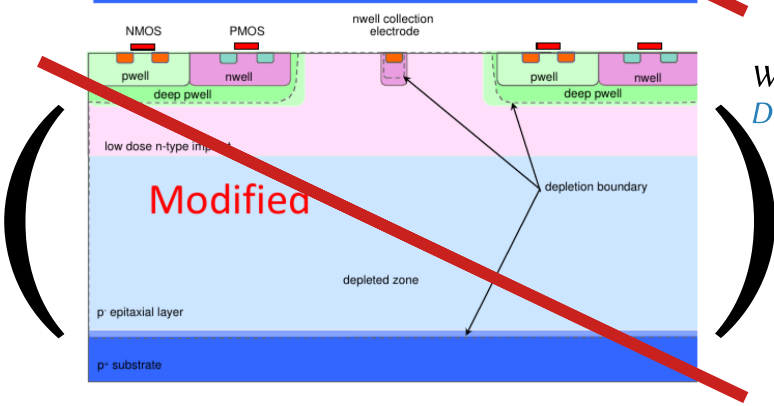
W. Snoeys et al, https://www.doi.org/10.1016/j.nima.2017.07.046

Courtesy Magnus Mager

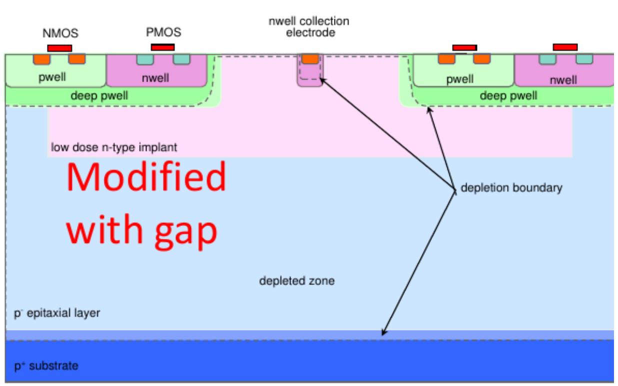
B.7 – ALPIDE: from ALPIDE to MOSS, lithography process



= <u>Default</u> by Tower (ALPIDE ITS2)



W. Snoeys et al,
DOI:10.1016/j.nima.2017.07.046



= <u>Basis for ITS3</u>

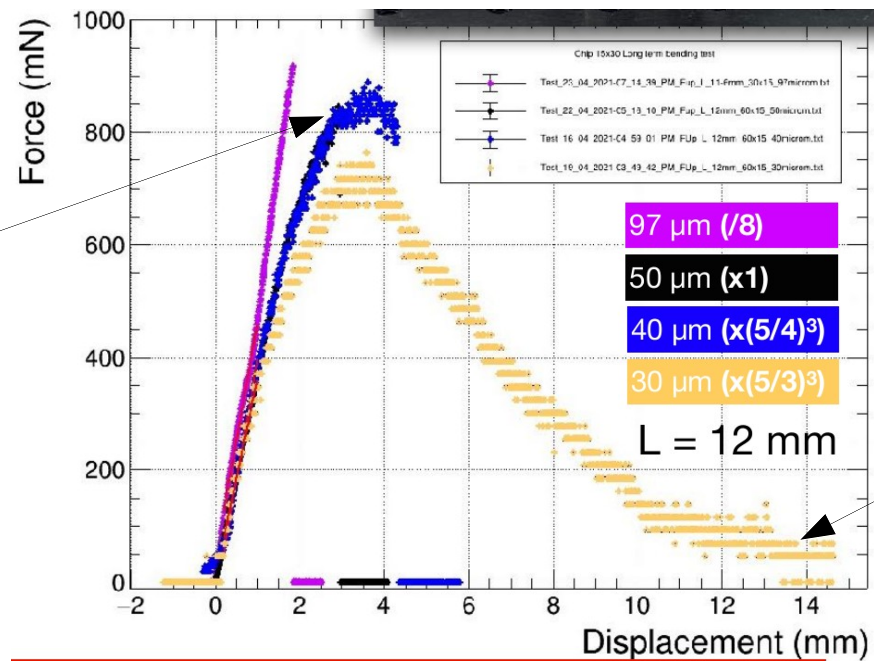
W. Snoeys et al, arXiv:1903.10190

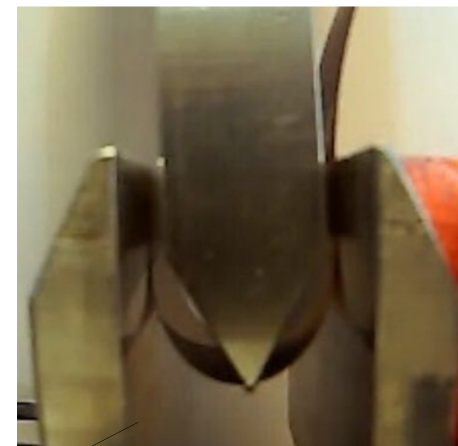
⟶ even ***faster*** *charge collection*

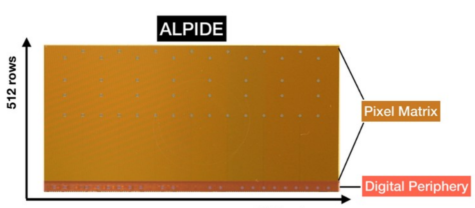
Back to App. TOC

App. C – bending R&D

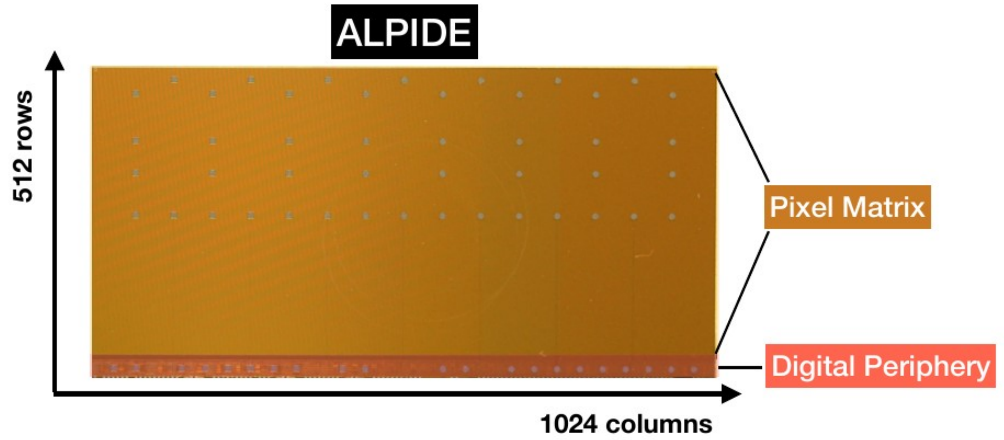
C.1 – MAPS bending : ALPIDE bending flexibility

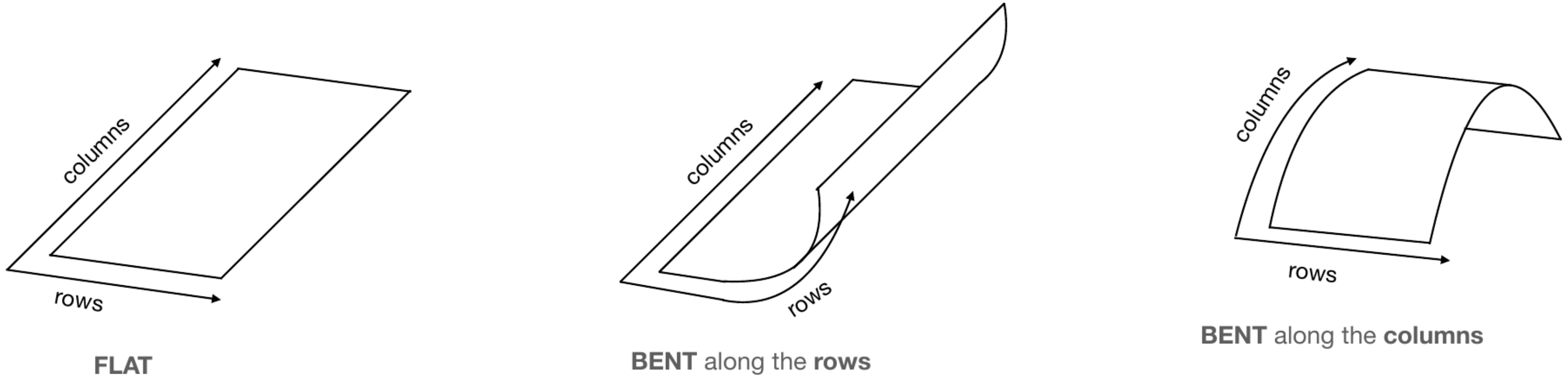






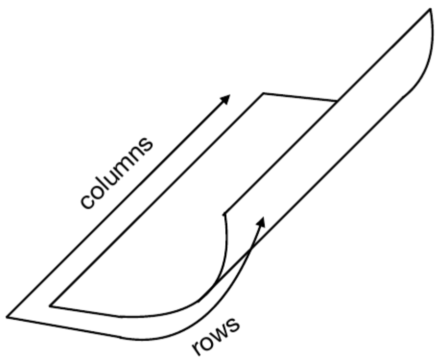
C.2 – MAPS bending : ALPIDE bent sensors





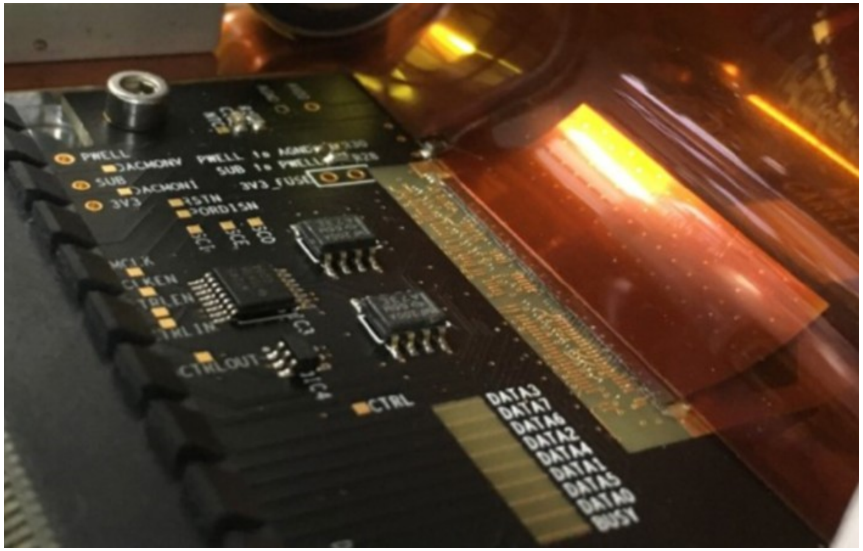
C.3 – MAPS bending : ALPIDE bent sensors, inefficiency

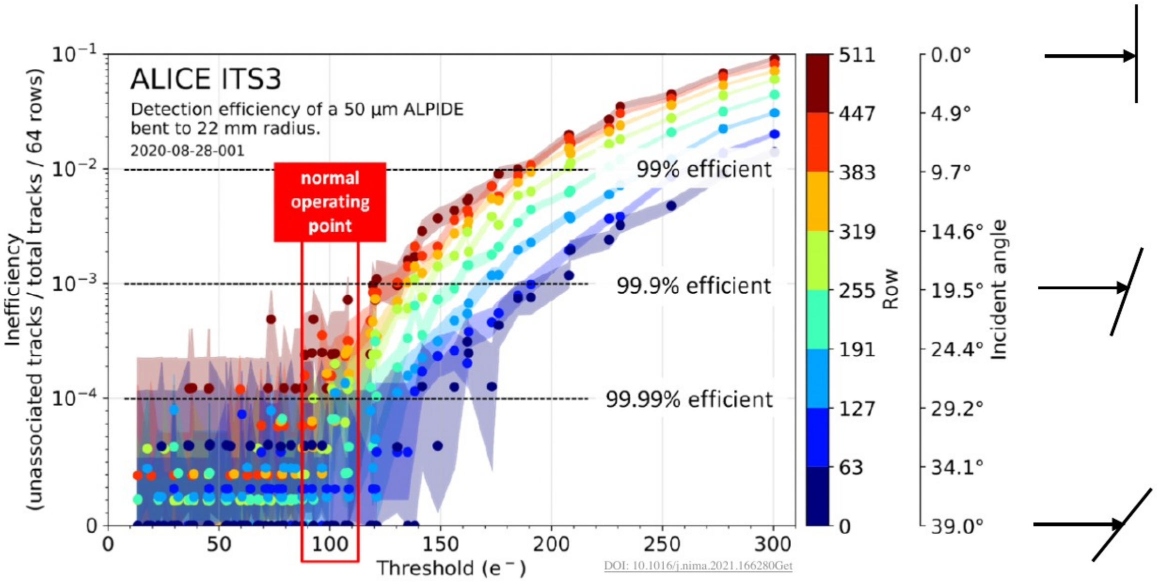
ALICE ITS, arXiv:2105.13000



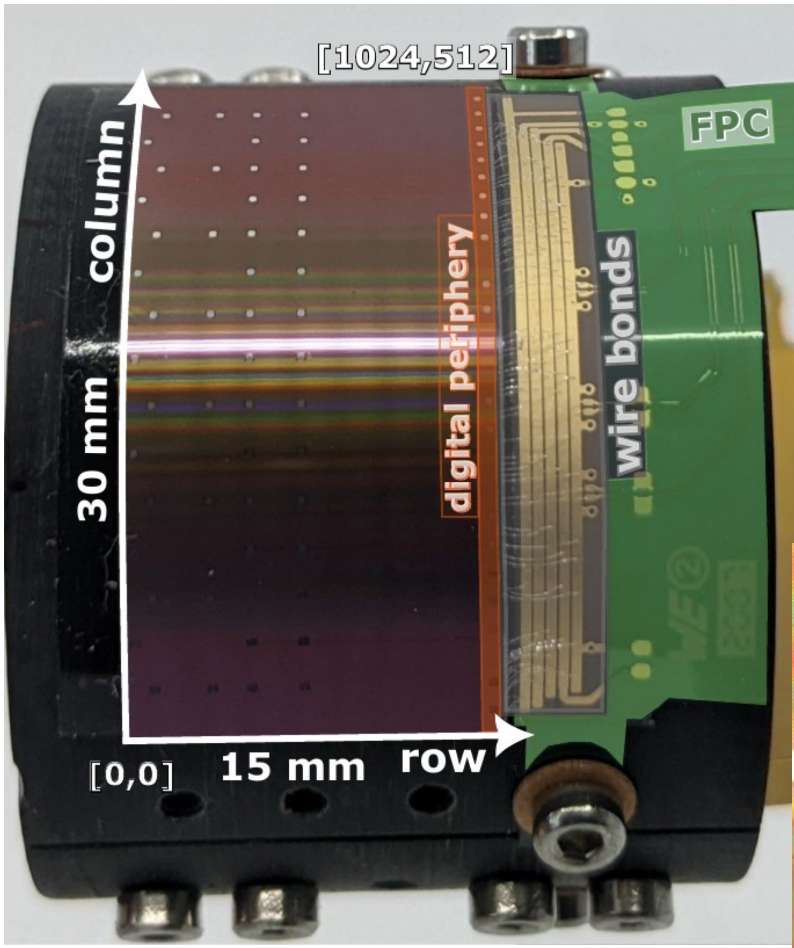
BENT along the **rows**

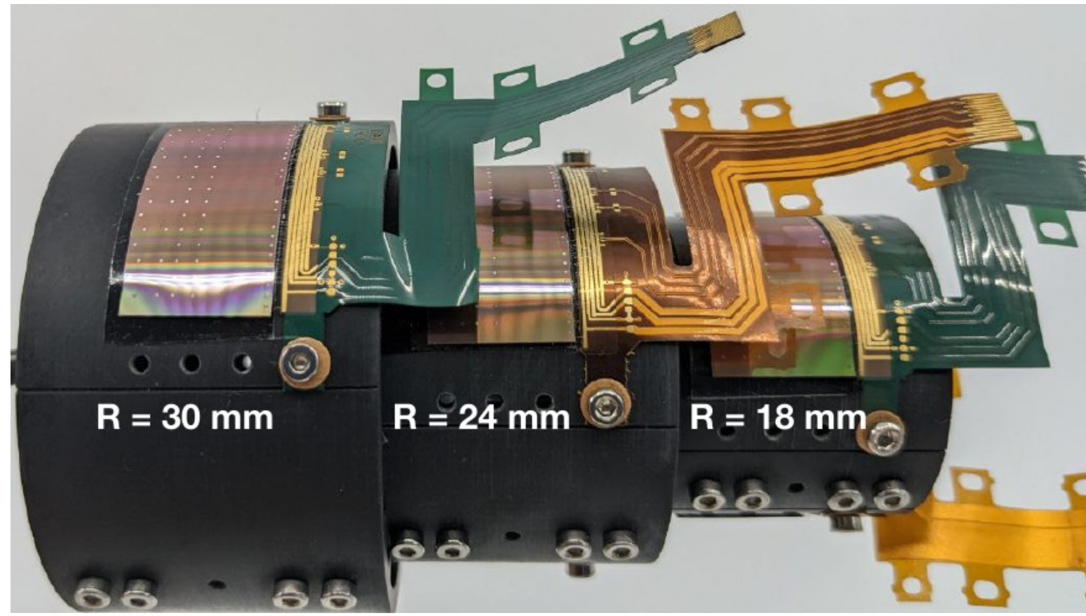
- ALPIDE bent along rows with flat digital periphery
- Demonstration : electric functionality and efficiency compatible with flat ALPIDE

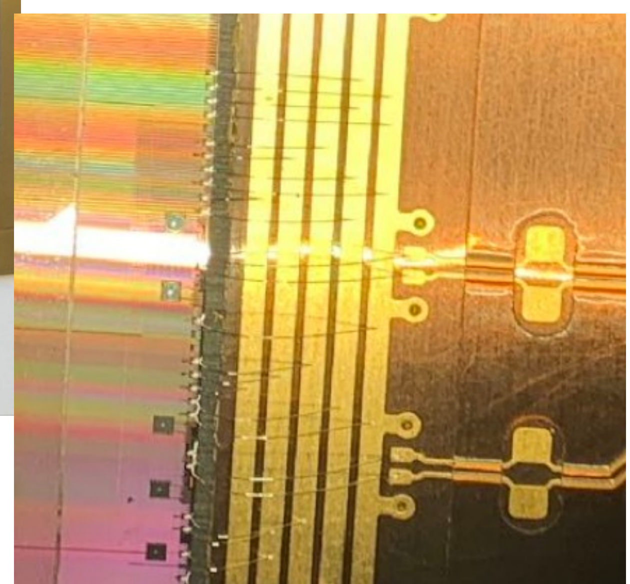




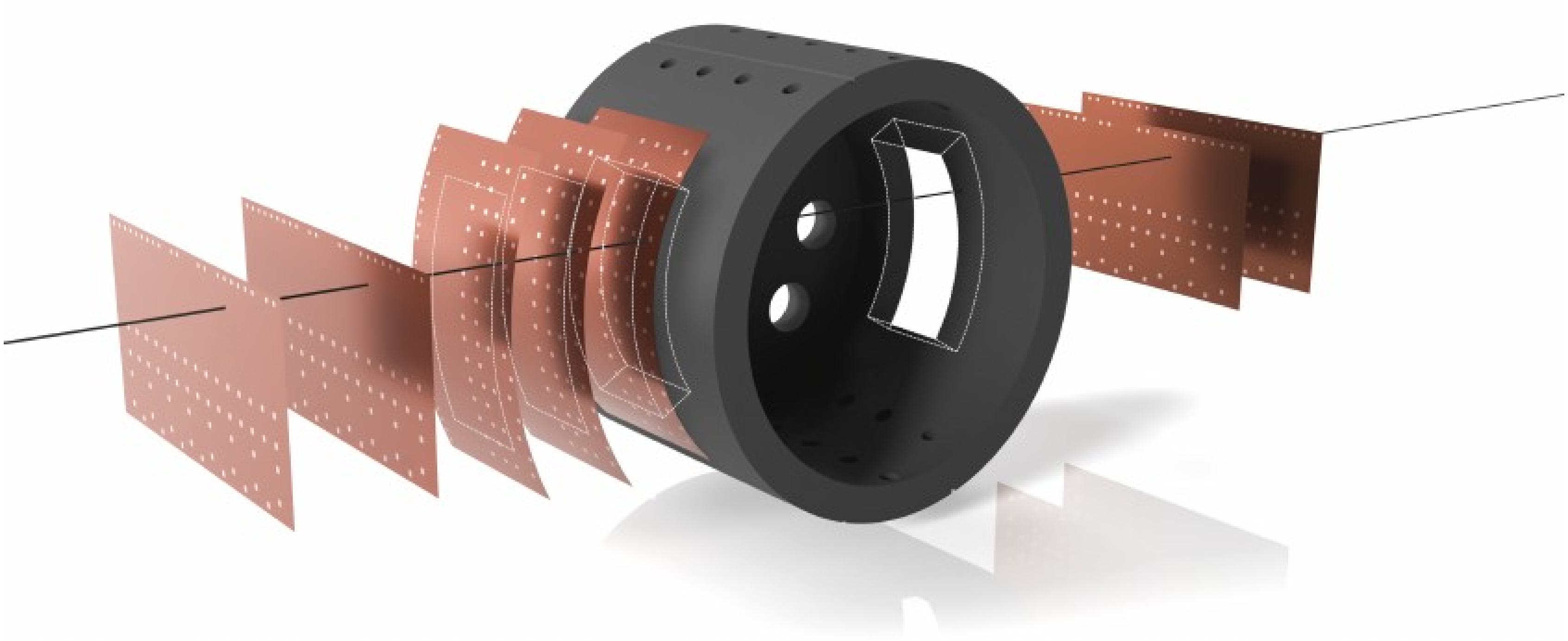
C.4 – MAPS bending : ALPIDE bent sensors, µITS3



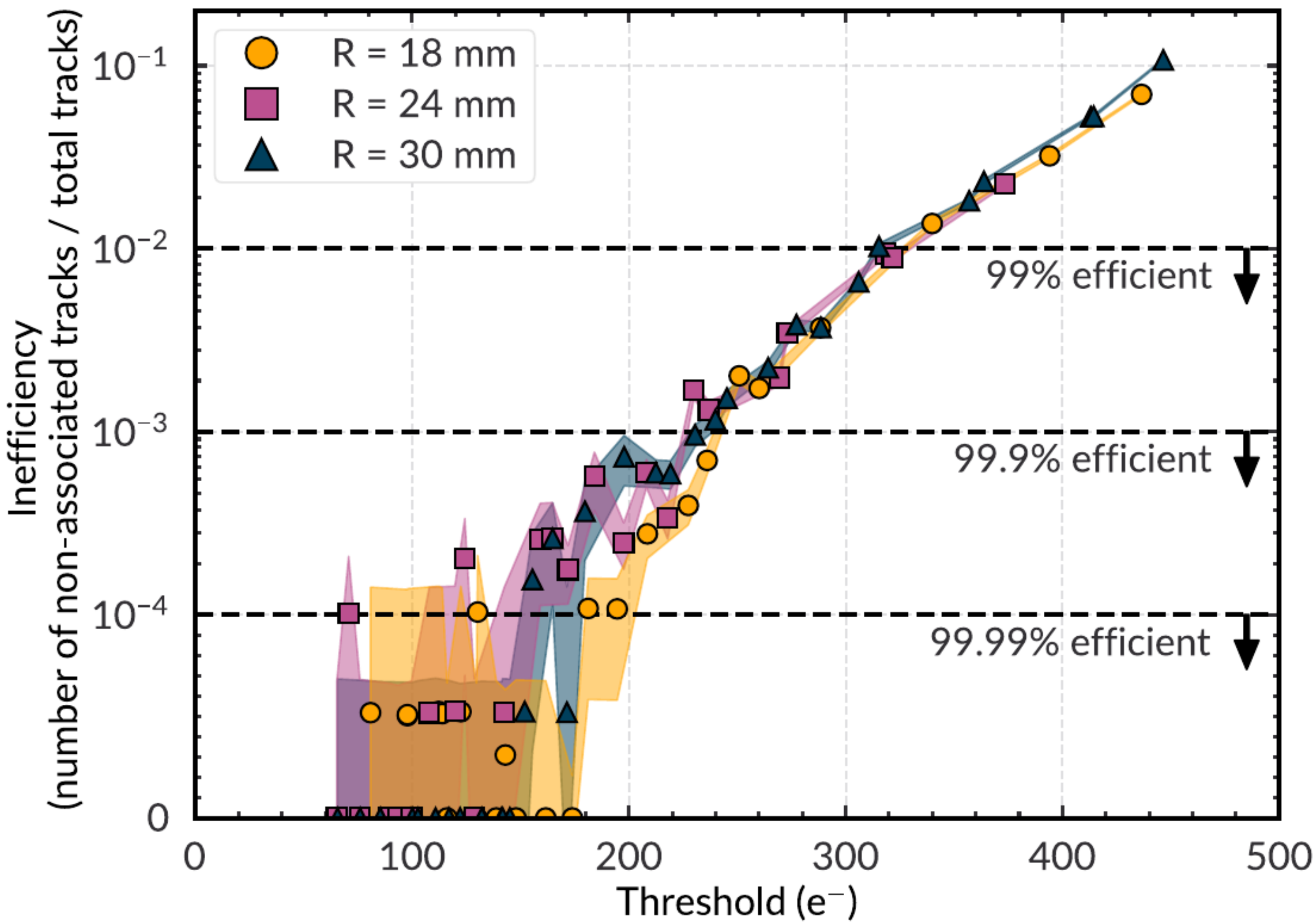




C.5 – MAPS bending : μITS3 under beams



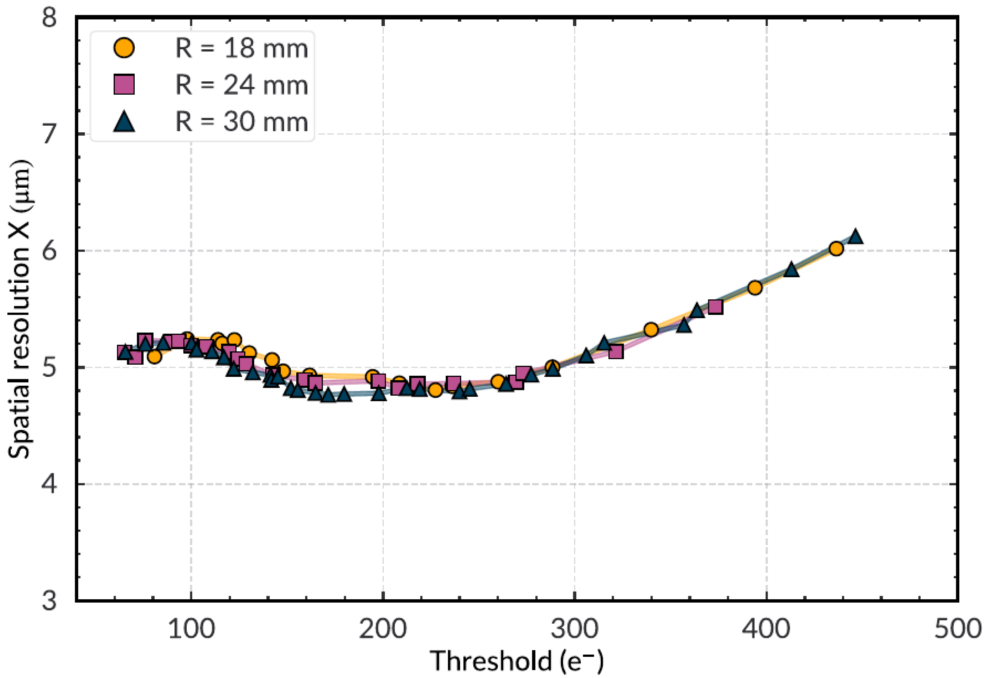
C.6 – MAPS bending : µITS3, detection inefficiency

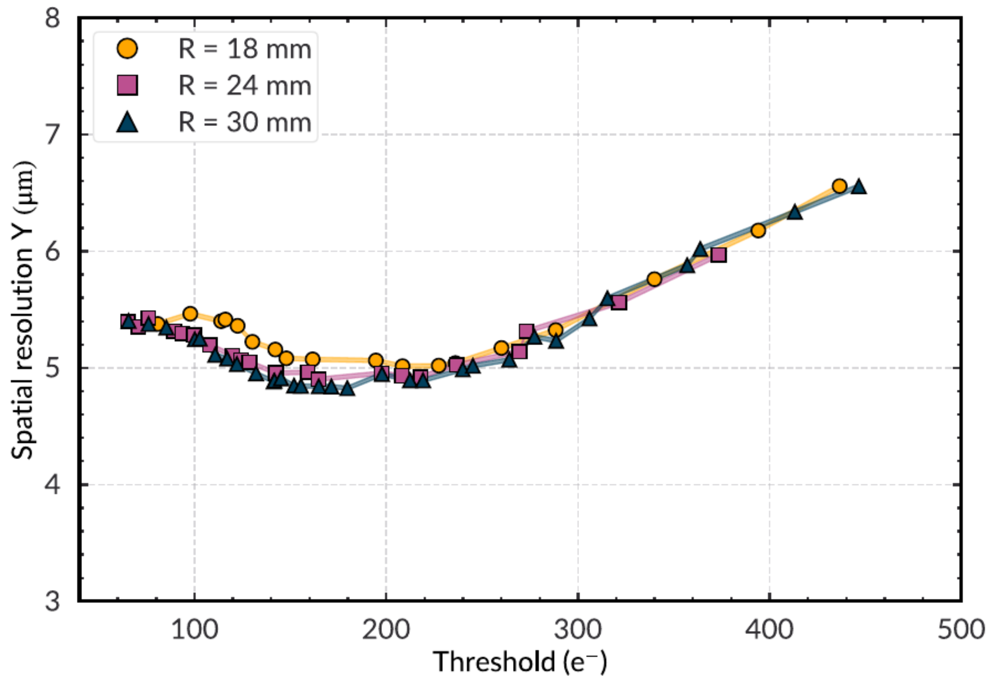


- No effects on bending radius observed
- Inefficiency compatible with flat ALPIDE
- Consistent with published results where chip was bent in the other direction

Lucas Lautner, ALICE Upgrade Week 2022-10
https://indico.cern.ch/event/1183733/contributions/5045649

C.7 – MAPS bending : μITS3, spatial resolution

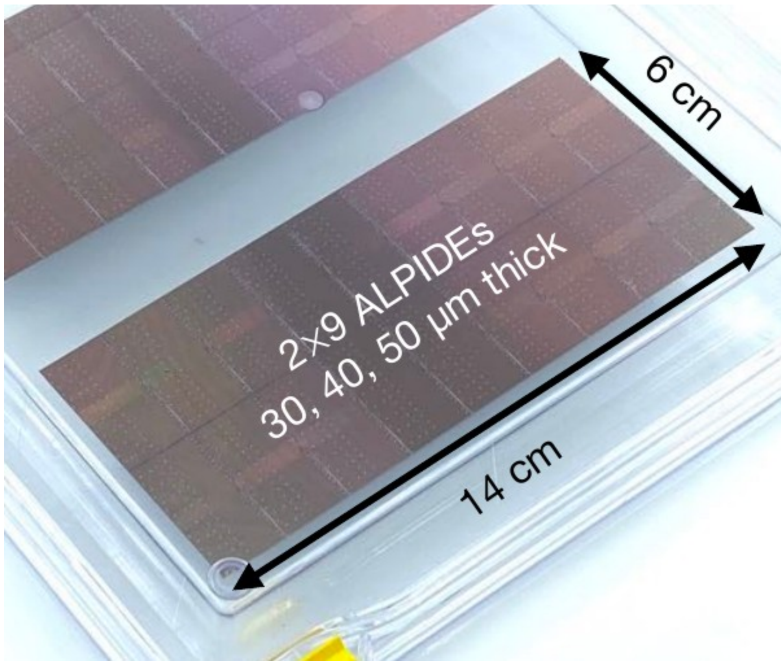


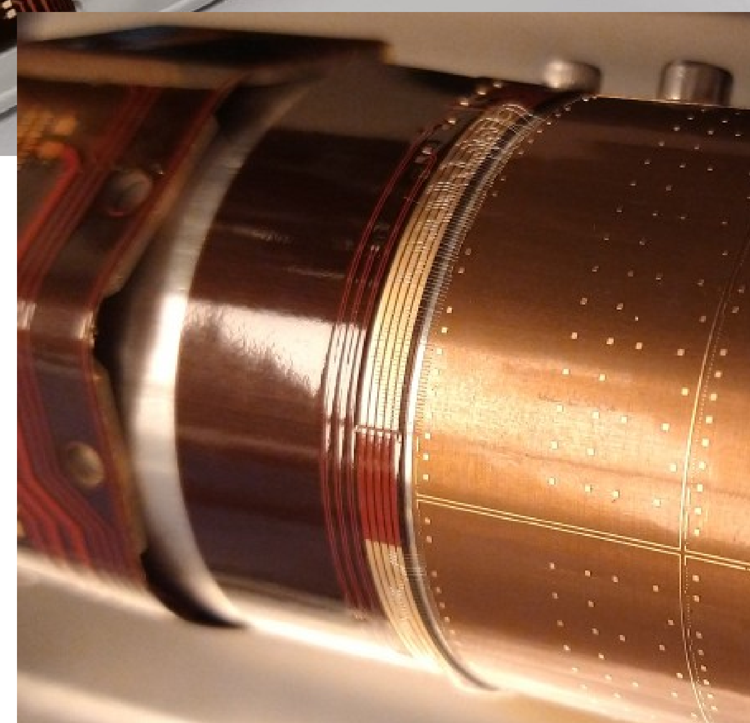


- No effects on bending radius observed
- Spatial resolution of 5 μm consistent with flat ALPIDE

Lucas Lautner, ALICE Upgrade Week 2022-10
https://indico.cern.ch/event/1183733/contributions/5045649

C.8 – MAPS bending : SuperALPIDE





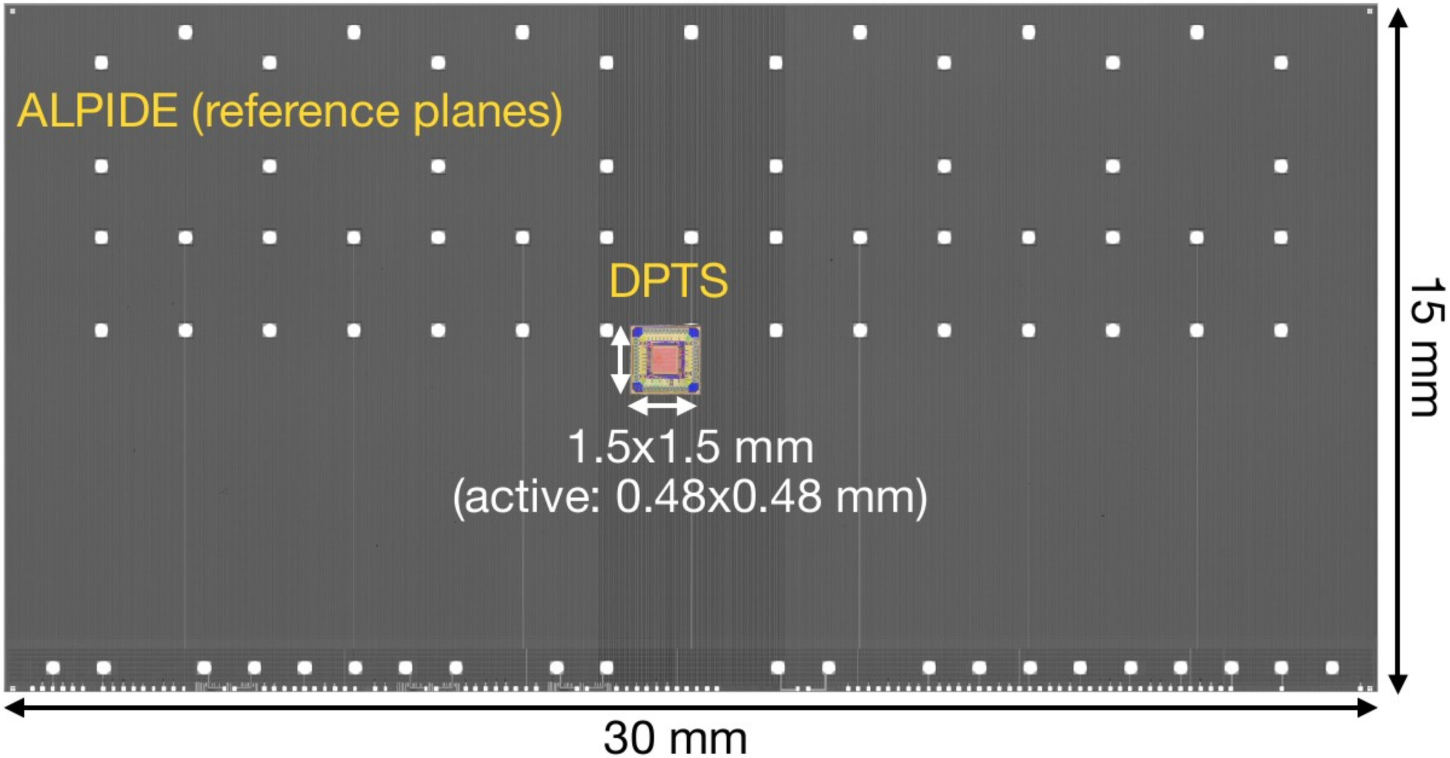
- One silicon piece from ALPIDE *wafer* :
  9x2 dies, ≈ half an ITS3 layer L0
- Exoskeleton that mimics L1
  + allow for interconnection between dies

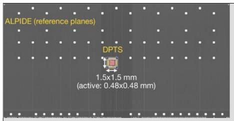
M. Mager, CERN Detector Seminar 2021-09-24

Back to App. TOC

App. D – (65-nm + stitched) sensor design

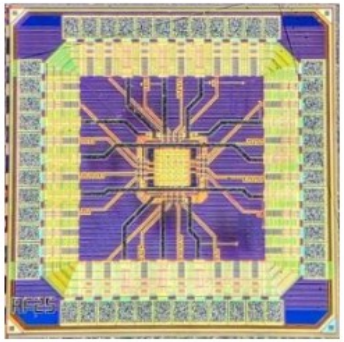
D.1 – 65-nm MAPS : tests of MLR1 65-nm sensors





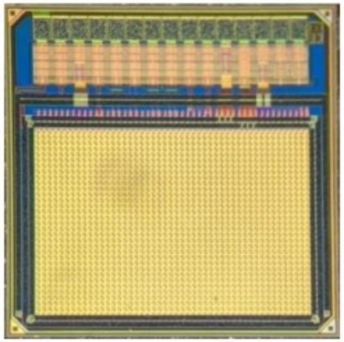
ITS3 1D-stitched sensor ≈ 1.88 x 28 cm²

D.2 – 65-nm MAPS : MLR1 65-nm sensors



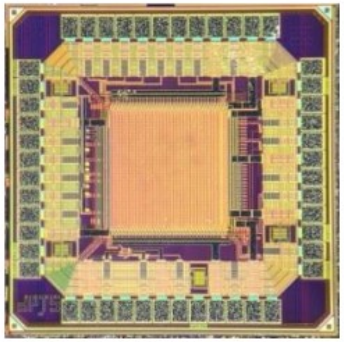
APTS
(Analogue Pixel Test Structure)

- Matrix: 6×6 pixels
- Pitch: 10, 15, 20, 25 μm
- Direct analogue readout of central 4×4 submatrix
- Two types of output drivers:
  - Source follower (APTS-SF)
  - Very fast OpAmp (APTS-OA)
- AC/DC coupling
- 3 process modifications



CE65
(Circuit Exploratoire 65 nm)

- Matrix: 64×32 or 48×32
- Pitch: 15 μm or 25 μm
- Rolling shutter readout (down to 50 μs integration time)
- 3 in-pixel architectures:
  - AC-coupled amplifier
  - DC-coupled amplifier
  - Source follower
- 4 chip variants:
  - Standard process 15 μm pitch
  - Modified process 15 μm pitch
  - Modified process with gap 15 μm pitch
  - Standard process 25 μm pitch

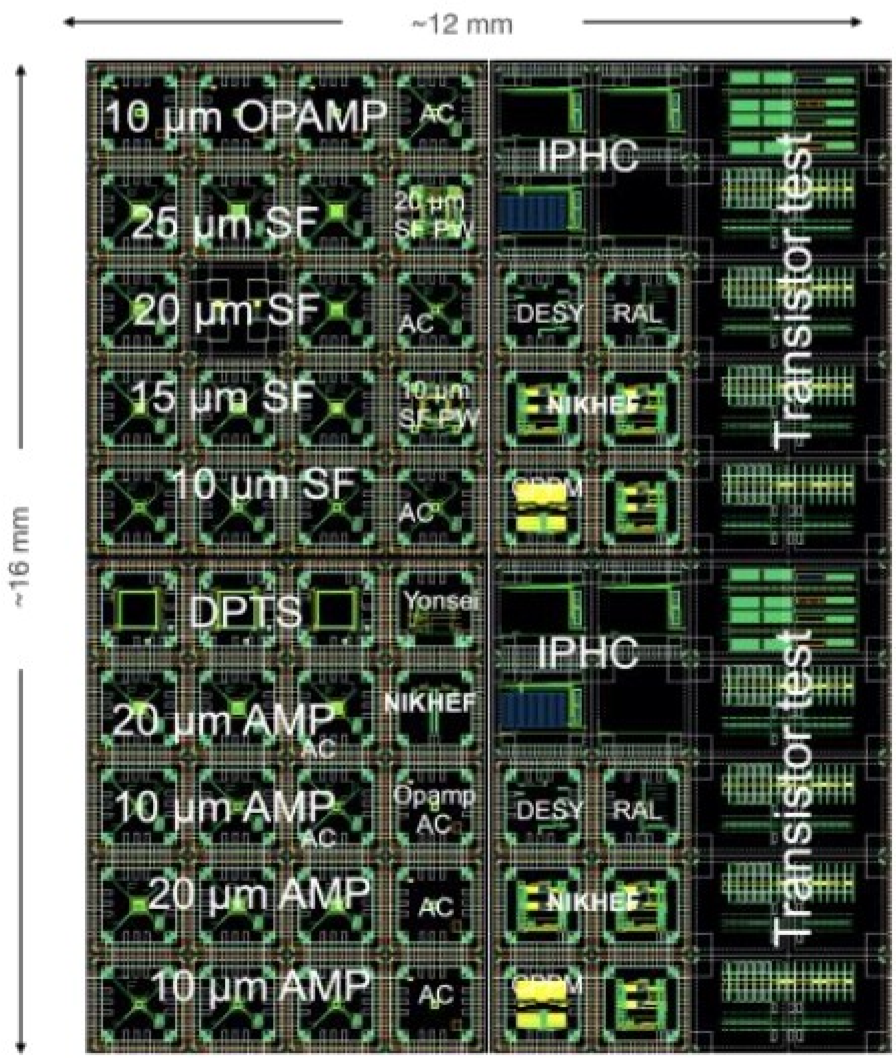


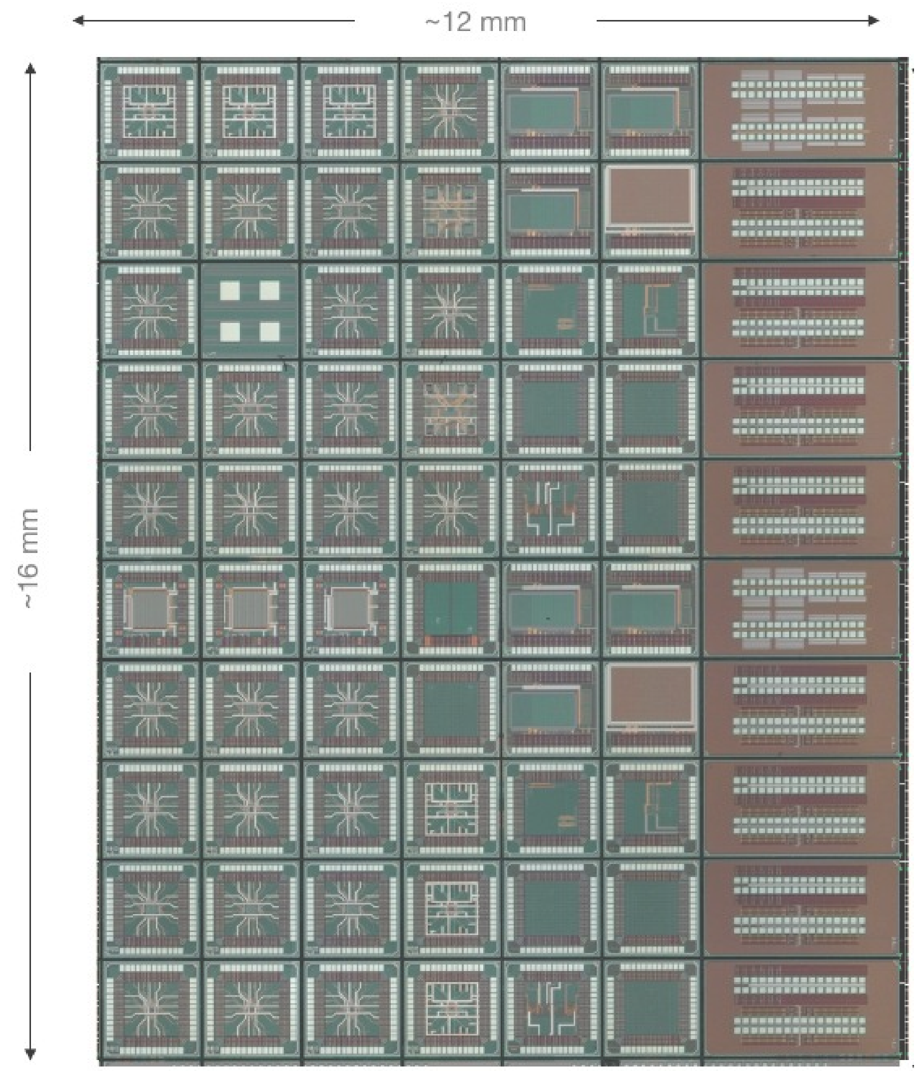
DPTS
(Digital Pixel Test Structure)

- Matrix: 32×32 pixels
- Pitch: 15 μm
- Asynchronous digital readout
- Time-over-Threshold information
- Only “modified with gap” process modification

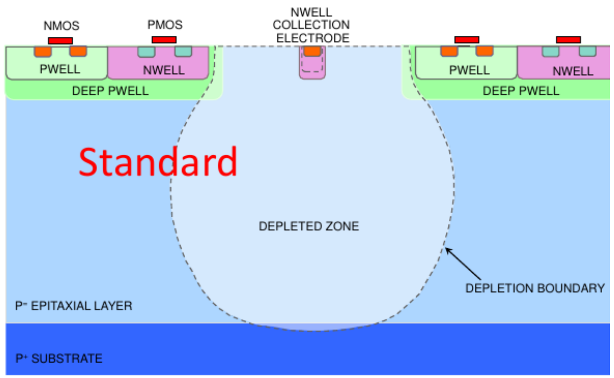
09-05-2023 3

D.3 – 65-nm MAPS : MLR1 65-nm sensors

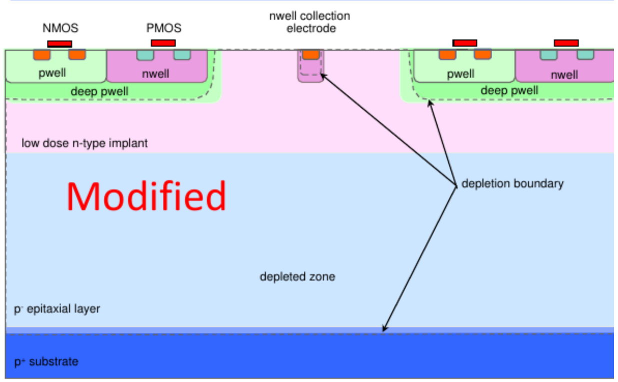




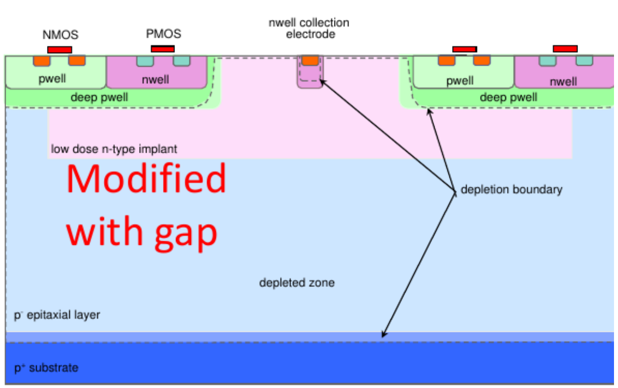
D.4 – 65-nm MAPS : modified process and charge collection



= Default by Tower (ALPIDE ITS2)



W. Snoeys et al,
DOI:10.1016/j.nima.2017.07.046

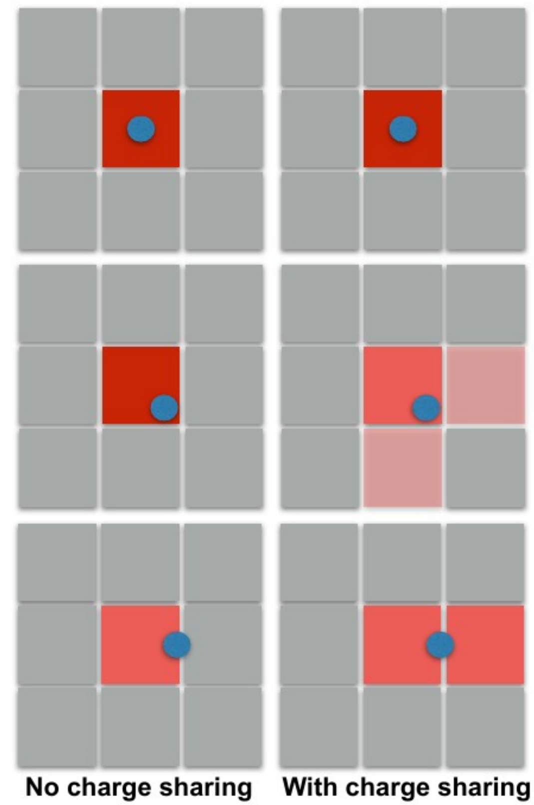


= Basis for ITS3

W. Snoeys et al, arXiv:1903.10190
→ even ***faster*** *charge collection*

Spatial resolution ≈ (pixel pitch)/√12

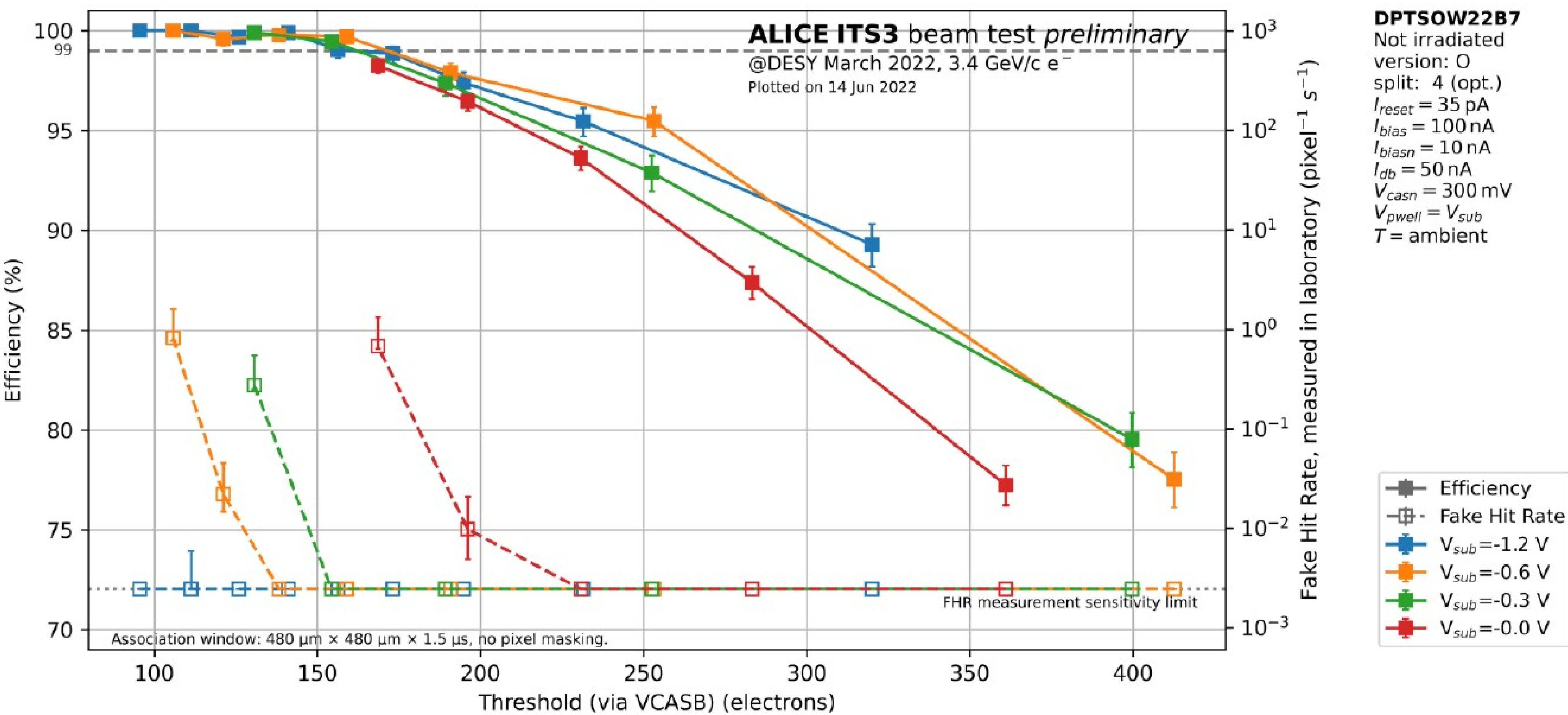
(i.e. not better than this, due to ~~cluster shapes~~)



Schematic comparison of cluster shapes without and with charge sharing Depending on the impinging point

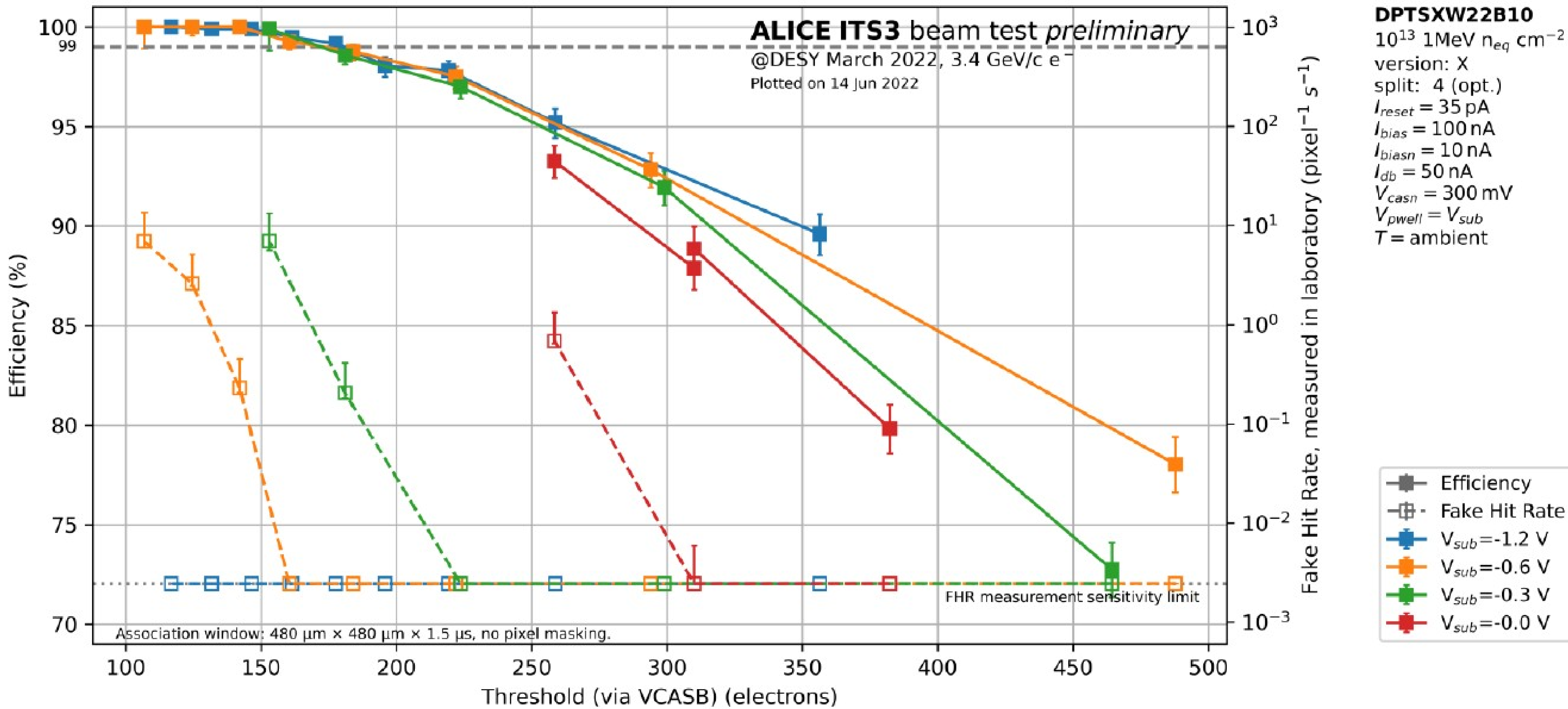
Courtesy Felix Reidt

D.5 – 65-nm MAPS : DPTS 65-nm, 0 radiation



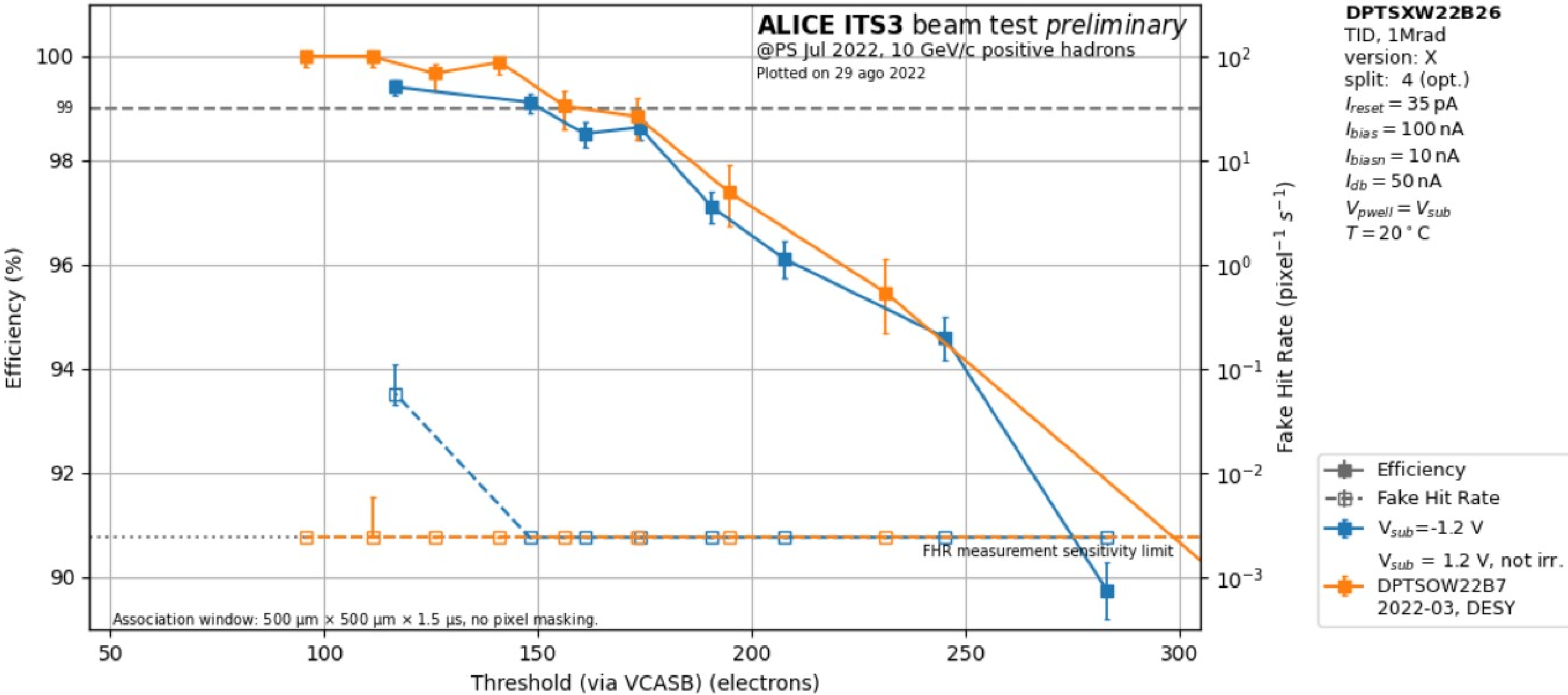
→ Excellent efficiency + low fake-hit rate

D.6 – 65-nm MAPS : DPTS 65-nm, $+10^{13}$ n_{eq} NIEL



→ larger fake-hit rate but still some margin

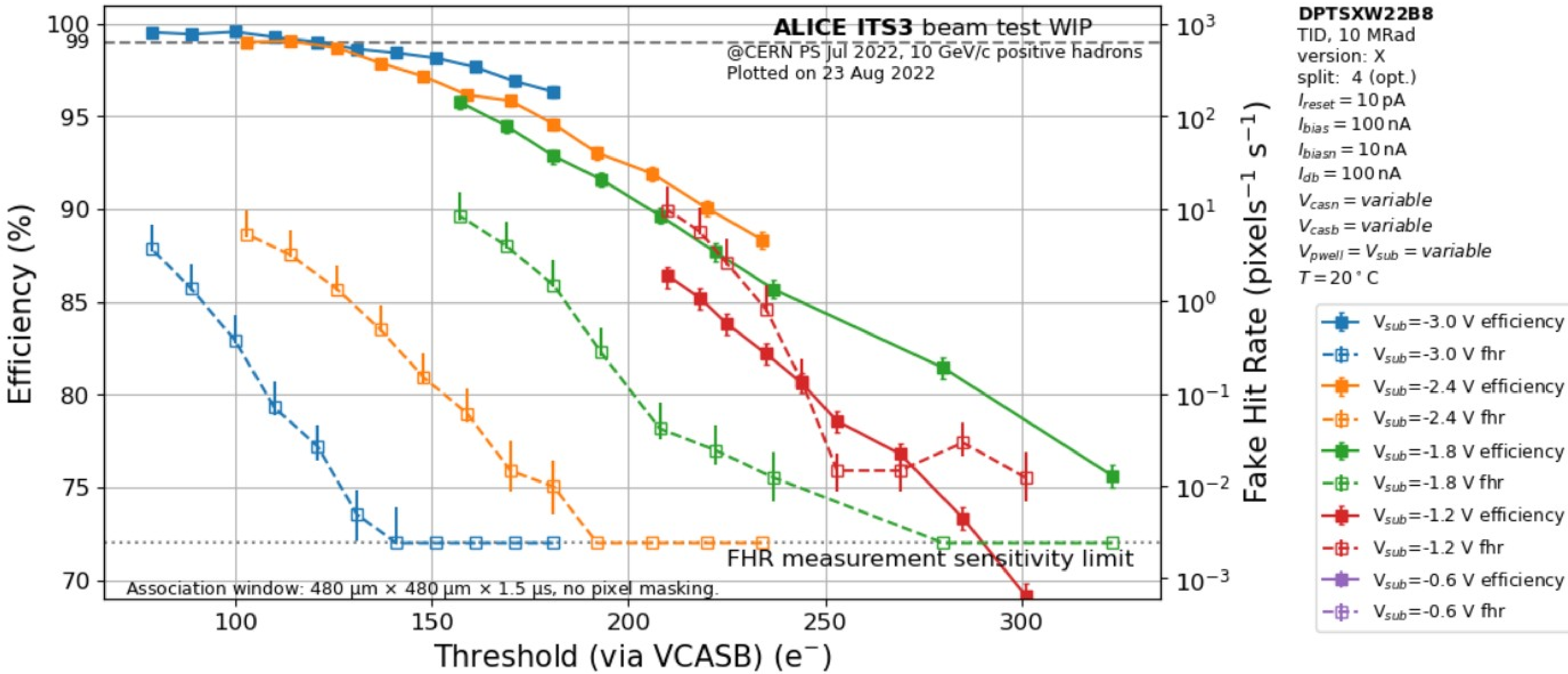
D.7 – 65-nm MAPS : DPTS 65-nm, +1 Mrad TID



→ Negligible effect

D.8 – 65-nm MAPS : DPTS 65-nm, +10 Mrad TID

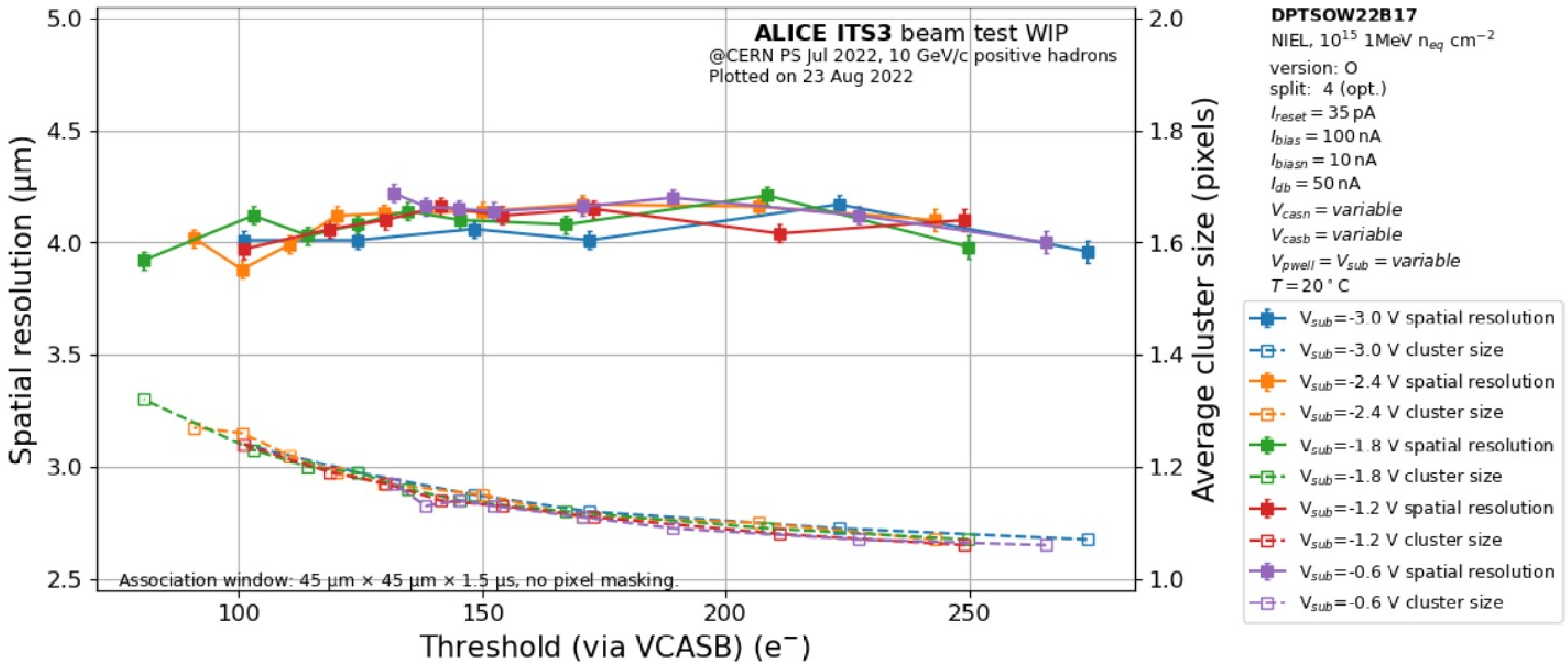
WORK in PROGRESS



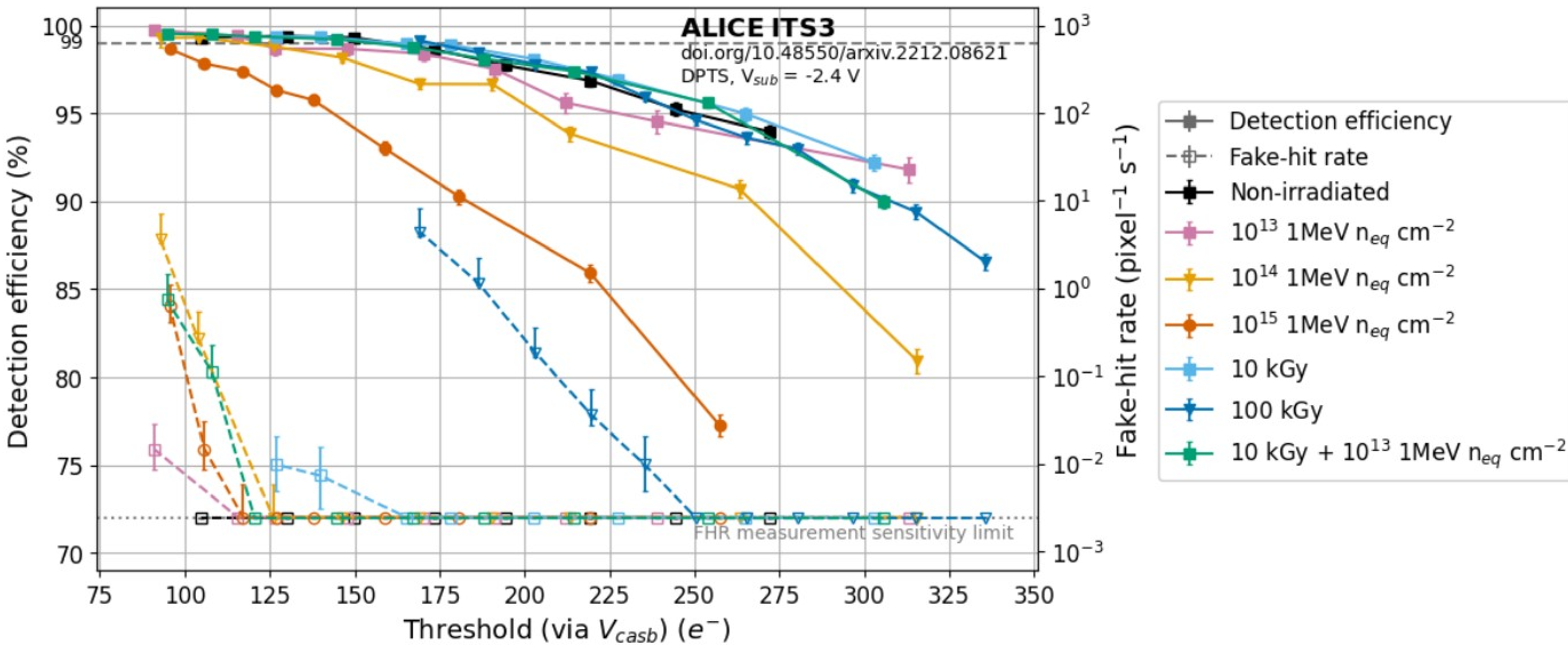
→ reverse back bias, necessary

D.9 – 65-nm MAPS : DPTS 65-nm, +10^{15} 1-MeV n_{eq}.cm^{-2} NIEL

WORK in PROGRESS



D.10 – 65-nm MAPS : DPTS 65-nm, eff = f(irradiation)

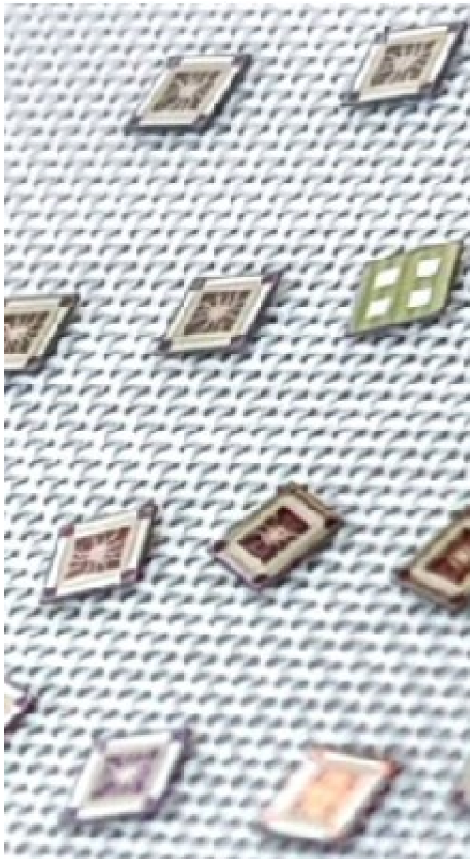


Miljenko Suljic, WP3 ITS3 Plenary 2023-05-09

D.10 – 65-nm MAPS : Analog chips 65-nm

Roadmap of (ongoing) characterisations :

Focus ≈ charge collection characteristics.
NB : rather small chips (*e.g.* 6x6 pixels) more difficult to bring to beam tests
+ full readout/steering to be deployed outside the chip itself



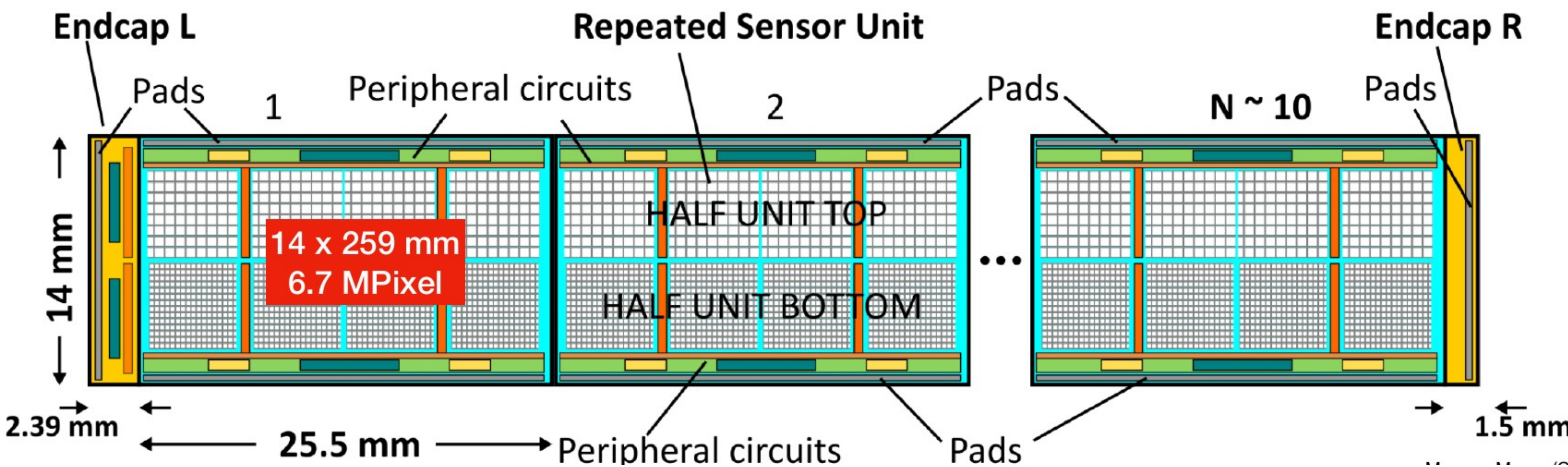
CE65
- Analogue signal distributions for 25 μm pitch
- Spatial resolution for 15 and 25 μm pitch

APTS-SF: analogue signal distributions, spatial resolution, cluster properties vs.
- Process modification: standard, modified, modified with gap
- Reverse back bias: -1.2, -2.4, -3.6, -4.8 V
- Pixel pitch: 10, 15, 20, 25 μm
- NIEL irradiation: 10^{13}, 10^{14}, 10^{15} 1-MeV n_{eq}/cm^2

APTS-OA
- Temporal resolution, efficiency and cluster properties

⟶ Dedicated publications for APTS-SF, APTS-OA and CE65 will follow

D.11 – 65-nm MAPS : ER1 submission, stitching



MOSS 2 pitches, 22.5 µm (top) + 18 µm (bottom)

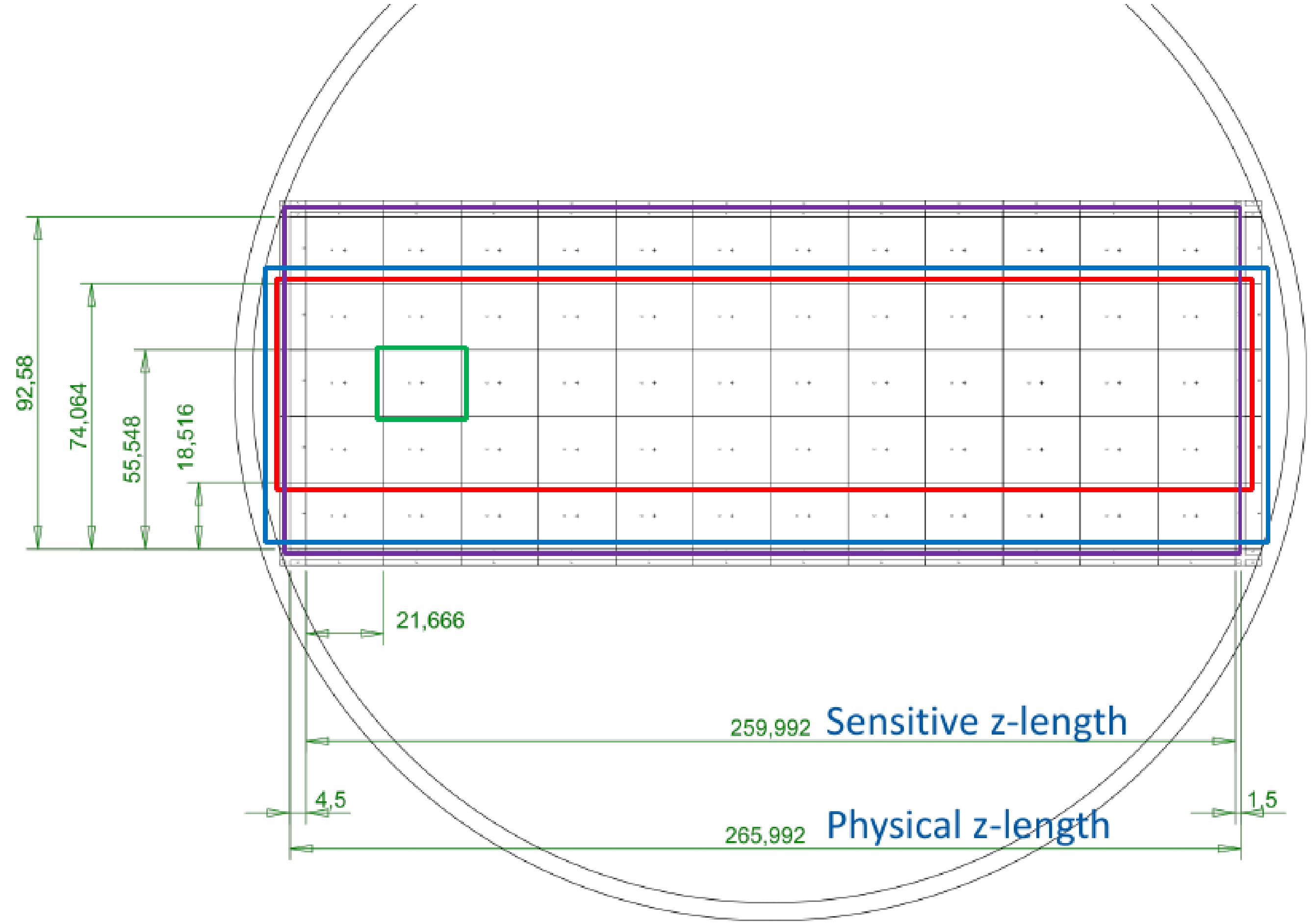
D.12 – 65-nm MAPS : ER2 submission, stitching

Layer 0: 12 x 3 repeated units+endcaps

Layer 1: 12 x 4 repeated units+endcaps

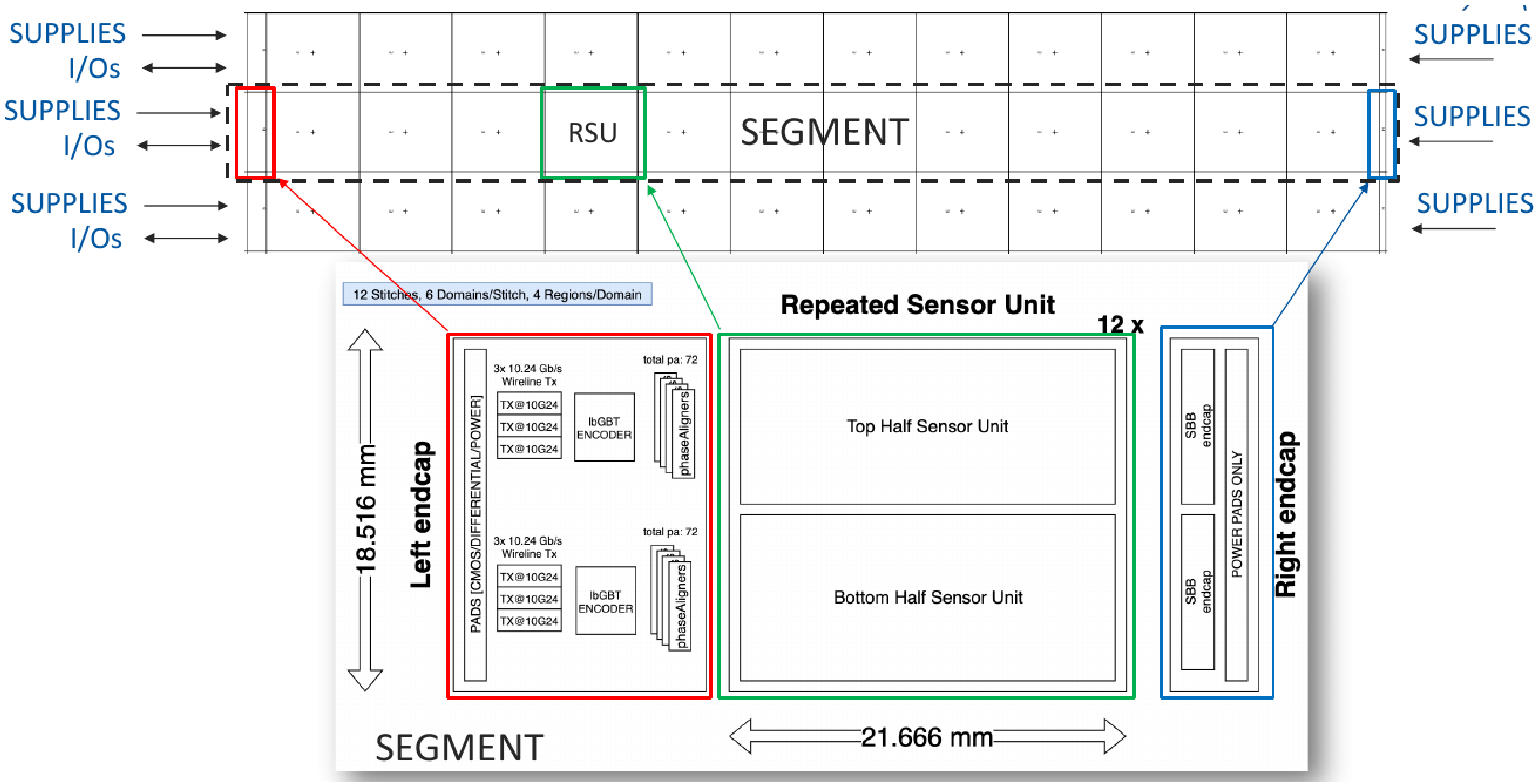
Layer 2: 12 x 5 repeated units+endcaps

Repeated (Stitched) Sensing Unit



Aglieri, WP2 ITS3 plenary 2023-05

D.12 – 65-nm MAPS : ER2 submission, stitching



Aglieri, WP2 ITS3 plenary 2023-05

D.13 – 65-nm MAPS : CERN EP R&D contributors

WP1.2, CERN EP R&D day 2023

EP R&D

Many contributors to WP1.2

EP R&D

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Bolu University: K. Oyulmaz
Talinn University: K. Rebane (also with CERN)
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EPFL: E. Charbon, F.Piro (also with CERN)
SLAC: M.D. Vassilev, C. Vernieri

CERN: G. Aglieri Rinella, I. Asensi Tortajada, R. Ballabriga, W. Bialas, G. Borghello, J. Braach, E. Buschmann, M. Campbell, F. Carnesecchi, L. Cecconi, F. Dachs, D. Dannheim, V. Dao, K. Dort, Joao de Melo, W. Deng (also with CCNU), A. Di Mauro, D. Dobrijevic, A. Dorda Martin, P. Dorosz, L. Flores Sanz de Acedo, A. Gabrielli, G. Gustavino, J. Hasenbichler (also with TU Vienna), H. Hillemans, A. Junique, I. Kremastiotis, A. Kluge, G. Kucharska, T. Kugathasan, M. LeBlanc, P. Leitao, M. Mager, P. Martinengo, M. Munker (now with U. Geneva), L. Musa, H. Pernegger, F. Piro, K. Rebane (also with Talinn University), F. Reidt, P. Riedler, I. Sanna (also with TU Munich), A. Sharma, W. Snoeys, C. Solans, M. Suljic, P. Svihra, G. Termo, M. Vicente (now with U. Geneva), J.B,. Van Beelen, J. Van Rijnbach (also with Oslo U.)

TPSCo: M. Nakamura, M. Suzuki, N. Takahashi
Tower Semiconductor Ltd: A. Fenigstein
Etesian Semiconductor Ltd: A. Haim, E. Toledano

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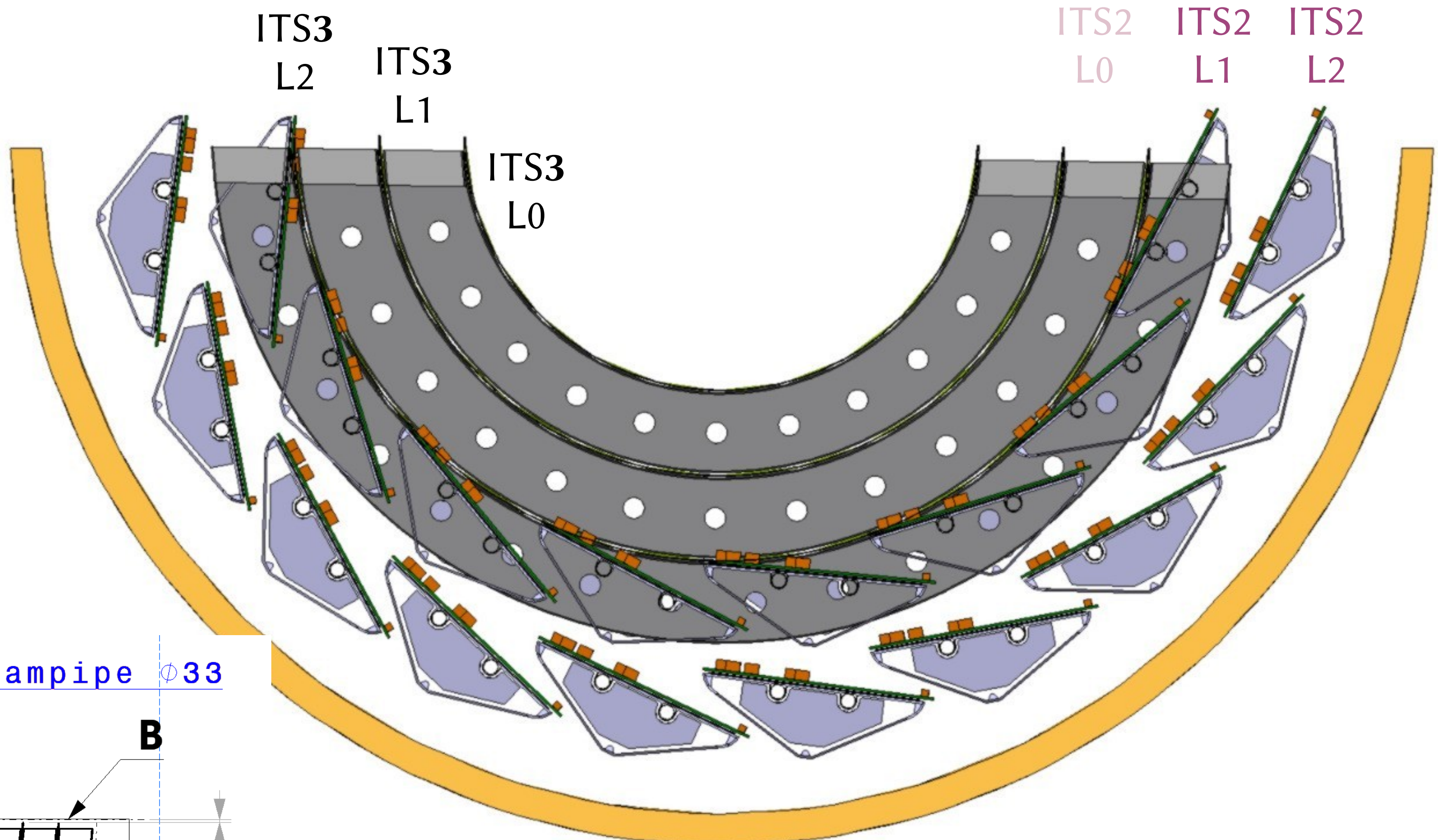
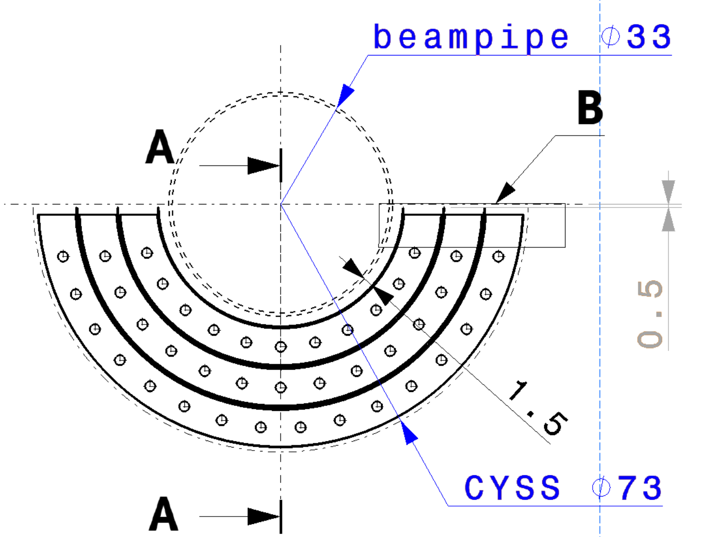
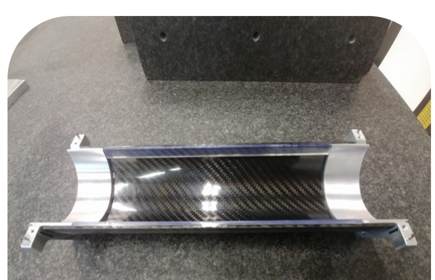
App. E – ITS3 mechanics

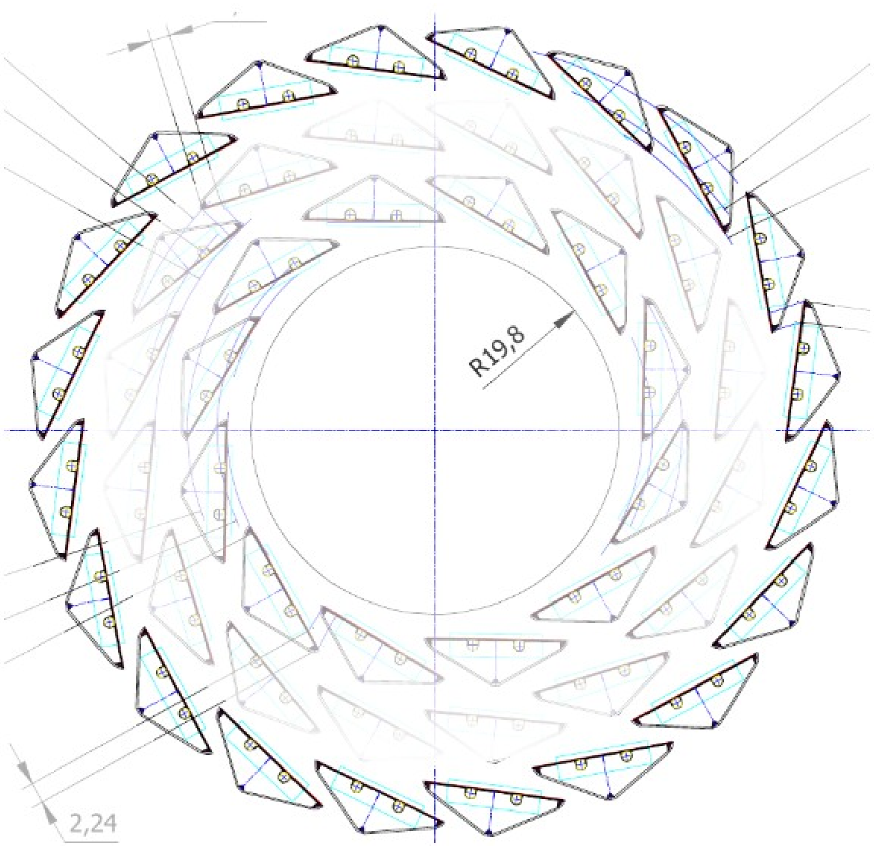
E.1 – ITS3 mechanics : layout sketch







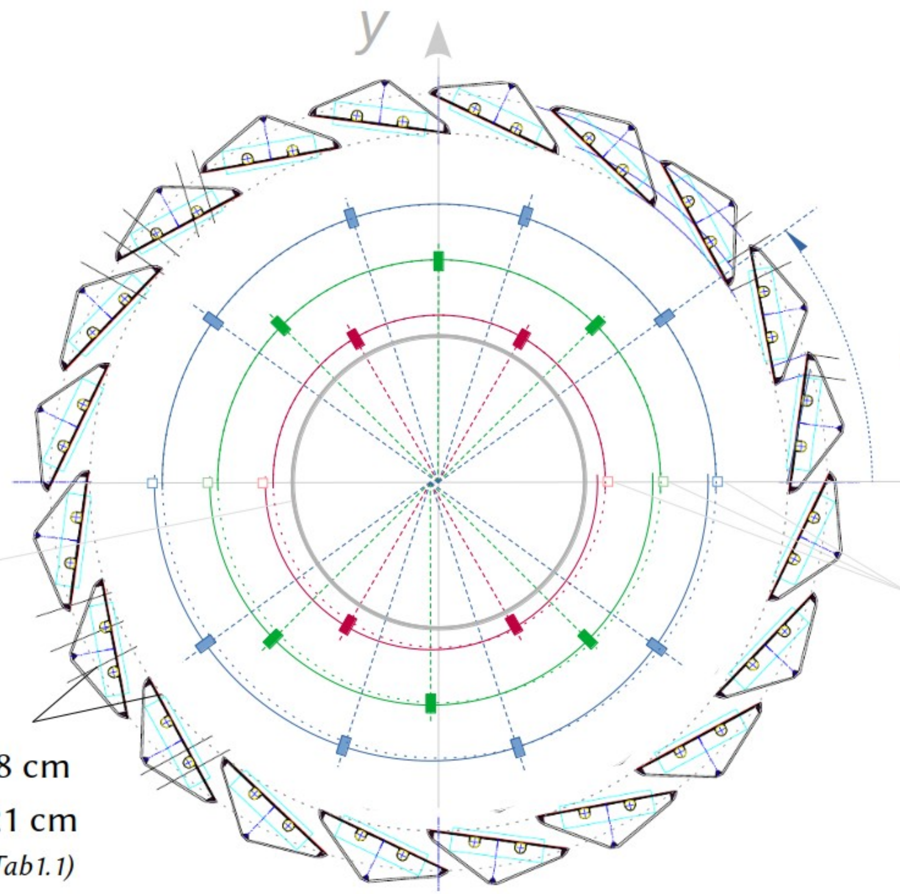
E.3 – ITS3 mechanics : layout sketch



Scale 1 cm ↔ 1 cm

beampipe

ITS2 **L2**
R_{min} = 3,78 cm
R_{max} = 4,21 cm
(TDR ITS2, Tab1.1)



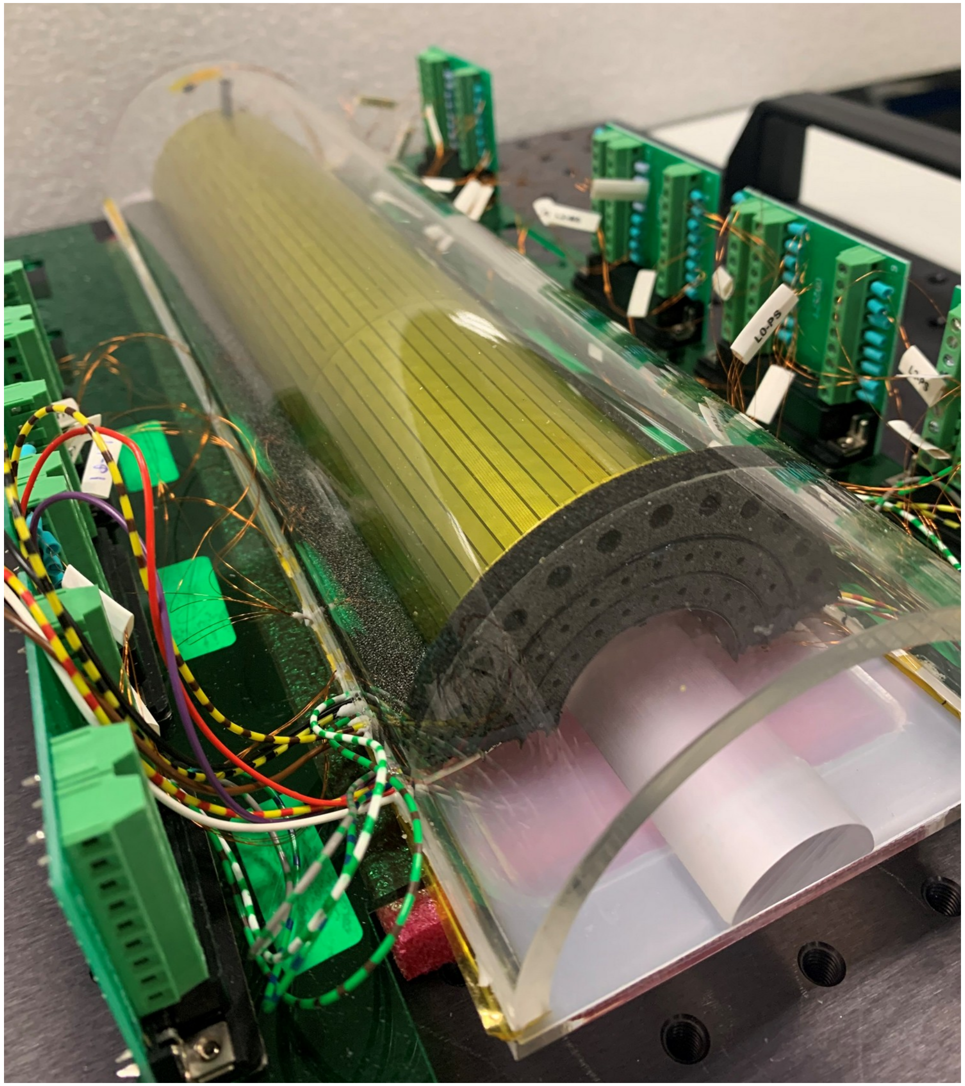
E.4 – ITS3 mechanics : mechanical integration

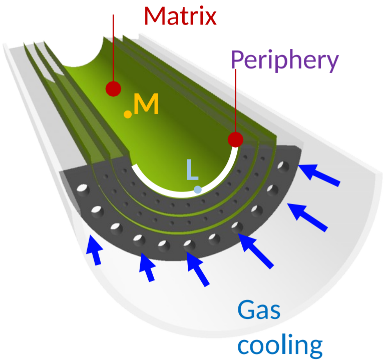
Engineering Model 2 (2022)

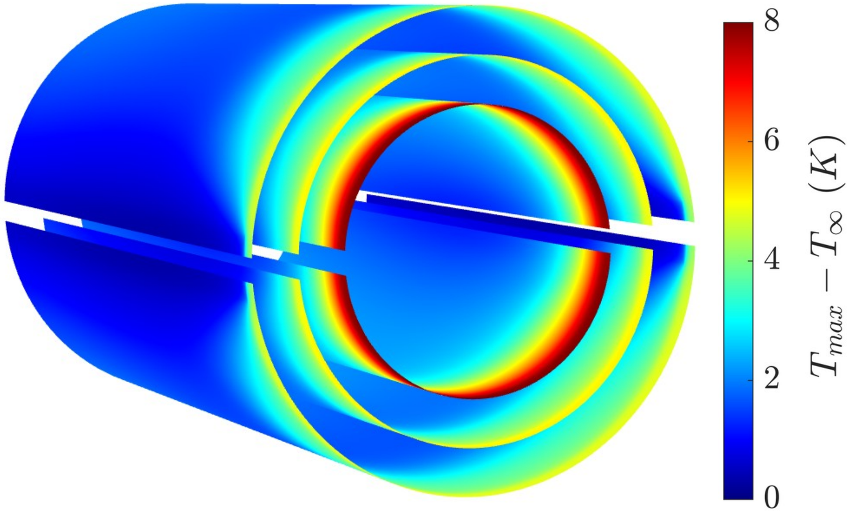
Items	Th. [µm]	L [mm]	Circ. [mm]
L0	40	280	56.5
L1	40	280	74.4
L2	40	280	93.2

Courtesy Corrado Gargiulo
ITS3 WP5

E.5 – ITS3 mechanics : wind tunnel



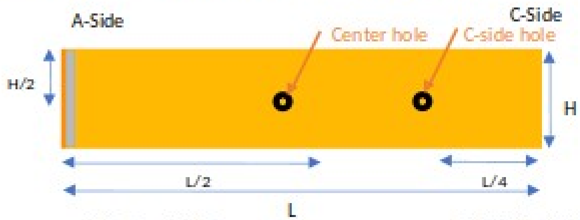


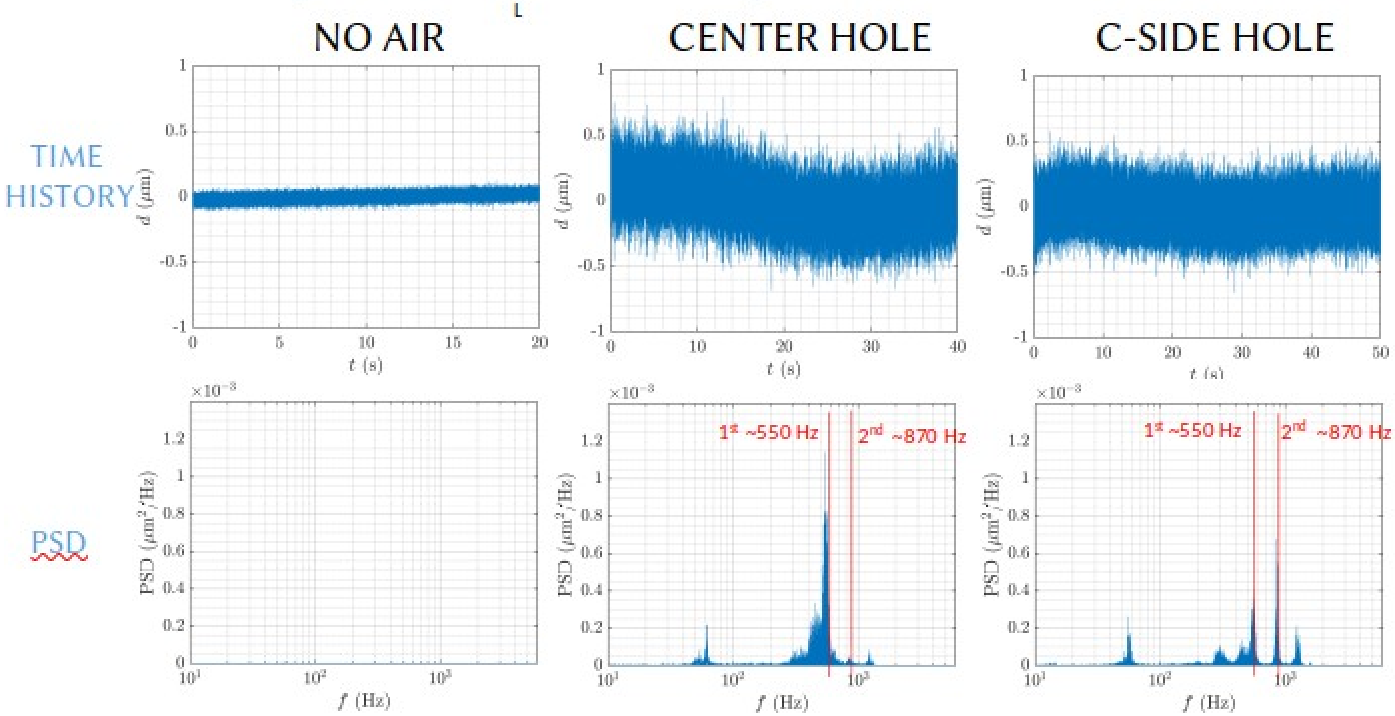


Temperature contours for v = 6 m.s^{-1}

E.6 – ITS3 mechanics : vibrations due to air flow

Maximum vibration level due to airflow measured on Layer2 is within ± **0.5 µm**



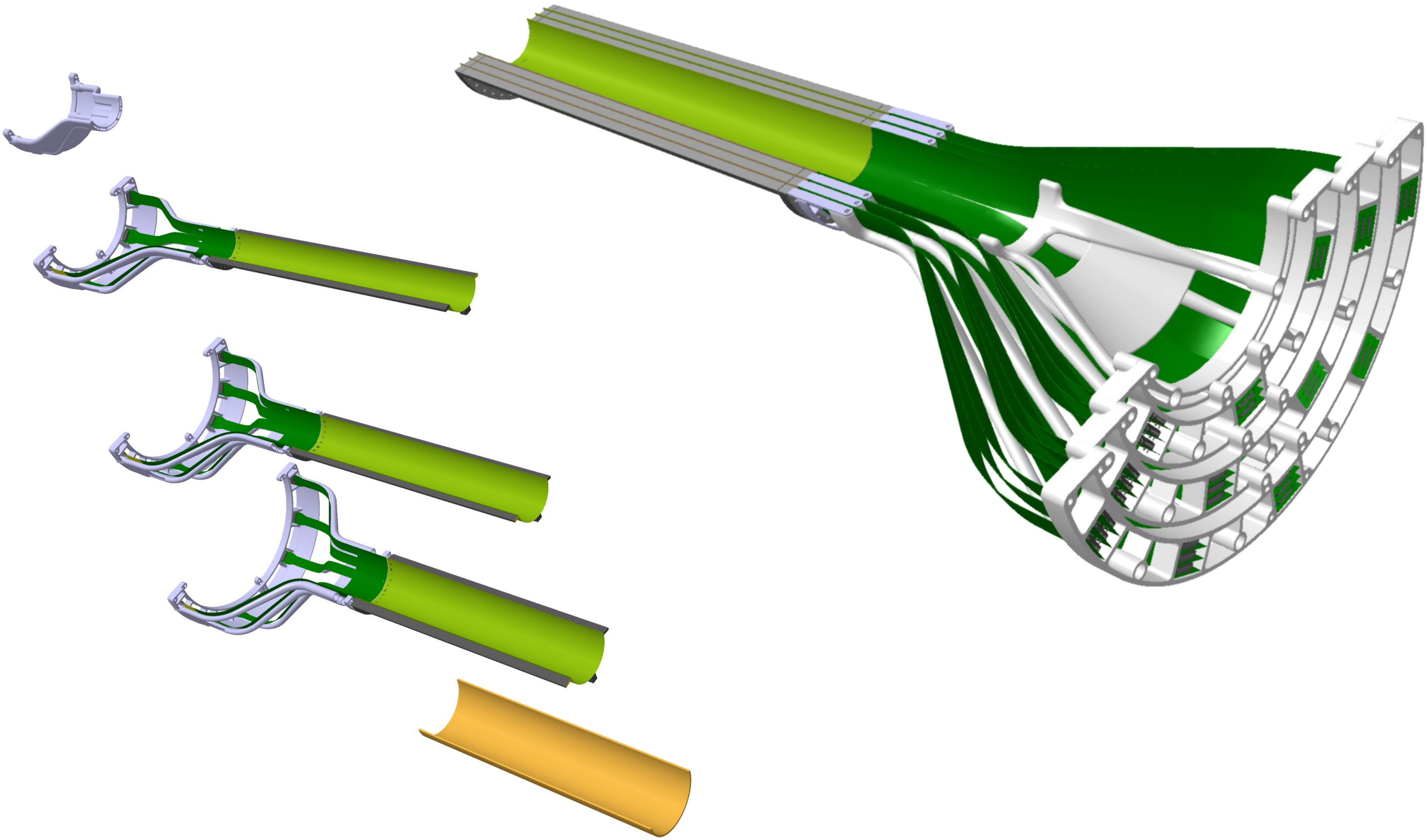


- Experimental test performed to assess dynamic stability of Layer 2 when exposed to 8 m/s air flow (maximum expected value)
- Noise with no air -> d m
- d m for 8 m/s
- Linearity (error) of the sensor md!! -> New sensors of lower error to be purchased

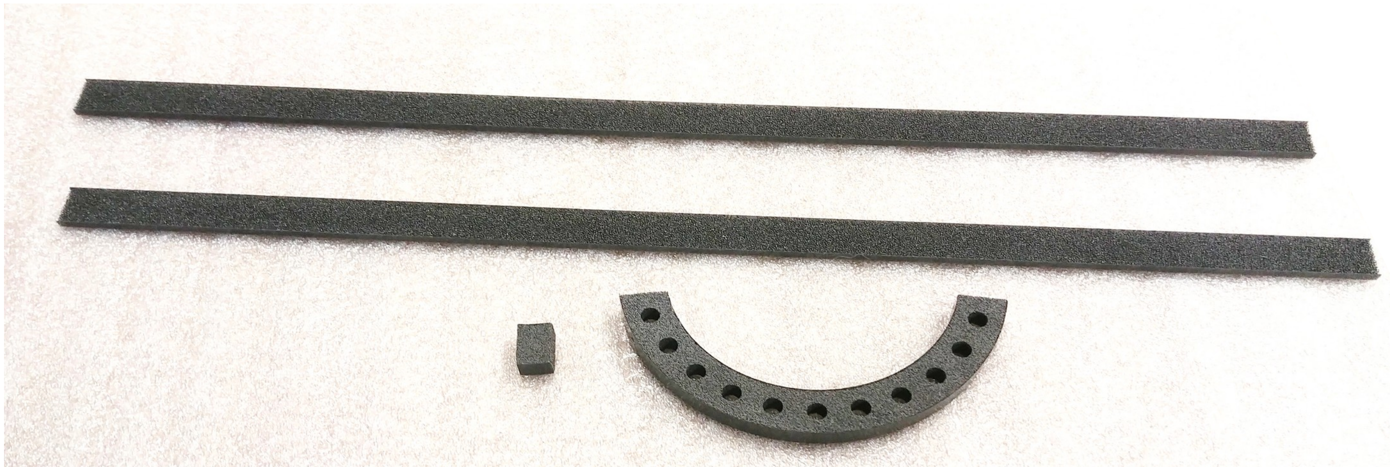
9

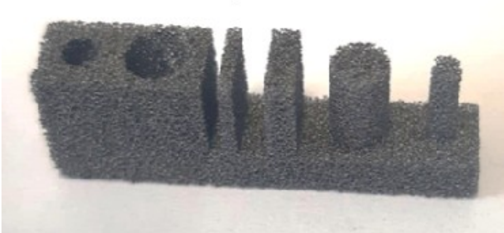
Corrado Gargiulo, WP5 ITS3 Plenary 2023-05

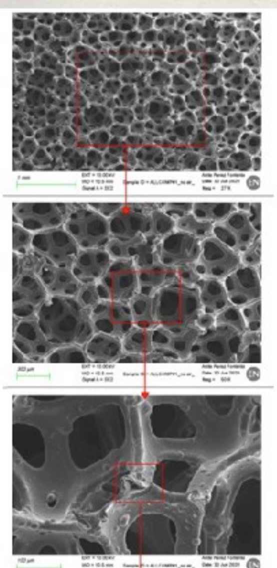
E.7 – ITS3 mechanics : Engineering Model 3



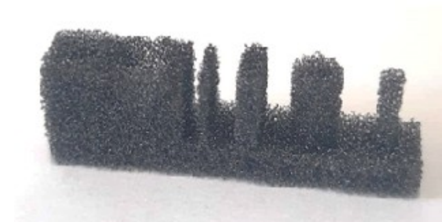
E.8 – ITS3 mechanics : mechanical integration

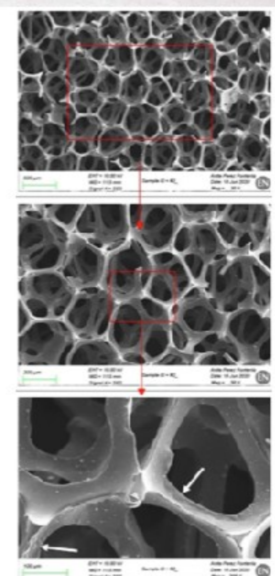






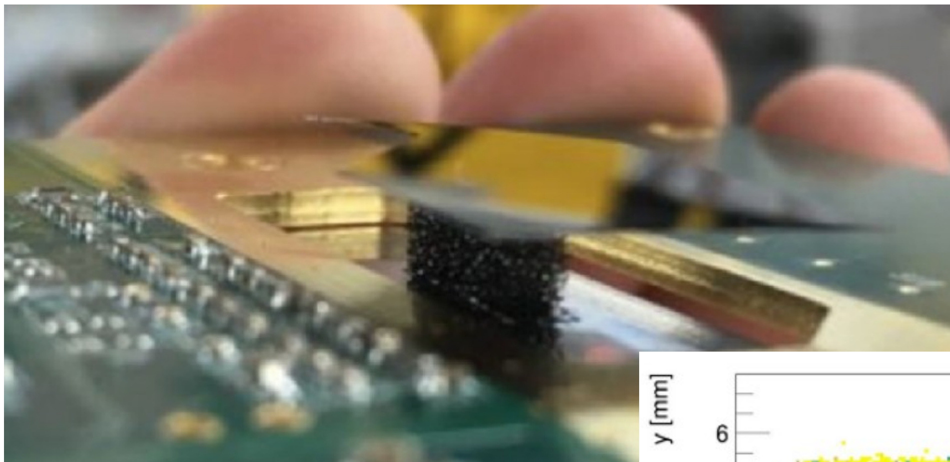
Rings :
ALLCOMP LD foam
ρ = 0.2 kg/dm³
k = 20 W/m.K



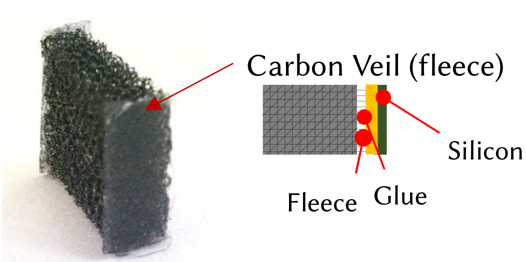


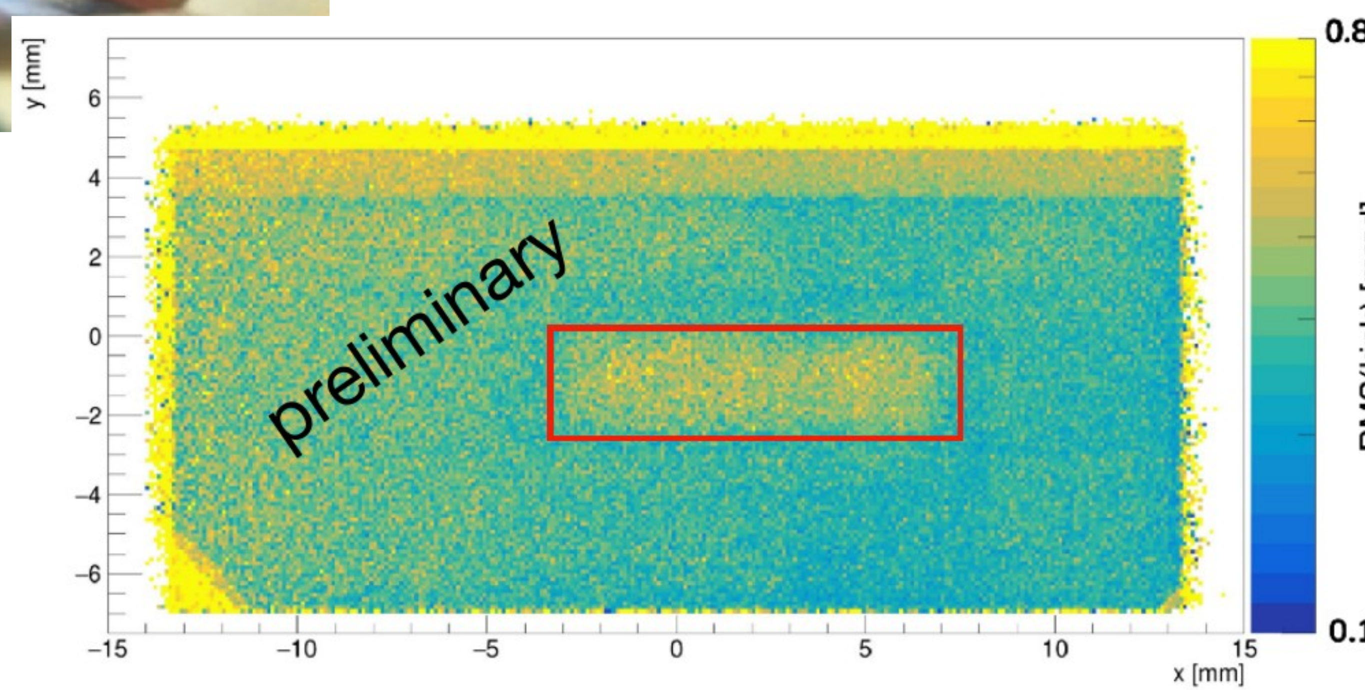
Longerons :
ERG DUOCEL foam
ρ = 0.07 kg/dm³
k = 0.05 W/m.K

E.9 – ITS3 mechanics : impact of carbon foam on material budget



- A sandwich of chip-foam-chip was brought to beam
- Scattering angle due to carbon foam is measured
- Very small (but visible) effect, as expected





Araldite 2011

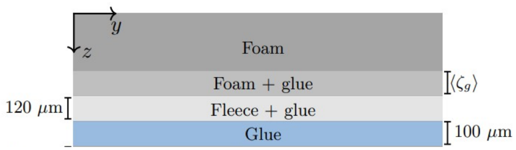
Minimized glue penetration
in the foam wedge

Fleece impregnated
with glue allows for glue control

M. Mager, CERN Detector Seminar 2021-09-24

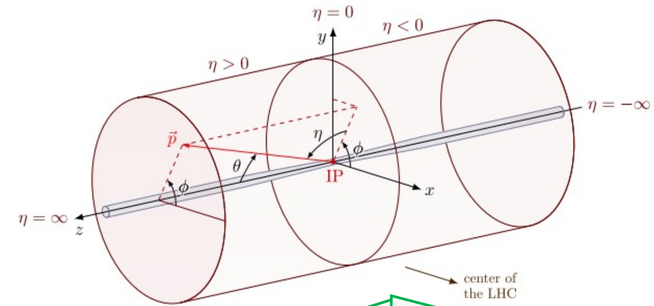
E.9 – ITS3 mecha. : impact of carbon foam on material budget

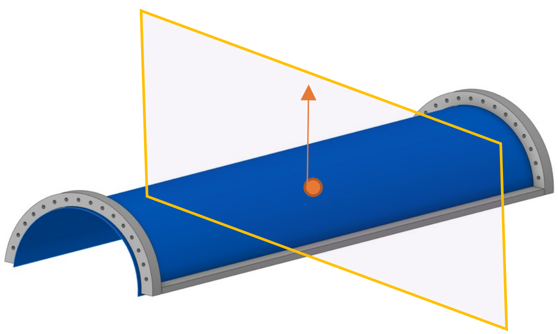
Thermal glue interface (less glue at the mechanical interface)

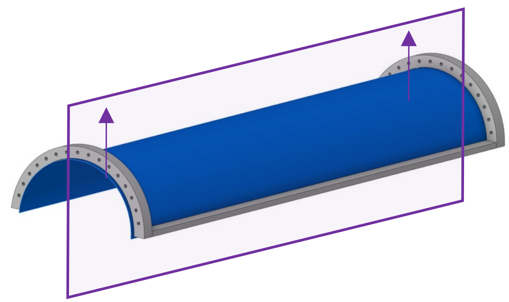


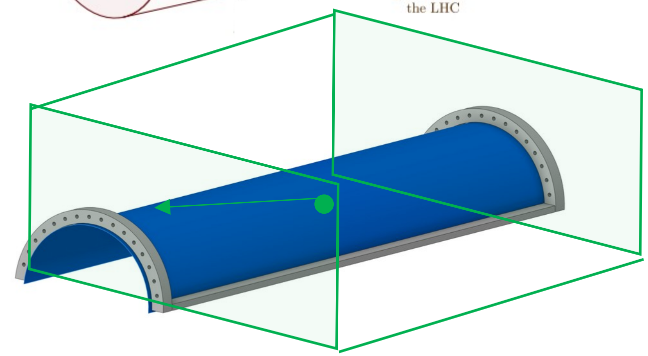
Baseline

180 µm glue penetration
120 µm Glue + Carbon Fleece
100 µm Glue (between Si-Carbon foam)

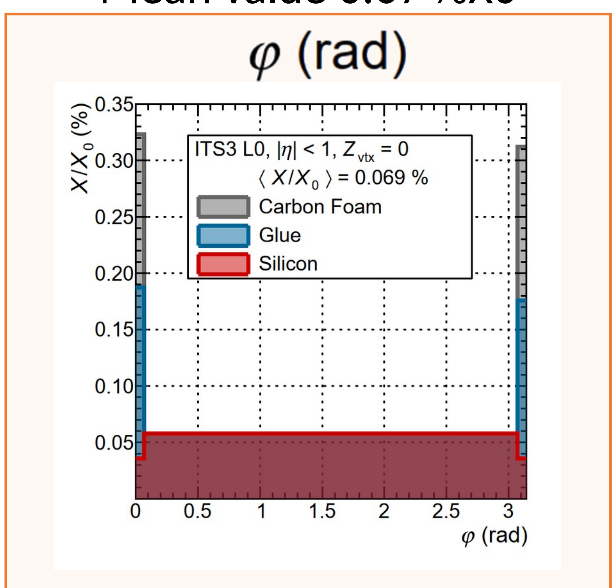




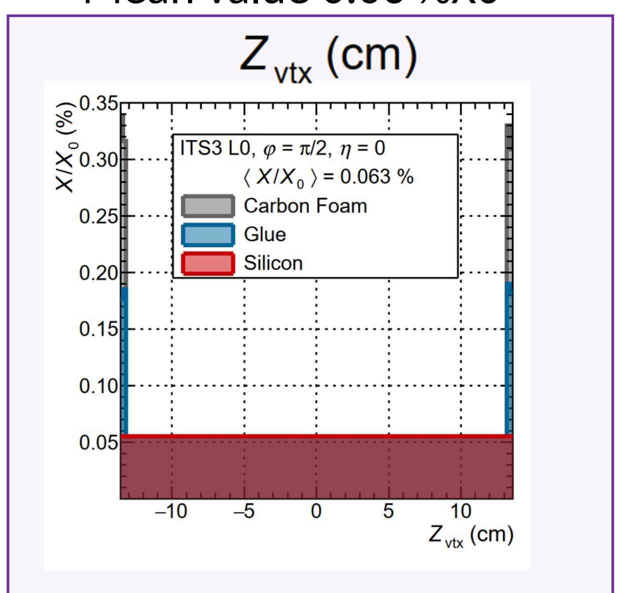




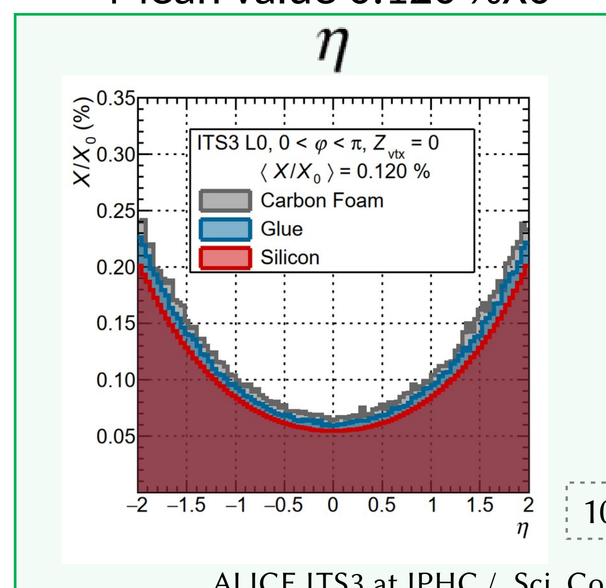
Mean value 0.07 %X0



Mean value 0.06 %X0



Mean value 0.120 %X0



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App. F – ITS3 as a project

F.1 – Synopsis : specifications (1), ITS2 vs ITS3

	ITS-2 (TDR)	**ITS-3** (LoI)
LHC period(s)	Run3 [2022-2025] + Run4	Run4 [2029-2032]
Number of layers	3+4	3 (*+4 ITS-2*)
beryllium pipe inner radius R_{pipe} (thickness ΔR)	1.82 cm [CERN-news] (0.08 cm, = 0.22% x/X_0)	1.6 cm (0.05 cm, = 0.14% x/X_0)
r_{L0} / r_{L1} / r_{L2} … r_{Last}	2.3 / 3.2 / 3.9 … *39.3 cm*	1.8 / 2.4 / 3.0 … *39.3 cm*
Magnetic field $B_{solenoid}$	0.2 and 0.5 T	0.2 and 0.5 T
Material budget per layer	0.3 % to *0.8 %* x/X_0	0.05 % to *0.8 %* x/X_0
CMOS technology	180 nm	65 nm *(180 nm)*
Pixel size	≈ 27 x 29 µm²	≈ 20 x 20 µm² (+ ≈ *27 x 29*) µm²
Size of *unitary* base sensor	≈ 1.53 x 3 cm²	≈ (5.6-9.5) x 27 cm²
Nb of sensors to assemble 3 inner layers	432	6 (!)
Non-Ionising Energy loss radiation	> 3.10^{12} 1-MeV $n_{eq}.cm^{-2}$	> 3.10^{12} 1-MeV $n_{eq}.cm^{-2}$
Total Ionising dose	> 0.3 Mrad	> 0.3 Mrad

F.2 – Synopsis : specifications (2), ITS2 vs ITS3

	ITS-2 (TDR)	**ITS-3** (LoI)
Consumed power (in the active volume, i.e. over the pixel matrix, ≠ in the periphery…)	< 35 mW/cm²	< 20 mW/cm²
Time resolution on hits	2-5 µs	≤ 2-5 µs
Time for charge collection per pixel	< 10 ns	≤ 1 ns
Spatial resolution	5 µm	≤ 5 µm
Coverage in η	|η| < 2,0 to *1,3*	|η| < 2,2 to *1,3*
$\varepsilon_{\text{tracking ITS}}$ ($p_T(h^{\pm})$ = X GeV/*c*)	1 GeV/*c* : 98% 0.1 GeV/*c* : ~60%	1 GeV/*c* : 98% 0.1 GeV/*c* : ~75%
Fake hit rate	<< 10^{-6} event^{-1}.pixel^{-1}	< 10^{-7} event^{-1}.pixel^{-1}
Particle hit density	5 MHz.cm^{-2}	8.5 MHz.cm^{-2}
Total costs [R&D + Construction] (+ beam pipe, out of the given project)	≈ 15.2 x10^6 CHF (…)	≈ 6.0 x10^6 CHF (1.5 x10^6 CHF)
Nb of institutes / Nb of countries	30 / 16	(≥19) / (≥ 8)

F.3 – ITS3 project : validation points towards TDR

1. Bending chips : with ALPIDE 180-nm
2. (MLR1) 65-nm validation in terms of radiation hardness + detection efficiency
3. (ER1) : stitching + foundry yields

Ultra-light mechanics and cooling

- mechanical concept to hold thin sensors "without" material
  - development of assembly procedure
  - qualification of carbon foams
- verification and optimisation of air cooling concept

Thinning, bending, interconnection

- development of procedures to handle and bend large thin chips
- characterisation of electrical and mechanical properties of sensors after bending
- development of electrical interconnection to bent chips

Wafer-scale sensor development

- switch to 65 nm technology (TPSCo)
  - verification of the technology for radiation tolerance and charge collection
- stitched sensor design and test
  - chip architecture
  - optimisation for yield

Courtesy Magnus Mager

F.4 – ITS3 project : current outline of the TDR

Contents

- TDR document and editorial team set up
- ALICE-internal procedure being defined
- Aiming at presentation to LHCC end 2023
- Targeting approval beginning 2024

Magnus Mager (CERN) | ITS3 | ALICE upgrade week | 09.05.2023 |

F.5 – ITS3 project : cost estimates for the whole ITS3

Project cost estimate breakdown for the whole ITS3 project (kCHF), ased on the ALICE ITS2 experience
Partial update wrt to LoI 2019 ?

i) the rising costs around **65-nm** Engineering Runs (foundry + tests)
- the costs of a foundry run which now amount to **650-700 k$ per run**, including post-processing like thinning and dicing (and not anymore 300-400 k$ like for the 180-nm technology node)
- **200-300 kCHF/run** for DAQ cards and tests

ii) **beam pipe** R&D (600 kCHF) and construction (900 kCHF) costs, now out of the ITS3 project itself + now covered by the ALICE collaboration as a whole.

Item	*R&D*	*Construction*	*Total Cost*
TOTAL	≈ 3450 *(LoI: ~~1900~~)*	≈ 2500 *(LoI: ~~3400~~)*	≈ 5950 *(LoI: ~~5300~~)*
Beampipe	*(LoI: ~~600~~)*	*(LoI: ~~900~~)*	*(LoI: ~~1500~~)*
Pixel CMOS sensors	3x700 = 2100 *(LoI : ~~600~~)*	700 *(LoI : ~~800~~)*	2800 *(LoI : ~~1400~~)*
Sensor test	3x250 = 750 *(LoI: ~~100~~)*	250 *(LoI: ~~150~~)*	1000 *(LoI: ~~250~~)*
Thinning & bending	200	300	500
Hybrid printed circuit	100	100	200
Mechanics	150	350	500
Assembly & test	50	200	250
Installation & alignment	-	200	200
Air cooling	100	150	250
Services	0	100	100
Patch panels	0	150	150

iii) middle-end readout Strategy
= update of Readout-units
i.e. new DSB (100 k€ for 3-layer ITS3)
+ 6-12 Extra CRU
≤ 6-12x (≈ 8k€/CRU)

2022-10 update of [ITS3-LoI] from 2019 (Section 7, p.29, Tab.8). See line by line explanation there

F.6 – ITS3 project : institutional partners and cost sharing

• CERN	≈ 2 M€
• Italy (INFN+Universities)	≈ 2 M€
• France (IN2P3+)	⟶ *TBD*
• the Netherlands (NIKHEF, Utrecht)	N/A ?
• Korea (Inha, Yonsei, Pusan)	≈ 300 k€
• Sweden (Lund)	≈ 300 k€
• Norway (Bergen, USN Vestfold)	≈ 300 k€
• Czech Republic (Prague Univ., Prague Nation. Acad. of Sci.)	≈ 150 k€
• USA (Berkeley, BNL ? LNL ? Stanford ? (*if USA are in, synergies with EIC and/or Cool Copper Collider*)	N/A ?

F.7 – ITS3 project : global milestones and timeline, Gantt

Milestone	Date	Comment
ER1 tape out	done!	
ER2 spec review	last steps	
ER1 sensors on bench	Jun 2023	
ER1 first test results	**Sep 2023**	
TDR	**Oct 2023**	
ER2 tapeout	**Feb 2024**	
ER2 produced & diced	Sep 2024	
ER2 first test results	**Dec 2024**	
QM (ER2 half-barrel)	**Feb 2025**	
ER3 EDR	Mar 2025	
ER3 tape out	**Jun 2025**	
ER3 produced & diced	Jan 2026	
ER3 qualified	**Apr 2026**	
FM (ER3 full detector)	**Jul 2026**	
commissioned	**Sep 2026**	
start of installation	**Nov 2027**	includes lumped contingency

Contingency

Magnus Mager, 9 May 2023, ALICE Upgrade Week 2023-05

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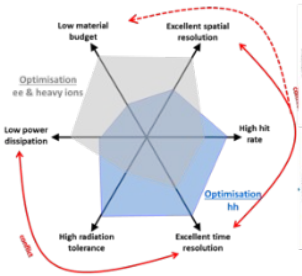
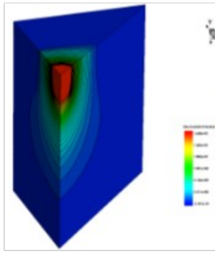
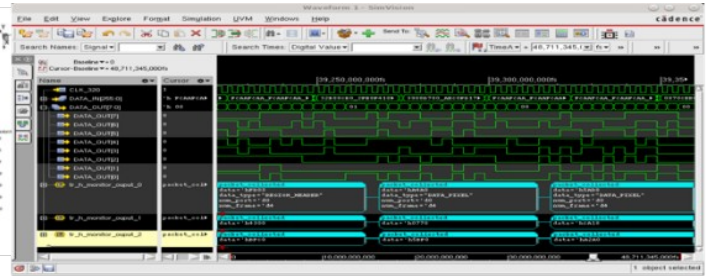
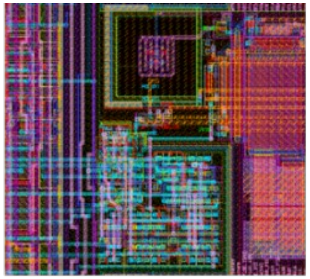
App. G – IPHC in the ITS3 project

G.1 – IPHC C4π platform : from chip design to integration









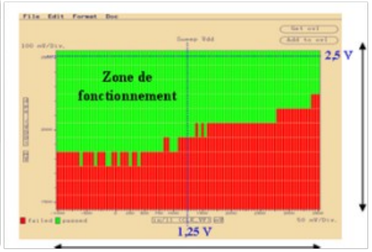
Transcription of the experiment's constraints into electronics specs. & Architectures

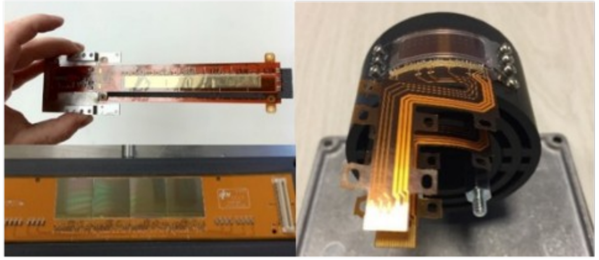
Evaluation of suitable CMOS processes
- TCAD Simulation & Optimization
  → Design validated by prototyping

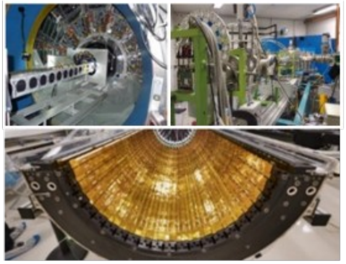
- Front-End Electronics Design
  - Very low noise and power
  - Robustness design (> 1M pixels), DfT
- Functional blocks (IP) for MAPS => SoC
  - A.w.a Complex Gates + Liberate Modelling

- System Design / Architecture of MAPS
  - Digital on Top Design & Verification Flow
  - Cadence Flowkit & UVM / systemVerilog
    - ✓ HDL modeling, synthesis,
    - ✓ Floorplan, IR-Drop, Routing + CTS, PostSim

Interaction with :
- CMOS foundries for specific manufacturing
- Post processing companies
  - ✓ Thinning, Dicing, ...







Design of Test and DAQ benches for:
- Functional test of sensors on probed wafers
- At Lab, Characterization :
- On Experimental Site

Characterization of Sensors and IP blocks
- At laboratory : X Fe55, Beta Sr90, laser
- On the experimental sites: beams, irradiations

Design, Integration and Test
- Detection systems based on MAPS (ladders)

Construction & Installation on sites
- STAR (USA)
- BEAST-BELLE2 (Japan)
- ALICE (Switzerland)

Courtesy Christine Hu

G.2 – IPHC C4π platform : from chip design to integration

Technical coordination

Architecture's definition

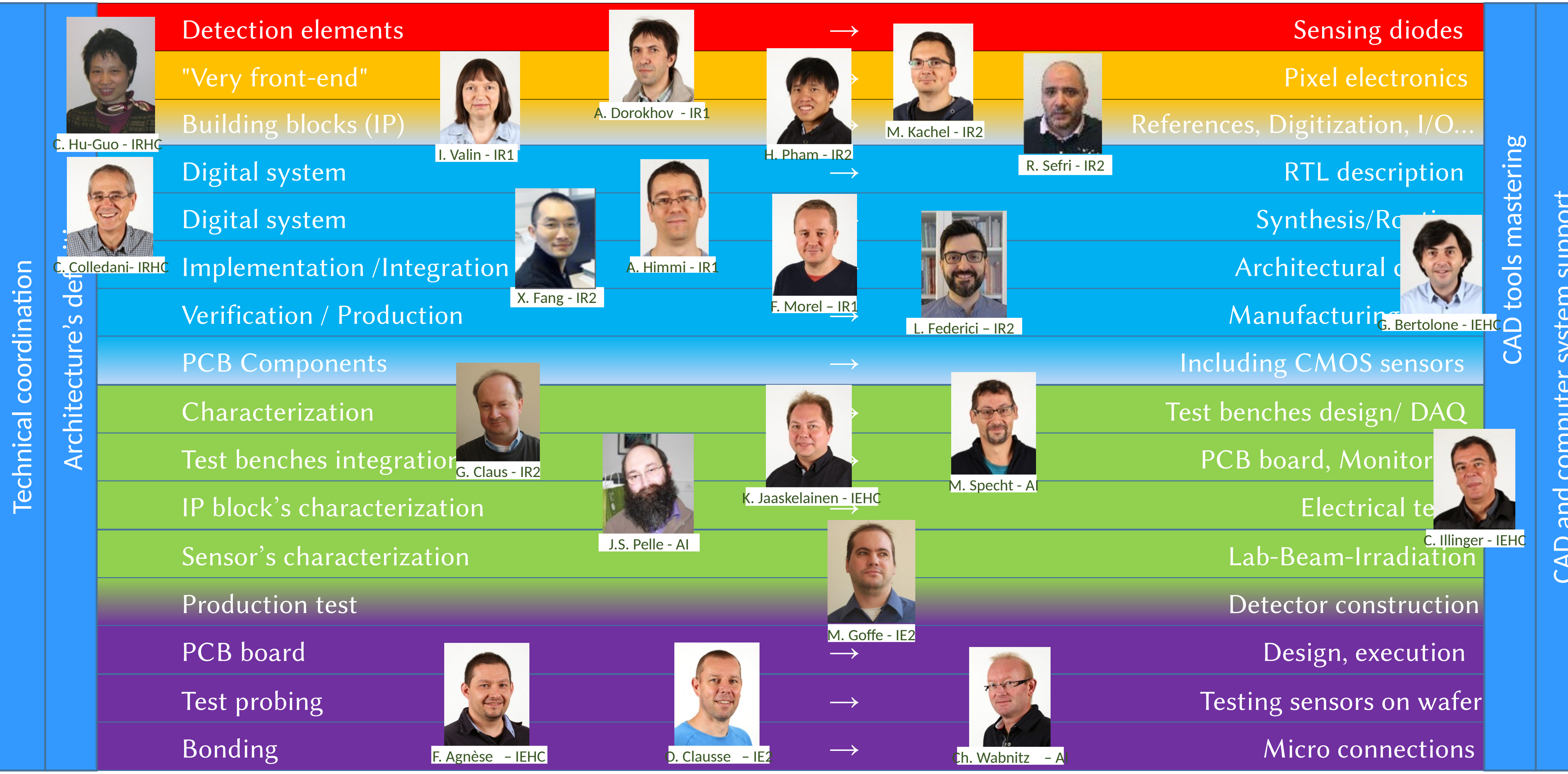
Detection elements	→	Sensing diodes
"Very front-end"	→	Pixel electronics
Building blocks (IP)	→	References, Digitization, I/O...
Digital system	→	RTL description
Digital system	→	Synthesis/Routing
Implementation /Integration (DoT)	→	Architectural design
Verification / Production	→	Manufacturing rules
PCB Components	→	Including CMOS sensors
Characterization	→	Test benches design/ DAQ
Test benches integration	→	PCB board, Monitoring
IP block's characterization	→	Electrical tests
Sensor's characterization	→	Lab-Beam-Irradiation
Production test	→	Detector construction
PCB board	→	Design, execution
Test probing	→	Testing sensors on wafer
Bonding	→	Micro connections

CAD tools mastering

CAD and computer system support

Courtesy Christine Hu

G.2 – IPHC C4π platform : from chip design to integration



21 persons (2022-10)

Courtesy Christine Hu

G.3 – ALICE-ITS3 & BelleII-VTX : simultaneously at C4π

Schedules overlap **BUT** Fits person-power & expertise available

- Sensor design: [2022-2024]
  - 3-4 FTEs for each project
  - → 7 FTEs in total for 10 available
  - leaving 3 FTEs for MAPS R&D (in synergy with ITS3)
- Sensor tests: [2023-2025]
  - Modest requirement ~1 FTE/project
  - thanks to commitment of Experiment collaboration teams
- Integration: [2023-2026/27]
  - ITS3 ~R&D tasks and small production
  - VTX, mostly production
  - Still close to saturate C4Pi staff in 2024-26
    → to be monitored closely

→ Detailed project planning for C4Pi under discussion with IPHC directorate, to be validated by platform COPIL – March 2023

Common slide J.Baudot (BelleII) and A.Maire (ALICE)

G.4 – Synopsis : signatories IPHC

In gray = persons identified on technical aspects

- group ALICE :

  Iouri BELIKOV (50-75%), Boris HIPPOLYTE (15-25%), Christian KUHN (20%), Antonin MAIRE (40-80%), Fouad RAMI (retired 2023-12), Christelle ROY, Yves SCHUTZ (retired 2019, emeritus)
  Marc IMHOFF (80%)
  (doctorants: Alexandre BIGOT, Romain SCHOTTER, Yongzhen HOU, Yitao Wu)

- group PICSEL :

  Auguste BESSON (5%), Ziad El Bitar (5%), Serhiy SENYUKOV (30-50%)

- plateform C4π :

  Jérôme BAUDOT (5%), Claude COLLEDANI (5%), Christine HU (15%), Gilles CLAUS (5%)
  Frédéric MOREL (50-70%),

  . design CMOS : Andrei DOROKHOV (70%), Xiaochao FANG (100%), Thanh Hung PHAM (15%), Isabelle VALIN (15%), Grégory BERTOLONE (20%), Abdelkader HIMMI (15-50%)

  . microconnectique : Franck AGNESE (30%), Olivier CLAUSSE (10%), Christophe WABNITZ (10%)

  . tests : Kimmo JAASKELAINEN (50-100% mais sur CE65v1+v2),

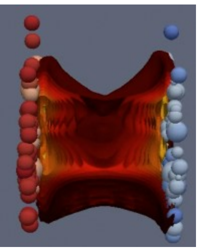
  (doctorants: Jean SOUDIER (50%, arch. numérique), Corentin LEMOINE (>50%, analogique))

Back to App. TOC

App. H – ITS3 physics

H.1 – Physics incentives : summary

g + u,d,s,c,b (t) <=>



Madai

u,d,s

- $\pi^\pm$ π^0 $K^\pm$ K^0_S … p Λ $\Sigma^\pm$(*uus*) $\Xi^\mp$ (*dss*), $\Omega^\mp$(*sss*) …

  η(547) ω(782) … K^0(892) ϕ(1020) $\Sigma^\pm$(1385) Λ(1520) Ξ^0(1530)

  + d t $^3He^{2+}$ $^4He^{2+}$ …
  + $^3_\Lambda H$, $^4_\Lambda \overline{He}^{2+}$ $\rightarrow$ $^3He^{2+}$ p π^- .

c

- (D^0 D^+ D^{*+} D_S^+)… η_c J/ψ χ_{Ci} ψ(2S) …

  Λ_C^+(*udc*) $\rightarrow$ p$K^-\pi^+$ or pK^0s (*cτ* ≈ 60 μm)

  Ξ_C^+(*usc*) $\rightarrow$ p$K^-\pi^+$ or $\Xi^-2\pi^+$ (*cτ* ≈ 136 μm)

  Ξ_C^0(*dsc*) $\rightarrow$ $\Xi^-\pi^+$ (*cτ* ≈ 45 μm)

  Ω_C^0(*ssc*) $\rightarrow$ $\Omega^-\pi^+$ (*cτ* ≈ 80 μm)

  + *c*-deuteron $(\Lambda_c n)^+$ $\rightarrow$ d$K^-\pi^+$? *c*-triton $(n\Lambda_c n)^+$?

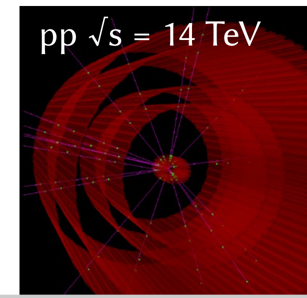
b

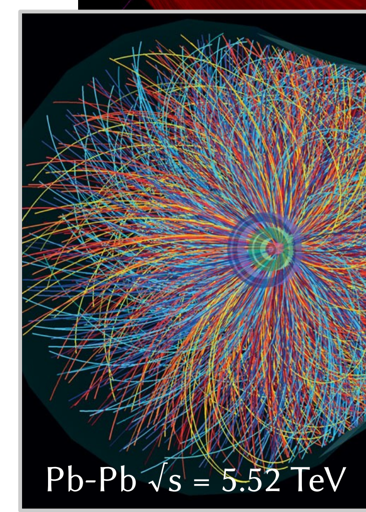
- heavy-flavour ($\mu^\pm$, $e^\pm$)
- B^0 $B^\pm$ B^0_S … Υ(1S,2S,3S)…

  Λ_b^0 (*udb*) …

(• $e^\pm$ $\mu^\pm$ γ)

(• $W^\pm$ γ/Z°)

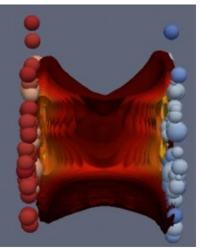




1. improve low-p_T Axε for stable particles

H.1 – Physics incentives : summary

$g + u,d,s,c,b\ (t)$ <=>



Madai

u,d,s

- $\pi^{\pm}\ \pi^{0}\ K^{\pm}\ K^{0}_{S}$ … $p\ \Lambda\ \Sigma^{\pm}(uus)\ \Xi^{\mp}(dss),\ \Omega^{\mp}(sss)$ …

  $\eta(547)\ \omega(782)$ … $K^{0}(892)\ \phi(1020)\ \Sigma^{\pm}(1385)\ \Lambda(1520)\ \Xi^{0}(1530)$

  + $d\ t\ {}^{3}He^{2+}\ {}^{4}He^{2+}$ …

  + ${}^{3}_{\Lambda}H,\ {}^{4}_{\Lambda}\overline{He}^{2+} \rightarrow {}^{3}He^{2+}\ p\ \pi^{-}$.

c

- $(D^{0}\ D^{+}\ D^{*+}\ D_{S}^{+})$… $\eta_{c}\ J/\psi\ \chi_{Ci}\ \psi(2S)$ …

  $\Lambda_{C}^{+}(udc) \rightarrow pK^{-}\pi^{+}$ or $pK^{0}s$ $(c\tau \approx 60\ \mu m)$

  $\Xi_{C}^{+}(usc) \rightarrow pK^{-}\pi^{+}$ or $\Xi^{-}2\pi^{+}$ $(c\tau \approx 136\ \mu m)$

  $\Xi_{C}^{0}(dsc) \rightarrow \Xi^{-}\pi^{+}$ $(c\tau \approx 45\ \mu m)$

  $\Omega_{C}^{0}(ssc) \rightarrow \Omega^{-}\pi^{+}$ $(c\tau \approx 80\ \mu m)$

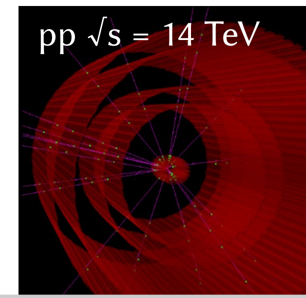
  + *c*-deuteron $(\Lambda_{c}n)^{+} \rightarrow dK^{-}\pi^{+}$? *c*-triton $(n\Lambda_{c}n)^{+}$?

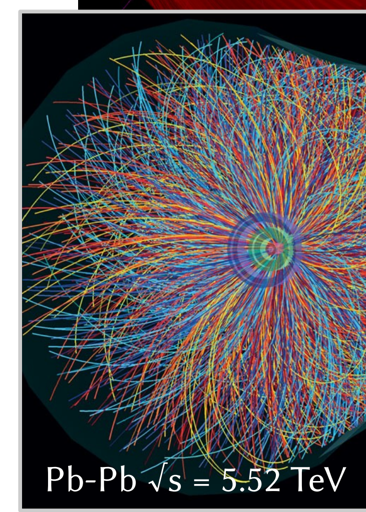
b

- heavy-flavour $(\mu^{\pm}, e^{\pm})$
- $B^{0}\ B^{\pm}\ B^{0}_{S}$ … $\Upsilon(1S,2S,3S)$…

  $\Lambda_{b}^{0}(udb) \rightarrow \Lambda_{C}^{+}\pi^{-}$ …

(• $e^{\pm}\ \mu^{\pm}\ \gamma$)
(• $W^{\pm}\ \gamma/Z^{\circ}$)

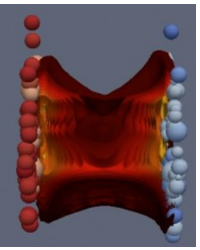


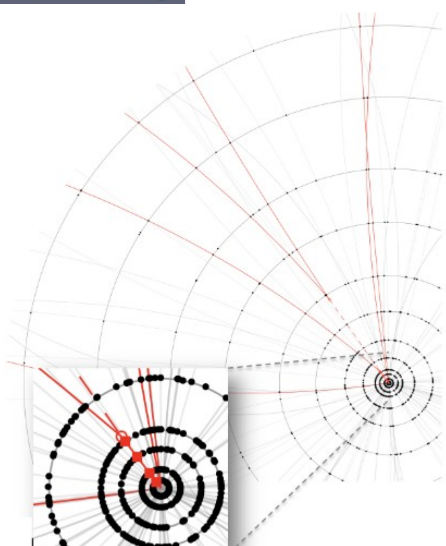


1. improve low-p_{T} Axε for stable particles
2. improve track pointing resolution : displaced vertexing, prompt/non-prompt

H.1 – Physics incentives : summary

$g + u,d,s,c,b\ (t)$ <=>





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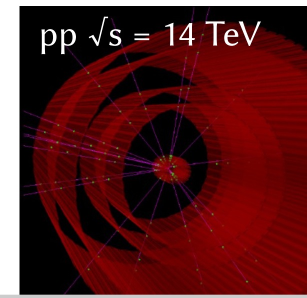
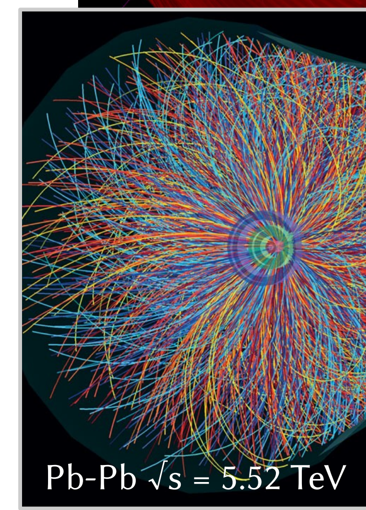
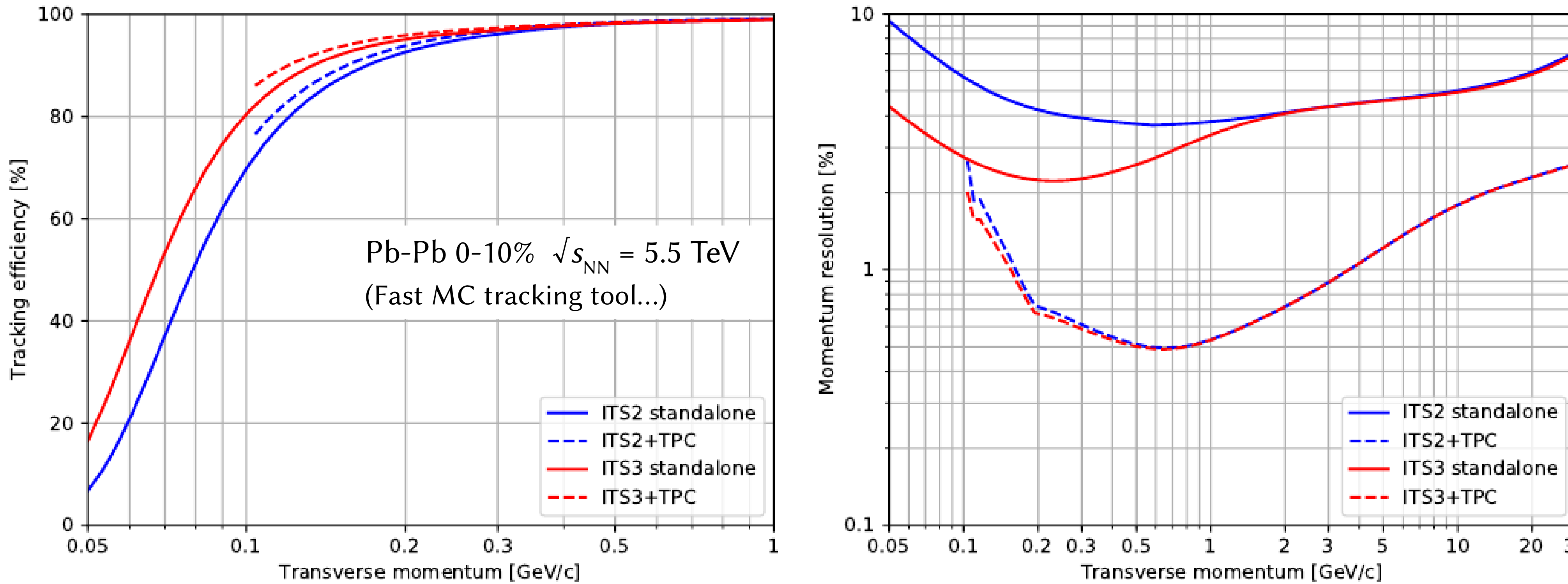




1. improve low-p_{T} Axε for stable particles
2. improve track pointing resolution : displaced vertexing, prompt/non-prompt
3. "strangeness tracking" [hits left by charged $\Xi^{\mp}(dss)$, $\Omega^{\mp}(sss)$, $\Sigma^{\pm}(uus)$]

H.2 – Physics incentives : improve low-p_T $A\times\varepsilon$

Fig.12, EoI ITS-3, ALICE-PUBLIC-2018-013



→ Importance to be as efficient as possible in low p_T detection, on an event-by-event basis …

Why ? crucial to study correlation between particles, get the particle of interest in its QCD context.
QCD+QGP physics happen essentially at *low* and *intermediate* p_T

… "Low p_T", but how low ?!

H.3 – 1st reason to commit : physics analyses

Heavy quarks (c,b) facing collectivity

- total cross-section of charm production for $p_T>0$ and $y \approx 0$ (baryons, mesons, quarkonia)
- single-charm baryons : $\Lambda_C^+(udc)$, $\Xi_C^+(usc)$, $\Xi_C^0(dsc)$, $\Omega_C^0(ssc)$ (with strangeness tracking)

→ hadronization of charmed quarks (recombination mechanisms)

+ their sensitivity to the QGP medium (hydrodynamisation, chemical equilibration, thermalisation / transport coefficients)

ITS3 help : a drastic increase in the significance of the reconstructed signal + in the spatial precision

(increasingly complex decay topologies, typically ranging from 2 to 6 bodies)

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Interactions between hard partons and with medium constituents

- intra-jet modifications (jet shapes, jet structures, reconstructed using charged particles)
- interplay between jets and surrounding underlying-event
- di-jets with flavour-tagging (*i.e.* complete topological reconstruction of heavy mesons and baryons within the jets)

→ measurements on the energy losses of charm and beauty as a function of multiplicity/centrality

ITS3 help : high granularity + access to the tracks that make up the jets down to low p_T^{track}

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ITS3 help : high granularity + access to the tracks that make up the jets down to low p_T^{track}

Correlations between rapidity domains

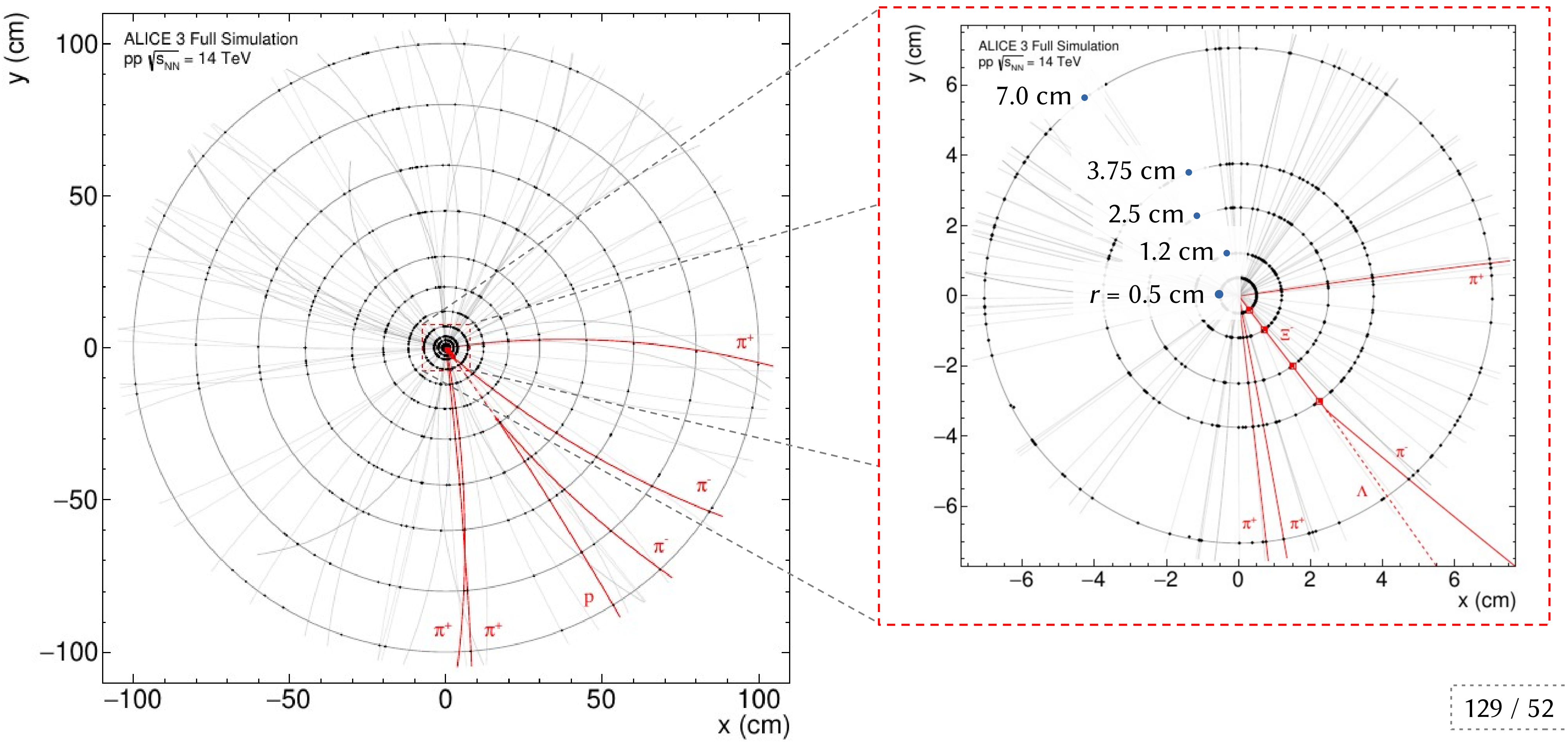
- correlation ITS3 ($|y|$ < 2.2) + MFT (y fwd)

→ map the event activity over a large y range

ITS3 help : ITS3 standalone tracking

H.4 – Physics : strangeness tracking, example of ALICE3

Figure 18: (left) Illustration of strangeness tracking from full detector simulation of the Ξ_{cc}^{++} decay into $\Xi_c^+ + \pi^+$ with the successive decay $\Xi_c^+ \to \Xi^- + 2\pi^+$. (right) Close-up illustration of the region marked with a red dashed box in the left figure, containing the five innermost layers of ALICE 3 and the hits that were added to the Ξ^- trajectory (red squares).



ALICE3 LoI, *CERN-LHCC-2022-009*

Back to App. TOC

App. I – LPSC Grenoble, ITS3 activities

Note d'organisation KDP2 (vFinale, 04 mai 2023)

I.2 – ALICE France : livrables français pour ITS3

1.a Conception de la matrice de pixels [IPHC]
- au niveau analogique (collection de charge et électronique de front-end)
- au niveau digital (traitements numériques et gestion de la puissance)

1.b Qualification et tests des prototypes CMOS soumis pour fonderie [IPHC, +IP2I]

2.a Cartes de l'électronique de *middle-end* (lecture, pilotage, alimentation d'ITS3) [LPSC]
- Conception des cartes
- Production des cartes
- Intégration mécanique et optronique (conception et réalisation des supports mécaniques)

2.b Pièces mécaniques pour le circuit de refroidissement [LPSC]

3. Intégration et micro-connectique électroniques en vue de l'installation finale [IPHC]

4. Assemblage d'un détecteur selon le plan de sauvegarde (Super ALPIDE) [IPHC]

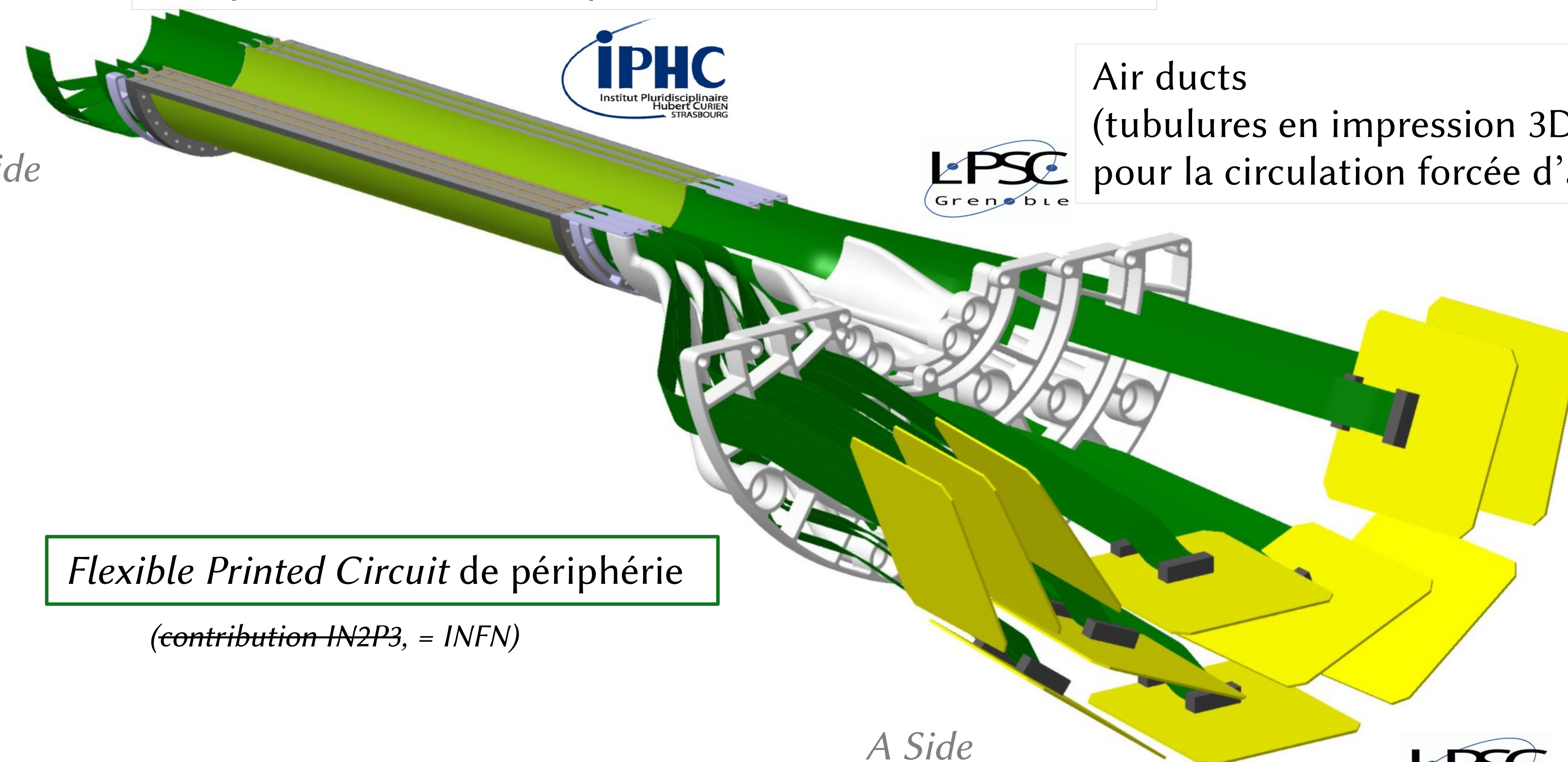
NB :
- ~~Calculs~~
- ~~algorithmes de reconstr° évts~~ (vertexing, tracking, alignement, simulations) + lien ~~reconstr° ITS2+3~~

  = relégués aux missions courantes des trois équipes ALICE [IPHC, IP2I, LPSC]

  ⟶ pas de livrable précis attendu de la part de la communauté française.

I.2 – Se repérer dans l'ITS3 : périphérie immédiate

(1 capteur stitché / hémicylindre) x 2 demi x (3-4 couches)



Air ducts
(tubulures en impression 3D,
pour la circulation forcée d'air)

Flexible Printed Circuit de périphérie

(~~contribution IN2P3~~, = INFN)

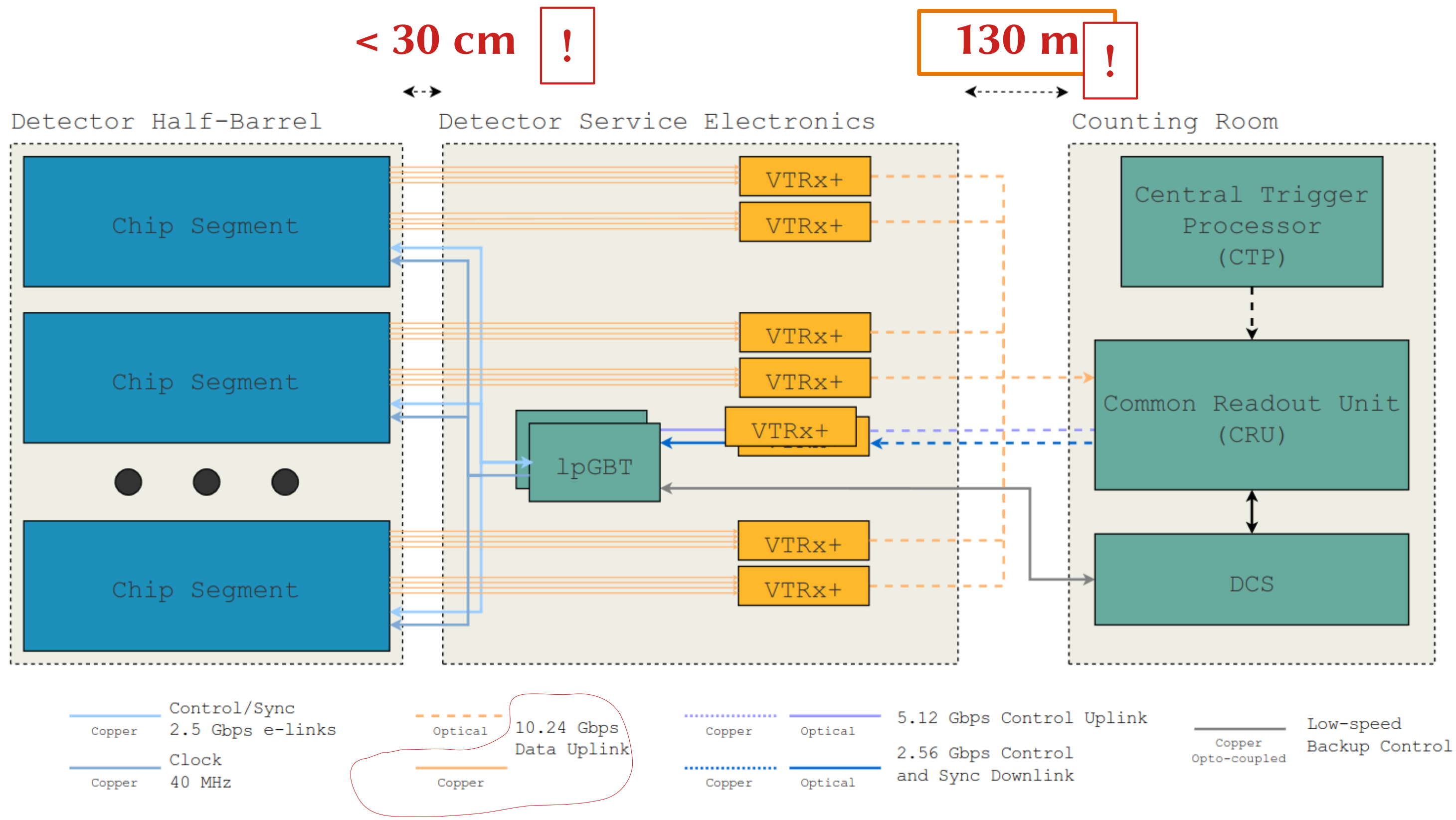
Cartes (readout+power), *Detector Service Boards* :
conception et production de l'électronique,
+ intégration mécanique

Corrado Gargiulo, WP5 ITS3 Plenary 2023-04

I.3 – Work breakdown : 2. électronique “middle-end”

A. Optronique de lecture + B. Électronique de contrôle-commande (DCS)

- Direct connection between detector and optical transceiver (VTRx+)
  - ! No data processing
  - lpGBT encoding
- Slow control via lpGBT
  - E-links to detector
- Multiple boards with board-to-board connections for control and power
  - A master board for control
- Radiation qualified CERN-developed components



! Difficulté claire de maintenir une telle cadence à travers des lignes Cu sur des distances > $O[10\text{ cm}]$

Ola Gröttvik, WP6, ITS3 Plenary 2023-05

I.2 – Se repérer dans l'ITS3 : périphérie immédiate

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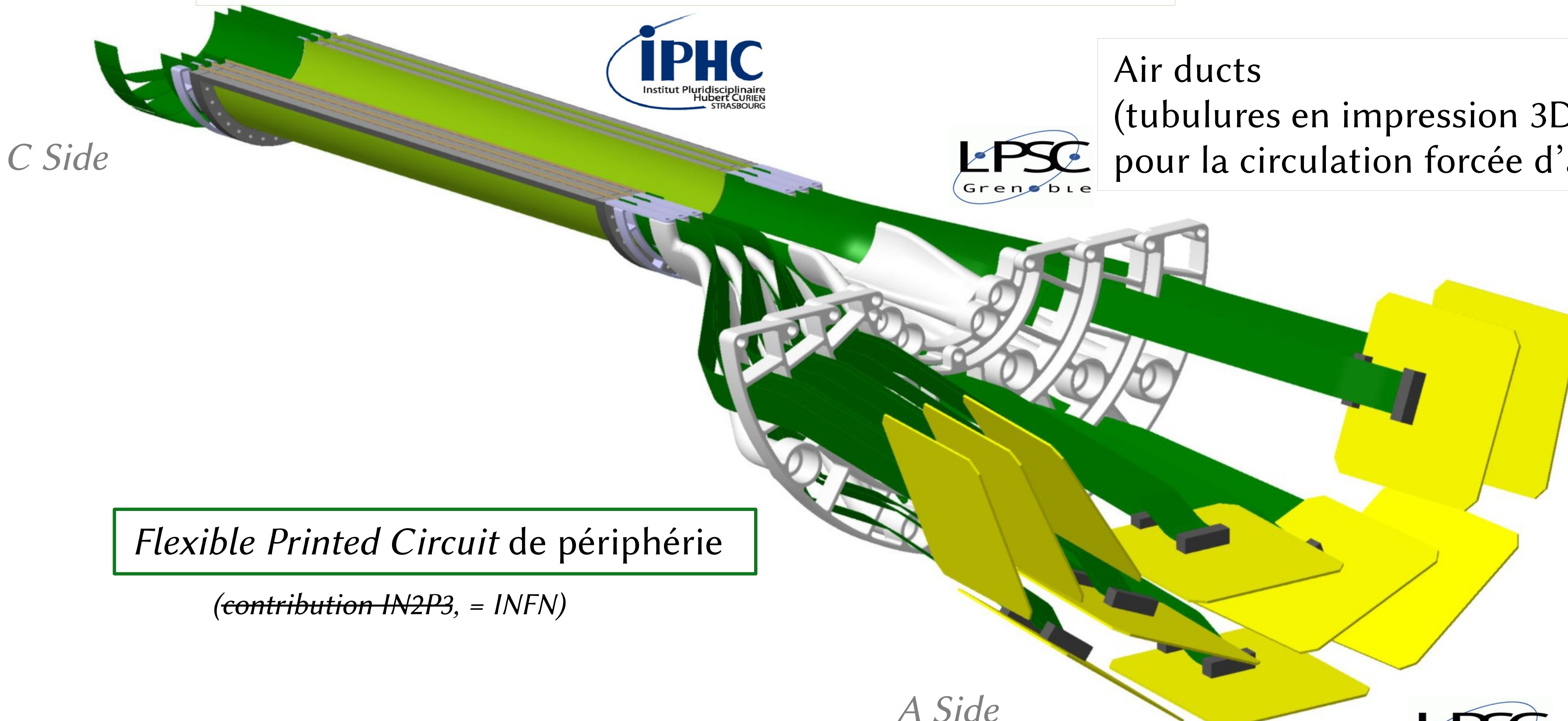

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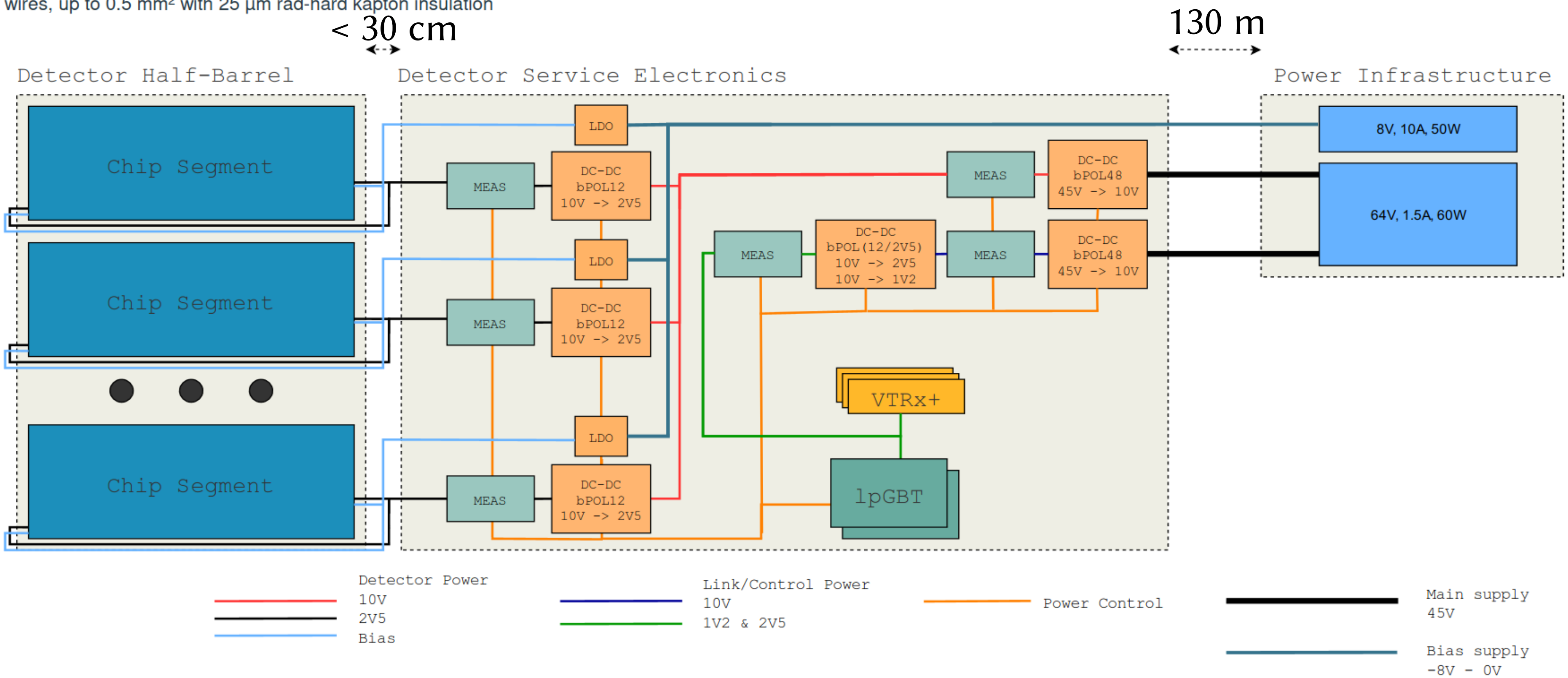
conception et production de l'électronique,
+ intégration mécanique

Corrado Gargiulo, WP5 ITS3 Plenary 2023-04

I.3 – Work breakdown : 2. électronique "middle-end"

C. Électronique liée à la répartition de **l'alimentation**

- Based on radiation hard DC-DC converters
  - CERN bPols (45V -> 10V, 10V -> 2.5V (detector supply), 2.5V -> 1.2V (services only))
- Low current towards infrastructure
- Supply detector on both A- and C-side
  - Need load balancing to avoid skewed v-drop
  - Enamelled wires, up to 0.5 mm² with 25 µm rad-hard kapton insulation
- Self-monitoring, controlled by lpGBT
- Main power separated between dector and link/control
  - Allow tripping of detector power at high level without affecting control links
- Back-end power infrastructure (e.g. CAEN A2554 & CAEN A2518)
  - Located in CR-4, neither magnetic nor radiation field



Ola Gröttvik, WP6, ITS3 Plenary 2023-05

I.3 – Work breakdown : 2. électronique “middle-end”

Dans le détails,

Item 1. Concevoir un ensemble démonstrateur de concept

- Valider les solutions d’alimentation (DCDC sous radiation + champ magnétique)
- Valider la conversion “cuivre” vers “optique” (≈ 10 Gb.s^{-1})
- Valider la mise en œuvre des solutions de monitoring tension/courant
  (= ASIC lpGBT et protocole associés)
  (*NB*: développement de firmware et software requis !)
- Premières validations des concepts à mettre en œuvre pour épouser le volume mécanique disponible (modularisation, connectique)

Item 2. Travail mécatronique avec l’appui de mécaniciens IN2P3
pour intégrer la solution complète dans le tracker

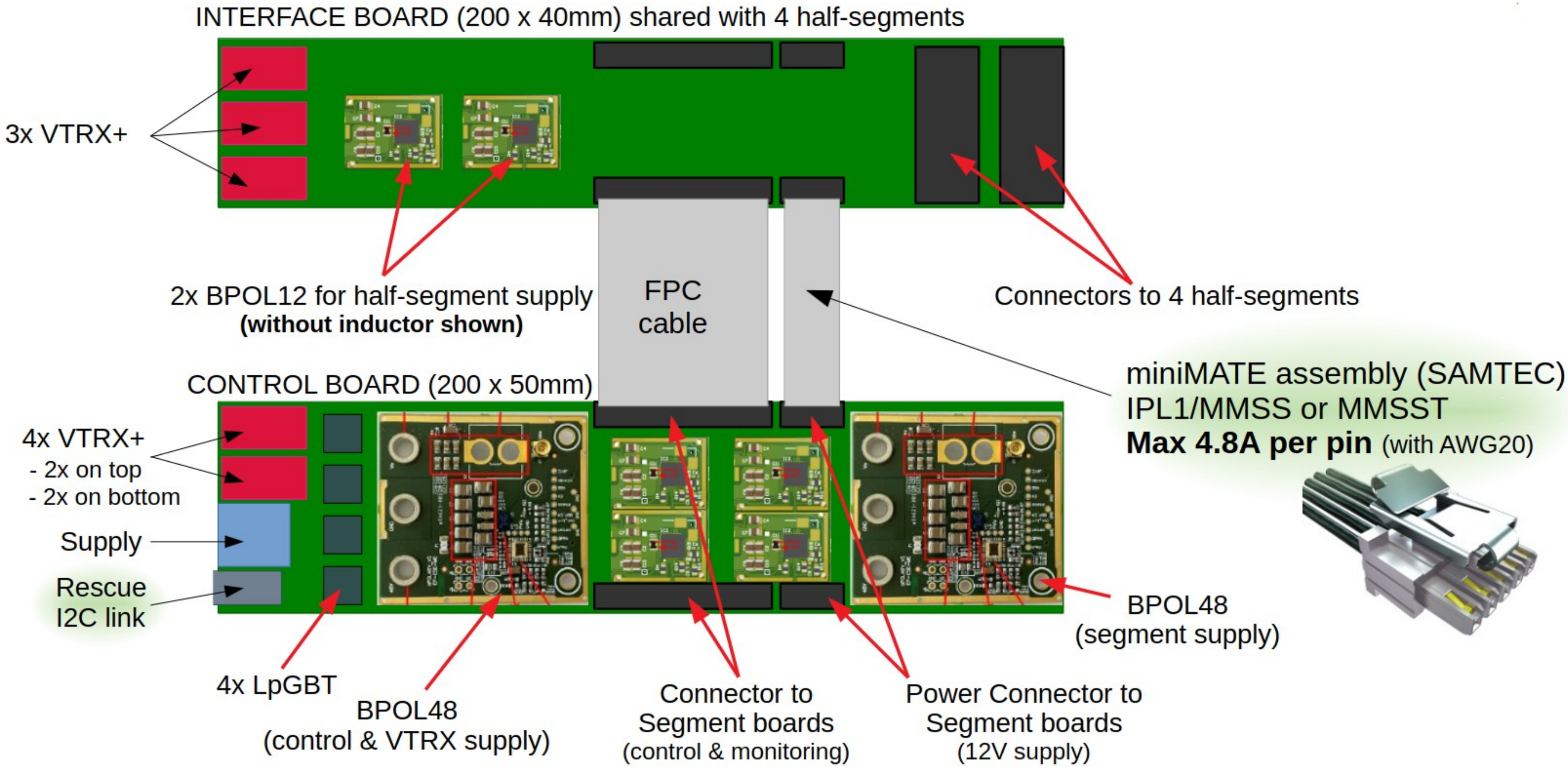
Item 3. Adapter le firmware CRU (opéré actuellement sur hardware PCIe40)
pour piloter et lire la solution.
Plusieurs hardwares envisagés (FELIX également)

I.3 – État technique : volet 2. Detector Service Boards, électro.

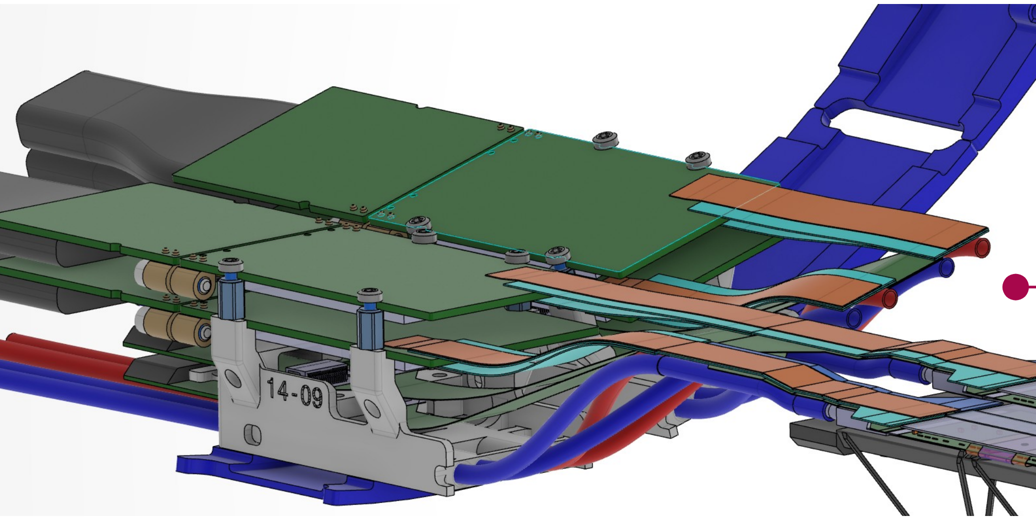
Schéma logique du 1er prototype de carte DSB (17 mai 2023)

→ composants connus (lbGBT, VTRx, bPOLxx + PCB),

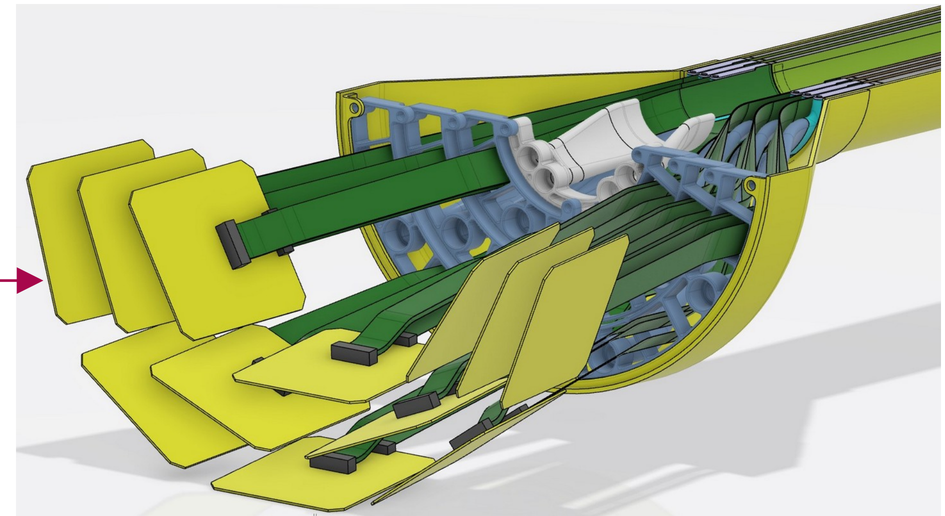
But : preuve de la maîtrise logique pour le TDR (*i.e. sans contrainte véritable de volume ou de radiotolérance*)



I.3 – État technique : volet 2.a Detector Service Boards, méca.



ITS2 middle-layer L3 remains! (stave extension + **support**)



ITS3 [L0+L1+L2] (v2023-03-23) ⟶ Supports à minimiser

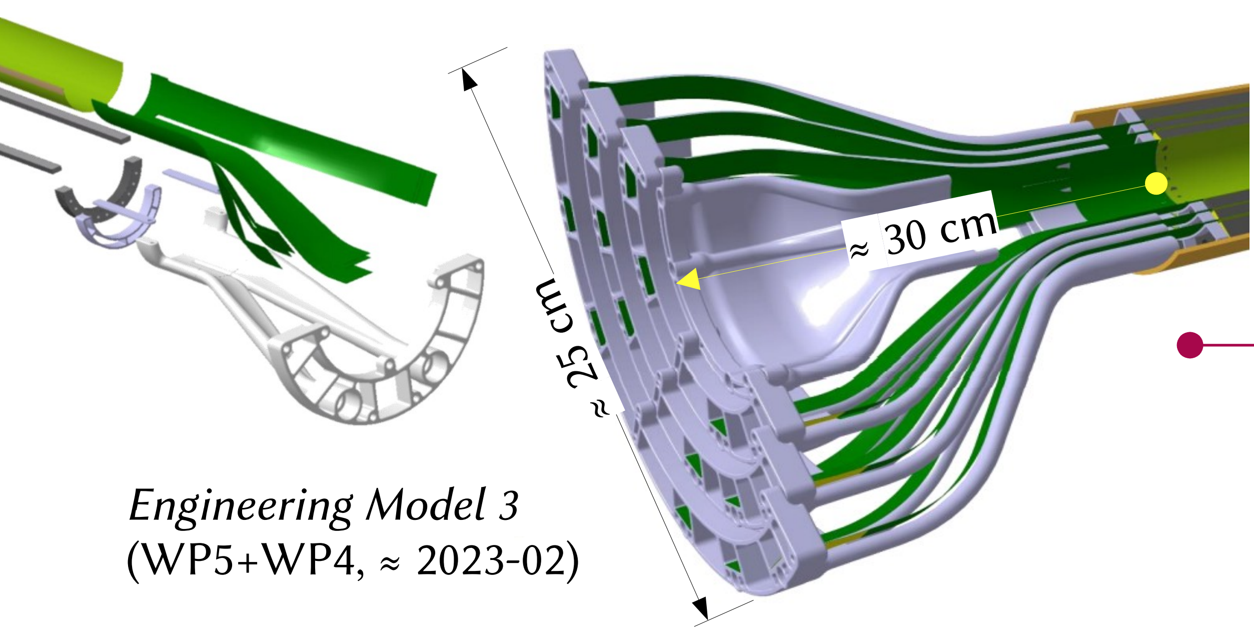
Définition technique du projet (exigences, performances), naissante
⟶ terrain de dvlpt encore mouvant, à l'interface de ≠ WP (donc ≠ interlocuteurs)

Objectif : Management du lot + tests intégration + ingénierie + qualité,
mais ~~intégration au CERN~~ (à ce stade)

Remarques :

- + : Développement de l'utilisation d'**imprimantes 3D** résines UV LCD et FDM Hte Température
- + : **Enveloppe de l'ITS2** connue + maturité des matériaux utilisés
- - : Grande incertitude sur les **contraintes thermiques** ... (risque de drain thermique traversant)
- - : **Complexification** de l'intégration ? ⟶ fort impact sur les *Ress. Hum.* nécessaires

I.3 – État technique : volet 2.b tubulures de refroidissement



Engineering Model 3
(WP5+WP4, ≈ 2023-02)

3D-printed air ducts L0 to L2
(LPSC, ≈ 2023-04)
3D résines UV LCD et FDM H[te] Temp.

Aspect attractif de cette R&D :

- au-delà des concepts classiques pour la fabrication des connecteurs bi-matière
  avec faible transmission des contraintes sur le détecteur
- Occasion de développer un nouveau concept d'intégration optimisé,
  minimisant le "material budget" avec des technologies au-delà de l'état de l'art actuel

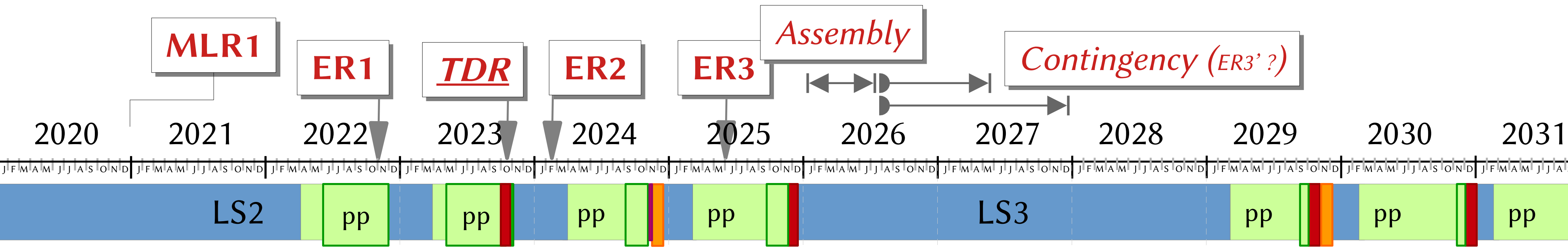
Définition technique, débutée (exigences, performances) + en évolution continue (EM3 ...)
1[er] prototypes déjà livrés (utilisation d'imprimantes 3D)
→ Ingénierie des process de fabrication à développer, qualité des interfaces à optimiser

Remarques :

- Grande incertitude sur les matériaux définitifs (ex: si bi-matériaux, → dvlpts particuliers)
- Complexification du process de fabrication ? → fort impact sur *Ress. Fin.*

v *1.1* (2023-05-16) v *1.2* (2023-05-17) v *1.4* (2023-05-22)

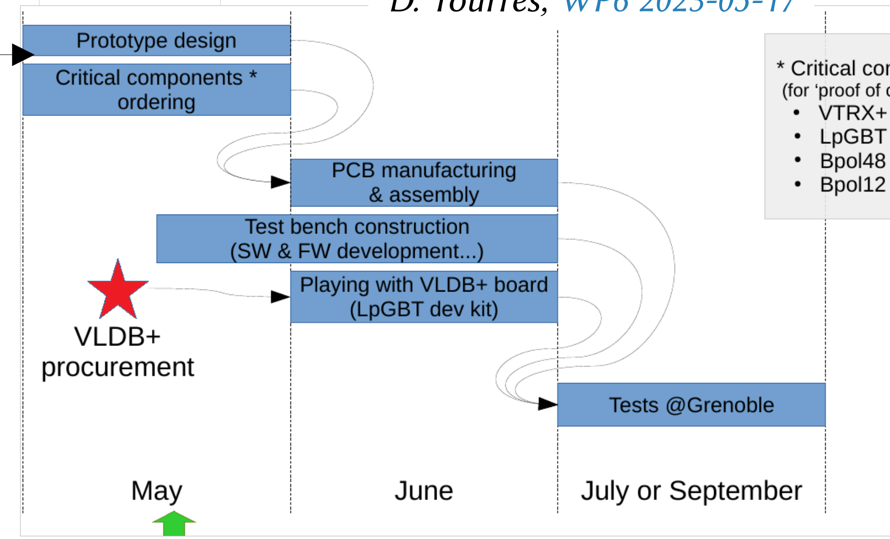
I.3 – ITS3 IN2P3 : 2.a.1 Conception + 2.a.2 Production des DSB



Démonstrateur de principe

Tests

D. Tourres, *WP6 2023-05-17*



Prototype *mécatronique* ER2

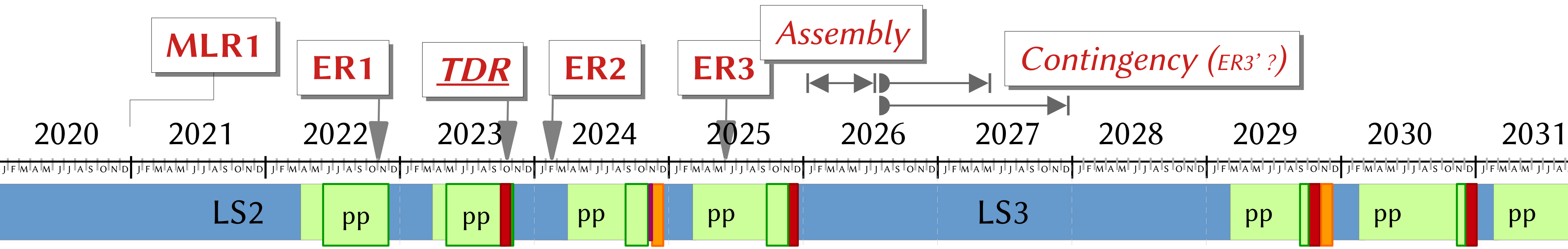
Tests avec capteurs ER2

Finalisation du prototype, pour ER3

Assemblage

Production + tests des DSB finales

I.5 – ITS3 IN2P3 : 2.a+b Integration mécanique de la périphérie



- Mécatronique des DSB

Prototype *mécatronique* ER2

- Tubulures du circuit de refroidissement

impressions 3D et process de fabrication

I.3 – Coûts In2p3 : 2.a.1 Conception des Detector Service Boards

RH :

- [2023-05 /2023-11] démonstrateur testé pour rédaction du TDR
  ≈ (2±0.5) ETP (2 concepteurs électroniciens + 1 CAO-PCB)

- [2024-01 / 2024-08] démonstrateur bis = prototype optimisé, en terme de *mécatronique*
  + [2024-08 / 2024-12] test du démonstrateur avec un capteur MOSS2 ER2
  ≈ $2.5^{+0.5}$ ETP concepteurs élec (2 concepteurs électroniciens, + 1 CAO-PCB + 1 mécanicien^{+})

- [2025] finaliser la DAQ + le contrôle commande avec ER3 ITS3 final
  ≈ 1.5 FTE (2 concepteurs électroniciens)

Budget :

- [2023-05 *2023-11] démonstrateur* = *composants CERN* + *PCB/*câblage + kit VLDB + p^{t} équipm^{t}
  = $1{,}164^{+1}$ kCHF + 4^{+1} k€ + 2k€ kit + 2k€
  ≈ 9^{+1} k€

- [2024-01 / 2024-08] Prototype mécatronique 1 = idem, ≈ **10 k€**
  + [2024-08 / 2024-12] Prototype mécatronique 2 ? = idem, ≈ **10 k€** (si (1) ne marche pas…)

v 1.5 (2023-05-25)

- [2023-2024] missions tests CERN = **5k€/an**, 2 ans

I.4 – Coûts In2p3 : 2.a.2 Production des Detector Service Boards

RH :

…
• [2025] finaliser la DAQ + le contrôle commande avec ER3 ITS3 final
≈ 1.5 FTE (2 concepteurs électroniciens)
• [2025-2026] production et tests des cartes finales
≈ 1 FTE

Budget :

• ~ **2x [15k€** pour la solution optimisée par demi-tonneau]
(= 15 k€ par hémicylindre L0+L1+L2, "2x" = hémicylindre top ou bottom)
+ **2x [15k€]**, en comptant 2 cartes en spares
(+ **1x [15k€]** en faisant l'hypothèse du besoin d'avoir au LPSC une réplique v 1.5 (2023-05-25)
pour débuggage/développement ultérieur au moment commissioning ou durant Run 4

(Attention : "+ si 4e couche à 2x5 =10 segments par hémicylindre",
⟶ chaque carte ≠ 15k€ par carte DSB, mais **37.5 k€** (=15k€ * [2+0.5]) v 1.5 (2023-05-25)
(facteur 2 ≈ simple facteur d'échelle (12+10 segments=22)/12 segments
+facteur 0.5 = pour le redesign éventuel à la conception]

• [2025-2028] missions tests CERN = **5k€/an**, 4 ans

I.5 – Coûts In2p3 : 2.a+b Integration mécanique de la périphérie

RH *SERM LPSC* : (mécanique cartes + refroidissement)

Denis GRONDIN [IR], 10% en 2023
Johan MENU [IE] 20% sur 3 ans [2023-2026] (T4) / 40% (si besoin refroidissement DSB)
Sébastien ROUDIER [IE] 5% sur 3 ans, [2023-2026] 3 ans (Impression 3D)
+ Atelier

Budget (mécanique cartes + refroidissement)

- Budget fonctionnement : ≈ **8 k€/an**, 4 ans [2023-2026]
  - Matériaux pour impressions 3D résines UV LCD et FDM Hte Température
  → Quels risques suivant les spécifications projet ?
  (2023-05-25) - Circuit de refroidissement *indépendant* pour DSB : (type cold plate/air) 8 k€ (ou /eau : 15k€)
  - Matériaux (mousse de carbone + composite): si nécessaire pour le projet, risque: > 10 k€
    Ex: 1 plaque de 12"x12"x1" en 2017 = (2600$ en densité 0.2 g/cc) ou (3600$ en 0.6 g/cc)
  - Sous-traitance mécanique ? (cuissons autoclave, moules, usinage de drains thermiques traversant le détect.): > 20 k€

- Budget missions : **1 k€/an**, 6 ans[2023-2028]

- Budget équipement : Imprimante UV LCD Gde dimensions : **4 k€** [2023]
  → Risque à terme, si la technologie évolue, Imprimante *bi-matière* H^{te} T° ?
  → demande IN2P3 mi-lourd 2025 ou sous-traitance ?

App. J – Organisation et responsabilités associées

J.1 – Organisation : Ressources managériales

- Responsabilité scientifique IN2P3 : Antonin MAIRE (IPHC), 0.1 ETP/an, [2023-2029]
- Responsabilité technique IN2P3 : *TbD*

- Responsabilités scientifiques locales :

IP2I :	Cvetan Cheshkov,	0.1 ETP/an,	[2023-2029]
IPHC :	Antonin MAIRE,	0.3-0.5 ETP/an,	[2022-2029]
LPSC :	Rachid GUERNANE,	0.4 ETP/an,	[2023-2029]

  ⟶ réunions (bi-)hebdomadaires : jeudis 09h30 pour 30-60 min

- Responsabilités techniques locales :

  IP2I : -

  IPHC :
  - design CMOS : Frédéric MOREL, 0.2-0.3 ETP/an, [2023-2025]
  - test et qualification : Serhiy SENYUKOV, ≈ 0.2 FTE/an, [2020-2026+]

  LPSC :
  - électronique: Olivier BOURRION, 0.3 FTE/an, [2023-2028]
  - mécanique Denis GRONDIN, 0.1 FTE/an, [2023-2024+]

App. K – État technique & TRLs

K.1 – Tech. Readiness Level : définitions

Niveau	Nom synthétique	Définition
TRL1	Principe de base	Principes de base observés et identifiés
TRL2	Application formulée	Concept technologique et/ou application formulés
TRL3	Preuve du concept	Preuve du concept analytique + preuve expérimentale de la fonction et/ou de la caractéristique critique
TRL4	Validation fonctionnelle	Vérification fonctionnelle en environnement de laboratoire au niveau composant et/ou maquette
TRL5	Modèles à échelle réduite	Vérification en environnement représentatif de la fonction critique au niveau composant et/ou maquette
TRL6	Validation de la conception	Démonstration en environnement représentatif des fonctions critiques de l'élément au niveau modèle
TRL7	Qualification d'un modèle	Démonstration en environnement opérationnel de la performance de l'élément au niveau modèle
TRL8	Qualification du syst. réel	Système réel développé et jugé apte à l'expérience
TRL9	Opération du syst. réel	Système réel ayant été utilisé à l'identique et avec succès lors d'une expérience dans l'environnement idoine.

basée sur la norme ISO 16290:2013

K.2 – Tech. Readiness Level : évaluations

1.a Conception de la matrice de pixels

TRL4 ◦ au niveau analogique (collection de charge et électronique de front-end)

TRL3 ◦ au niveau digital (traitements numériques et gestion de la puissance)

TRL6 ***1.b*** Qualification et tests des prototypes CMOS soumis pour fonderie

2.a Cartes de l'électronique de *middle-end* (lecture, pilotage, alimentation d'ITS3)

TRL2 ◦ Conception des cartes

\- ◦ Production des cartes

TRL1 ◦ Intégration mécanique et optronique (conception et réalisation des supports mécaniques)

TRL5 ***2.b*** Pièces mécaniques pour le circuit de refroidissement

TRL3 ***3.*** Intégration et micro-connectique électroniques en vue de l'installation finale

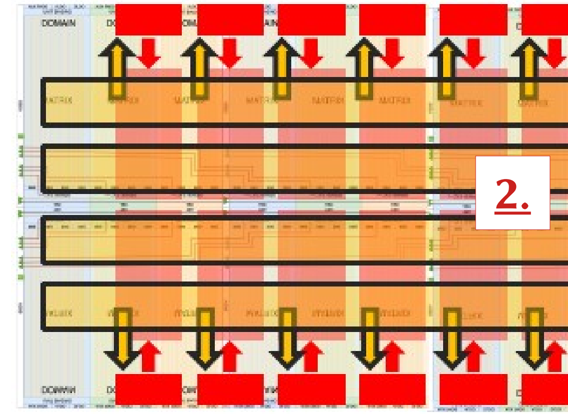
TRL3 ***4.*** Assemblage d'un détecteur selon le plan de sauvegarde (Super ALPIDE)

App. L – Portefeuille de risques

L.1 – Risques : 1.a design CMOS de la matrice de pixels

1. **Stitching** selon *z*, capteur 100% opérationnel ?
→ clarfication avec tests ER1 MOSS1…

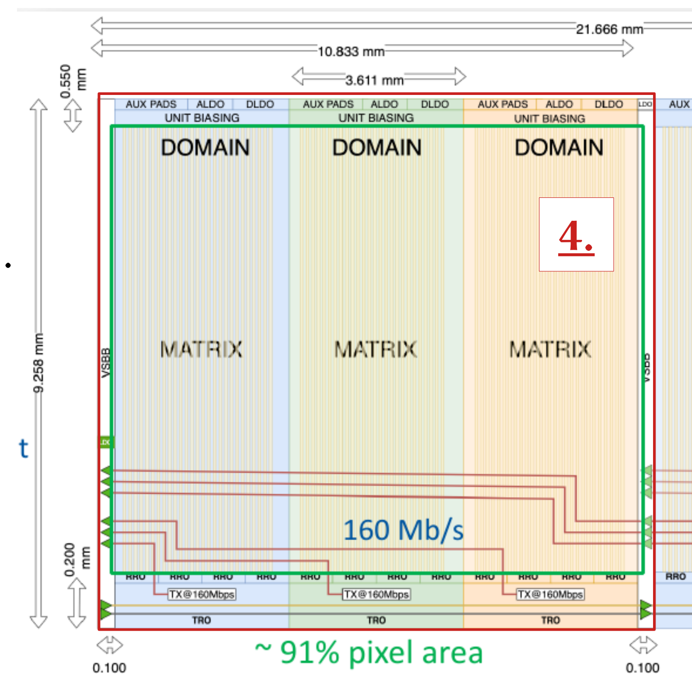
2. Distribution/**régulation de puissance** le long du capteur
2,5 V stabilisés sur … $Z \approx 26$ cm
Pb : rails classiques d'alimentation → chute de qq 100^n mV
Régulation par domaines de puissance
Pb : régulation dissipe elle-même de la puissance…



Distributed LDO regulators

3. Architecture de lecture numérique :
pertes de données Vs profondeurs des mémoires FIFO
= f(type de collisions, ex : pp MB, pp haute multiplicité, Pb-Pb, ..
taux de collisions $.s^{-1}$, 50-500 kHz
temps d'intégration, 2-10 µs)

4. Réduction des **zones mortes** (acceptance pour la physique: ≈ -9%)

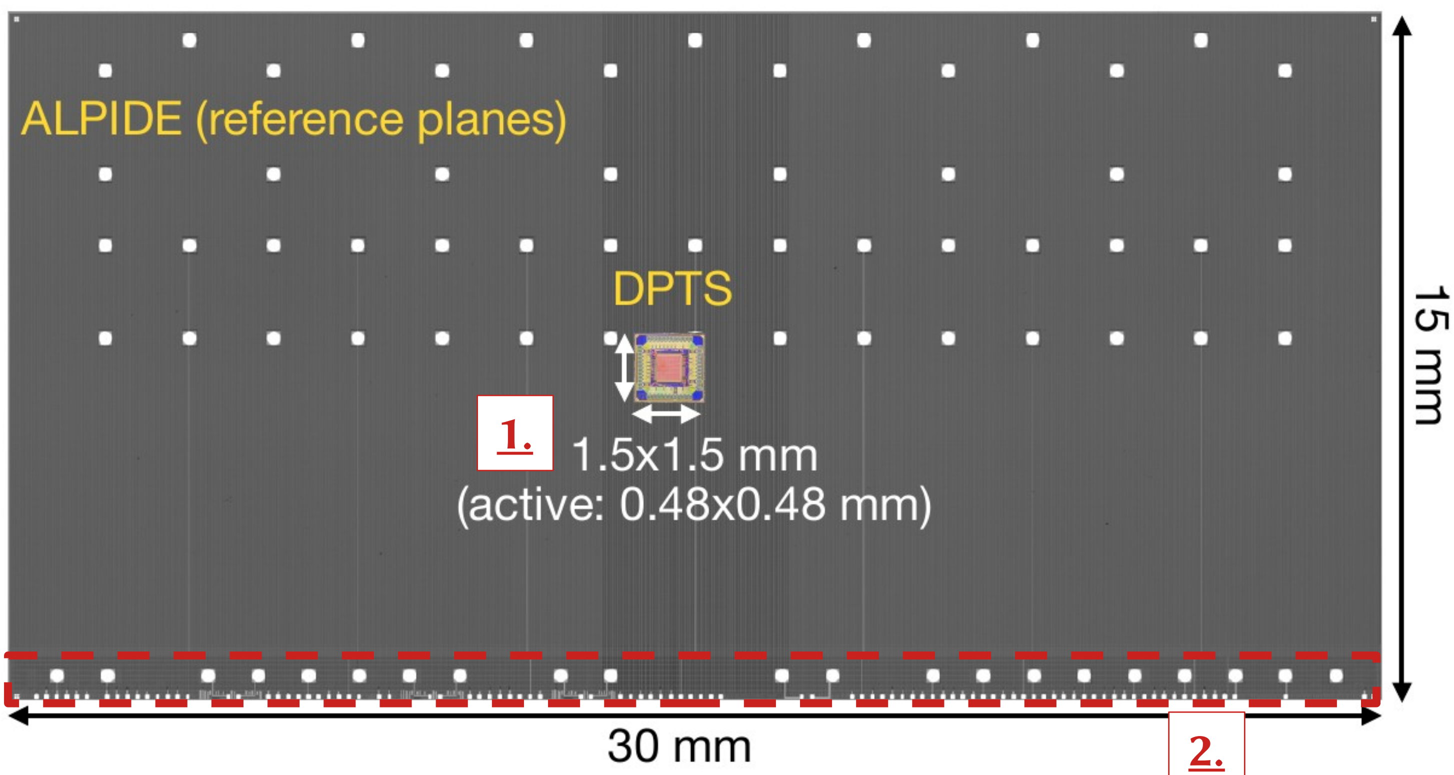


L.1 – Risques : 1.a design CMOS de la matrice de pixels

5. Ratio of **active surface** to **periphery surface**,
to pull out "*O*[MB.s^{-1}.cm^{-2}]"
to ship (even low) current/voltages over sensor distance, not even talking about ladder length

Endcap A-side

Endcap C-side



Pixel matrix
13.8 mm

Periphery
1.2 mm

L.2 – Risques : 1.b Tests et qualification des capteurs

Enjeu : validation des paramètres dans un espace à *n* dimensions
→ complexité de la tâche

Campagnes de tests ALICE = systématiques + massives
ex : 4 campagnes de 7-10 jours déjà prévues en 2023 pour le retour ER1 (>2023-06)
→ très demandeurs en RH pour :
- les semaines de faisceau +
- les analyses subséquentes

→ Effort de collaboration ALICE, = proprement dimensionné et suffisant ?
i.e. WP3 = en permanence sur le fil avec la cadence imposée par les ERx

- [ER1 → ER2] = réduction du type de chiplets à tester Vs capteurs de grandes tailles, dans un nombre limité de variantes

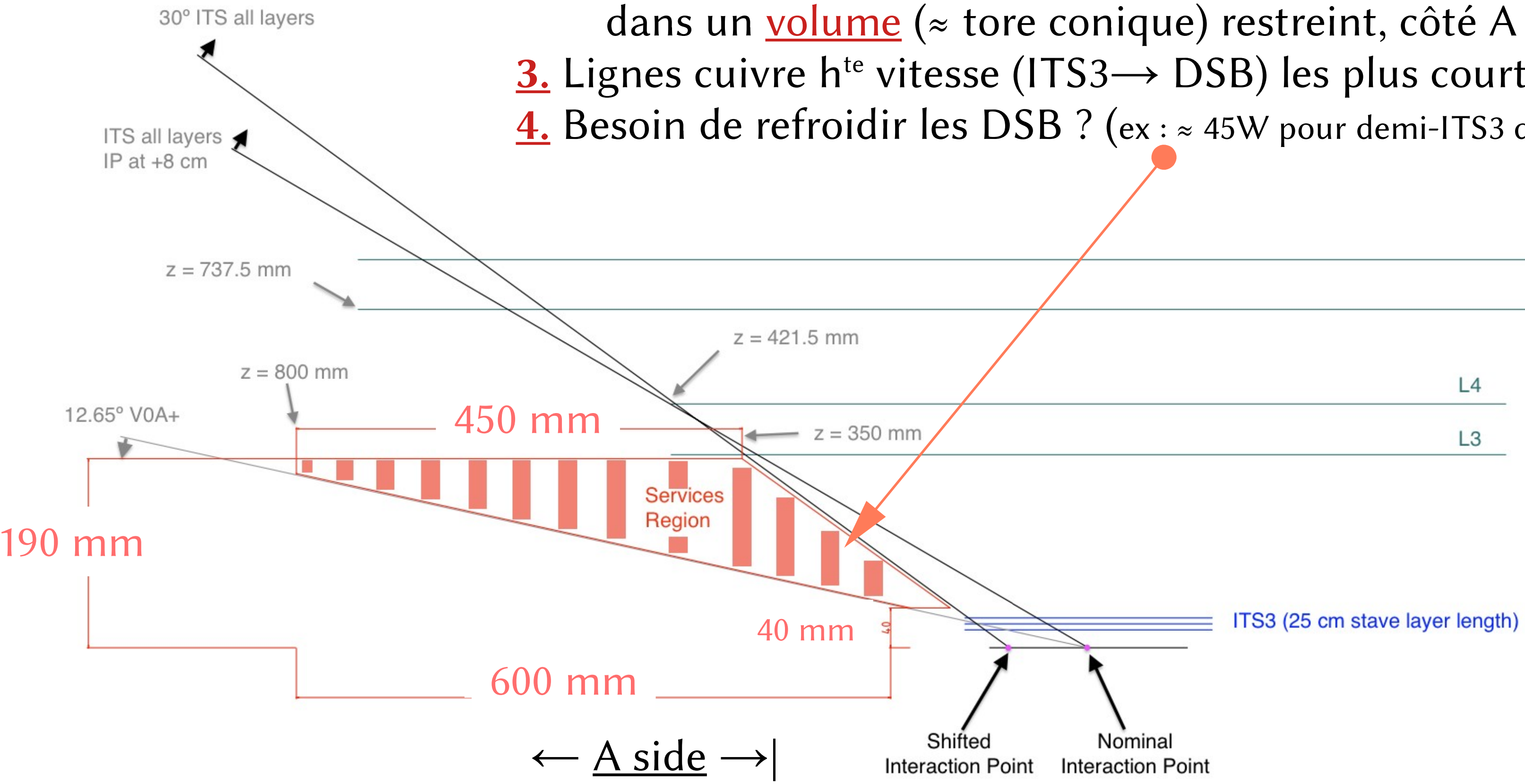
L.3 – Risques : 2. intégration *mécatronique* des services

0. cahier des charges ITS3 désormais figé ? - Design, en cours...

+ Combinaison: 1. Radiotolérance de tous les composants de DSB
(< 10^{12} néq.cm-2.s-1 NIEL + <100 krad TID)
PCB, **ok!** / lbPOL, **ok!** / VTRx, **ok!** / LpGBT, **ok!** / Mutliplexeur **?**)

2. DSB + passage des FPC + tubulures du refroidissement à intégrer dans un volume (≈ tore conique) restreint, côté A de l'expérience
3. Lignes cuivre h^te vitesse (ITS3⟶ DSB) les plus courtes possibles (O[20 cm])
4. Besoin de refroidir les DSB ? (ex : ≈ 45W pour demi-ITS3 ds hyp. "3 couches")

v 1.5 (2023-05-25)

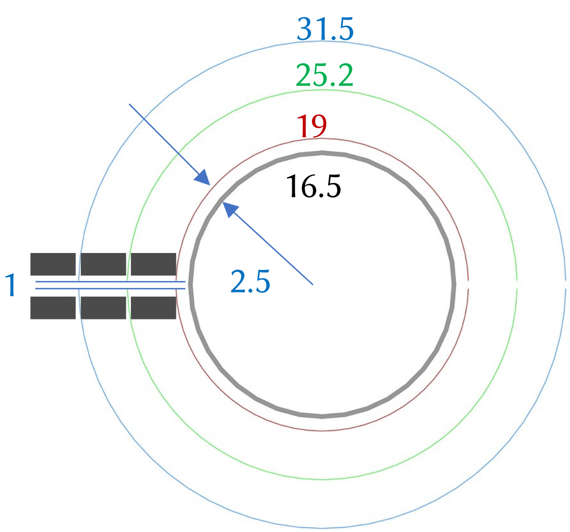


Felix Reidt, WP6 meeting, 26 Apr 2023

L.4 – Risques : 3. Integration

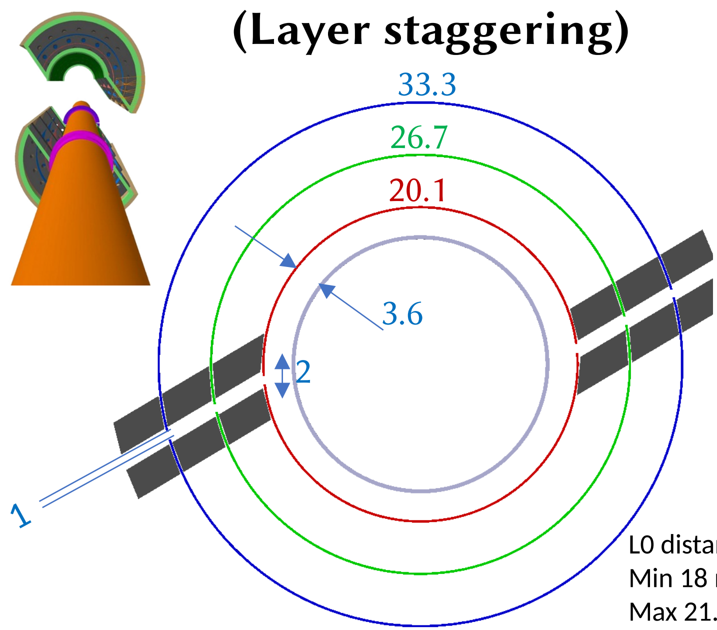
- incurvation de capteurs MOSS-like fonctionnels = ?
- quel accès aux endcaps MOSS pour connectique électronique vers les DSB ?
- assemblage ("distant") des demi-cylindres top Vs bottom

Baseline (2023)



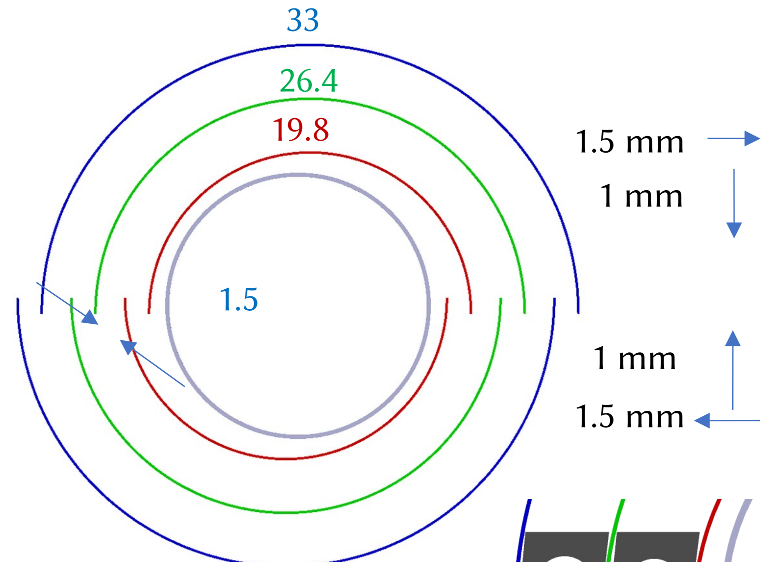
Early 2015

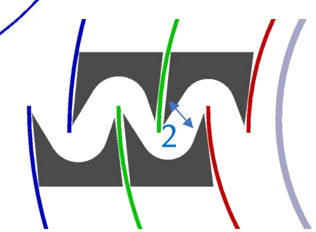
Sensor rotation (Layer staggering)



L0 distance from IP
Min 18 mm
Max 21.3 mm

Overlap (Half-Barrel shifting)

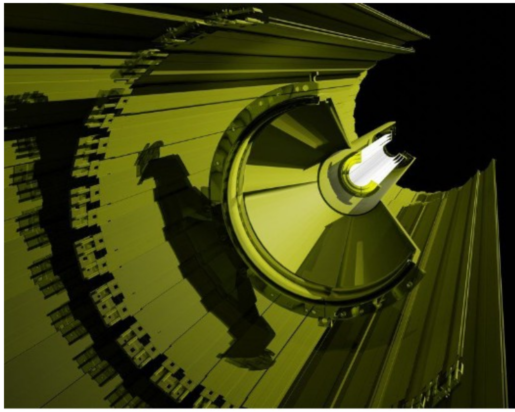




Gargiulo WP5, ITS3 Plenary 2023-05

L.4 – Risques : 3. Integration

- incurvation de capteurs MOSS-like fonctionnels = ?
- quel accès aux endcaps MOSS pour connectique électronique vers les DSB ?
- assemblage ("distant") des demi-cylindres top Vs bottom



- +**4e couche** ITS3 à $r_{L3} \approx 6.0$ cm ?
  360° d'azimut couverts avec ~~2x5 segments stitchés~~ (= L2 ITS3),
  mais 4x5 segments

→ + : avantage fort pour la physique, l'acceptance,
la performance des algorithmes de tracking, …
NB : r_{Lnext}(ITS2 L3) = 19 cm (*i.e.* loin…)
~ : budget de matière supplémentaire ? sans doute, ok…
- : intégration plus complexe au global …

(études en cours)

Grosa, WP1, ITS3 Plenary 2023-05
(Courtesy D. Chinellato)