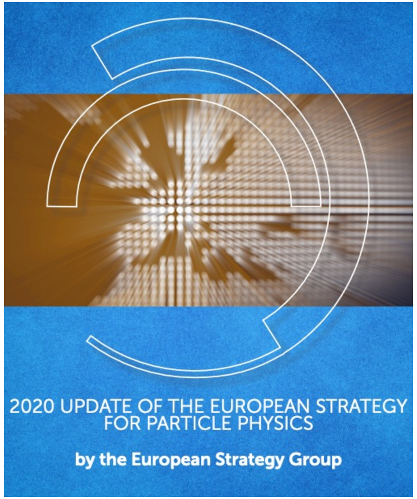
CMOS 65 nm R&D

Marco Bomben
APC & UPC

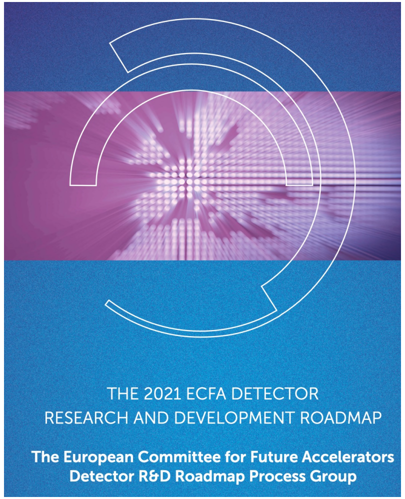
ECFA Detector R&D Roadmap

2020 European Particle Physics Strategy Update (EPPSU)



High-priority future initiatives:
e+e- Higgs/Z/top factories

2021 ECFA Detector R&D Roadmap



https://cds.cern.ch/record/2784893/

Roadmap organised in "Detector R&D Themes" (**DRDTs**) and "Detector Community Themes" (**DCTs**)

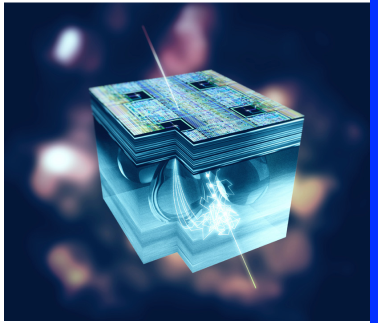
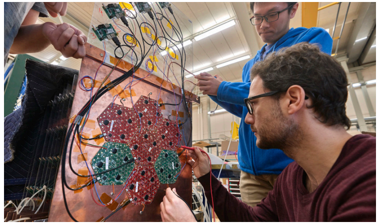


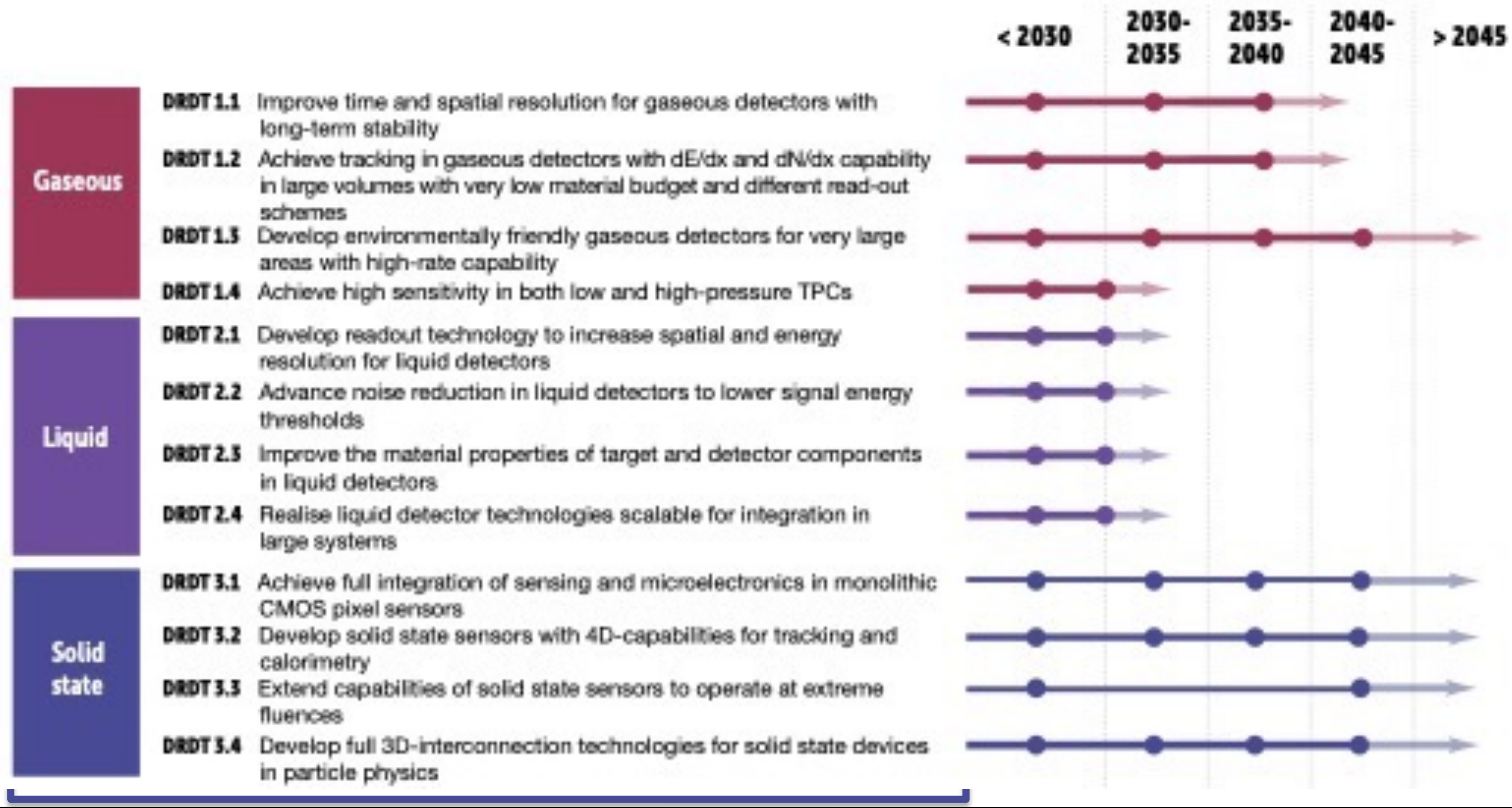
Illustration of microelectronics circuitry integrated with a detecting medium as a single monolithic solid-state detector. (© ALICE collaboration)



Students and young scientists working on the construction of prototype detector modules. (© CERN)

Takeaway message: ***"detector readiness should not be the limiting factor in terms of when the facility in question can be realised"***

DETECTOR RESEARCH AND DEVELOPMENT THEMES (DRDTs) & DETECTOR COMMUNITY THEMES (DCTs)



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Proposition to DRD3 ws @ CERN, 22-23/3

https://indico.cern.ch/event/1214410/

DRD project: Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments

DRD technology area

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.

Proposing participants

Institute	Contact	Foreseen main areas of contribution
APC Paris	M. Bomben	Simulations, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Hynds	Testing, simulations
Zurich University	A. Macchiolo	Testing, DAQ, simulations

R&D using **65 nm technology** to achieve high **single point resolution** (3 μm), high **temporal accuracy** (5ns), low **mass** (100 μm thick) & low **power** (< 50 mW/cm^2)

Access to TPSCo65 CMOS imaging process with 65 nm feature size via **CERN**/ALICE

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Lightweight, granular and fast detector

- ***Tempting eh?*** ☺

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Multi-year expertise in simulations (TCAD/MC) and testing (cleanroom/testbeams)

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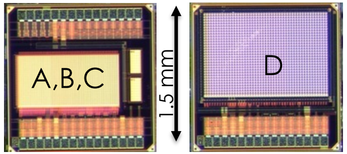
Access to TPSCo65 CMOS imaging process with 65 nm feature size via **CERN**/ALICE

Staged project – see next slide

Timeline

- Characterisation of existing chips — Mid 2024
- Design of beam-telescope demo matrix — Mid 2025
- Characterisation of demo matrix — Mid 2026
- Telescope sensor ready for integration — End 2027
- Design demonstrator for collider exp — End 2028
- Characterisation of sensor for collider — End 2029

Opportunity for contribution – now ☺



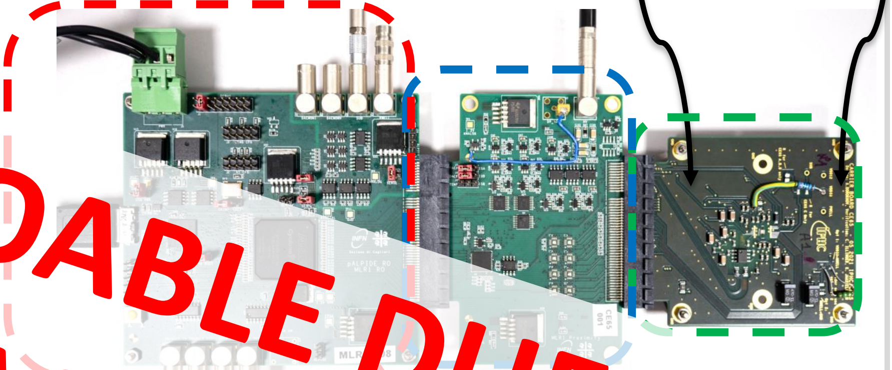
NO LONGER DOABLE DUE TO THE LACK OF DAQ BOARD

IPHC is ready to provide us soon a complete setup to test the existing chip CE65V1

Goal: training for the arrival of the CE65V2

➢ **We can start to work on 65 nm shortly!**

▪ Well Suited for µ-el./instrumentation engineer



VCI2022

QUESTIONS?

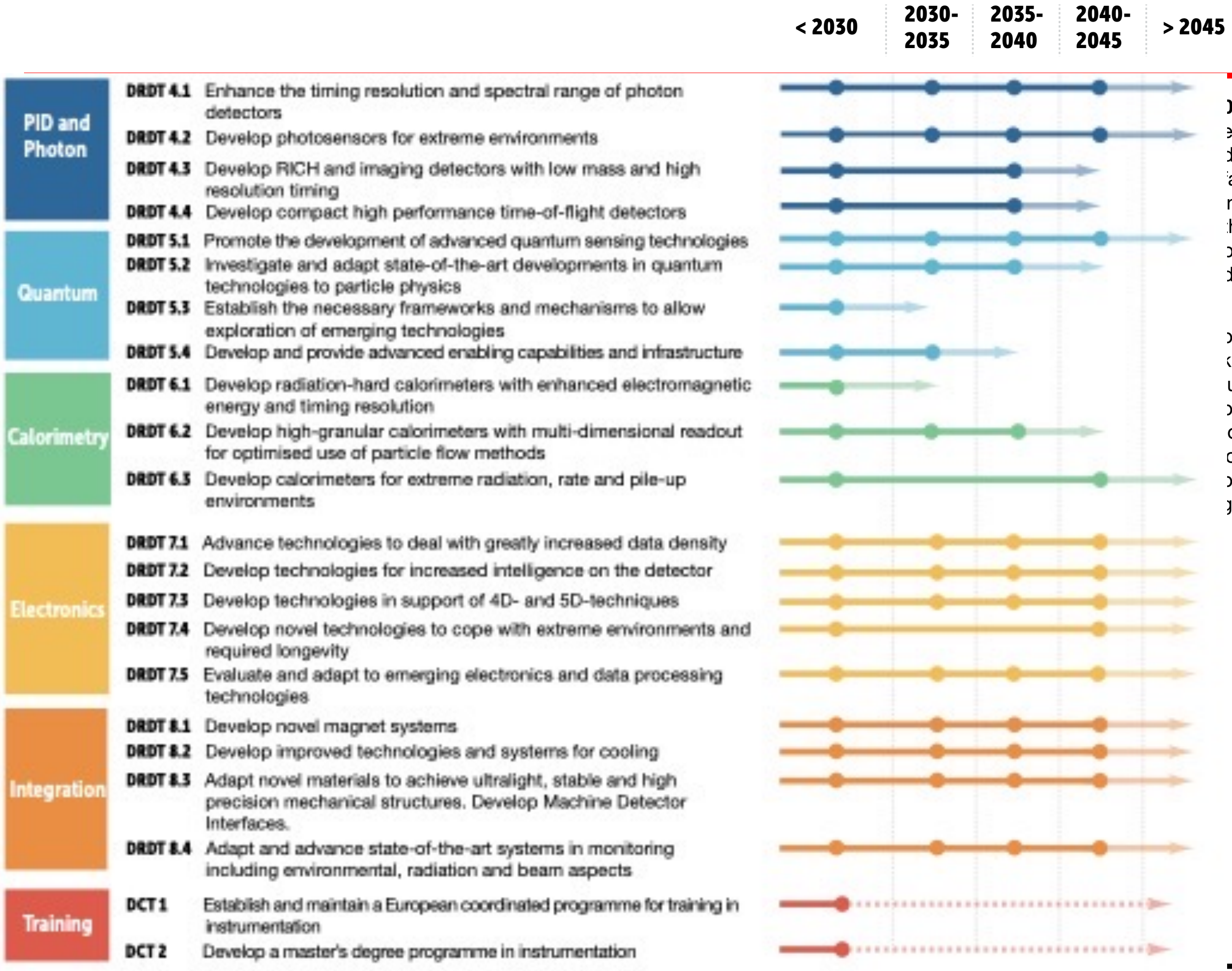
Backup

European Particle Physics Strategy Update (2020)

- Projects listed in the Deliberation Document of the European Particle Physics Strategy Update (EPPSU) [Ch0-2] as either "High-priority future initiatives" or "Other essential scientific activities for particle physics"; e.g.:

- HL-LHC
- Long baseline neutrino detectors
- **e+e- Higgs/Z/top factories**
- hh machine @ 100 TeV

*The **highest priority** laid down by the updated ESPP is for a **future Higgs factory** to **thoroughly explore the properties of this completely new type of particle**, which is seen as a **key to a much deeper understanding of how the Universe works**.*



etector R&D Themes (DRDTs) and Detector Community Themes (DCTs). Here, xcept in the DCT case, the final dot position represents the target date for completion of the R&D required by the latest known future acility/experiment for which an R&D programme would still be needed n that area. The time from that dot to the end of the arrow represents he further time to be anticipated for experiment-specific prototyping, rocurement, construction, installation and commissioning. Earlier dots represent the time-frame of intermediate "stepping stone"

rojects where dates for the corresponding facilities/experiments are nown. (Note that R&D for Liquid Detectors will be needed far into the uture, however the DRDT lines for these end in the period 2030-35 because developments in that field are rapid and it is not possible oday to reasonably estimate the dates for projects requiring onger-term R&D. Similarly, dotted lines for the DCT case indicate that beyond the initial programmes, the activities will need to be sustained going forward in support of the instrumentation R&D activities).

Exploring a new technology: TPSCo 65 nm

=> SEE NEXT TALK BY WALTER SNOEYS <=

IPHC motivation to join CERN-lead effort

- Smaller feature size = smaller pixel
- Lower voltage hence power
- Stitching over 12" wafer

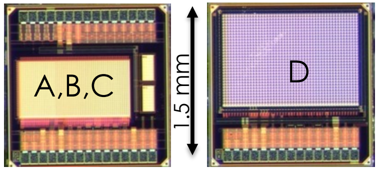
- Key requirements (future e+e- coll. / heavy-ion exp)
  - Position resolution $\sigma_{sp} \lesssim 3$ µm
  - Low material budget 0.05 to 0.15 % X_0 (power <<100 mW/cm^2)
  - Large detection surface (> 100 cm^2)

- Smaller feature size
  = more embedded functionalities

- Generic interest for MAPS performance
  - Large hit rate (>> 100 MHz/cm^2 e.g. for Belle II)
  - Time resolution from ns to ~10 ps (4D tracking, PID)

IPHC contribution for charge collection studies

- **CE-65** square pixel matrices
- Analogue output w rolling-shutter readout 10-40 MHz



https://indi.to/zL5xc
S.Bugiel VCI 2022

Variant	pitch	Matrix size	Front-ends	Collection diode structure	Split
A	15 µm	64x32	DC-SF DC-Amp AC-Amp	Basic	various doping profiles
B				N-implant w gaps	
C				N-implant	
D	25 µm	48x32		basic	

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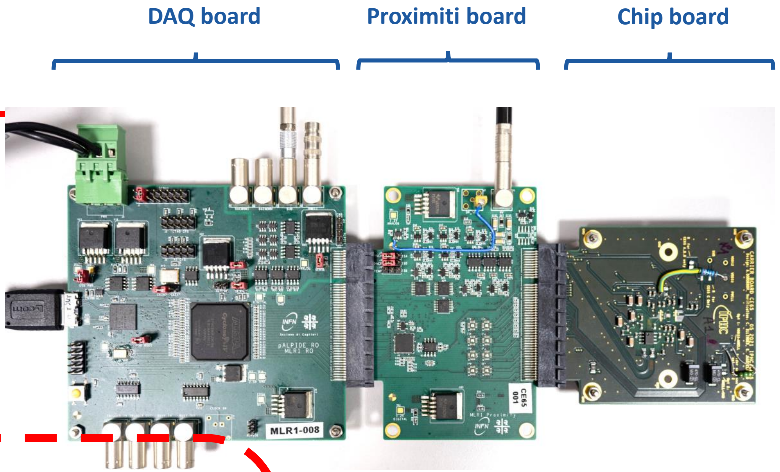
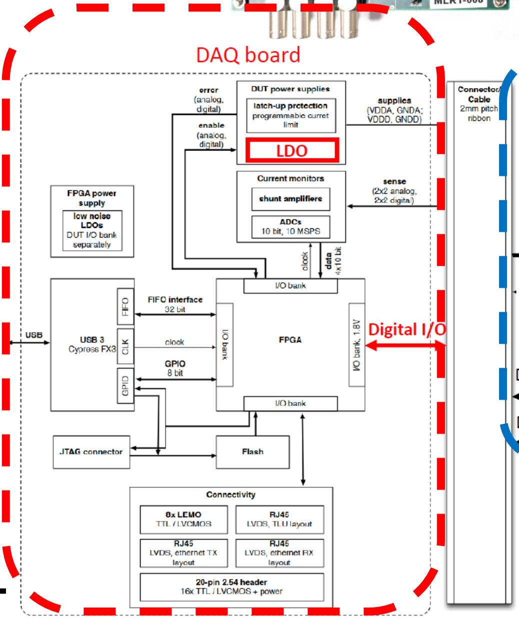


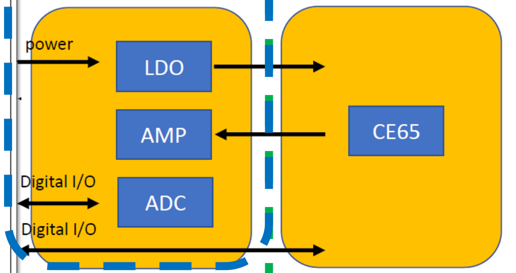


Proximity board

Interface between DAQ board and DUT carrier boards

CE65

- 64x32 matrix, rolling shutter



- Single analogue output
- 7 inputs (biasing, clock, control) + power, ground, pwell, sub
- Objective: sample the analogue output at clock frequency (up to 50 MHz)

65 vs 180 nm in a nutshell

65nm

pro: digital density of course

pro: 300mm wafers vs 200mm in 180

con: much less choice in substrate (essential only thin EPI 10-15um)

con: much more limited access to foundry than in 150/180 and typically no MPW for prototyping

con: cost in engineering run ~ factor 2.7 over 150/180nm difficult in development cycle

180nm

pro: much wider range of substrate possible

pro: easier access to foundries and multiple foundries established in HEP and cheaper/ possibility of MPW for prototyping

con: logic density much smaller

con: costs at very large detectors (e.g. 50m2 +) higher in 180 because 150/180 runs on 200mm wafers versus 65 on 300mm wafers