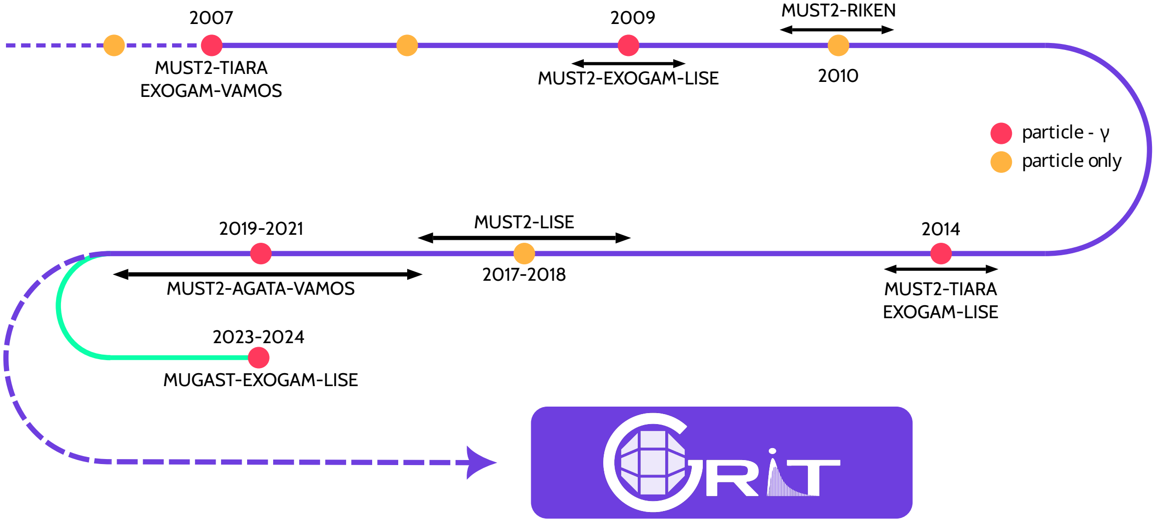
Challenges of the next generation silicon array

A. Matta, LPC Caen, CNRS/IN2P3

In-Beam Spectroscopy WS 2023

Back to the future

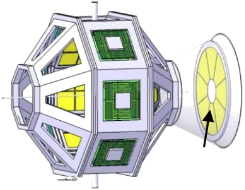


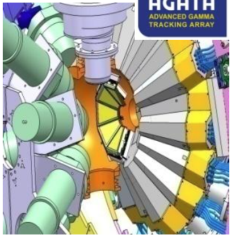
History

GASPARD (IN2P3)

GASPARD

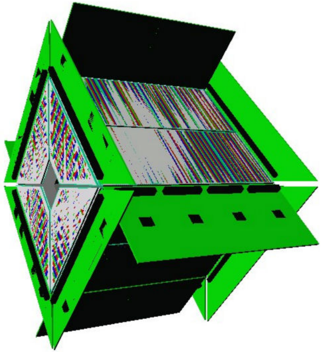
GAmma SPectroscopy and PArticle Detection





- Beam: SPIRAL2 Phase2
- γ-rays: AGATA & PARIS
- Cryotarget: CHyMEN

TRACE (INFN)



- Beam: SPES
- γ-rays: AGATA & GALLILEO
- Special target: Tritium foil

Organisation

GRIT

Management Board

- Spokespersons: D. Beaumel (IJCLab), D. Mengoni (INFN)
- Technical Coordinator: C. Soulet (IJCLab)

WP0 Management	WP1 Detectors	WP2 Mechanical	WP3 FEE	WP4 DAQ/Analysis	WP5 MUGAST	WP6 Simulation	WP7 Targets
D. Beaumel (IJCLab)	F. Galtarosa (INFN)	P. Rosier (IJCLab)	L. Alvado (LPC Caen)	A. Matta (LPC Caen)	M. Assié (IJCLab)	S. Bottoni (INFN)	A. Gottardo (INFN)
	Thin Trap. – M. Assié (IJCLab)	Det. Design – Y. Peinnaud (IJCLab)	iPACI – L. Leterrier (LPC Caen)	DAQ – D. Etasse (LPC Caen)	AGATA VAMOS – M. Assié (IJCLab)	AGATA – S. Bottoni (INFN)	
	Thick Trap. – F. Flavigy (LPC Caen)	Integration – Y. Peinaud (IJCLab)	PLAS – S. Drouet (LPC Caen)	BEE & Conn. – D. Etasse (LPC Caen)	LISE EXOGAM – V. Alcindor (IJCLab)	Annular – C. Paxman (University of Surrey)	
	Square – D. Mengoni (INFN)	Cooling – P. Rosier (IJCLab)	TOT – S. Capra (INFN)	Data analysis – A. Matta (LPC Caen)		nptool v4 – A. Matta (LPC Caen)	
	Annular – F. Galtarosa (INFN)	Vacuum – P. Rosier (IJCLab)	FEB – L. Alvado (LPC Caen), E. Rauly (IJCLab)	C2 – A. Matta (LPC Caen)			

Steering Committee

- INFN Milano, Chair – S. Leoni
- IJCLab – Y. Blumenfeld
- University of Surrey – W. Catford
- INFN LNL – G. De Angelis
- GANIL – G. de France
- IFIC – A. Gadea
- LPC Caen – N. Leneindre
- INFN Milano – A. Pullia

Funding

Institution

MoU guaranteed founding ∼600 kEUR → next MoU in preparation

Grants

SIREN (2020-2023 - LPC):

- PI: Freddy Flavigny
- 350 kEUR (150 for GRIT)
- 12 Thick detectors

RÉGION NORMANDIE

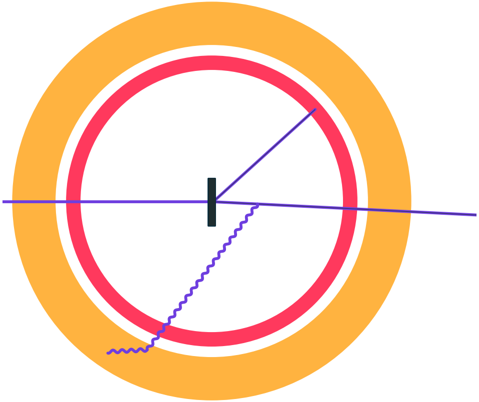
ETSI (2021-2024 - LPC/GANIL):

- PI: Adrien Matta
- 373 kEUR
- IR (LPC) & AI (GANIL)

One-off

- University of Surrey
- University Santiago de Compostela

Conceptual detection system



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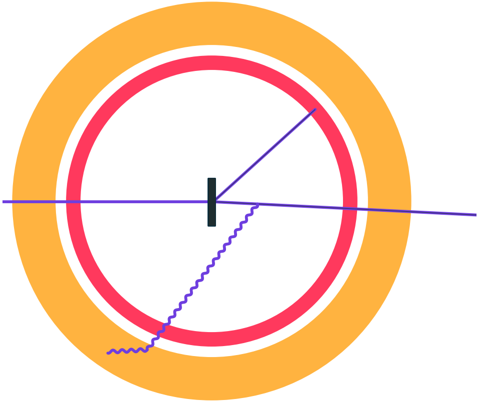
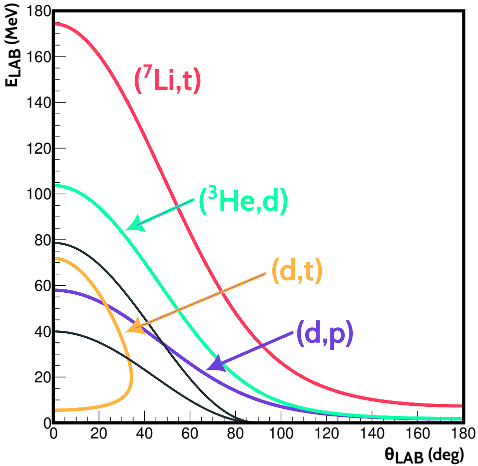


Kinematic of ^{132}Sn at 10A MeV



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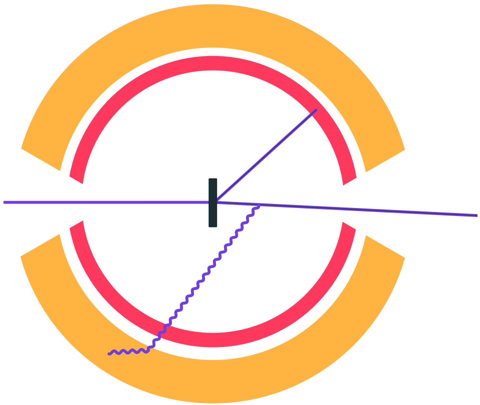

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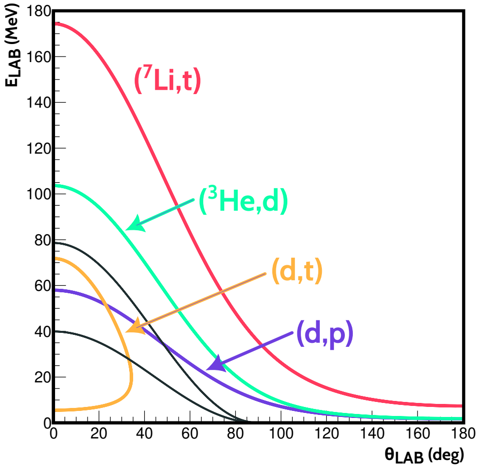

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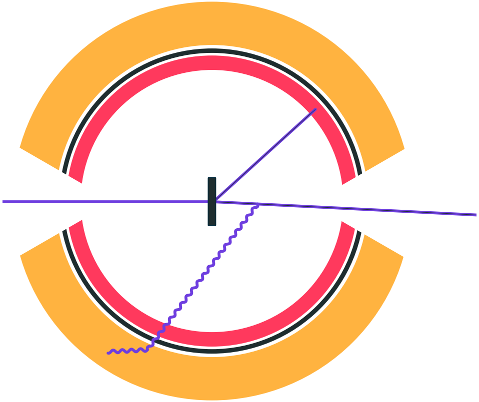

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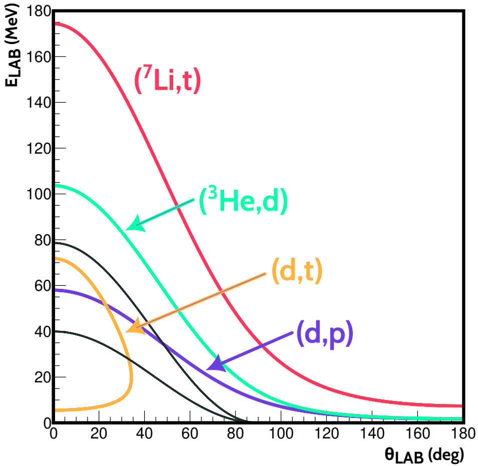

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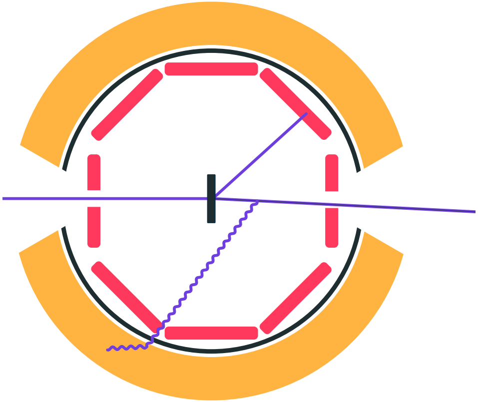

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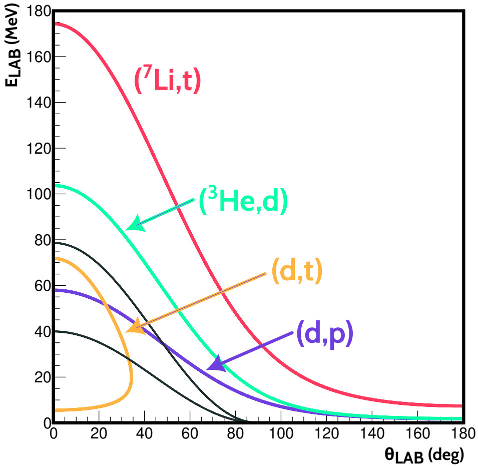

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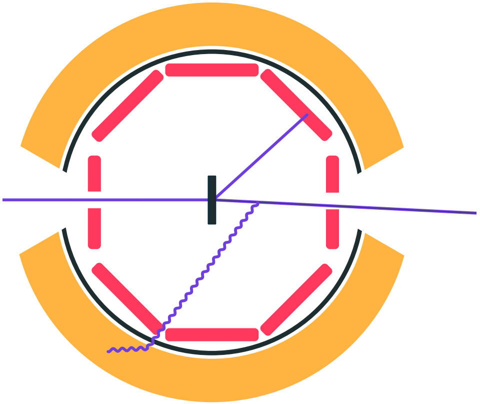

Key features: G.R.I.T

- Two body kinematic
  - Granularity
    - DSSD
  - Resolution
    - ~35keV

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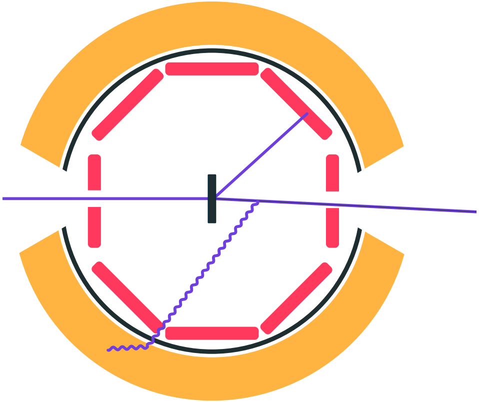

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→ ~ **7000 individual channels**

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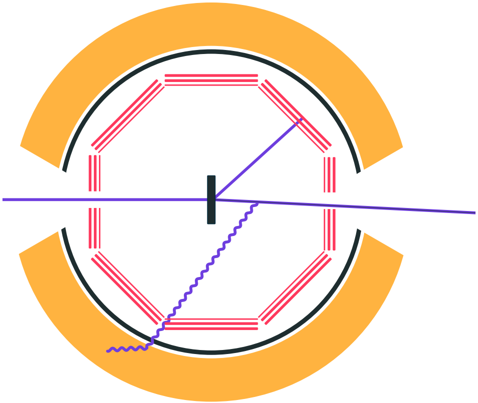

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- Many reaction channel
  - Identification (NIM A 908(2018)250-255)
    - TOF (mass only, low energy)
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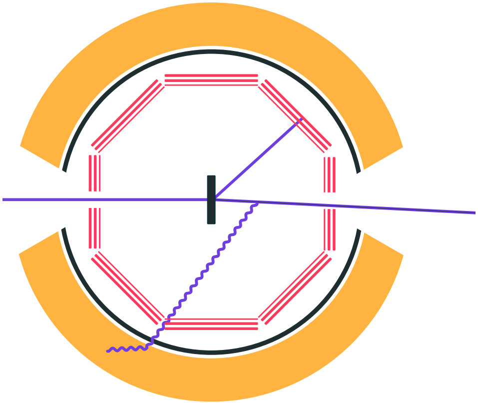

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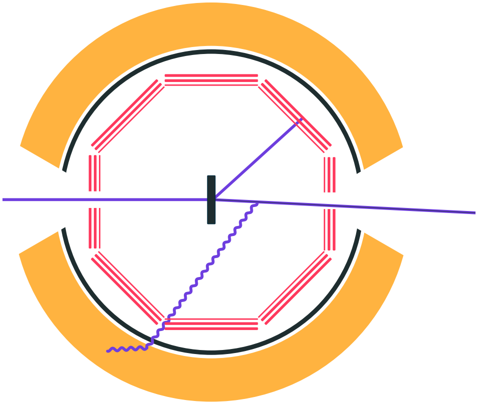

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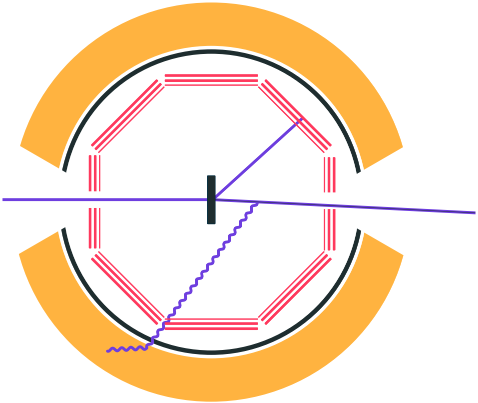

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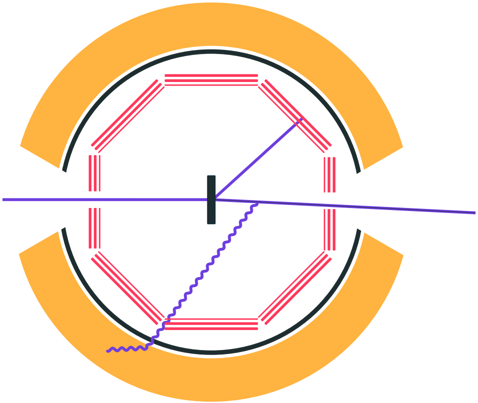

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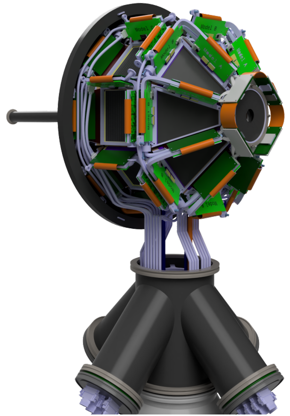
Challenge of integration!

Overall architecture Y. Peinaud (IJCLab)



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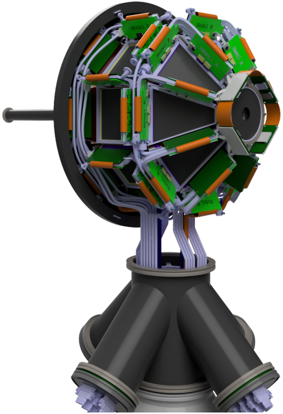
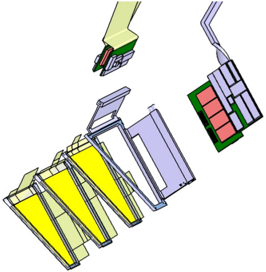


Early telescope design E. Rindel (IJCLab)



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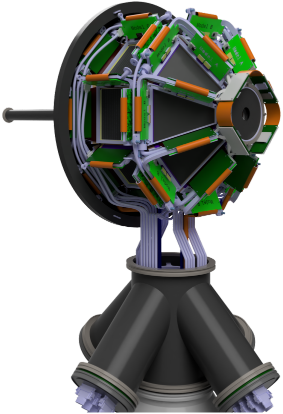
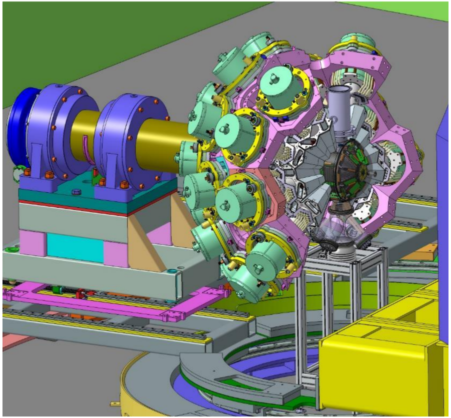
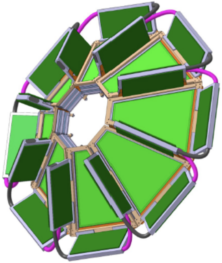


GRIT/AGATA@SPES Y. Peinaud (IJCLab)

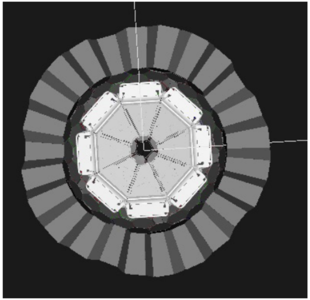


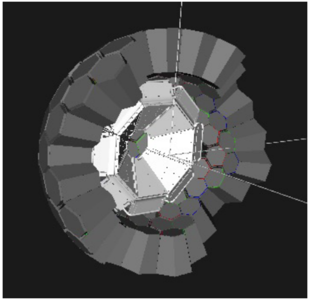
Geant4 simulation S. Bottoni (Milano)

CAD



GDML-GEANT4*





*E. Gamba

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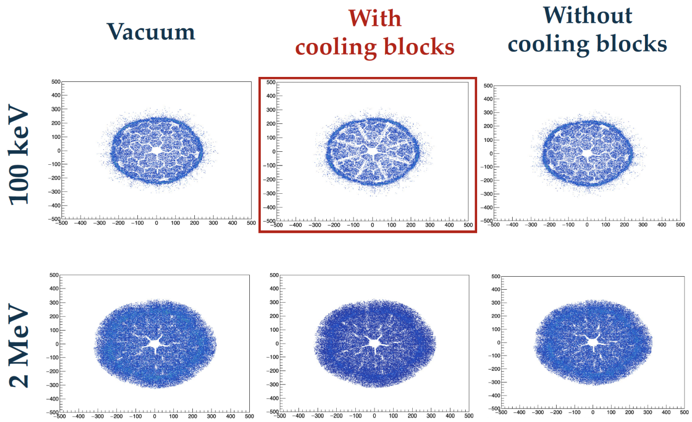

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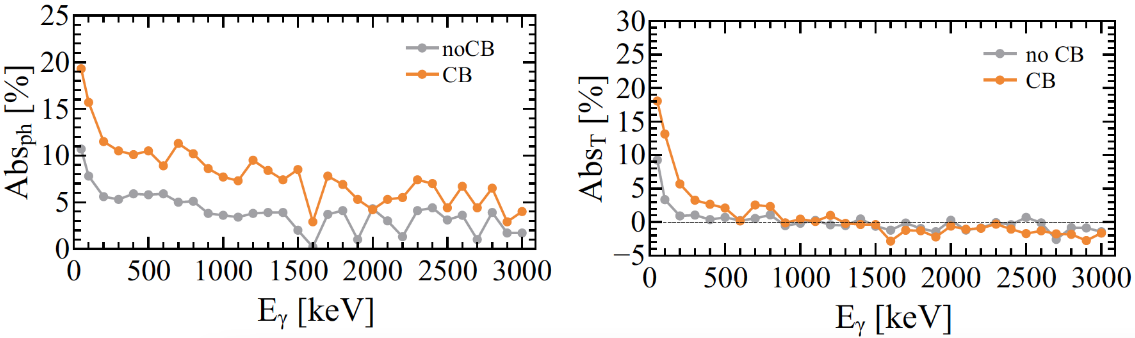
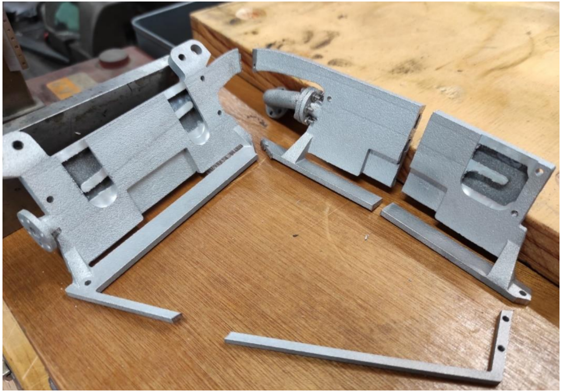


3D printed Frame Y. Peinaud (IJCLab)



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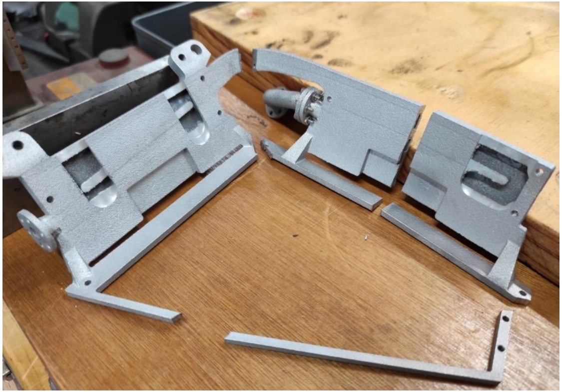
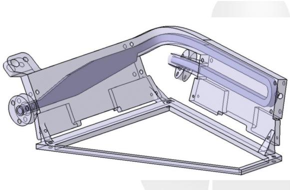
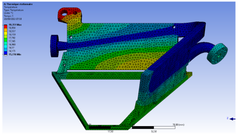
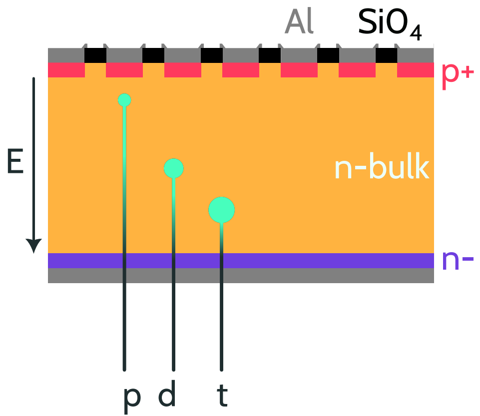


Thermal Study P. Rosier (IJCLab)





Stopping power at 5 MeV



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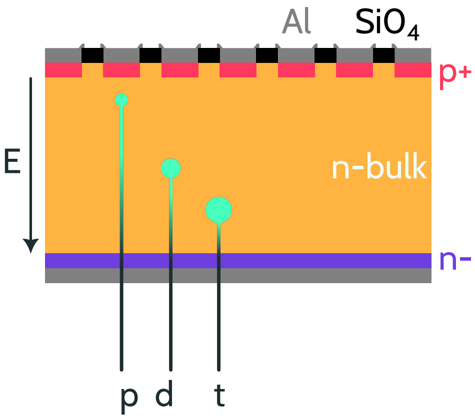
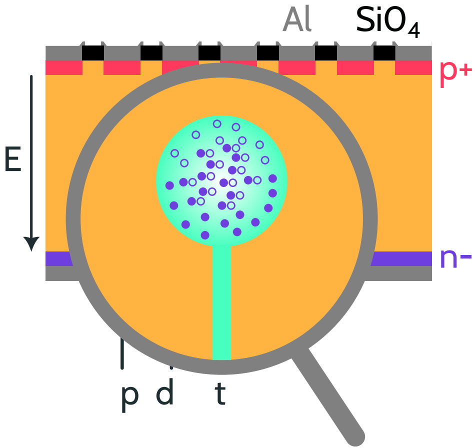


Physics at play

Energy loss:

- Higher Z, Higher A
  → Faster deposit

Stopping power at 5 MeV



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  - → **in smaller area**

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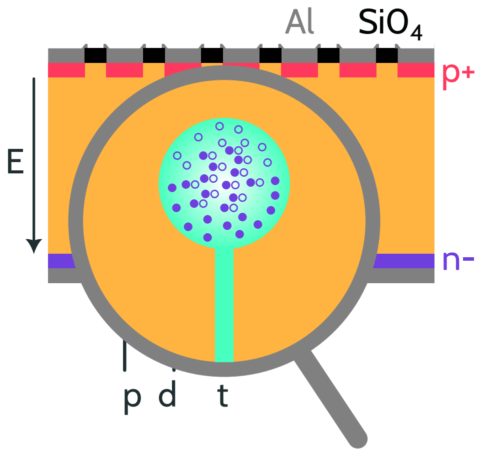

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Charge collection:

- High density of charge
  → **slower collection!**

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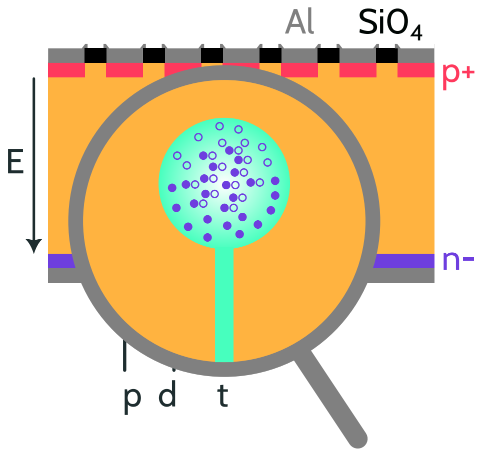

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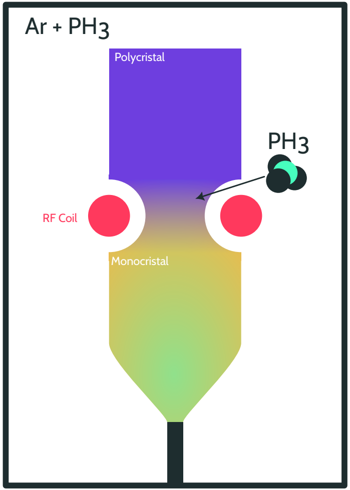
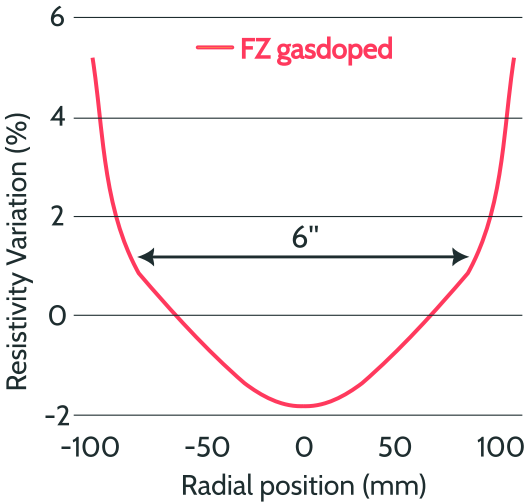
Implications

- Strong dependence to bulk resistivity
  - **High Resistivity → production process**
  - **High Homogeneity → doping process**

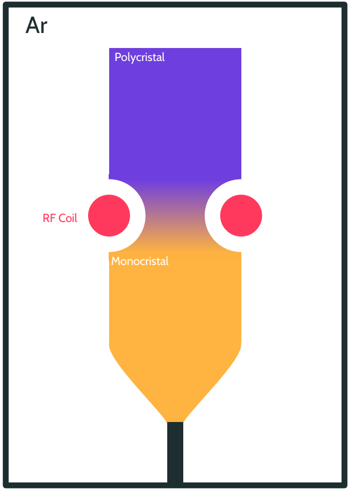
making Float Zone ingot



Resistivity profile (JCG 512(2019)65-68)



making nTD ingot 1/6



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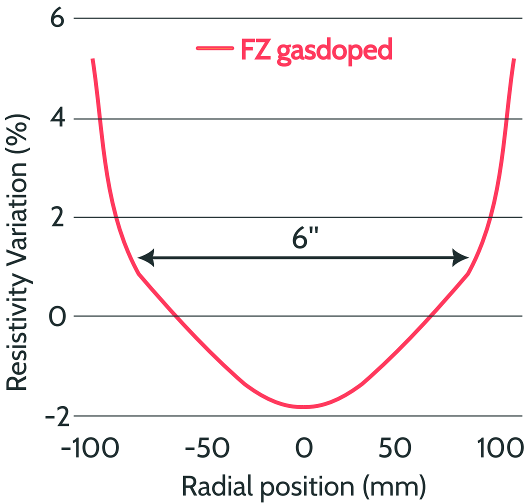
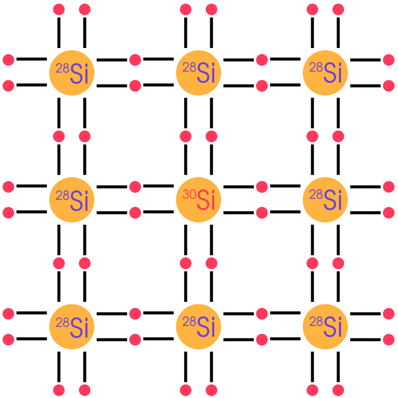


making nTD ingot 2/6



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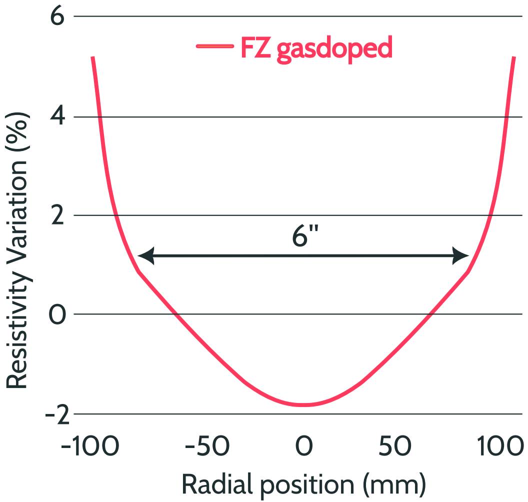
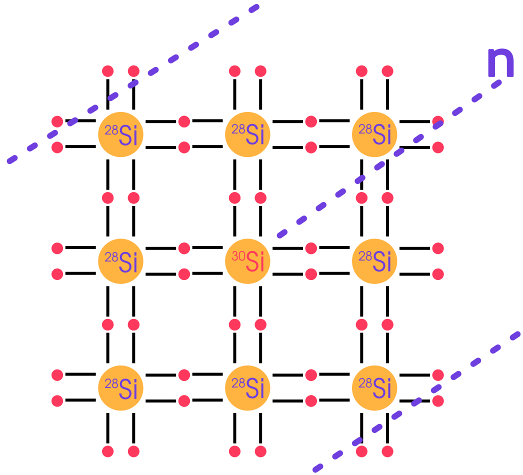


making nTD ingot 3/6



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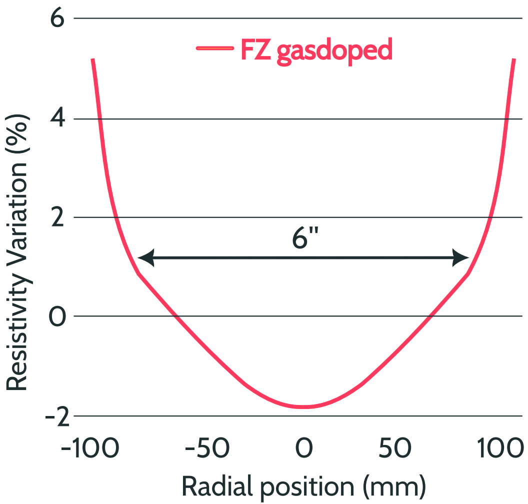
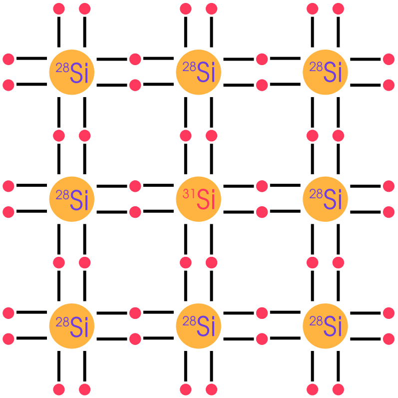


making nTD ingot 4/6



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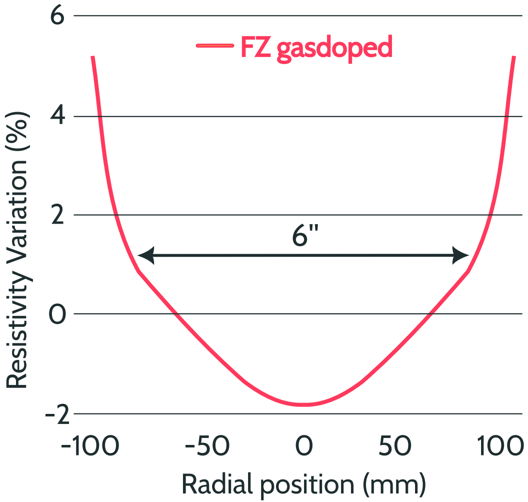
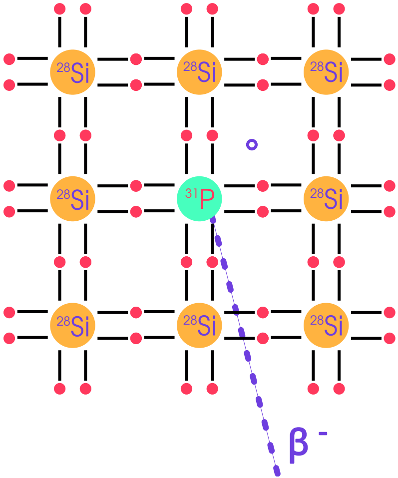


making nTD ingot 5/6



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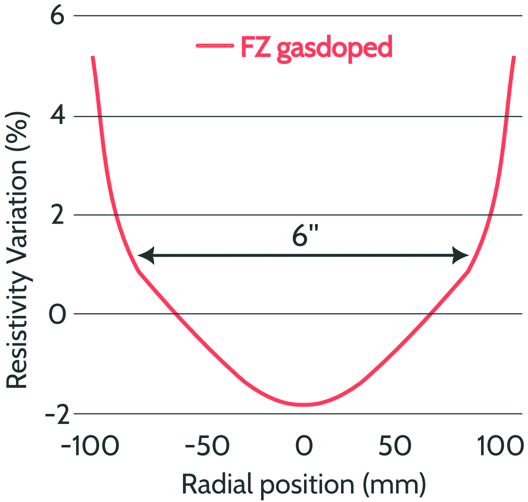
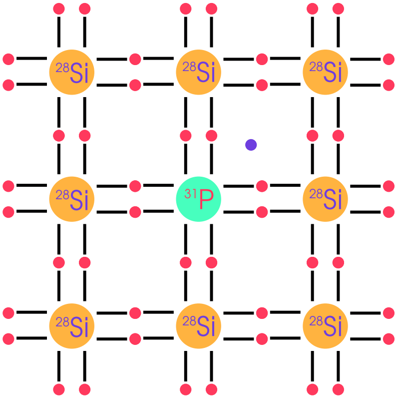


making nTD ingot 6/6



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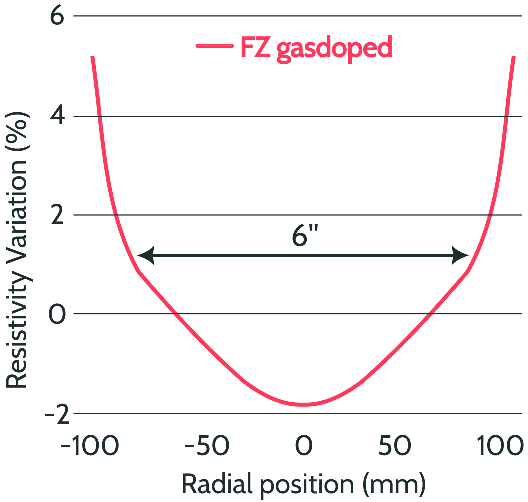

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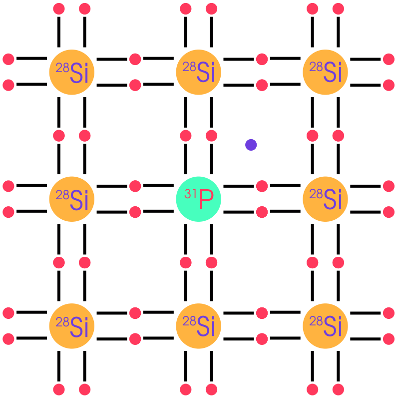
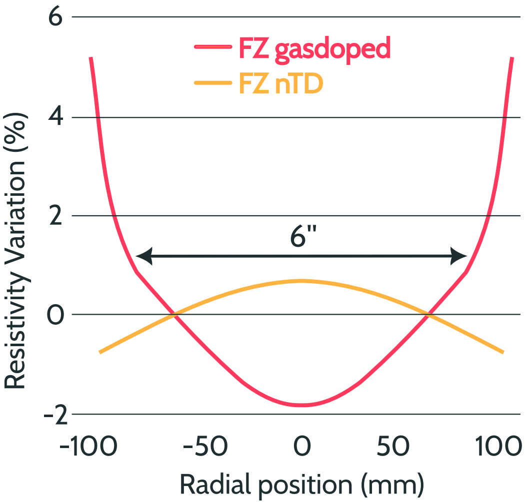
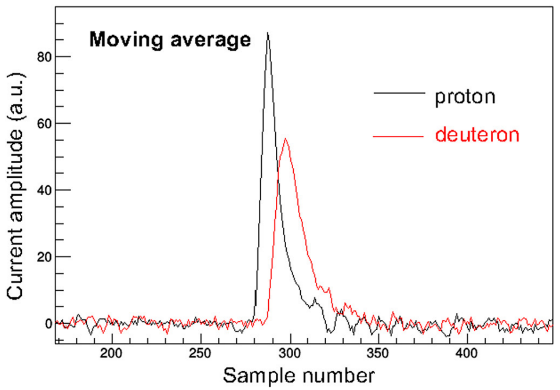


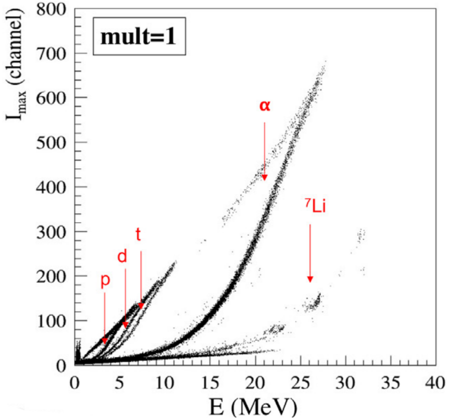
Resistivity profile (JCG 512(2019)65-68)



Current Signal



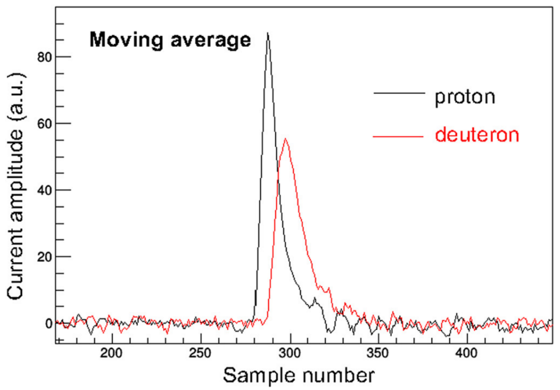
ID from PSA



M. Assié, *et al*, EPJA 51-11(2015) → **at least 200 Msample/s**

JJ.Dormard, M. Assié, *et al*, NIMA 1013(2021)165641 → **integrated PAC (iPACI)**

Current Signal



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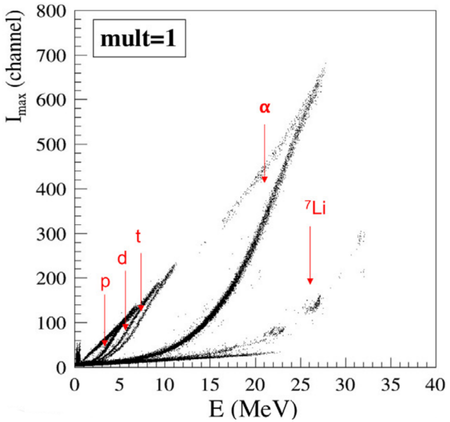

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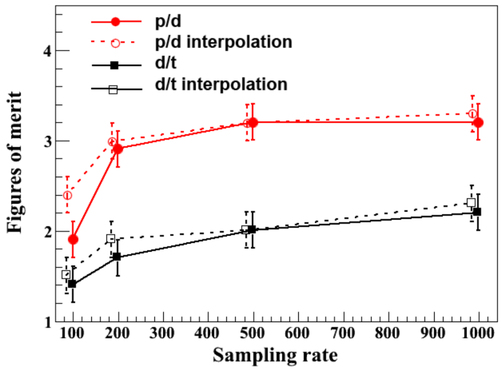
FOM vs Sampling Rate



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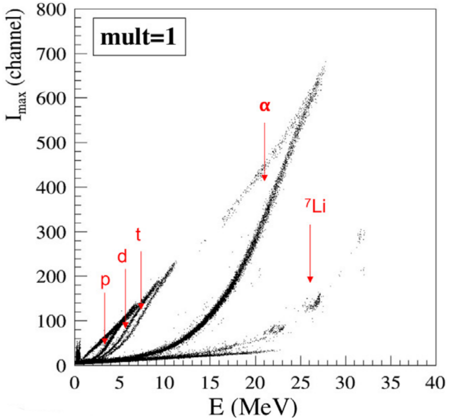

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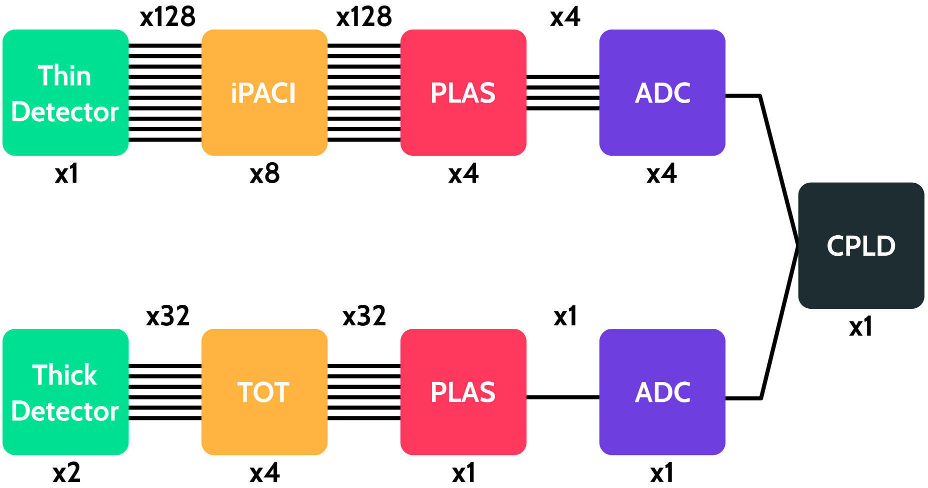
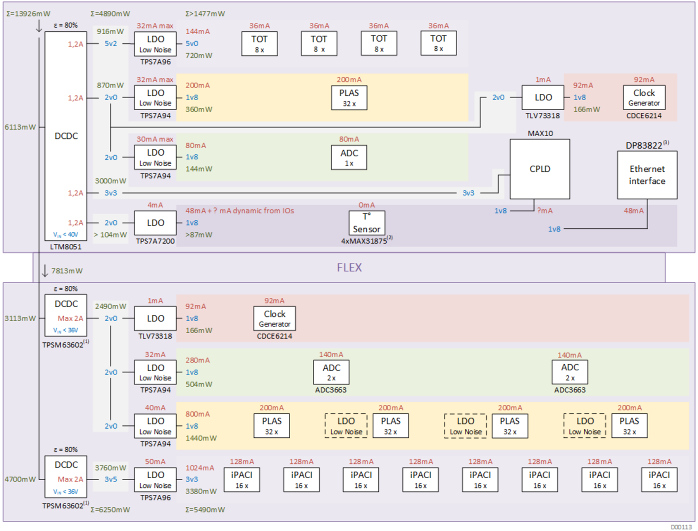
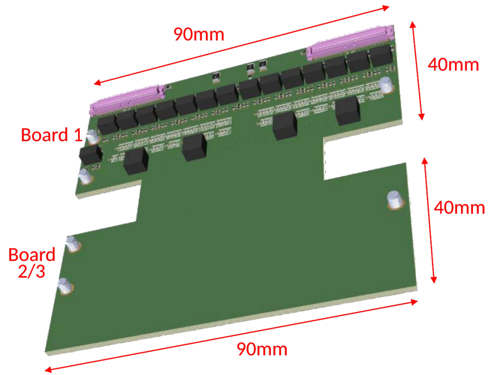
Chain layout



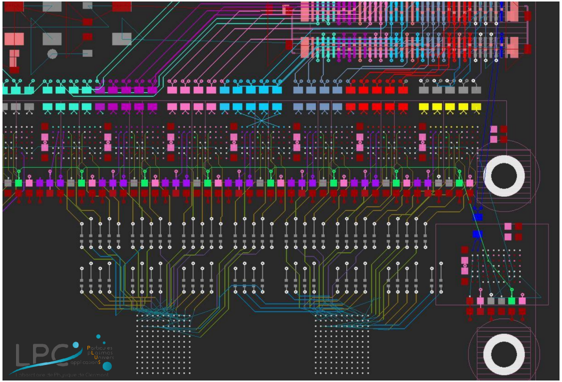
Power appraisal (L. Alvado, LPC Caen)



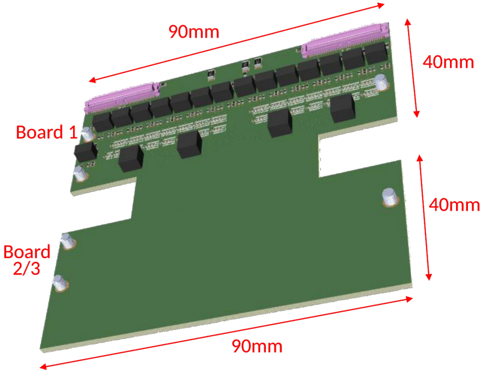
Schematic (E. Rauly, IJCLab)



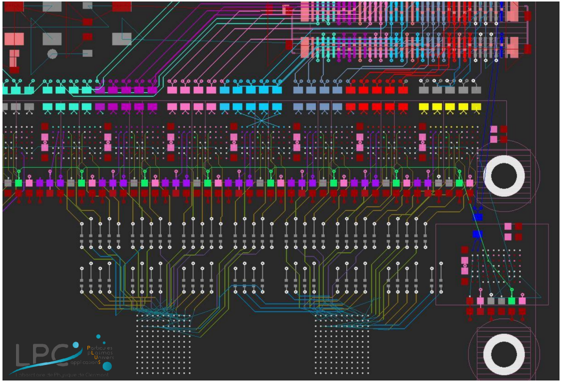
Routing (M.L. Mercier, LPClermont)



Schematic (E. Rauly, IJCLab)



Routing (M.L. Mercier, LPClermont)



BGA packaging difficult to route!

Packaging (L. Alvado, S. Drouet LPC Caen)

Bonding Diagram – PLASv2 QFN

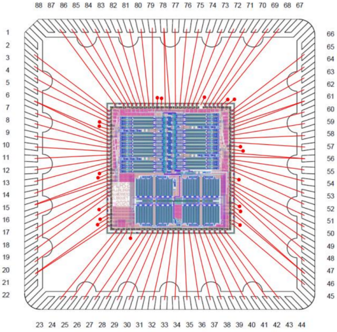
Cell name:
TOP_PLAS

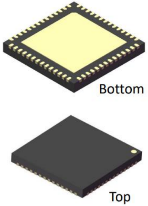
ASIC name:
PLAS2

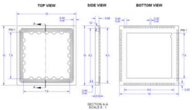
Techno:
TSI 180nm CMOS

Boitier:
- 88 pins
- QFN 88
- Cavité: 7,6 x 7,6 mm
- Boitier: 10 x 10 mm
- Pas: 0,4 mm

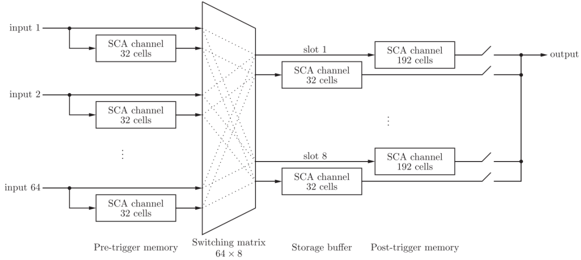
Taille circuit:
X = 3830,12 µm
Y = 4030,12 µm
Area = 15,44 mm²







PLAS ASIC principle



PLAS history

- Original idea from R. Aliaga
  (Uni. Of. Valancia / IFIC)
- V1 not functional
  issue with logic block
- V2 designed but never submitted
  submitted by LPC Caen in 2020
- V3 design at LPC Caen
  Submission in 2024

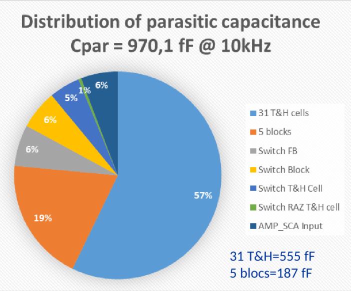
R. Aliaga *et al*, NIMA 800(2015)34-39

PLAS Redesign (S. Drouet, G. Martinez, L. Alvado, L. Leterrier, LPC Caen)

- **The total parasitic capacitance is 970 fF** compared to the memory capacitance which is 270 fF. This gives us a capacitive gain of about 4.6

- Parasitic capacitances of each elementary device:

	[illegible]
1 cellule de T&H (Hold)	17,9
1 bloc	37,4
Switches contre-réaction	62,3
Switchs Bloc V-	59,2
Switch TH V- (Tracking)	46,5
Switch de RAZ du TH	4,4
Entrée V- AMP_SCA	55,8



- The parasitic capacitance is mainly dominated by the capacity of the 31 T&H switches in "hold" mode followed by the capacity of the 5 blocks. About 742 fF for these 2 blocks

PLAS Redesign (S. Drouet, G. Martinez, L. Alvado, L. Leterrier, LPC Caen)

	Sampling Noise [892,857 kHz; 1 GHz]	Reading Noise [200 kHz; 1 GHz]	Total Noise	SNR	DC ENOB
PLASv2 Schematics	672 μV_{RMS}	755 μV_{RMS}	917 μV_{RMS}	52,5 dB	8,4 bits
Modified Schematics [1]	227 μV_{RMS}	478 μV_{RMS}	455 μV_{RMS}	58,6 dB	9,4 bits
Modified Schematics [3]	**178 μV_{RMS}**	**282 μV_{RMS}**	**293 μV_{RMS}**	**62,5 dB**	**10,08 bits**
Modified Schematics [4]	170 μV_{RMS}	271 μV_{RMS}	281 μV_{RMS}	62,8 dB	10,14 bits
Without input amp + [4]	117 μV_{RMS}	271 μV_{RMS}	253 μV_{RMS}	63,7 dB	10,30 bits

Be careful: $TotalNoise = \sqrt{{\sigma_S}^2 + \left(\frac{\sigma_R}{1,21}\right)^2}$

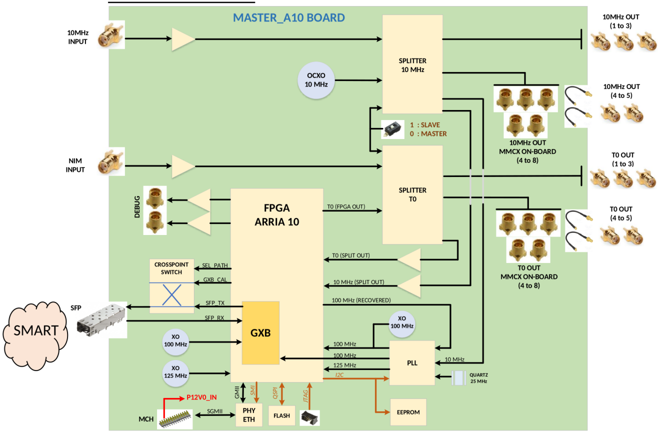
Modified Schematics :

- AMP_IN :
  - Input stage modified by Ludo
  - Cc=732 fF instead of 579 fF
- [1] : BUF_REF deleted + decoupling Cap added
- **[3]** : [1] + **Cmem=540 fF** + AMP_SCA Cc=1,53 pF + **Swap T&H Cells**
- [4] : [3] + 1 AMP_SCA per block

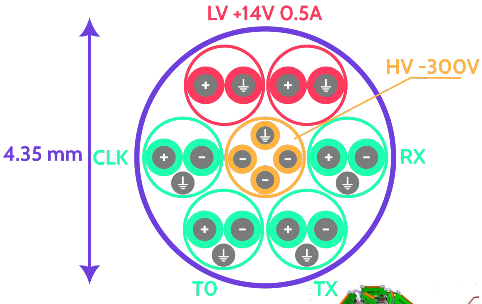
MASTER A10 (F. Ingouf, G. Wittwer, GANIL & D. Etasse, B. Carniol, LPC Caen)

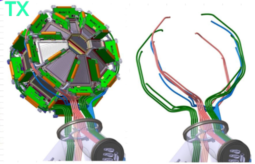
GRIT : SMART protocol with FASTER

BOARD SYNOPSIS :

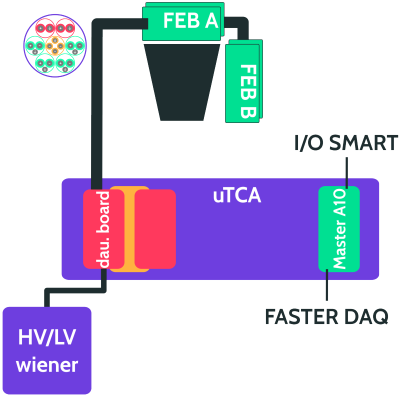


Cable D. Etasse, LPCCaen, Y Peinaud, IJCLab

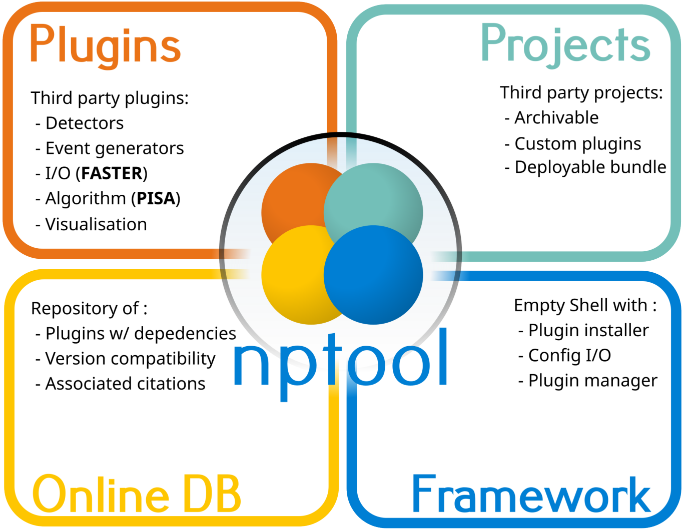




BEE (D. Etasse, B. Carniol, A. Matta, LPC Caen)



development framework



IJCLab

M. Assié, D. Beaumel, Y. Bluxmenfeld, V. Girard-Alcindor, Y. Peinaud, E. Rauly, P. Rosier, C. Soulet

LPC Caen

L. Alvado, B. Carniol, S. Drouet, D. Etasse, F. Flavigny, L. Letterrier, G. Martinez, A. Matta, J. Poincheval

GANIL

F. Ingouf, G. Wiettwer, G. de France

Italy

S. Bottoni, S. Capra, F. Galtarosa, A. Gottardo, D. Mengoni

UK

W. Catford, C. Paxman

Spain

A. Gadea, B. Fernandez-Dominguez

The GRIT timeline