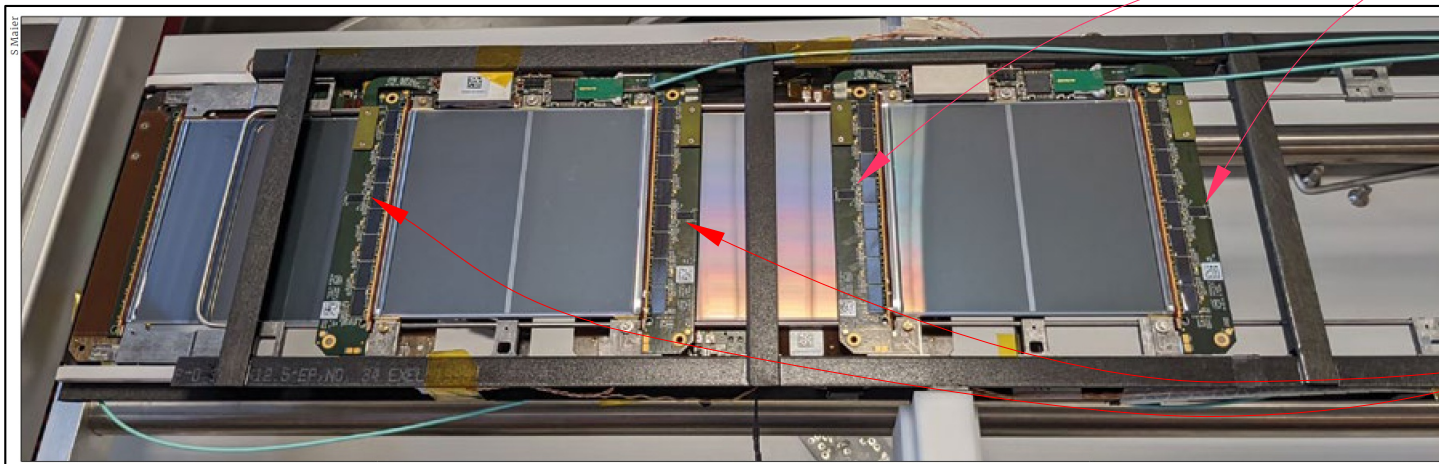
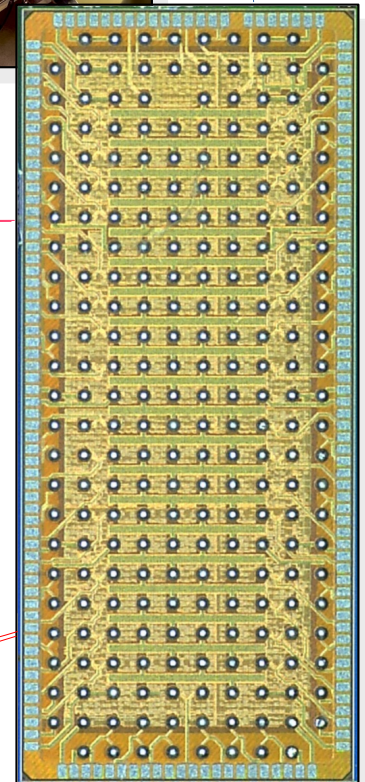
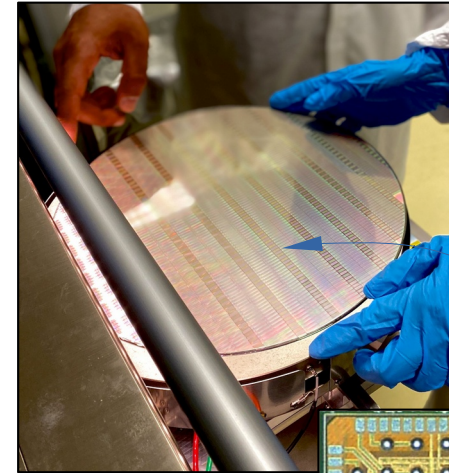


The design of the CIC

- Concentrator IC (CMS upgrade for the High Luminosity LHC)
- TSMC 65n technology
- flipchip (bumps) + wirebond pads (for testing purposes) without encapsulation
- radiation tolerance: $\sim 100\text{Mrad}$ TID in worst case
- Single Event Transient and Upset resistant
- 3 IRs full time from 2017 to 2019 (IP2I)
- three foundry submissions (2018, 2019, 2021)
- punctual support from CERN ASICS group (management, design and tools)
- wafers production already started: 30K diced and tested chips to be integrated in the CMS OT Tracker

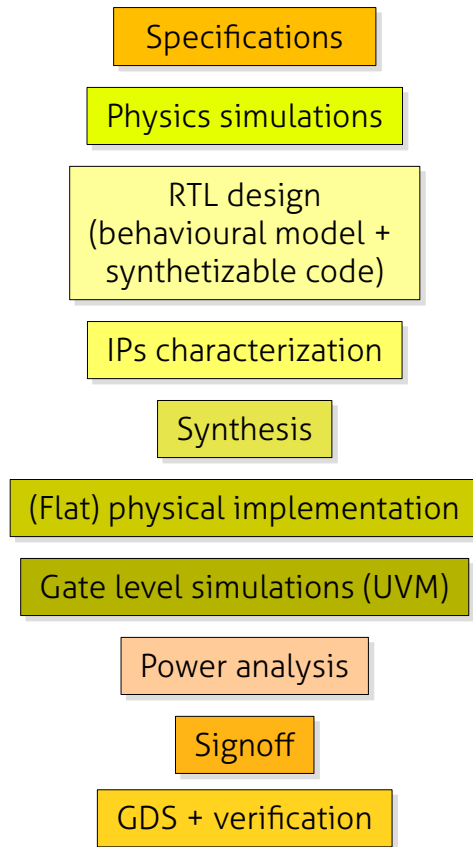


Photograph of two CMS Outer Tracker Strip-to-strip (2S) modules: the CICs are highlighted

Design methodology at IP2I

The CIC design followed a Digital On Top methodology:

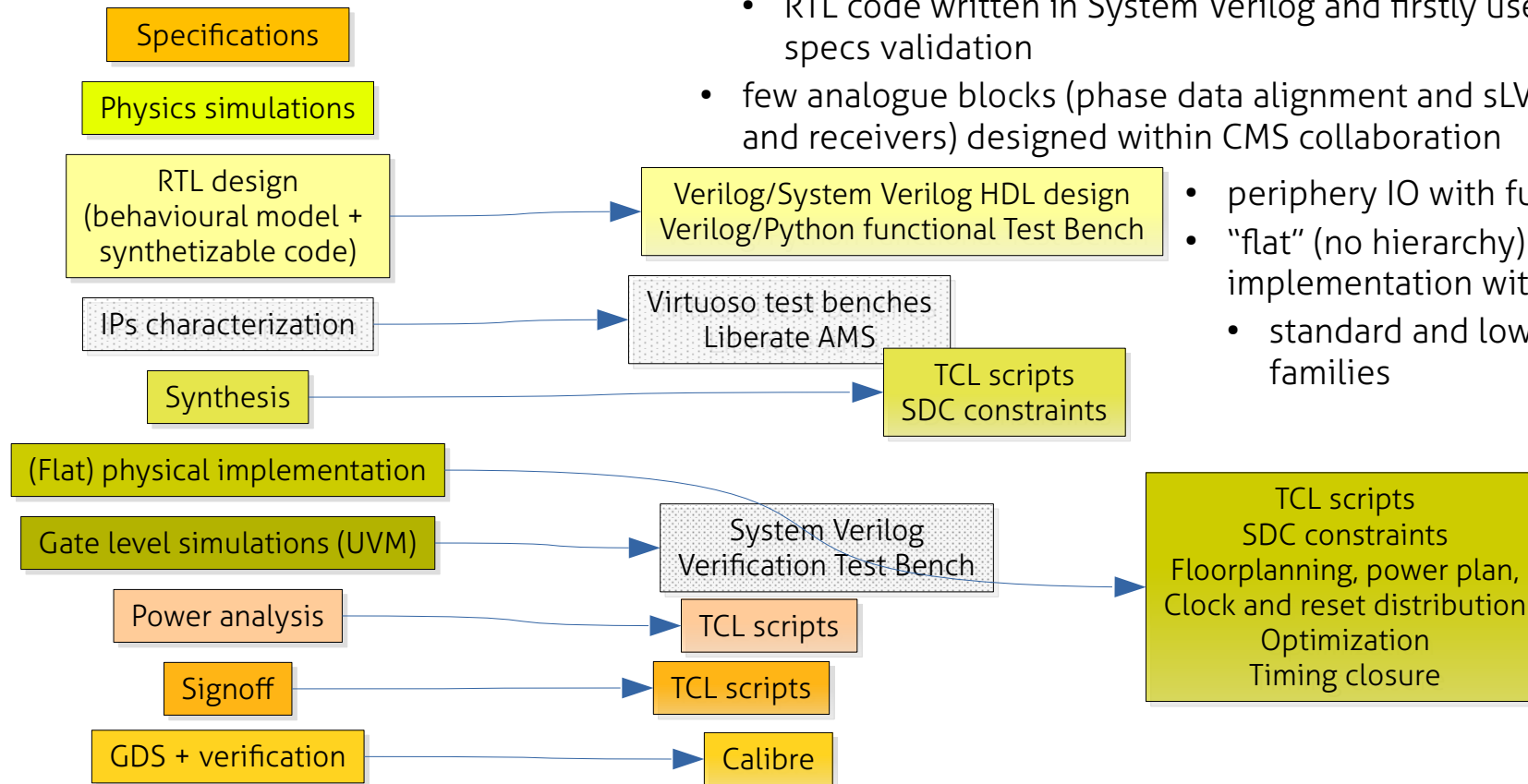
- fully digital core design (data handling, store and forward)
 - RTL code written in System Verilog and firstly used for design specs validation
- few analogue blocks (phase data alignment and sLVS transmitters and receivers) designed within CMS collaboration



Design methodology at IP2I

The CIC design followed a Digital On Top methodology:

- fully digital core design (data handling, store and forward)
 - RTL code written in System Verilog and firstly used for design specs validation
- few analogue blocks (phase data alignment and sLVS transmitters and receivers) designed within CMS collaboration
 - periphery IO with full custom ESD and IOs
 - “flat” (no hierarchy) digital implementation with single core supply:
 - standard and low VT standard cell families



(many) questions

