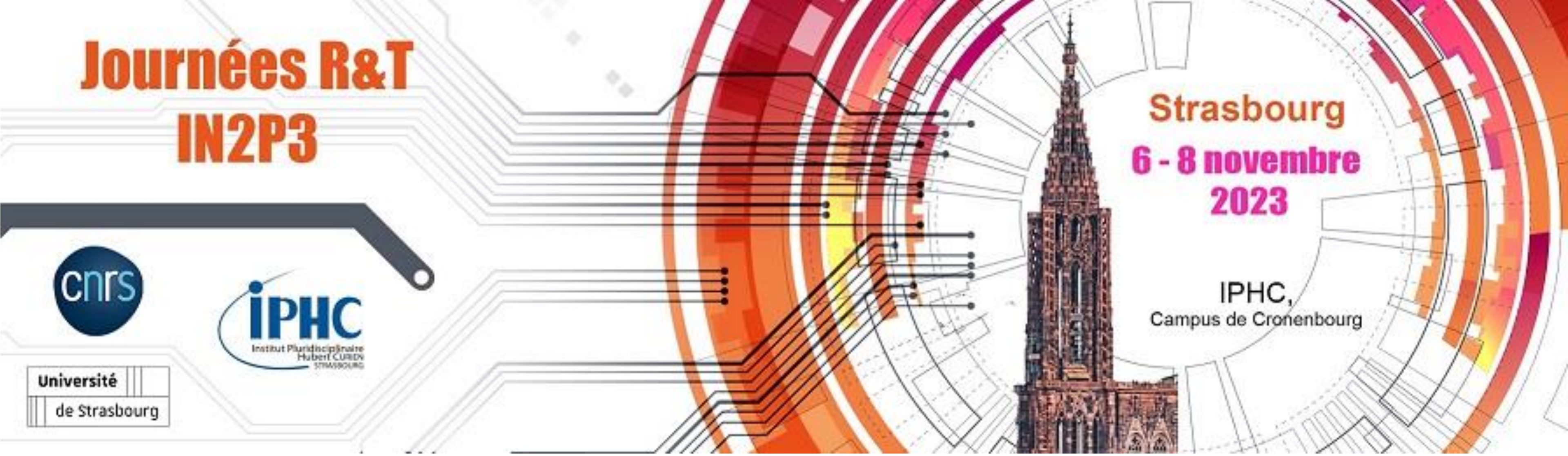
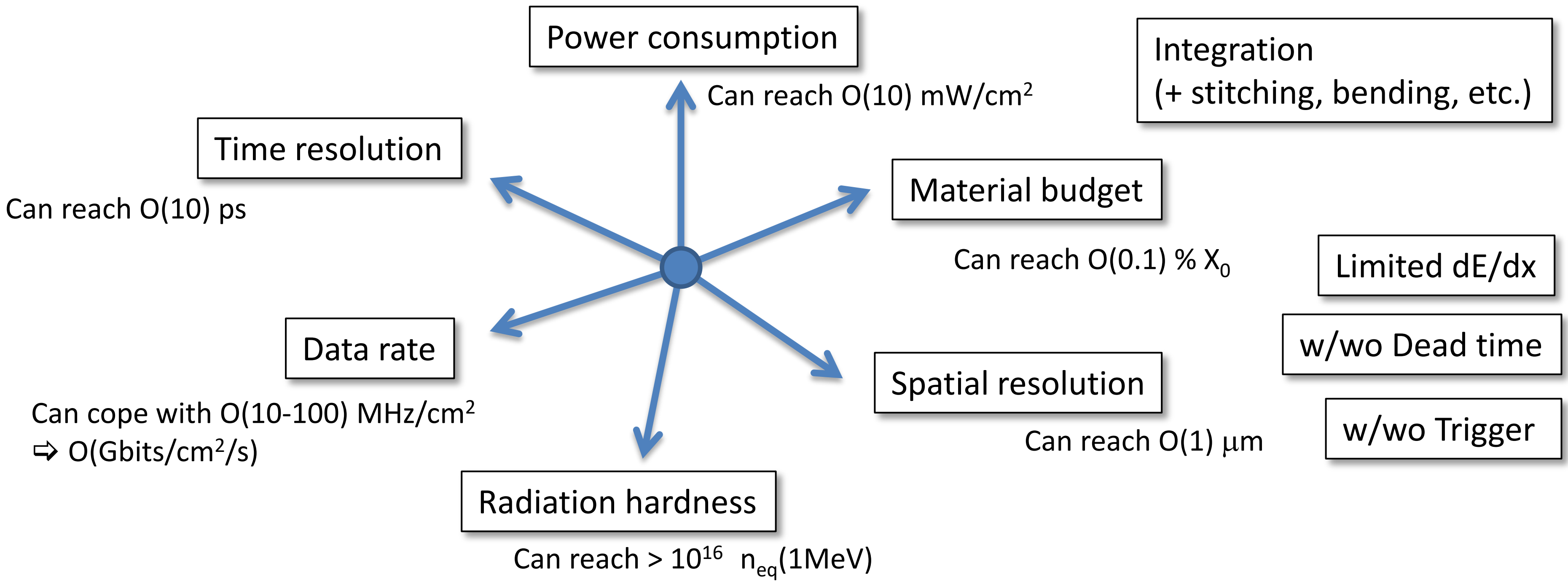


GRAM
Développement de capteurs GRAnulaires, Minces et basses puissances pour la trajectométrie et le vertexing

- Scientific context and motivations
- Tasks
  - ❑ Task 1: Full size prototype MIMOSIS
  - ❑ Task 3: Generic R&D and CMOS 65 nm technology
  - ❑ Task 2: Tests & integrations
  - ❑ Task 4: spin off
- Summary

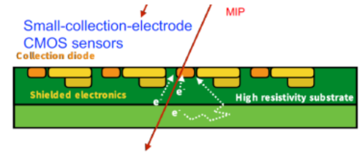
Silicon detector figure of merit for HEP

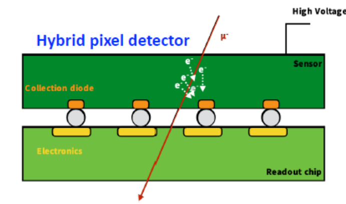


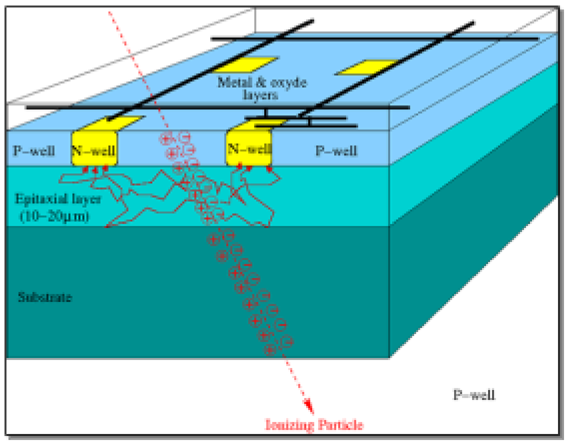
- Ultimate performances look like the ideal tracking or vertexing detector. However
  - ✓ Very antagonist requirements (e.g. Data rate and Power, time vs spatial resolution, etc.)
- Need a **hierarchy** and/or **specialized** layers
  - ✓ Governed by physics requirements and experimental conditions
  - ✓ R&D needed to improve the parameter space
- CMOS Monolithic Active Pixels Sensors (MAPS)
  - ✓ Offers the best compromise in many applications

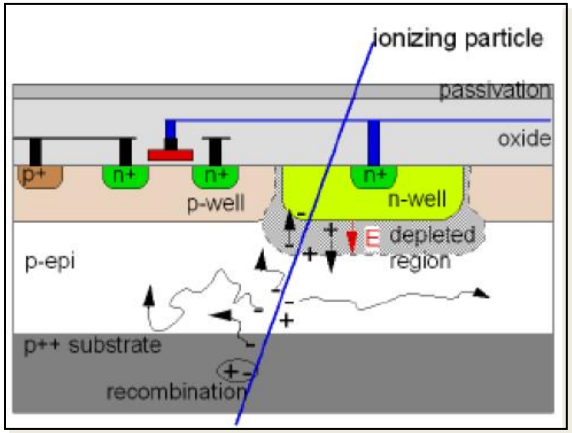
CMOS-MAPS for charged particle detection

- Main features
  - ✓ Monolithic, p-type Si
    - Signal created in low doped thin epitaxial layer ~O(10) µm
    - ~ 80 e- /µm ⇨ total signal ~ O(1000 e-) ⇨ low noise electronic
  - ✓ Charge collection: diffusion of e- ⇨ N-Well diodes
    - Partial depletion ⇨Charge sharing ⇨ resolution
    - Possible full depletion ⇨Higher S/N & rad. tol.
  - ✓ Continuous charge collection
    - No dead time
- Main advantages
  - ✓ Granularity
    - Pixel pitch down to 10 x 10 µm^2 ⇨spatial resolution down to ~ 1 µm)
  - ✓ Material budget
    - Sensing part ~ 10-20 µm ⇨ whole sensor routinely thinned down to 50 µm
  - ✓ Signal processing integrated in the sensor
    - Compacity, flexibility, data flux
  - ✓ Flexible running conditions
    - From ≤ 0°C up to 30-40°C if necessary
    - Low power dissipation (~ 150-250 mW/cm^2) ⇨ material budget
    - Radiation tolerance: >~ MRad and O($10^{13\text{-}14}$ n_{eq}) ⇨f(T,pitch)
  - ✓ Industrial mass production
    - Advantages on costs, yields, fast evolution of the technology,
    - Possible frequent submissions
    - Smaller feature size, adapted epitaxial layers, doping profile to enhance depletion
- Main limitations
  - ✓ Industry addresses applications far from HEP experiments concerns
    - Different optimizations on the parameters on the technologies
    - R&D costs
  - ✓ High expertise needed (from design to tests & characterizations)
  - ✓ Long R&D needed for a given application





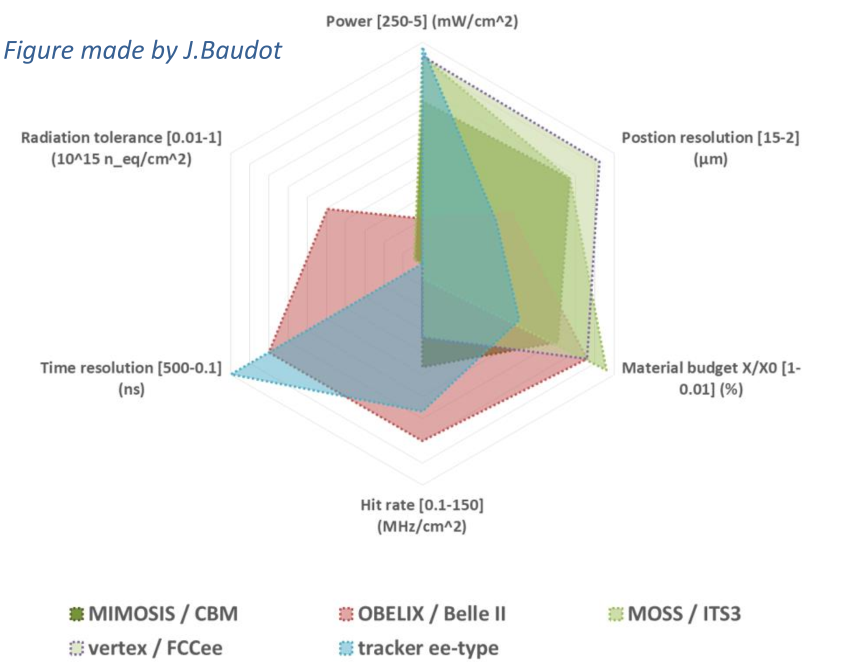




Pixel detector requirements

	past			present			future					
	MIMOSA28 STAR	ALPIDE ITS2	MIMOSIS CBM	OBELIX Belle II	MOSS ITS3 ALICE	ITK R&D ATLAS	Vertex ALICE3	vertex FCCee	Tracker ALICE3	tracker ee-type	Up. Tracker LHCb	Tracker hh-type
Power (mW/cm^2)	170	35	70	200	20	200,0	20	20	10	10	100	100
Postion res. (µm)	4	5	5	9	5	10,0	2,5	3	10	5-10	10	15
Mat. budget X/X$_0$ (%)	0,37	0,3	0,3	0,15	0,05	1,0	0,05	0,15	0,5	0,5	0,3	1
Hit rate (MHz/cm^2)	0,1	1	70	120	10	120,0	35	50	0,005	10-100	200	200
Time resolution (ns)	200000	5000	5000	100	5000	25,0	100	500	100	1-500	1	0,1
Rad. tolerance (10^{15} n_{eq}/cm^2)	0,001	0,05	0,05	0,5	0,05	2,0	1	0,0011	0,01	0,001-1	3	9
Sensor size (cm^2)	4,6	4,5	5,4	5,7	300,0	5,0	300,0	6,0	100,0	100,0	6,0	100,0

Figure made by J.Baudot



« high granularity vertex »
(ALICE ITS-3, FCCee, ALICE3 vtx)

GRAM

« outer trackers »
(Belle-II trk, ALICE-3 trk, FCCee trk)

DEPHY

« high flux & rad. tol. »
(ATLAS, LHCb upgrades, FCChh)

European programs (AIDAInnova, Eurizon)

ECFA Detector Technology roadmap

DRD3/DRD7

IN2P3

GRAM Master Project

DEPHY

C4PI platform

Design, build and exploit CMOS pixels sensors with <u>low material budget</u> & <u>high granularity</u>
In order to contribute to the construction of a vertex & a tracking detector

Future Higgs Factories

Heavy ions experiments, Belle-2, etc.

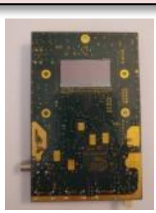
Approach the Higgs factories vertex detector requirements

Input for detector simulations

Exploit fully the potential of the CMOS technology

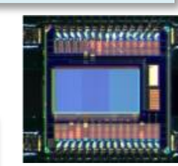
Optimize the parameters of the technology (e.g. sensitive layer)

MIMOSIS chip family (180 nm)



Maintain & develop the know how to build sensors to be installed in real experiments

R&D 65 nm



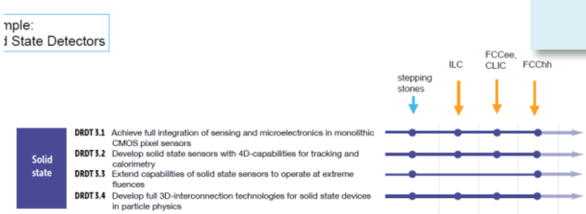
Large surfaces (stitching)

Bent sensors

Exploring new architectures

Integration

Emerging technologies
(e.g. double tier)



GRAM organization

- Recent changes
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  - ✓ Tests, characterizations
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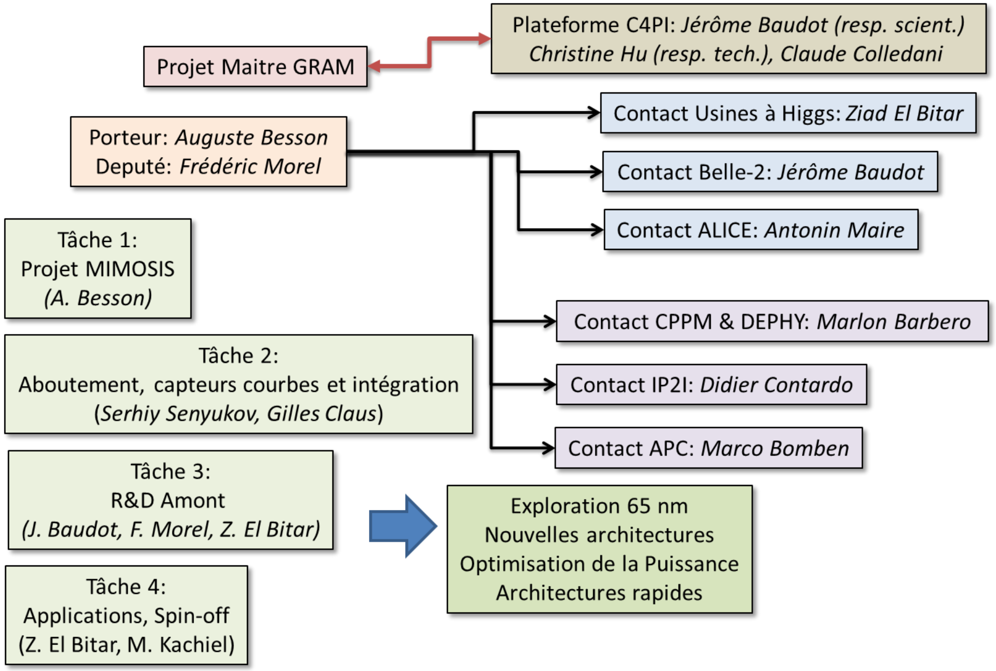
  - ✓ DRD-3 project (telescope demonstrator)
  - ✓ Architectures
    - Asynchronous read-out
    - In pixel preamplification
    - In pixel ADC
    - Timing measurement
- Task 4: applications, spin off



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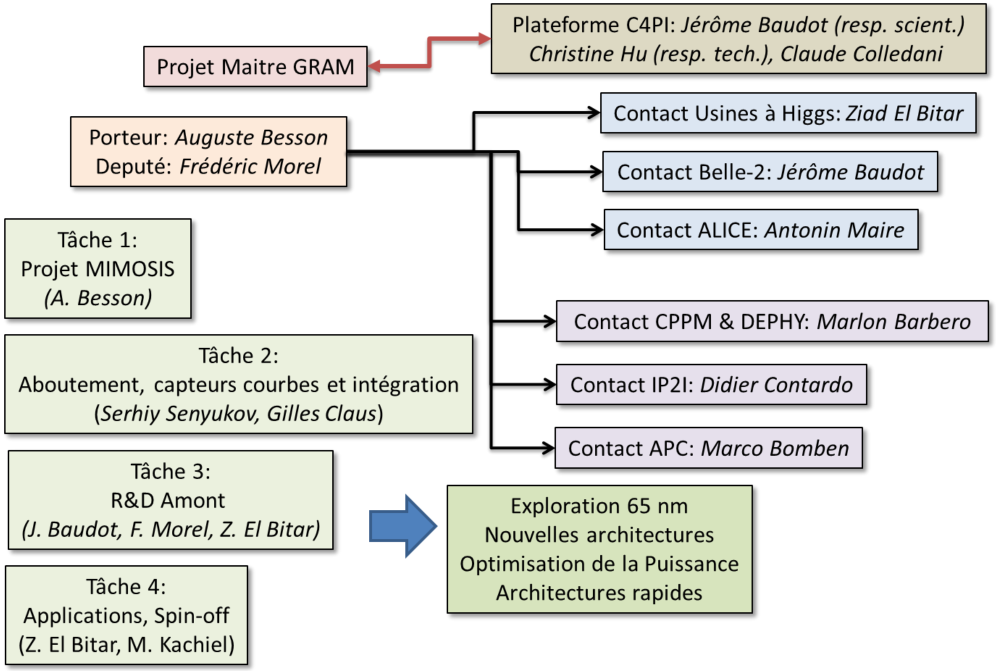
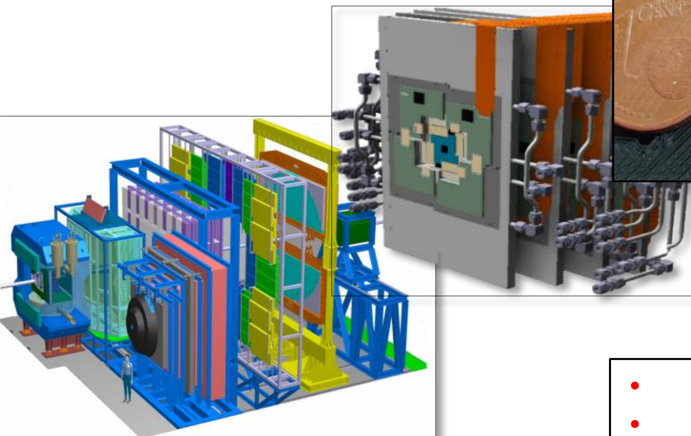
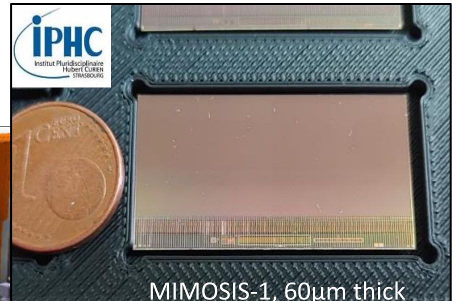


CBM Micro Vertex Detector (MVD) / MIMOSIS requirements

- Requirements





CBM – Experiment @ FAIR

Physics parameter	Requirements
Spatial resolution	~ 5 um
Time resolution	~ 5 us
Material budget	0.05% X_0
Power consumption	< 100 – 200 mW/cm^2
Operation temperature	- 40 °C to 30 °C
Temp gradient on sensor	< 5K
Radiation tol* (non-ion)	~ 7 x 10^{13} n_{eq}/cm^2
Radiation tol* (ionizing)	~ 5 MRad
Data flow (peak hit rate)	@ 7 x 10^5 / (mm^{2}s) > 2 Gbit/s

Similar to ALPIDE (spatial resolution, time resolution, material budget)

~ x10 ALPIDE (radiation tolerance)

~ x2 ALPIDE (data flow)

- 4 double-sided thin planar detector stations
- 100 kHz Au+Au @ 11 AGeV and 10GHz p+Au @ 30 AGeV
- Non uniform hit density in time and space
- High radiation environment, operating in vacuum

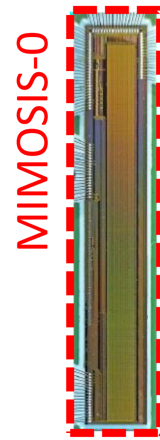
- MIMOSIS chip
  - ✓ Based on ALPIDE architecture
  - ✓ Discriminator on 27x30µm² pixel
  - ✓ Multiple data concentration steps
  - ✓ Elastic output buffer
  - ✓ 8 x 320 Mbps links (switchable)
  - ✓ Triple redundant electronics

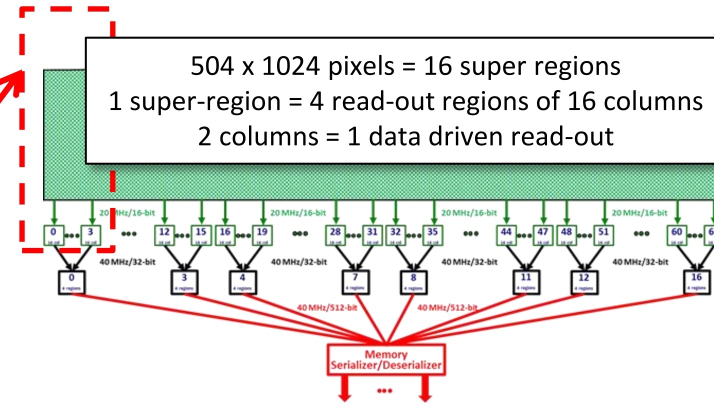
Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	$\sim 25\,\mu m$
Epi layer resistivity	$> 1k\Omega cm$
Sensor thickness	60 µm
Pixel size	$26.88\,\mu m \times 30.24\,\mu m$
Matrix size	1024 × 504 (516096 pix)
Matrix area	$\approx 4.2\,cm^2$
Matrix readout time	5 µs (event driven)
Power consumption	40-70 mW/cm^2

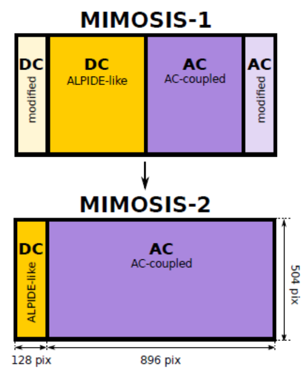
MIMOSIS = a milestone for Higgs factories (5 µm / ≤5 µs)

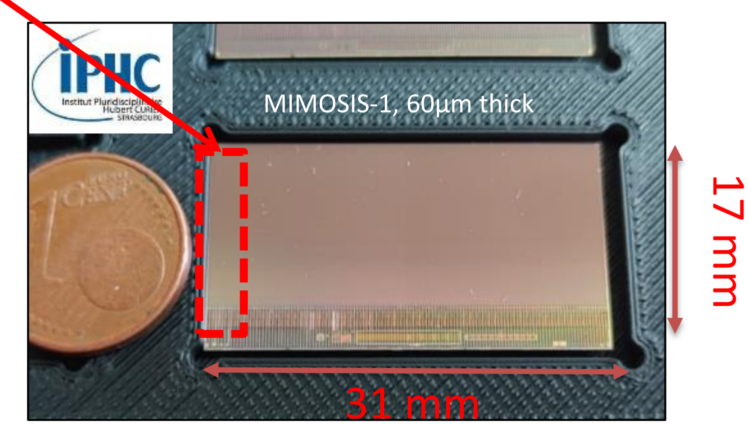
MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - ✓ Tests (2018-2019)
    - Testability
- MIMOSIS-1: 1st full size prototype
  - ✓ Elastic buffer, SEE hardened
  - ✓ Fabricated in 2020
  - ✓ Intense test campaign in 2021-22
    - Lab and beam tests
    - Irradiations
    - Latchup tests
- MIMOSIS-2:
  - ✓ On-chip clustering
  - ✓ Triplication added
  - ✓ Back from foundry Q2 2023
  - ✓ Major issues ⇨ resubmission of MIMOSIS 2.1 Q4 2023
- MIMOSIS-3: final pre-production sensor
  - ✓ ≥2025









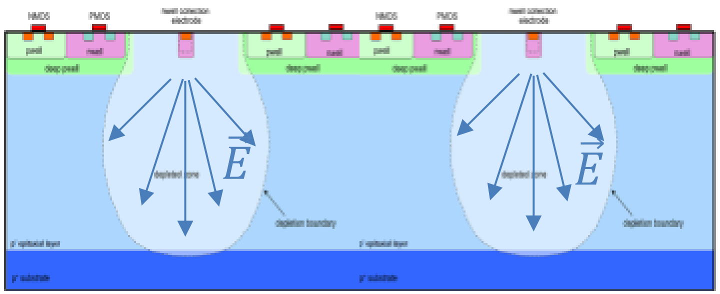
⇨ architecture adaptable to a fast sensor for a future e^+e^- collider vertex detector

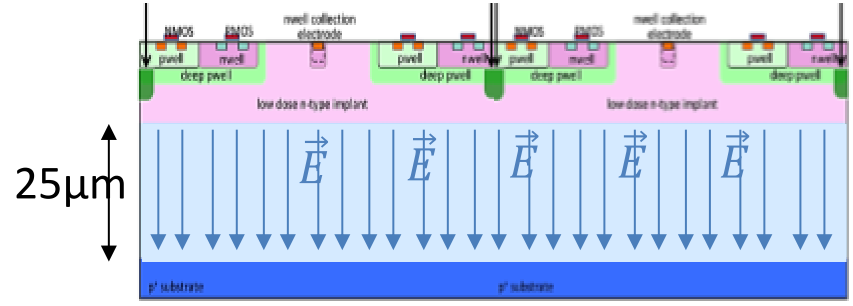
⇨ Opportunity to study different designs/options

Example: MIMOSIS (CBM-MVD) & Decision on options for sensing elements

Process modification: Standard? P-stop? N-Gap?

25 or 50 µm epi?



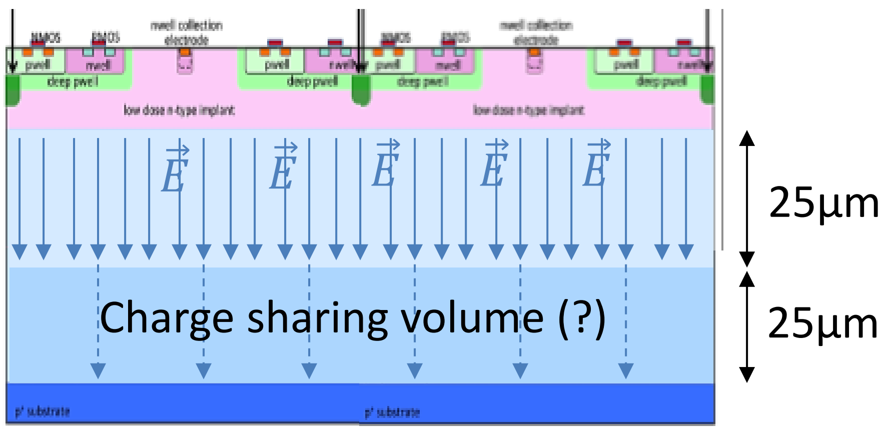


$\sigma = 4 - 5$ µm
> 3 x $10^{13} n_{eq}/cm^2$

Spatial resolution
Rad. hardness

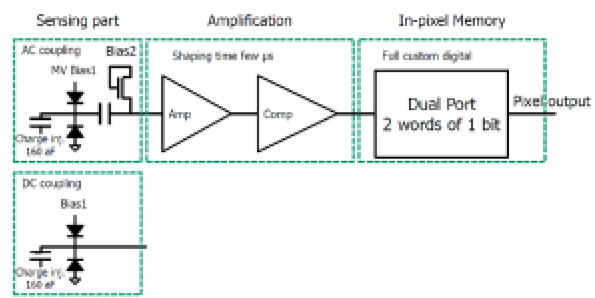
$\sigma = 5 - 7$ µm
> 30 x $10^{13} n_{eq}/cm^2$

Process options inherited from ALPIDE



- Better spatial res. at given rad. tolerance?
- Higher S/N => Robustness to external noise?
- Nuclear fragment ID by dE/dx?

AC? DC? pixel



- DC pixel – limited rad. hardness.
- AC Pixel – more biasing lines.

W. Snoeys et al., NIM-A Vol.871 (2017) 90–96.
Munker, Vertex 2018, Status of silicon detector R&D at CLIC

Lessons learned up to now

Mimosis-1

Lab tests for all different versions (pixels, process)

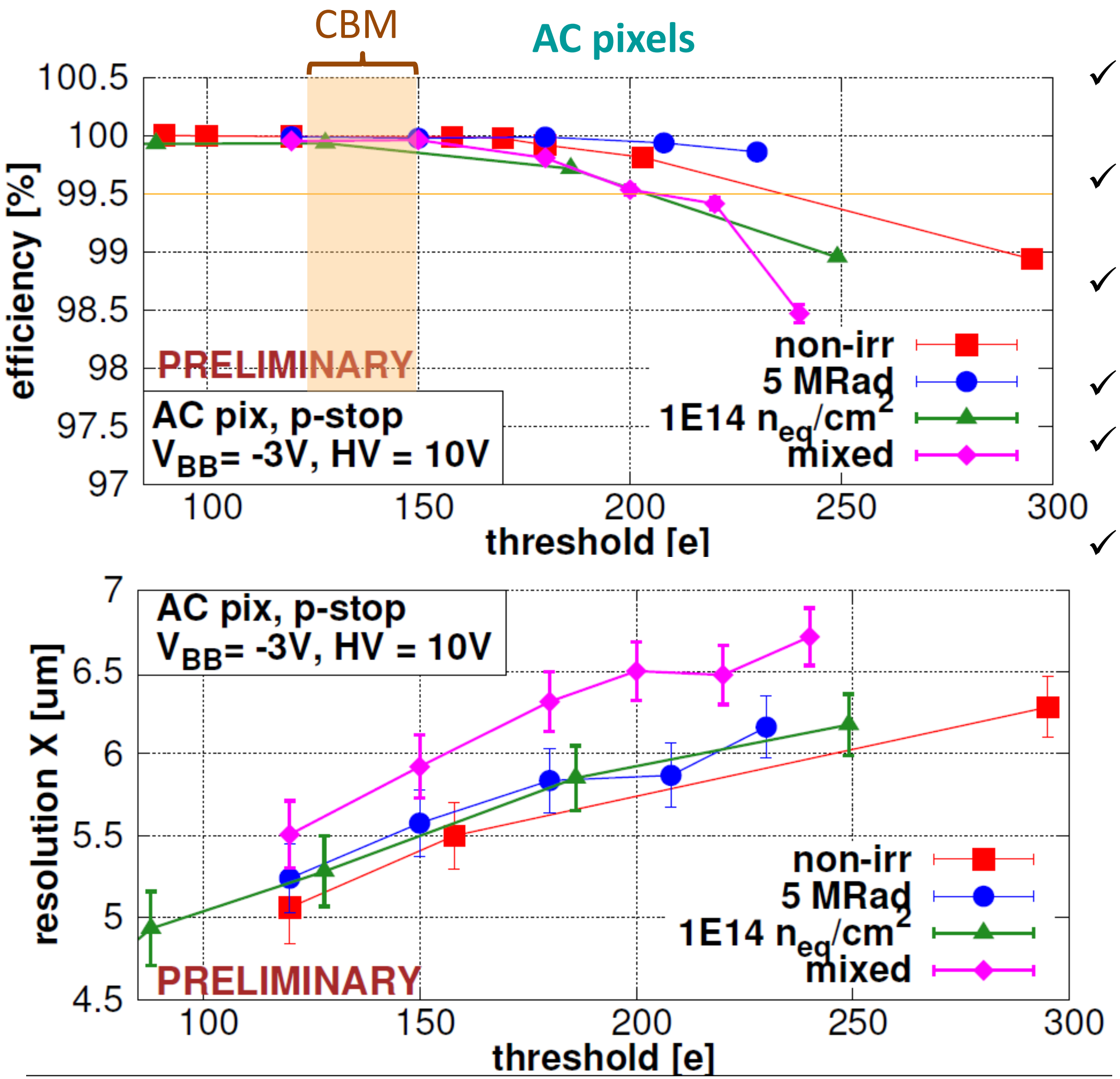
~10 beam test campaigns over 2 years (2021-22)

Single Event Effect studies (not covered here)

3 irradiations campaigns

Large FTE effort

Putting all together: Irradiations - efficiency - resolution



- ✓ Det eff. >> 99% for 10^{14} n_{eq}/cm^2 (p-stop)
- ✓ Reasonable performances after 3x 10^{14} n_{eq}/cm^2.
- ✓ Spatial resolution in the 5-6 μm range for p-stop process
- ✓ Noise under control
- ✓ Fake rate < 10^{-6} for all pixel types tested.
- ✓ "AC pixels + p-stop process" offer a very good compromise efficiency – resolution – radiation hardness
  - ✓ Performances matches requirements

⇨ Working point demonstrated after iraddiation (10^{14} n_{eq} + 5 Mrad)

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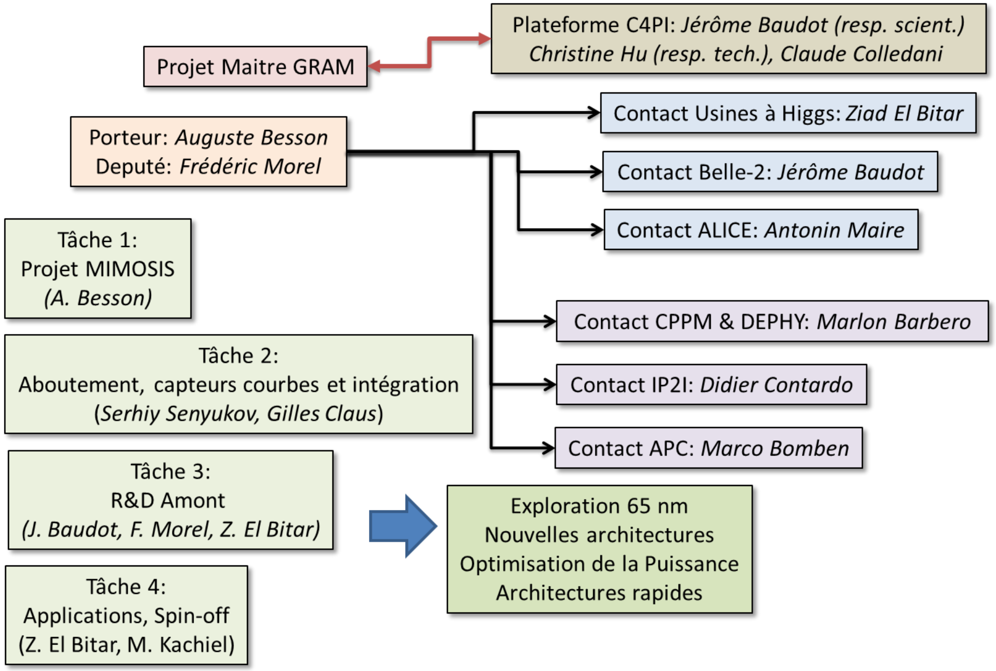
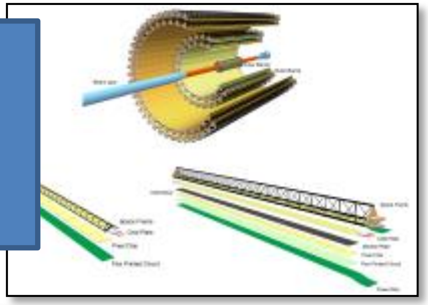
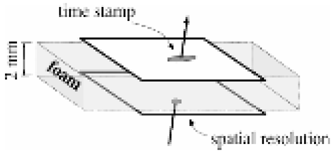


Material budget: starting from the layers

Classical single sided layers (e.g. ALICE ITS-2)



Double sided layers

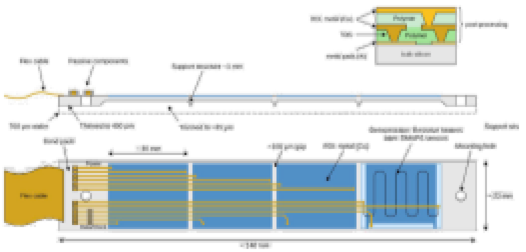


PLUME
(Bristol, DESY, IPHC)

Double sided ladders with minimized material budget
0.35% X_0 reached ⇨ ~0.3 X_0 doable (with air flow cooling)

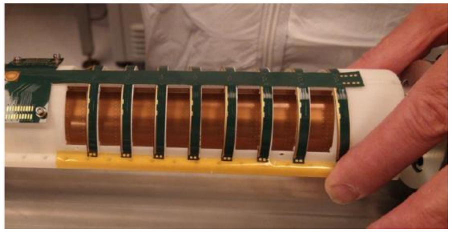
Self supported silicon (Belle-2 upgrade)

7.1x1.5 cm²
Thickness (edge/center) 430/90 µm
Planarity ~17 µm



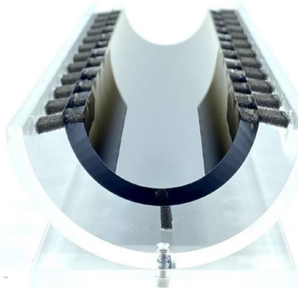
Pseudo stitching + bent sensors (superALPIDE)

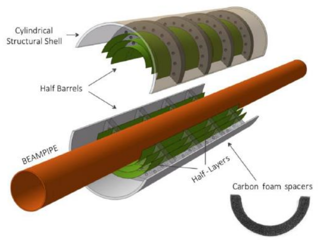
- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)



Stitching + bent sensors ALICE-ITS3

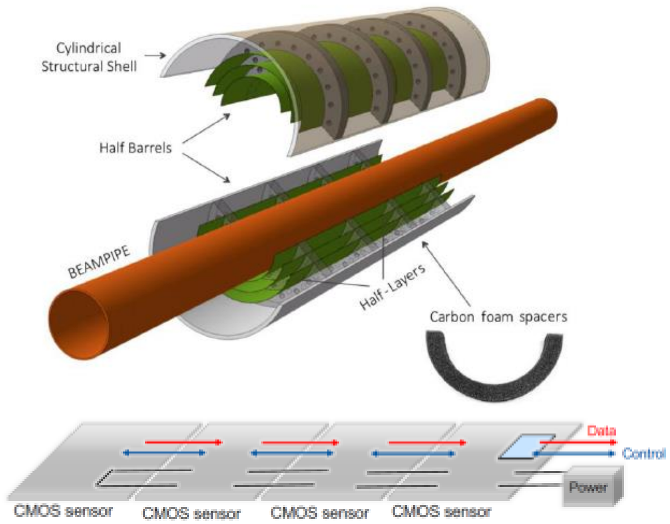
Layers 2+1

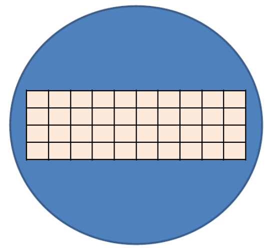


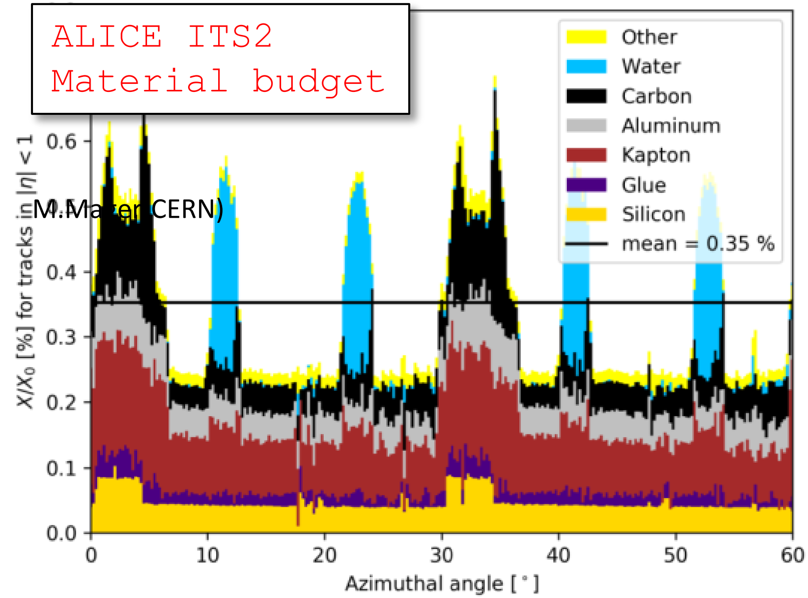


Inputs for engineering studies

ALICE ITS3: Bent sensors & stitching (MOSS)







https://indico.cern.ch/event/1071914/

- ALICE-ITS3/CERN drives the R&D on

Stitching + bent sensors:

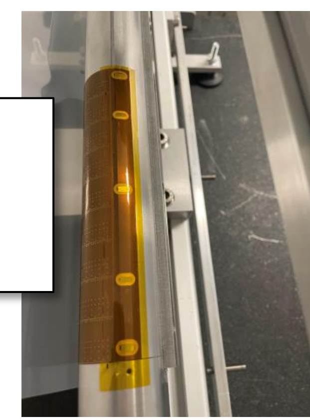
- ✓ Sensor part ~15% of total material budget
- ✓ Sensors thinned down to 50 µm
- ✓ Minimizing overlapping regions,

minimizing minimal radius around the beam pipe

- Challenges and caveats (for e^+e^- colliders)
  - ✓ Mechanics ? Bonding ? Air cooling only ?
  - ✓ Design: Minimizing peripheral circuits (Fill factor ~90%)
  - ✓ Bent sensor performances ? Yield ? Radiation hardness ?
  - ⇨ design rules constraints the minimal pitch (~22 µm)
  - ✓ ITS-3 do not have disk (chip periphery adds Z position constraint)
  - ✓ Approach validated in a limited radius range (R> 18mm)

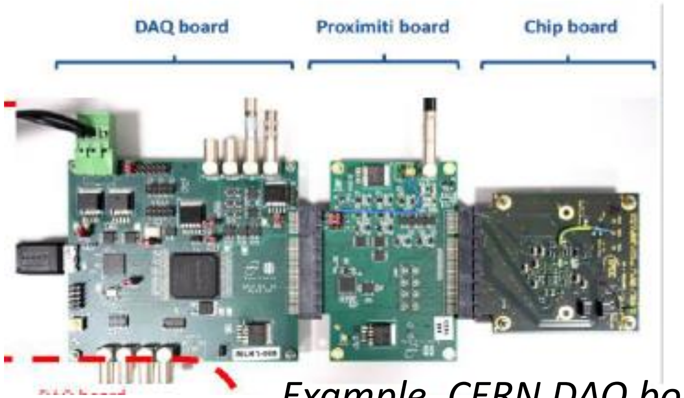
Questions potentially adressed by GRAM with MIMOSIS

1st bending tests by C4PI microtechnics



Tests & characterizations

- Nerf de la guerre
  - ✓ Demanding in resources (funds, FTE, time)
    - Large fraction of the FTEs in all activities (C4PI & physicists)
- Major challenges
  - ✓ Provide test benches / test beam DAQs
  - ✓ Stay time/cost effective, keep using what works
  - ✓ Share/support DAQs system with partners
  - ✓ Anticipate needs for the future (e.g. high bandwidth, Test beam setups, compatibility with collaborations, analog/digital outputs, small/large sensors, etc.)
- Strategy built with C4PI (July-October 2023)
  - ✓ Be compatible with the EUDAQ system (including software, TLU)
  - ✓ Make the proximity boards compatible with all DAQS
    - Develop interface boards
  - ✓ Develop new DAQ based on FPGAs cards + ADC/interface + home made carrier cards



Example, CERN DAQ board system

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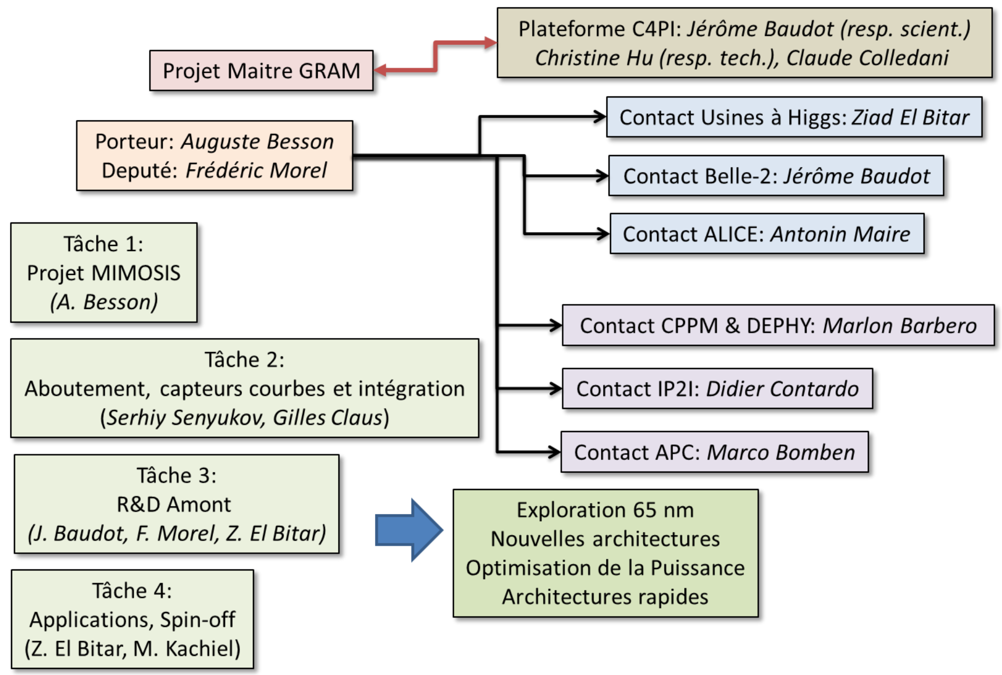
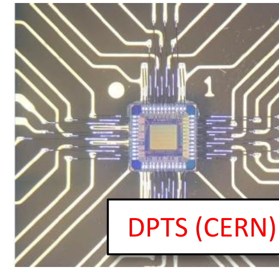
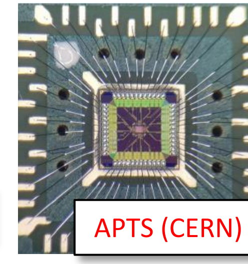


An example of R&D: TPSCo 65 nm CMOS technology

- 65 nm feature size technology
  - ✓ Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades
    - ▪ Privileged relation between CERN with the foundry
- Added values
  - ✓ Larger wafers (⇨ 30 cm)
  - ✓ More functionalities inside the pixel
  - ✓ Keeps pixel dimensions small ⇨ spatial res.
  - ✓ Potentially faster read-out
  - ✓ Lower power consumption
  - ✓ Synergy with Higgs factories requirements
- First submission: MLR1 (2020)
  - ✓ Validated the technology for HEP
- 2nd Submission ER1 (2022-23)
  - ✓ Dedicated to ITS3 (MOSS/MOST; stitching)

ALICE


DPTS (CERN)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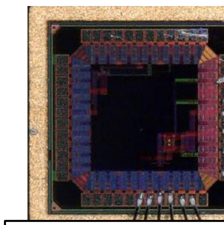
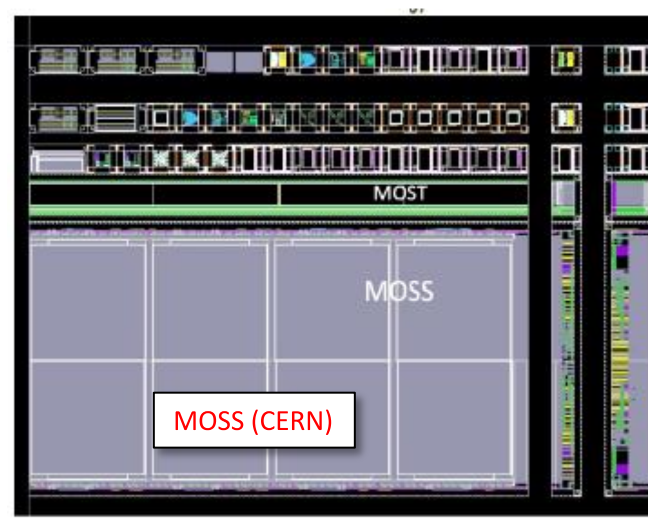
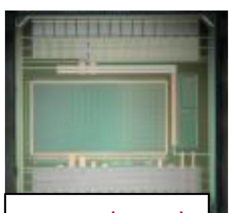

TANGERINE (DESY)



MOSS (CERN)


CE-65 (IPHC)


PICSEL

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

cnrs IN2P3 Les deux infinis

iPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

eurizon European network for developing new horizons for RIs

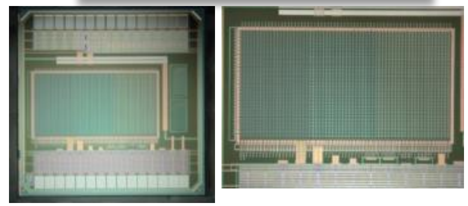
AIDA innova

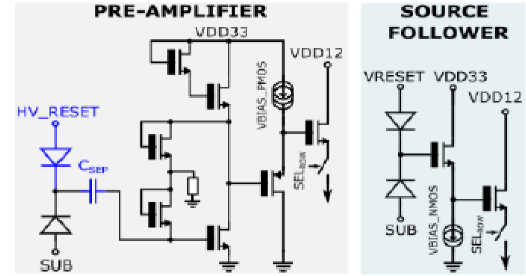
C4PI-Platform

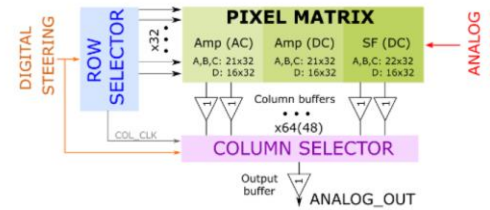
- CE_65v2 (MLR1 submission)
  - ✓ prototype designed @IPHC
  - ✓ Analog output, various designs (pitch, amplification)
- CE_65v2 (ER1 submission)
  - ✓ 18/22 μm pitch, hex design
  - ✓ 1st test beam in November 2023
- ✓ More results: PSD13, Oxford, El Bitar

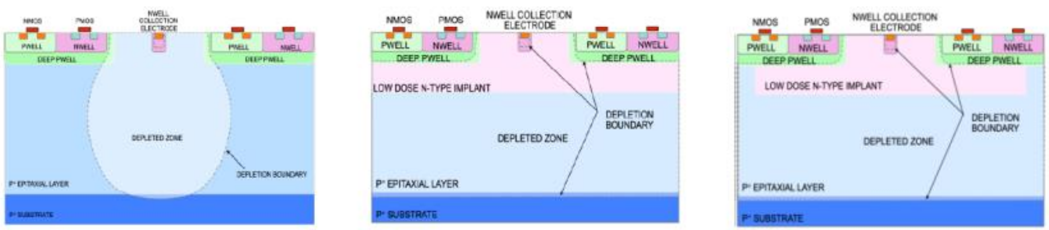
CE65_v1

CE_65 prototypes



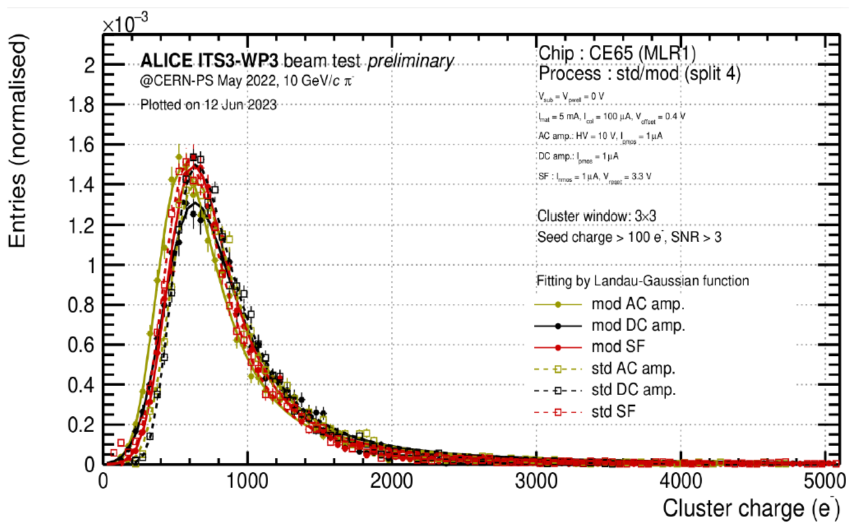




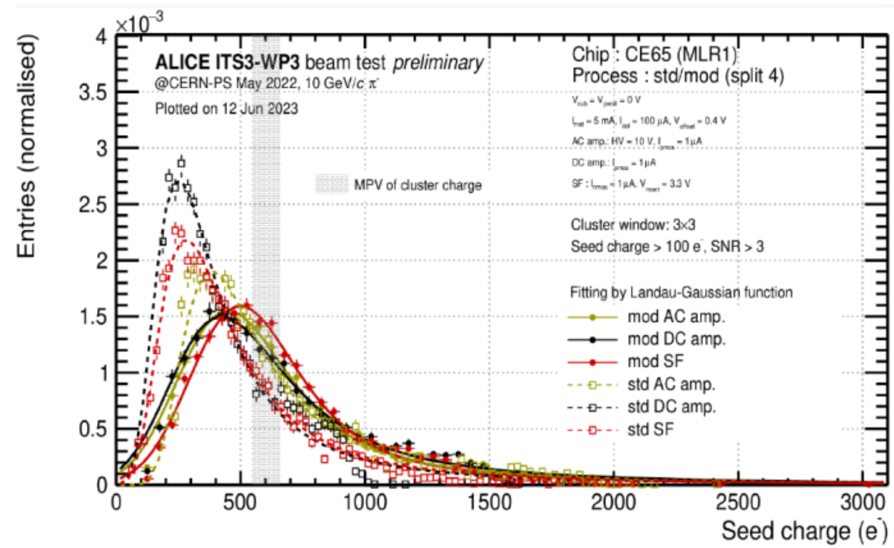


(a) Standard (b) Modified (c) Modified with gap

Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15μm	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15μm	64×32	AC/21, DC/21, SF/22
CE65-C	mod	15μm	64×32	AC/21, DC/21, SF/22
CE65-D	std	25μm	48×32	AC/16, DC/16, SF/16



Total charge not affected by process/pixel

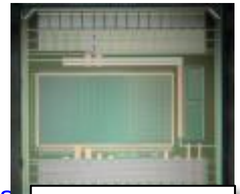


Charge sharing affected by process/pixel

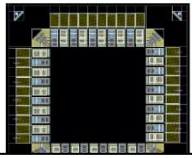
WG3.1: CMOS TPSCo-65 nm submissions and connexion with DRD3/DRD7

IPHC, CPPM, APC, IP2I

- CMOS TPSCo 65nm (ALICE ITS-3 + EP R&D WP1.2)
  - ✓ Main CMOS technology supported by CERN in the coming years
  - ✓ TJ 180nm probably less (or not) supported in the future
- 2 lines of submissions in CMOS TPSCo 65nm
  - ✓ Submissions dedicated to ALICE ITS-3 (ER2 & ER3) ⇨ stitching, bent sens
  - ✓ Submissions for generic R&D, supported by CERN EP R&D WP1.2 (« MLR2 and beyond)
- Generic R&D possible contributions
  - ✓ One expression of interest submitted with M1/M5 main driver (future e+e- colliders vertex detectors)
    - Targets 3 μm spatial resolution, improved time resolution (5-500 ns), controlled Power (< 50 mW/cm²), data flow (10-100 MHz/cm²) and low material budget (50 μm thickness)
    - Demonstrator to equip new generation beam telescope
  - ✓ Other projects in discussion (tracking, timing, calorimeters, link to MP DEPHY ?)
    - e.g. Fast timing (<100 ps); low power architecture, etc.



CE-65 (IPHC)



Ring Oscillator (CPPM)

DRD project: Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments

DRD technology area

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.

Proposing participants

Institute	Contact	Foreseen main areas of contribution
APC Paris	M. Bomben	Simulations, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Hynds	Testing, simulations
Zurich University	A. Macchiolo	Testing, DAQ, simulations

MLR1
- CE_65_v1
- APTS/DPTS

ER1
- CE_65_v2
- MOSS/MOST

ER2
- CE_65_v3 ?
- MOSS2

- Demonstrator for Higgs factories/beam telescope

DRD3/7 R&D 1st submission
- Proposal to DRD3/DRD7

2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029

Joined effort for ALICE-ITS3

Minimize pixel pitch
Time res. O(100 ns)
Explore architectures

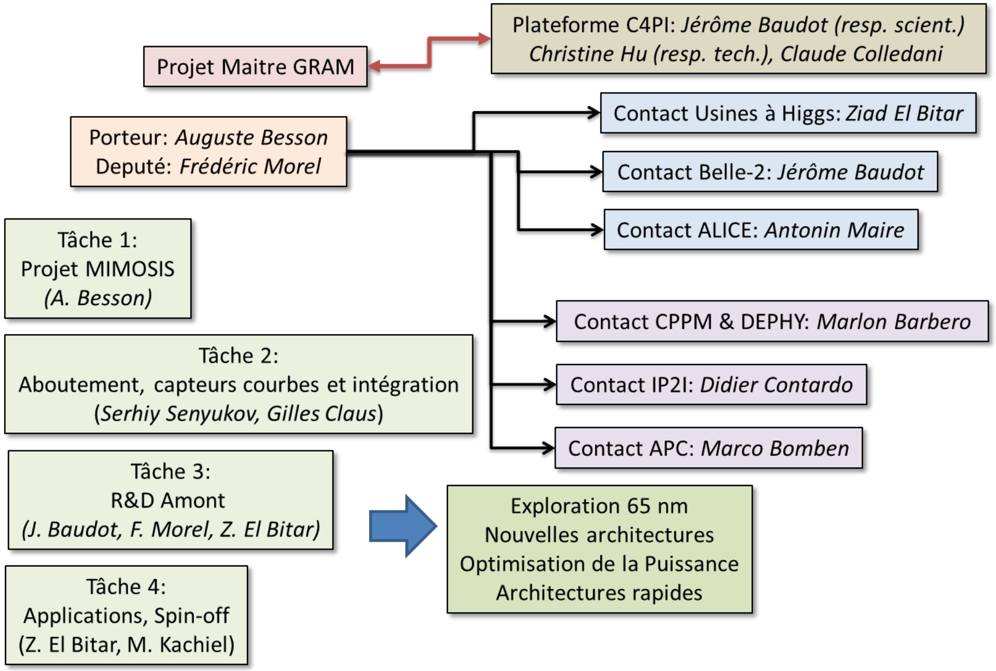
Minimize Power

Fast timing prototypes ?

GRAM organization

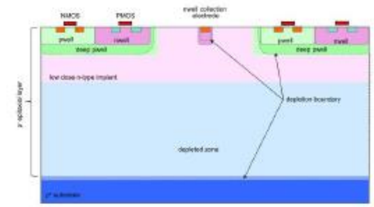
- Recent changes
  - ✓ Open to emerging activities (APC, IP2I)
  - ✓ Not focus exclusively on VTX Higgs factories

- Task 1: Full size prototype MIMOSIS
- Task 2: Integration
  - ✓ Stitching & bent sensors
  - ✓ Tests, characterizations
- Task 3: R & D
  - ✓ 65nm R&D
  - ✓ DRD-3 project (telescope demonstrator)
  - ✓ Architectures
    - ▪ Asynchronous read-out
    - ▪ In pixel preamplification
    - ▪ In pixel ADC
    - ▪ Timing measurement
- Task 4: applications, spin off

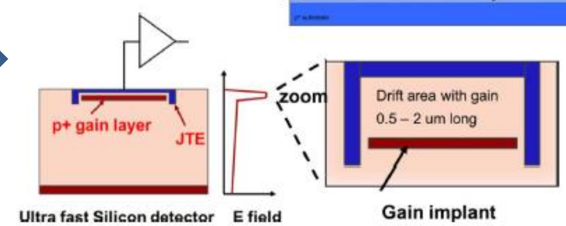


Other R&Ds

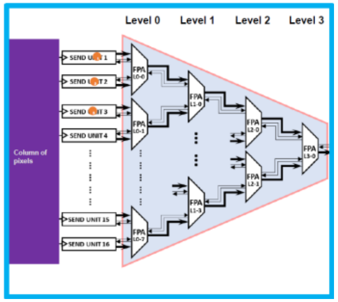
- Generic R&D to be put in balance with GRAM scientific goals
  - ✓ if fully generic ⇨ C4PI is the key player



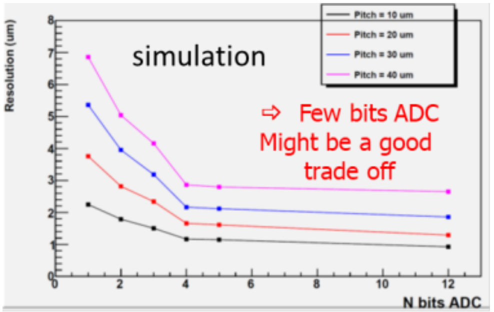
- CMOS with Preamplification
  - ✓ Carried by C4PI & ANR APICS 2023 (J. Baudot, CPPM/IPHC/ICUBE)
  - ✓ Interest: amplification of primary charges in the sensitive layer ⇨Spatial resolution, Fast time resolution & Power optimization



- Asynchronous read-out
  - ✓ Carried by C4PI/ICUBE + PhD
  - ✓ Interest: low power, fast read-out architecture & increased bandwidth
  - ✓ Challenge: make it compatible wit small pitchs



- In pixel ADCs
  - ✓ with APC
  - ✓ Interest: optimize the spatial resolution vs pitch figure of merit



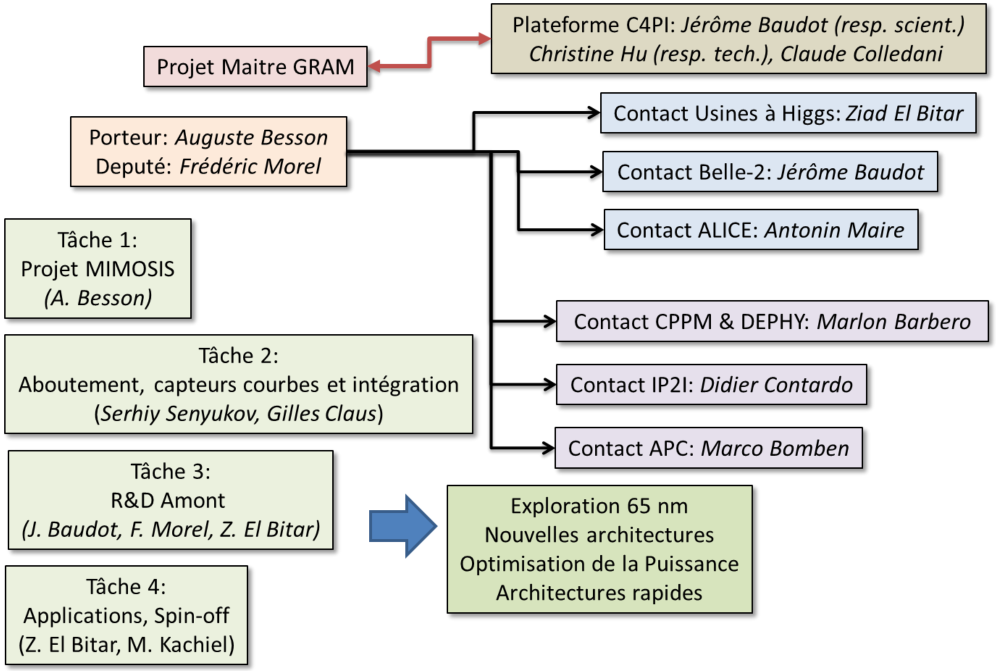
- Fast timing (ToF via TDC)
  - ✓ with IP2I/APC
  - ✓ Interest: ⇨ MAPS with 4D measurements

ANR 4D MAPS submitted in 2023 (IPHC/APC/IP2I, Bomben)

GRAM organization

- Recent changes
  - ✓ Open to emerging activities (APC, IP2I)
  - ✓ Not focus exclusively on VTX Higgs factories

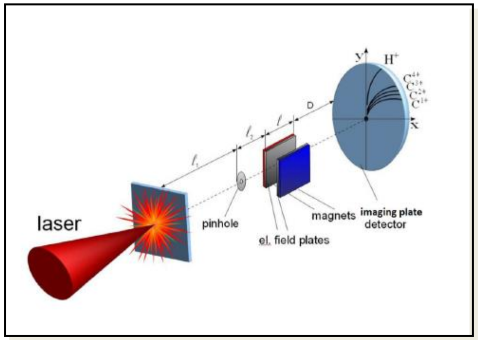
- Task 1: Full size prototype MIMOSIS
- Task 2: Integration
  - ✓ Stitching & bent sensors
  - ✓ Tests, characterizations
- Task 3: R & D
  - ✓ 65nm R&D
  - ✓ DRD-3 project (telescope demonstrator)
  - ✓ Architectures
    - Asynchronous read-out
    - In pixel preamplification
    - In pixel ADC
    - Timing measurement
- Task 4: applications, spin off



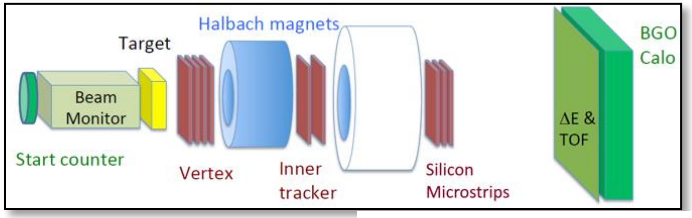
Applications & spin off (few examples)

- Caveats
  - ✓ Must be mainly founded by other sources
  - ✓ FTE limitations
  - ✓ Added value:
    - Full size chips applications, support for other IN2P3 projects

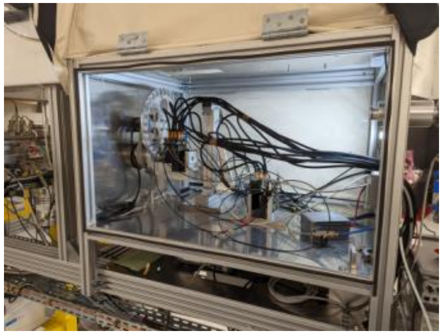
- ALP-ION R&T + C4PI
  - ✓ Monolithic Imager
  - ✓ Ion detection in laser plasma beam environnement
  - ✓ (EMP)

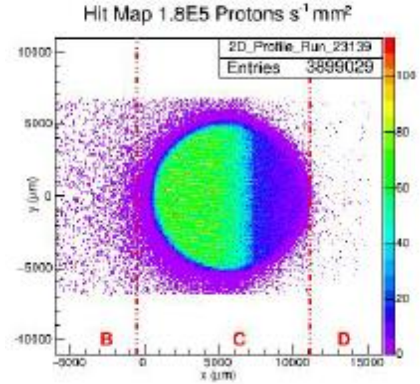


- MIMOSIS chips to be provided to FOOT experiment (IPHC, INFN)
  - ✓ Hadrontherapy (nuclear fragmentation cross-section of medium-light ions)



- MIMOSIS test beam at CYRCE (IPHC)
  - ✓ 25 MeV protons
  - ✓ Localized irradiation, Intensity measurement, DAQ & high flux/bandwidth tests





A. Altingun

GRAM: Summary

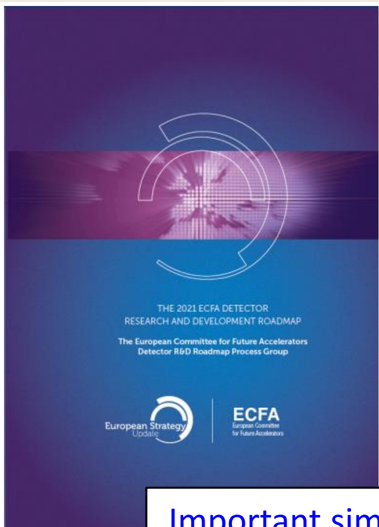
- CMOS-MAPS technology:
  - ✓ After 20 years of R&D, the technology has reached a level of maturity which allows it to be widely used in HEP
  - ✓ The technology has not yet reached its full potential
- Scientific goals:
  - ✓ Exploit fully the potential of the technology, targeting future Higgs factory (FCCee) and any applications where granularity is a leading requirement
- Strategy definition:
  - ✓ Synergies: Mid-term projects are still the way to go
    - Carried by GRAM : MIMOSIS OR carried by other MPs: ALICE ITS-3, Belle-2 upgrade (Obelix)
    - Provides invaluable milestones, maintains/develops the know-how for full size chips
  - ✓ Leading technology: 65nm TPSCo R&D
    - Supported by CERN and DRDs
- Strategy implementation:
  - ✓ Local:
    - Crucial role of C4PI (e.g. R&D strategy coordination between GRAM & C4PI, manpower)
    - Strategy for Higgs factories/ALICE-ITS3/Belle II endorsed by IPHC scientific council (2023), HCERES.
  - ✓ National:
    - GRAM extended to emerging activities (IP2I, APC) and to other applications (e.g. outer trackers)
    - Contribute to projects carried by experiments (ALICE ITS-3, Belle-II) (e.g. technical coordinator of ITS-3 @ in2p3)
    - Continue to strengthen the community targeting FCCee (e.g. ANR submitted (Bomben, APC/ IP2I/IPHC)
    - Find the right balance between generic R&D and specific requirements & mid-term vs long term
  - ✓ International:
    - DRD3/DRD7 and program of submission in 65 nm technology
    - Exploit synergies and maintain the network of partners (CERN, DESY, KEK, Zurich, etc.)

backup

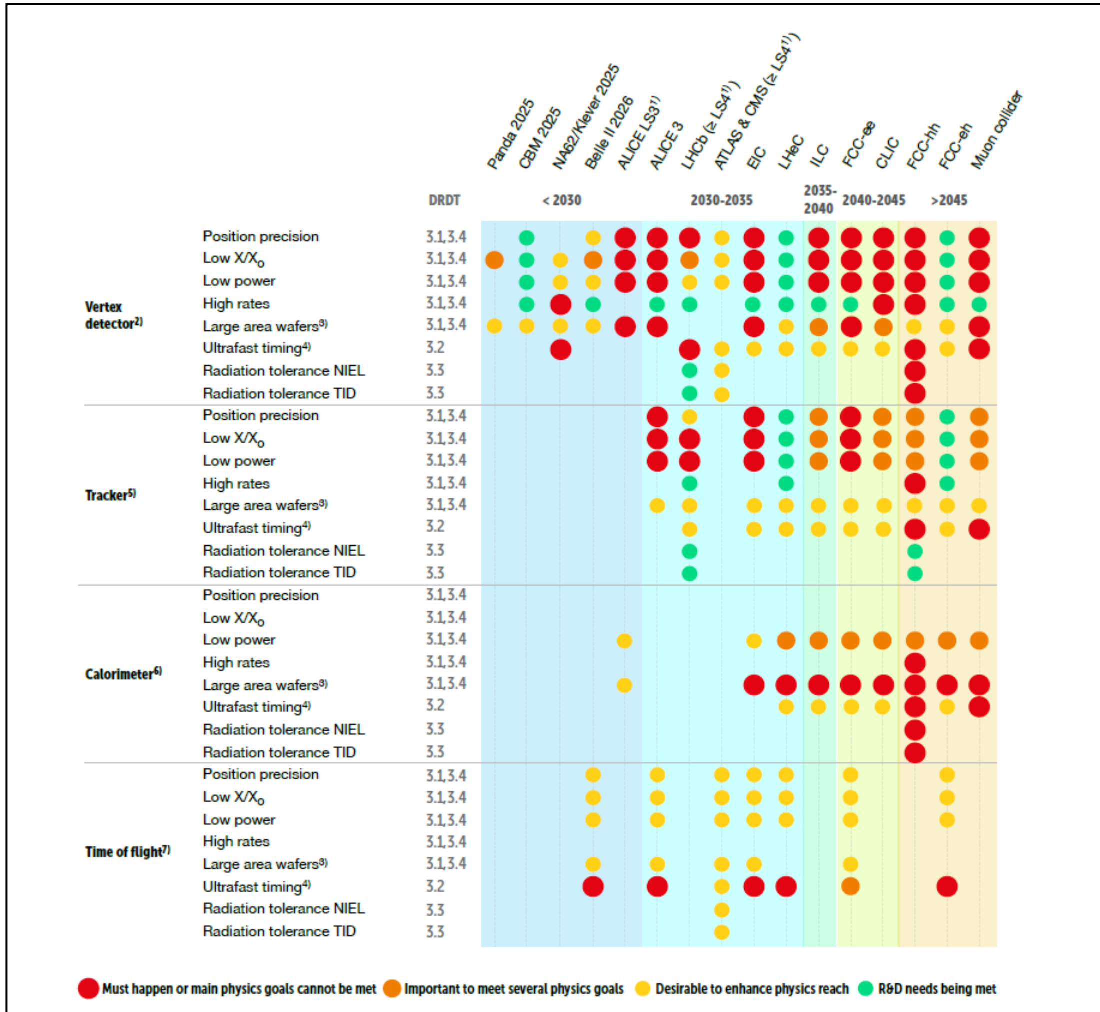
The 2021 ECFA Detector R&D roadmap: Solid State detectors

The 2021 ECFA Detector Research and Development Roadmap

Prepared by the Detector R&D Roadmap Process Group of the European Committee for Future Accelerators



Important similarities between FCCee requirements & Heavy ions experiments (ALICE ITS3, ALICE3, EIC, etc.)



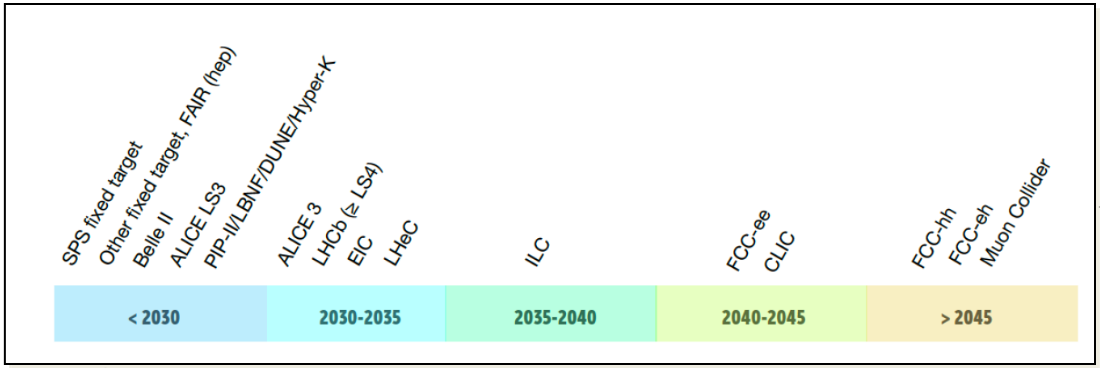
Time of flight

Granularity, low power, low material budget

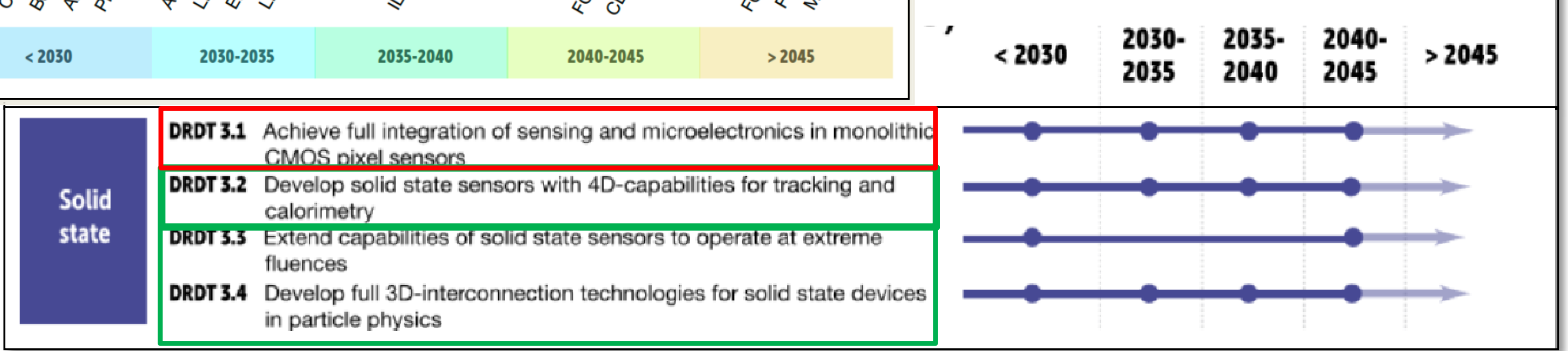
High rates, radiotolerance, fast timing

Calorimeters

Detector R&D Roadmap: themes (DRDTs)

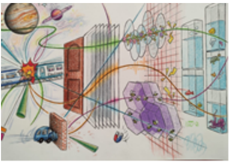


References: ECFA/RC/21/510
CERN-ESU-017
DOI: 10.17181/CERN.XDPL.W2EX



DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors

DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.



Ball park performance targets MCMOS

DRD3

Three main time scales/phases to define program up to: 2027-28, 2029-2035, >2035

Ball park generic performance targets* mandatory/desireable

	Tracking VD/CT	Timing Layer + Calorimeter
Heavy Ion	ultralight low power tracker pitch 10 - 30 µm @ O(100) MHz/cm², O(1) µs	O(20) ps (TL)
Flavour collider	ultralight low power tracker pitch 10 - 30 µm @ O(100) MHz/cm², O(1) ns	O(20) ps in (TL)
Lepton collider	e-e : ultralight low power tracker pitch down to ≲10 µm, @ O(100) MHz/cm² timing driven by power timing driven by power dissipation µ-µ : O(20) ps rates and irradiation tbc	O(10) ps in TL O(< 50) ps in calorimeter driven by power power dissipation
pp collider	HL-LHC: 25-50 µm @ O(5) GHz/cm² $5x10^{15}$ to $5x10^{16}$ neq/cm², 250 - 500 MRad timing O(<50) ps timing O(<50) ps	HL-LHC: pitch O(<1) mm O(20) ps in TL, NIEL $5x10^{15}$
	FCC-hh: < 10 - 20 µm @ 30 GHz/cm² 4D tracking 4D tracking O(<10)ps up to O(10^{18}) to O(10^{18}) neq/cm², up to O(50) GRad	FCC-hh: 5D calorimeter O(<10)ps up to O(10^{18}) neq/cm², up to O(50) GRad O(50) GRad

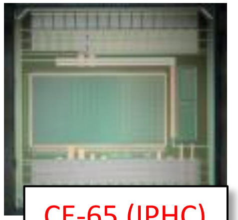
* ranges representative, ex. for VD and CT with more stringent constraints to be achieved in VD

ECFA

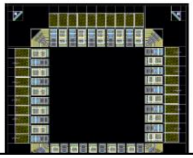
WG3.1: CMOS TPSCo-65 nm submissions and connexion with DRD3/DRD7

IPHC, CPPM, APC, IP2I

- CMOS TPSCo 65nm (ALICE ITS-3 + EP R&D WP1.2)
  - ✓ Offers attractive perspectives w.r.t. TJ180nm
    - Stitching (12 inches wafers)
    - Potentially smaller pitch, faster, less power consumption, etc.
  - ✓ Main CMOS technology supported by CERN in the coming years
  - ✓ IPHC & CPPM already in the consortium participating to the technology validation
  - ✓ TJ 180nm probably less (or not) supported in the future



CE-65 (IPHC)



Ring Oscillator (CPPM)

- 2 lines of submissions in CMOS TPSCo 65nm
  - ✓ Submissions dedicated to ALICE ITS-3 (ER2 & ER3) ⇨ stitching, bent sensors
  - ✓ Submissions for generic R&D, supported by CERN EP R&D WP1.2 (« MLR2 » and beyond)
- Generic R&D possible contributions
  - ✓ One expression of interest submitted with M1/M5 main driver (future e+e- colliders vertex detectors)
    - Goal: gather groups to reach a critical size
    - Targets 3 μm spatial resolution, improved time resolution (5-500 ns), controlled Power (< 50 mW/cm^2), data flow (10-100 MHz/cm^2) and low material budget (50 μm thickness)
    - Demonstrator to equip new generation beam telescope
    - Proposing Institutes: CERN, DESY, IPHC, APC, etc.
    - Open to other participations
  - ✓ Other projects in discussion (tracking, timing, calorimeters, link to MP DEPHY ?)
    - e.g. Fast timing (<100 ps); low power architecture, etc.

DRD project: Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments

DRD technology area

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Proposing participants

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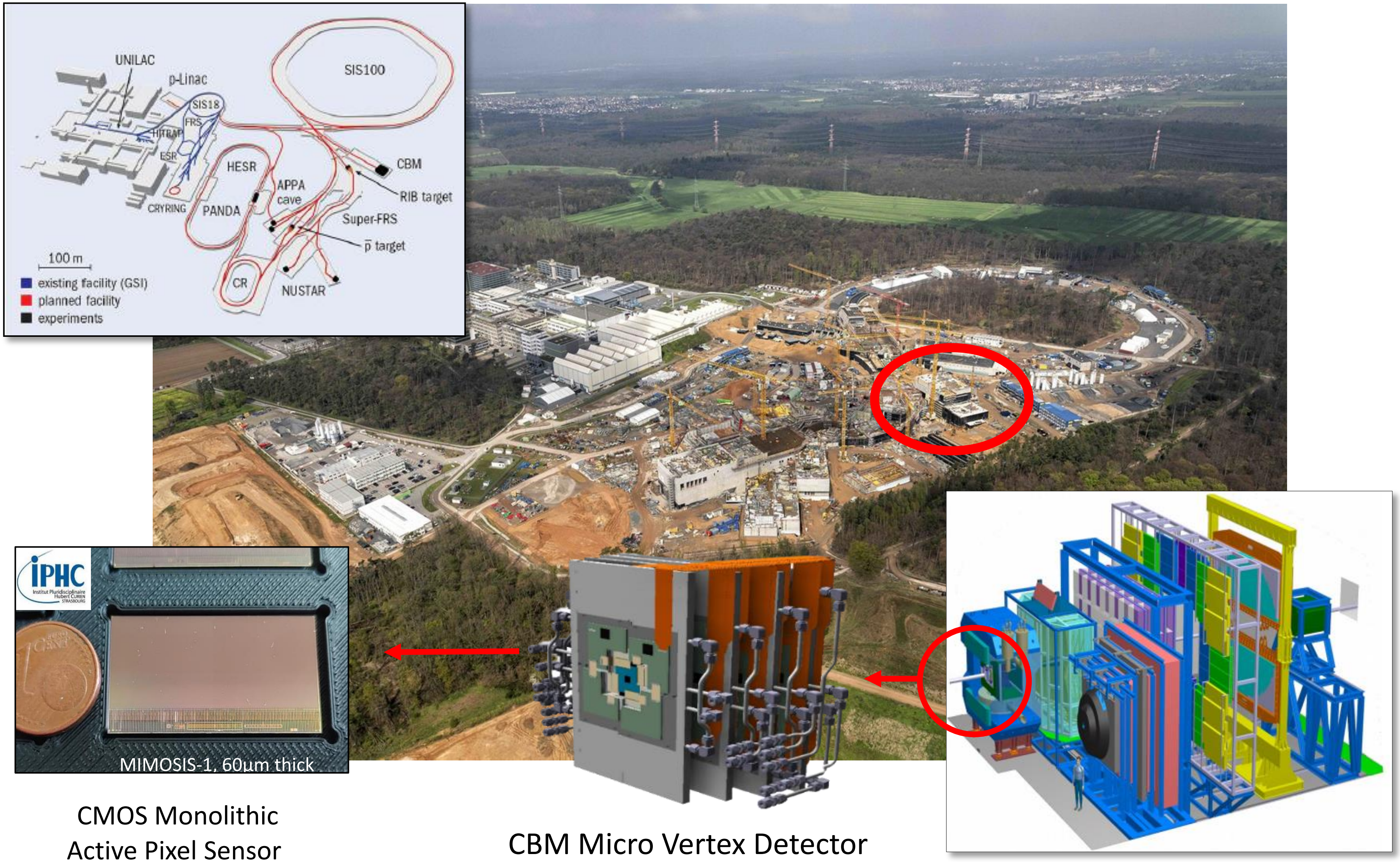
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Hynds	Testing, simulations
Zurich University	A. Macchiolo	Testing, DAQ, simulations

MIMOSIS

The MVD @ CBM

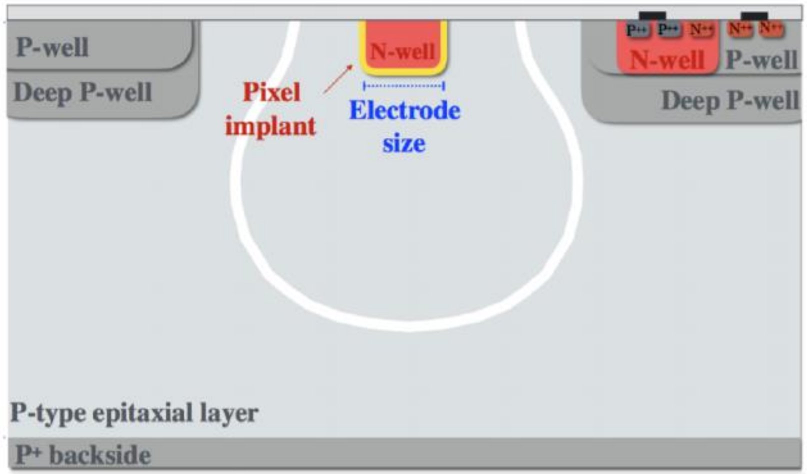


CMOS Monolithic
Active Pixel Sensor
MIMOSIS

CBM Micro Vertex Detector
(MVD)

CBM – Experiment @ FAIR

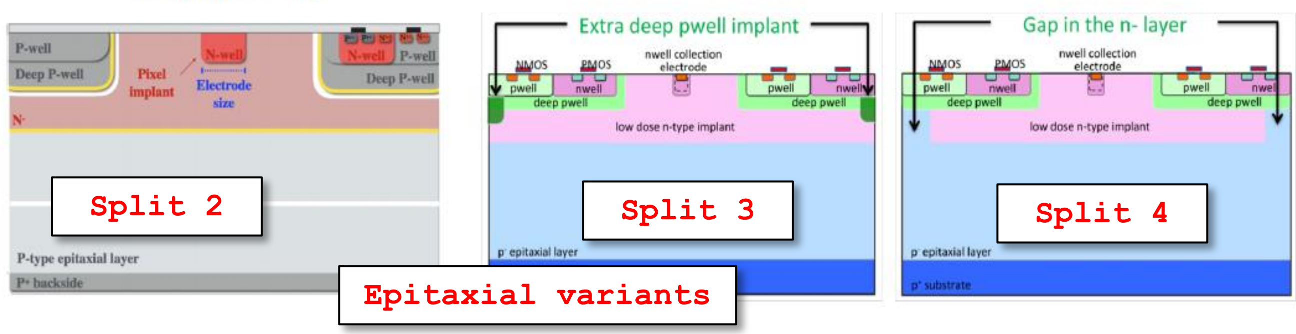
Process modifications



Pic from: Munker, Vertex 2018, Status of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

- standard process (3 available wafers)
- continuous n-layer (blanket) (3 wafers)
- additional p-implant (3 wafers)
- gap in n-layer (3 wafers)

continuous n-layer | additional p-implant | gap in n-layer



Pic from: Munker, Vertex 2018, Status of silicon detector R&D at CLIC
Carlos, TREDI 2019, Results of the Malta CMOS pixel detector prototype for the ATLAS Pixel ITK

Synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

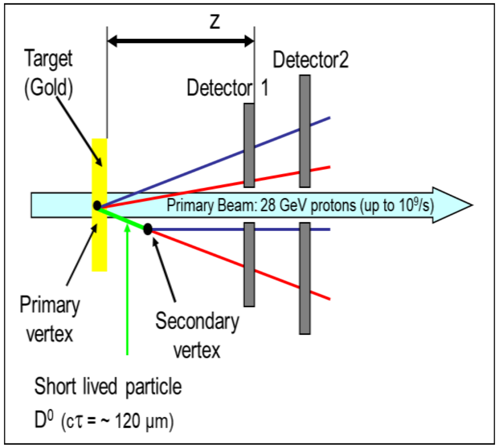
Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

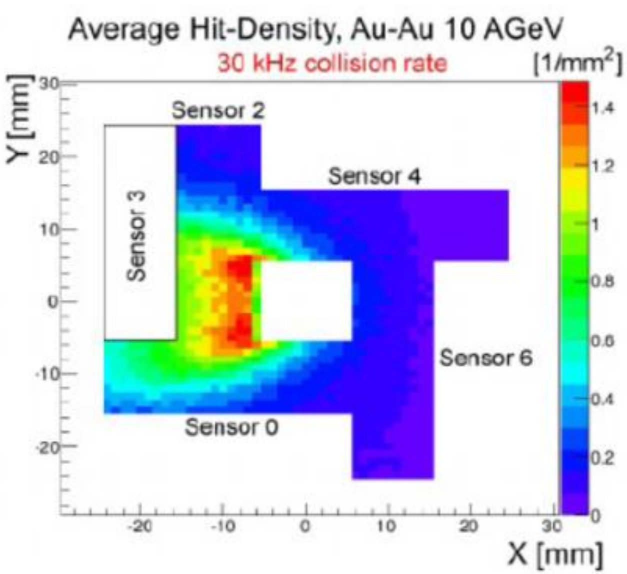
K. Jakobs, FCC Physics Workshop, Feb 2022

Must happen or main physics goals cannot be met | Important to meet several physics goals | Desirable to enhance physics reach | R&D needs being met

MVD Physics goals

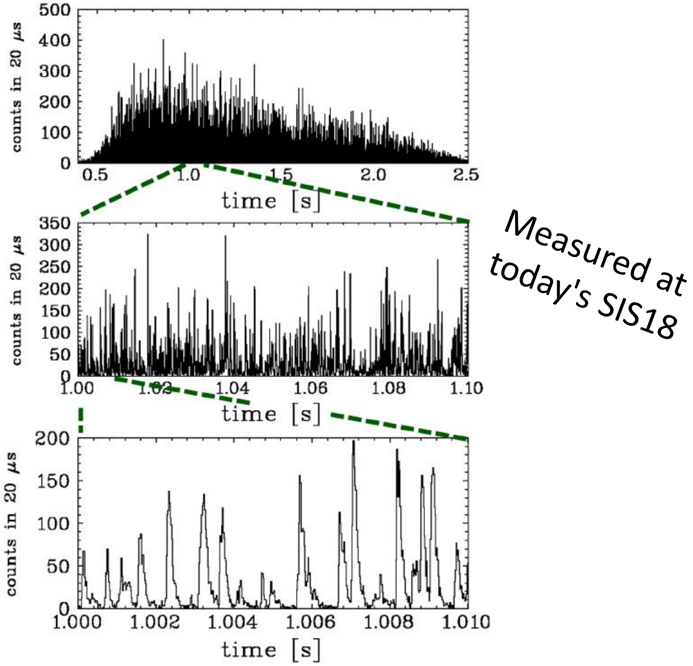
- CBM @ FAIR (GSI)
  - ✓ Fixed target experiment to study the QCD phase diagram in the high baryon density region
- Micro-Vertex Detector (MVD)
  - ✓ High precision reconstruction of secondary vertices
    - e.g. charm mesons ~ 100 μm flying distance
  - ✓ High rate, high irradiation, non homogenous in time and space





Space inhomogeneity

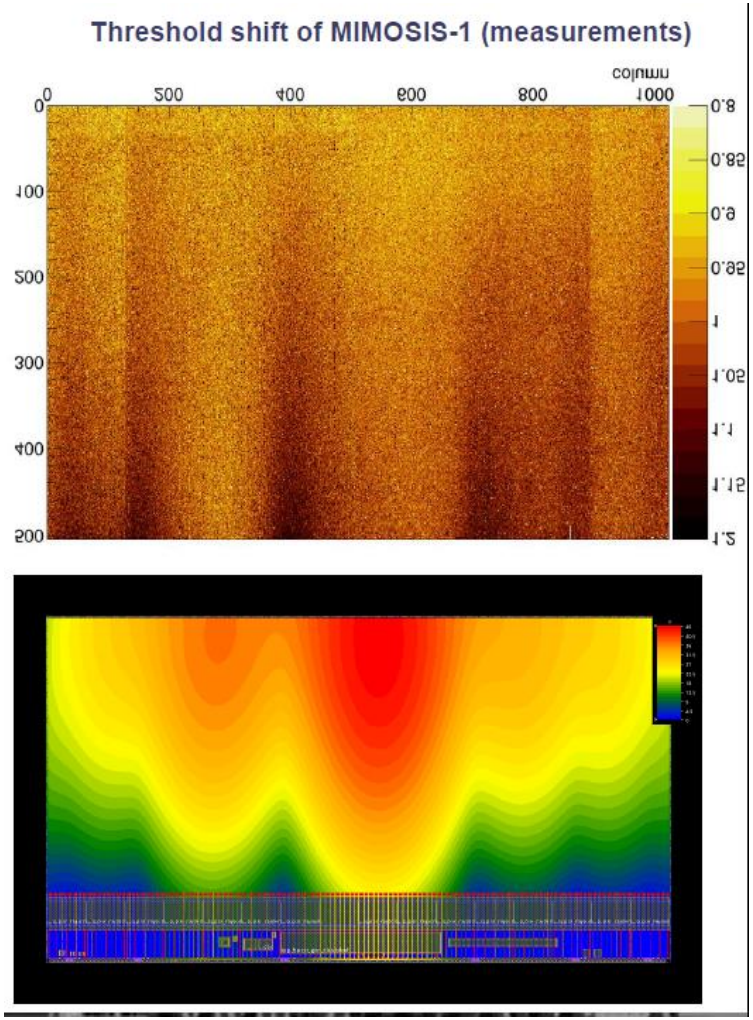
Time fluctuations



Mimosis-1 Verification tools example

- Large and complex designs need
  - ✓ A hierarchy in the work flow to keep submission on schedule
  - ✓ Verification tools that can be run in a reasonnable time
  - ✓ Knowledge of these tools is crucial
- Example Power-grid problem observed in MIMOSIS-1
  - ✓ Threshold shifts
  - ✓ Problem fixed quickly

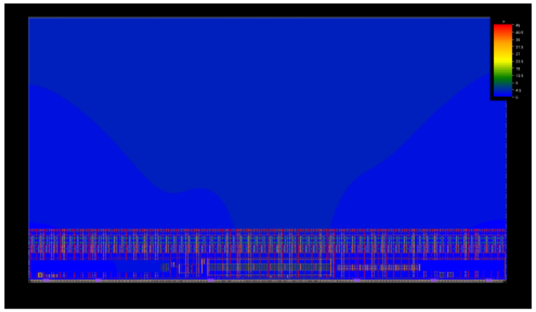
F. Morel DRD7 kick-off meeting



IR drop on AVDD (simulations)
0-45 mV scale

MIMOSIS-1
Mean= 26 mV

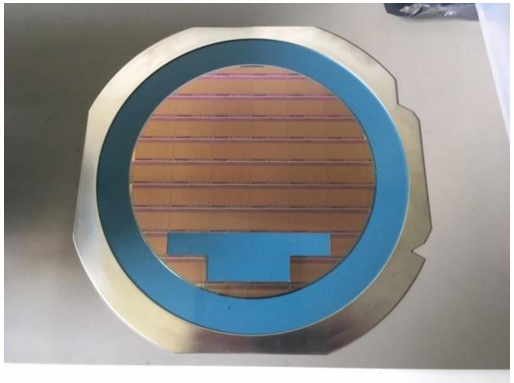
MIMOSIS-2
Mean = 3 mV

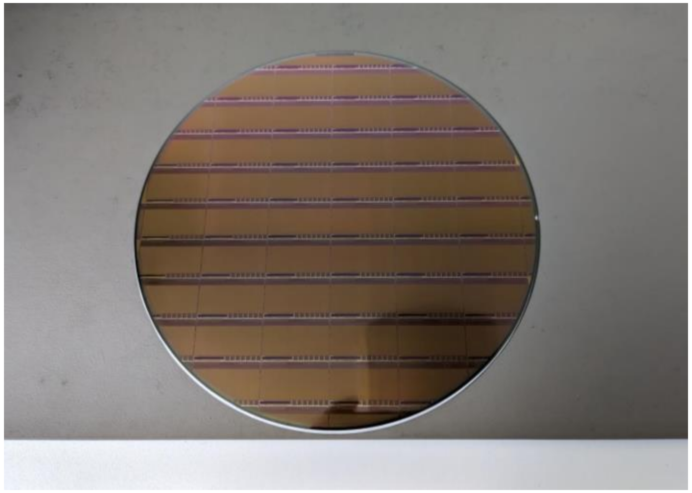


MIMOSIS-2 first tests

- 9 chips diced and tested (from different wafers/process)

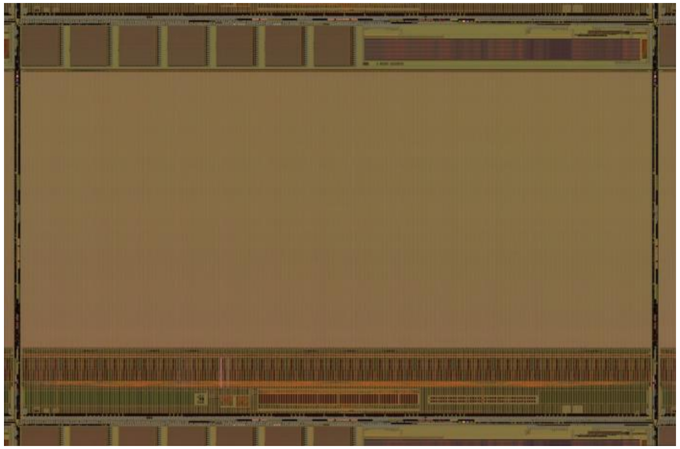
PCB	Process	IA
13	W3 Ngap 25µm	OK
51	W1 Std 25µm	OK
52	W1 Std 25µm	OK
53	W1 Std 25µm	500 mA
54	W1 Std 25µm	OK
55	W1 Std 25µm	OK
56	W1 Std 25µm	OK
57	W6 Pstop 25µm	500 mA
58	W11 Pstop 50µm	OK





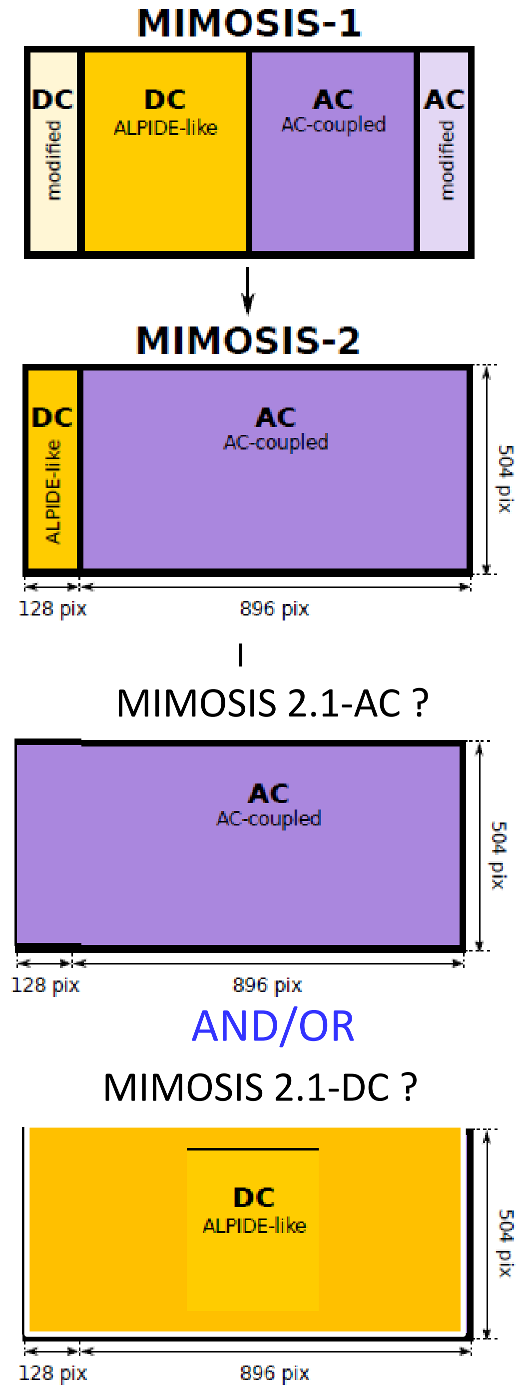
- MIMOSIS-2 does not work properly
  - ✓ **Unexpected issues on the design** (e.g. frequency limitation for some standard cells, reset)
  - ✓ Ongoing discussions with the foundry (NDA)

- Status:
  - ✓ The CBM-MVD collaboration worked hard the last 4 months to identify the sources of the problems.
  - ✓ **The sources of all the identified problems has been understood.**
    - the critical issues can probably be corrected by resubmitting with only 2 modified metal masks
  - ✓ **The current version of MIMOSIS-2 will not allow to fully characterize its performances but it validates the additional features with respect to MIMOSIS-1** (on-chip clustering, triplication).



MIMOSIS-2: Action plans

- Focused Ion Beam correction on few chips (FIB)
  - ✓ The Focused Ion Beam process is a circuitry modification protocol that will allow to modify 2 x 2 columns.
  - ✓ It confirmed the problems identification
  - ✓ It validated the clustering and the triplication.
- Lessons learned
  - ✓ Unexpected issues which could have occurred in MIMOSIS-1
  - ✓ Analog simulation tools for the digital part provided valuable input
    - **verification process improvement**
  - ✓ **MIMOSIS-2 played its role (validation of the final design, verification process optimization)**
- A possible compromise is to resubmit a fabrication with less options :
  - ✓ MIMOSIS 2.1 ?
  - ✓ Less different splits/process, less wafers, perhaps only AC matrix) to optimize costs vs delay vs tests.
  - ✓ Submitting a version closer to the final sensor design (e.g. only one pixel type on the whole matrix) might offer some added value to be estimated.
- Plans
  - ✓ Validate all corrections (in particular thanks to chips corrected with FIBs)
  - ✓ Final decision about to be taken in the coming month



Particle ID & Timing

Power vs fast timing vs pixel size

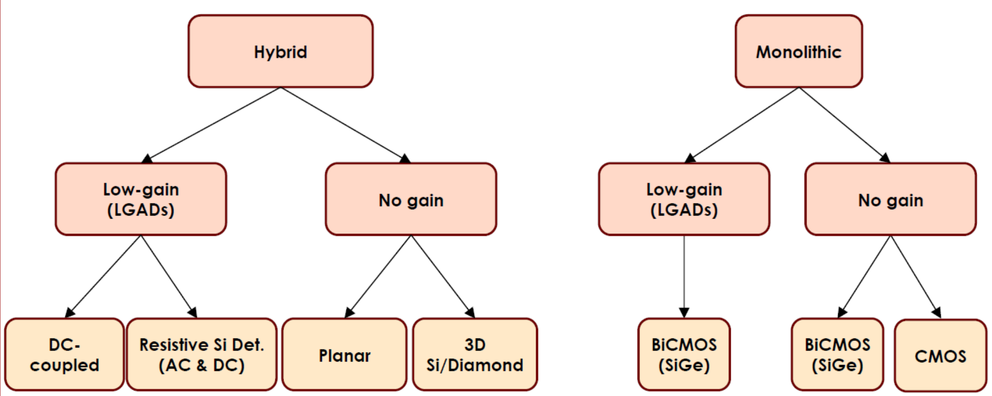
Brief considerations about electronics: power

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

45

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22



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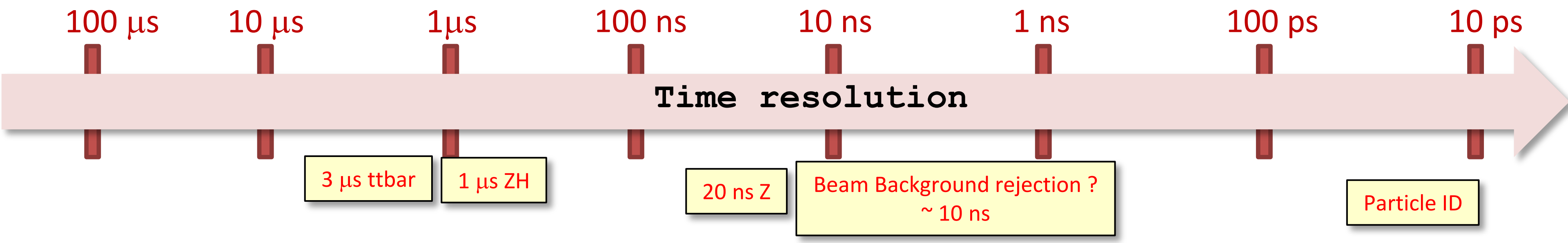
16

Price to pay: additionnal cooling system (addtionnal material)

Timing & 4-D tracking



- Time resolution Δt
  - ✓ Bunch separation (3 μs / 1 μs / 20 ns @ FCCee)
  - ✓ Background rejection ? (1-10 ns range)
  - ✓ Particle ID (10-100 ps)
- Usual drawbacks to go faster
  - ✓ Power consumption
  - ✓ Active Cooling & geometrical acceptance due to services
  - ✓ In pixel circuitry ⇨ larger pixels (or multipixels)
  - ✓ Fill factor, dead time
  - ✓ PID Restricted to low momentum particles (~< few GeV/c)
- Still
  - ✓ Forward region not covered by a central gazeous detector (TPC)
  - ✓ Added value for intermediate radii (e.g. LLPs ?)
- Specialized layers
  - ✓ Doesn't compromise the other requirements (material budget and granularity)
    - Probably not in the most inner layers

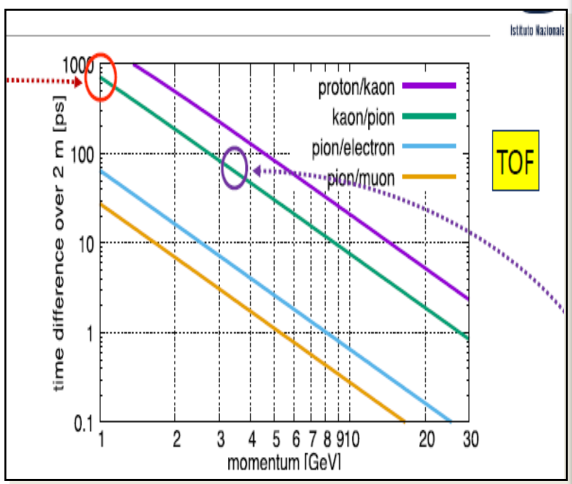
Particle ID and time resolution DRD4 & 1/3

More details here: https://indico.cern.ch/event/1202105/contributions/5402790/attachments/2662086/4612032/FCC-DRD4.pdf

- Goal:
  - ✓ K/π, π/e$^-$ separation, etc. ⇨ Interest to push beyond 10 ps resolution
  - ✓ Even more important for the physics program @ Z peak

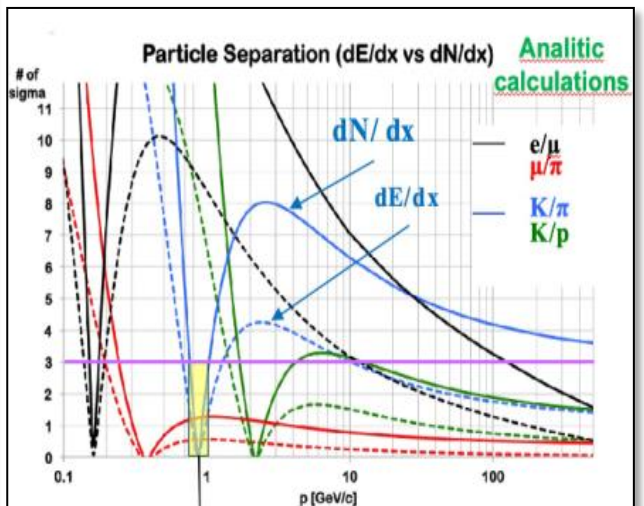
Fast timing (<100 ps) Solid state (pixelated) detector (DRD3)	dE/dx + dN/dx Mainly gazeous detector, e.g. TPC, RICH (DRD1)

Time difference (ps)



Time of Flight

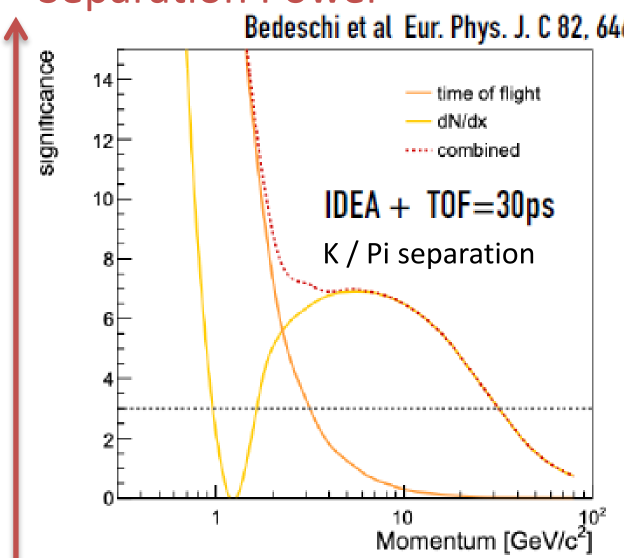
Separation Power (significance)



dE/dx – dN/dx

Separation Power

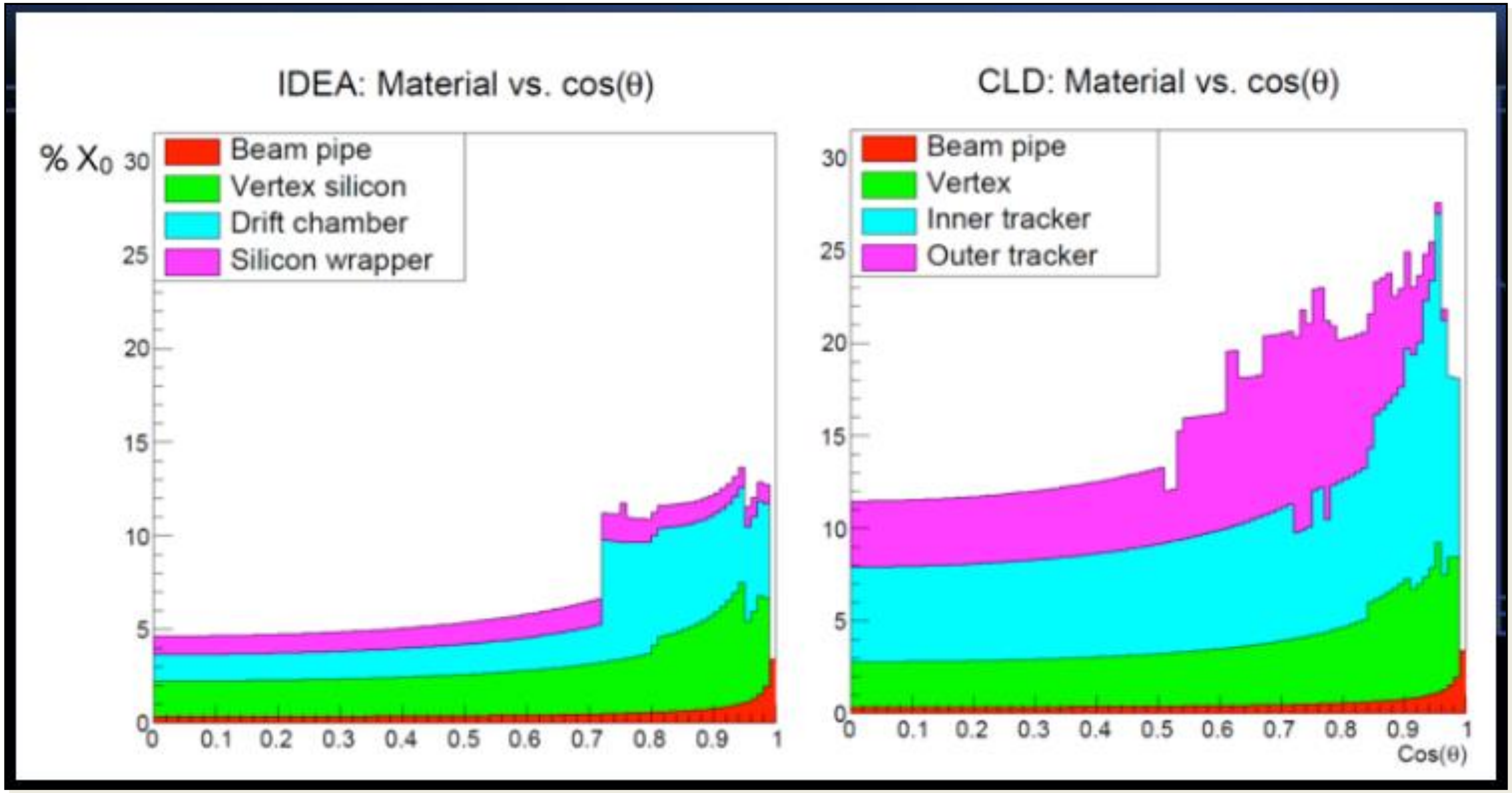
Bedeschi et al Eur. Phys. J. C 82, 646



Combined measurement

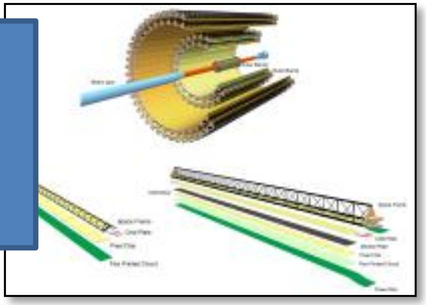
Momentum (GeV/c)

Material budget

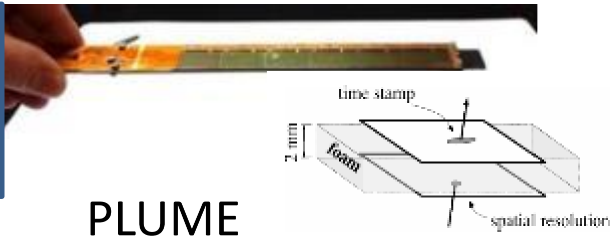


Material budget: starting from the layers

Classical single sided layers (e.g. ALICE ITS-2)



Double sided layers

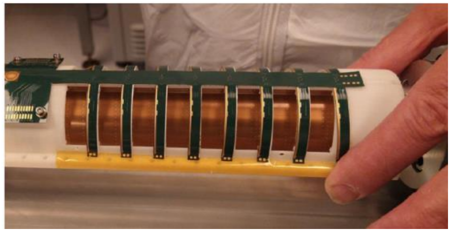


PLUME
(Bristol, DESY, IPHC)

Double sided ladders with minimized material budget 0.35% X_0 reached ⇨ ~0.3 X_0 doable (with air flow cooling)

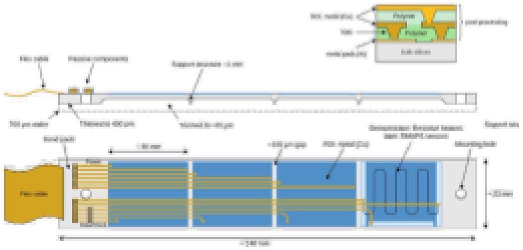
Pseudo stitching + bent sensors (superALPIDE)

- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)

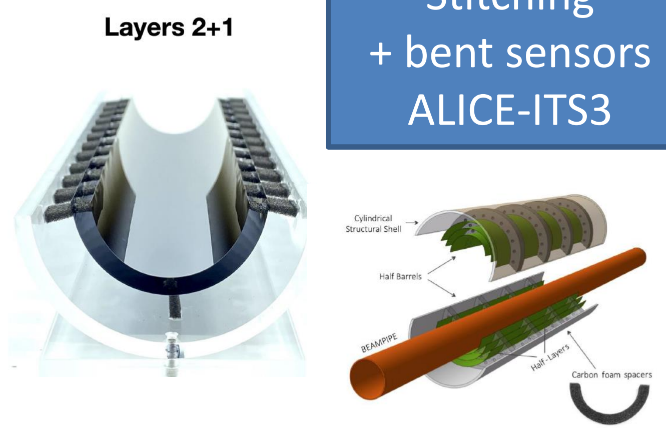


Self supported silicon (Belle-2 upgrade)

7.1x1.5 cm²
Thickness (edge/center) 430/90 µm
Planarity ~17 µm

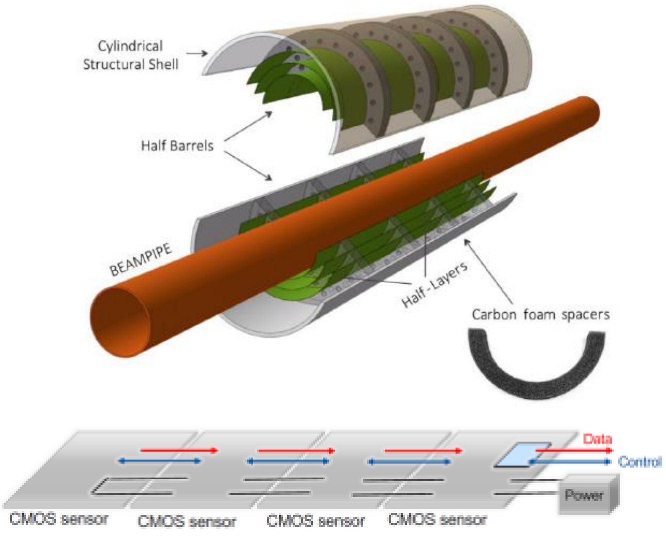


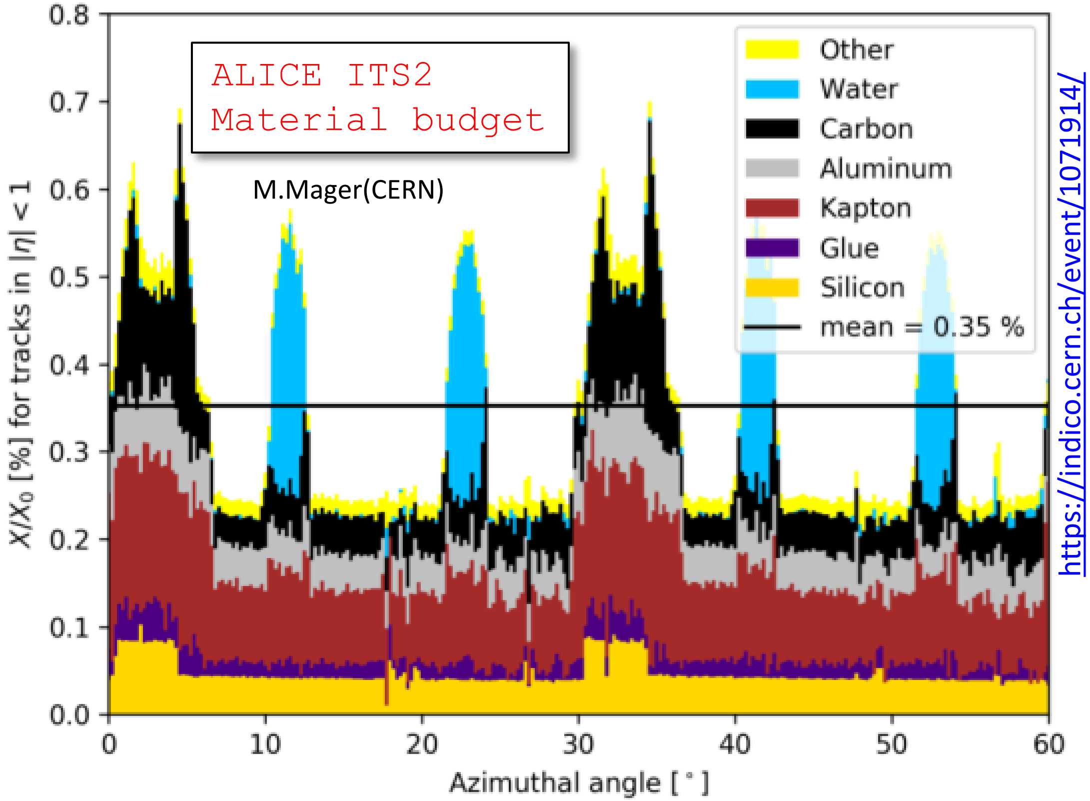
Stitching + bent sensors ALICE-ITS3



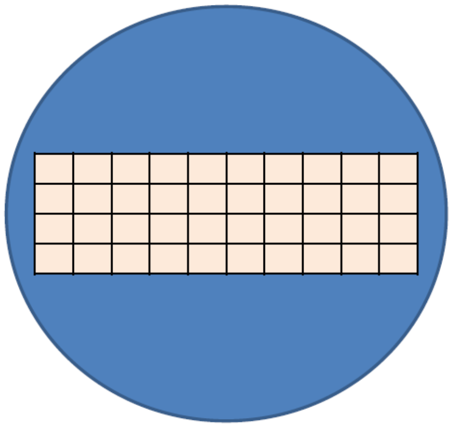
Inputs for engineering studies

ALICE ITS3: Bent sensors & stitching





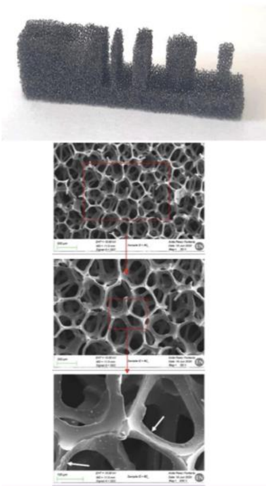
- ALICE-ITS3/CERN drives the R&D on Stitching + bent sensors:
  - ✓ Sensor part ~15% of total material budget
  - ✓ Sensors thinned down to 50 µm
  - ✓ Minimizing overlapping regions, minimizing minimal radius around the beam pipe
- Challenges and caveats (for e^+e^- colliders)
  - ✓ Mechanics ? Bonding ? Air cooling only ?
  - ✓ Design: Minimizing peripheral circuits (Fill factor ~90%)
  - ✓ Bent sensor performances ? Yield
  - ⇨ design rules constraints the minimal pitch (~22 µm)
  - ✓ ITS-3 do not have disk (chip periphery adds Z position constraint)
  - ✓ Approach validated in a limited radius range (R> 18mm)



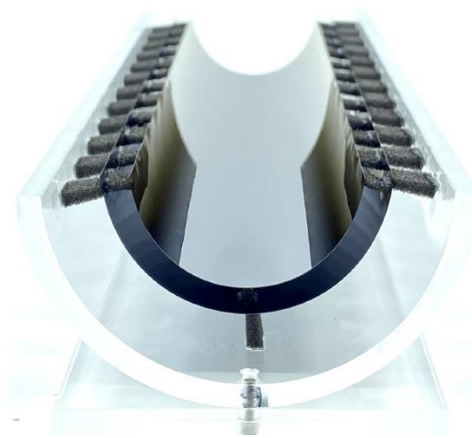
ALICE ITS3 tests

A. Kluge
on behalf of the ALICE collaboration
22 February, 2022
VCI

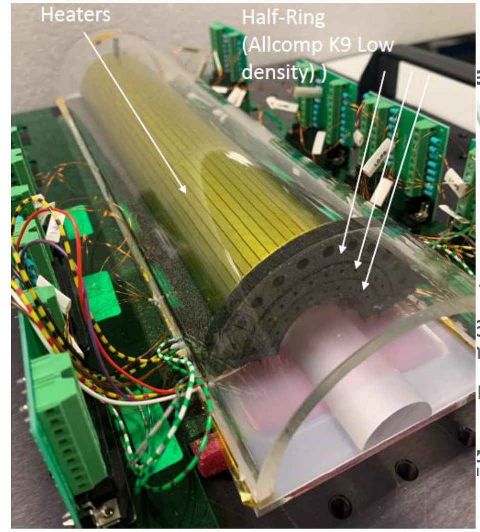
ERG DUOCEL_AR
0.06 kg/dm³
0.033 W/m·K

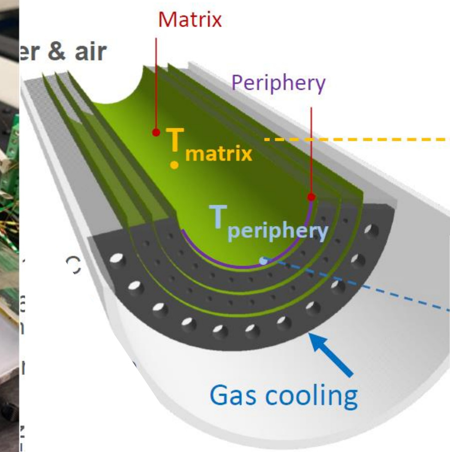


Layers 2+1

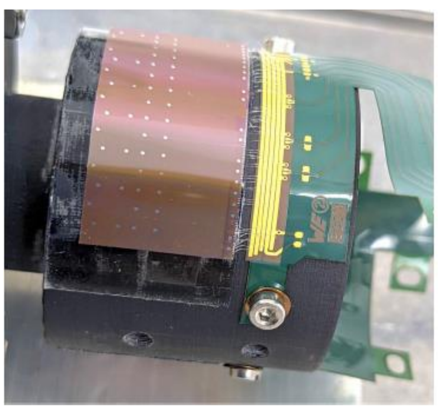


Carbon fiber foam spacer





Integration and cooling studies



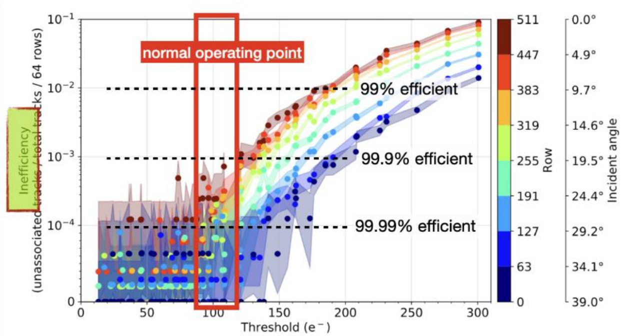
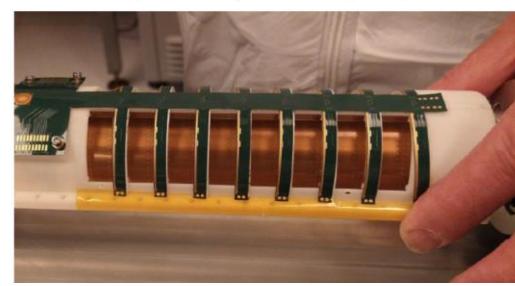
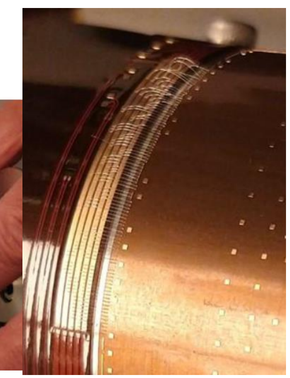


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

Bent sensors in test beam

- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)

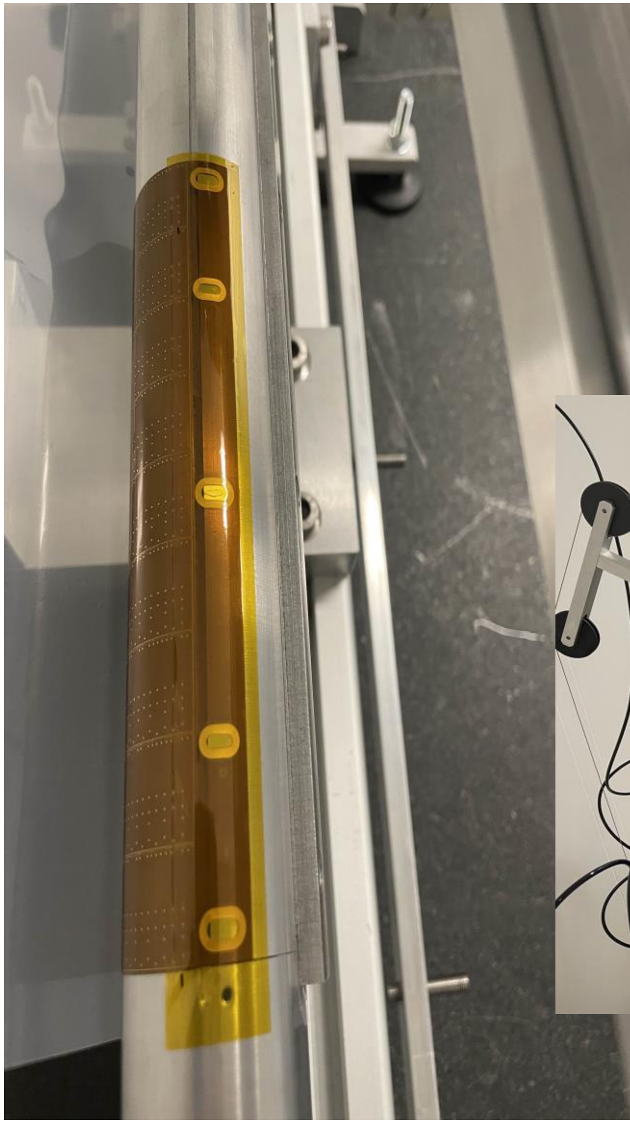


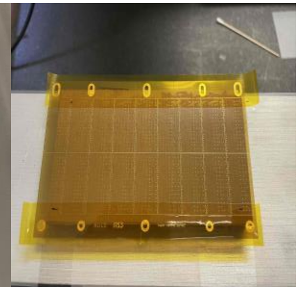


Inteconnexion tests (superALPIDE)

On going experiments pave the road for Higgs factory detectors
(many other examples)

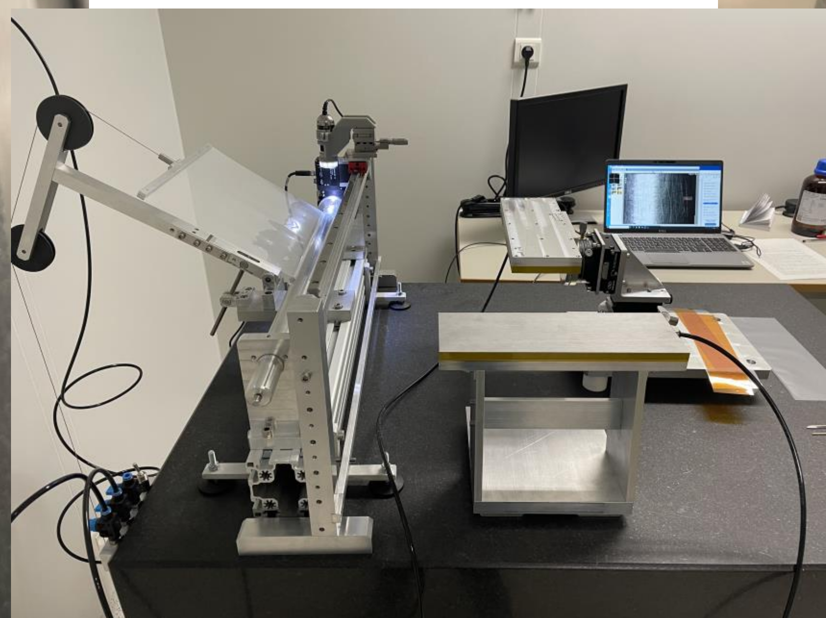
C4PI: What have we already done ?

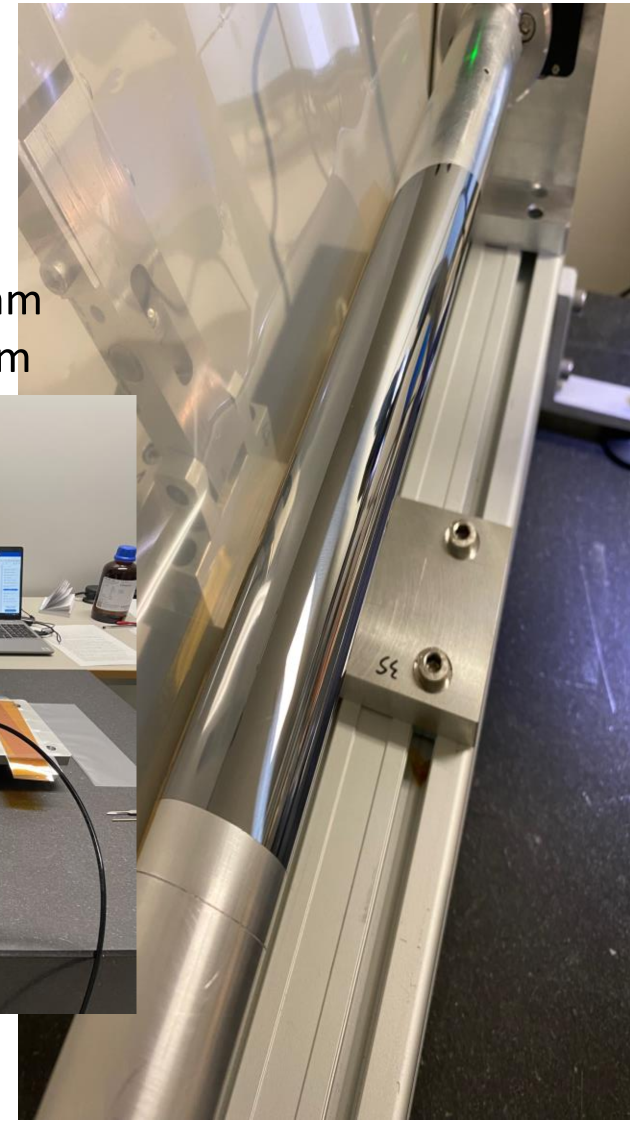




60x140mm

80x280mm
Ep. : 50um





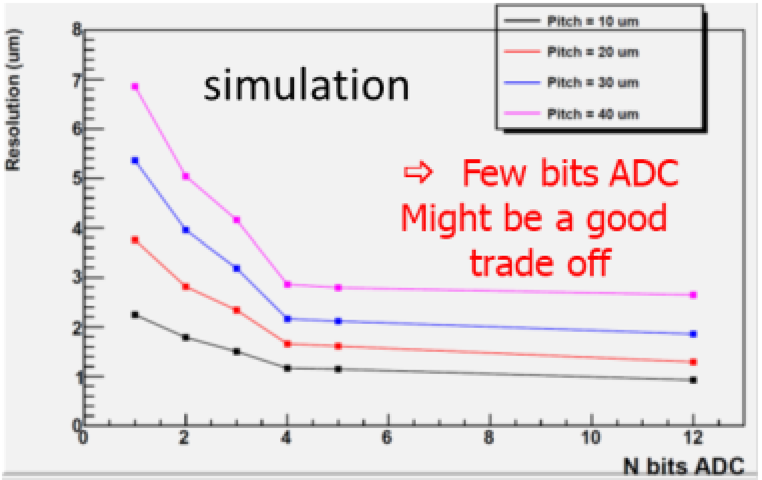
Kapton-dummy-SuperAlpide bending
Procedure done several times

Mezza-Luna bending
Procedure done twice without damages

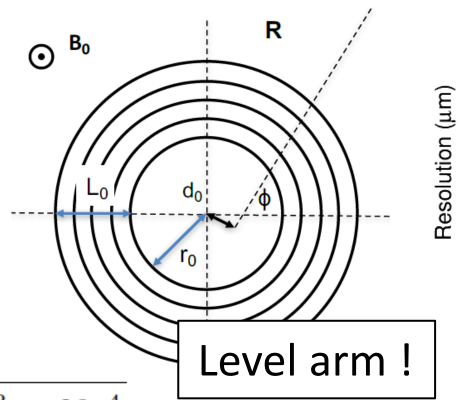
Challenge 1: the spatial resolution

Spatial resolution in Higgs factories

- Typical targets:
  - ✓ σ_{sp}~3 µm for the vertex layers
  - ✓ σ_{sp}~5-10 µm for the outer tracker layers
- Resolution in each layer depends on
  - ✓ Pitch
    - In conflict with the functionnalities inside the pixel
    - Favored by small feature size technology
  - ✓ Charge deposition
    - Sensitive layer thickness
  - ✓ Charge sharing (SNR vs resolution)
    - Depletion:
    - Staggered pixels
  - ✓ Charge encoding
    - Binary output / ADC / Tot / etc.

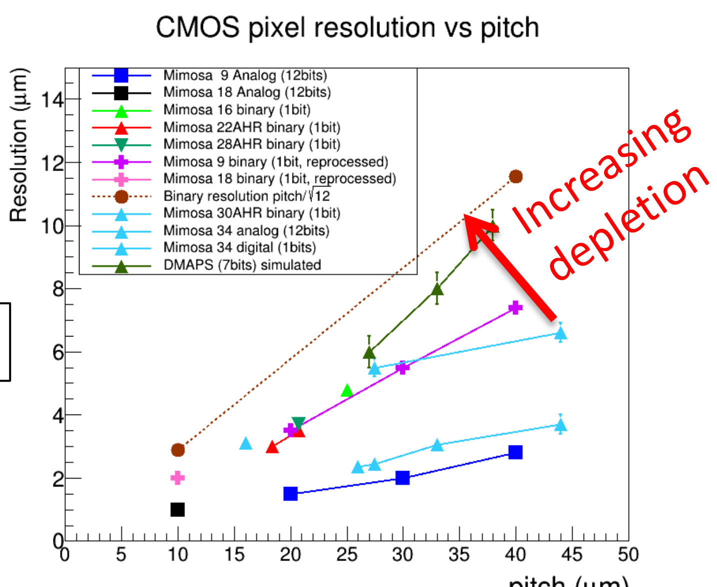


$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\sin^{3/2}\theta}\right)^2$$



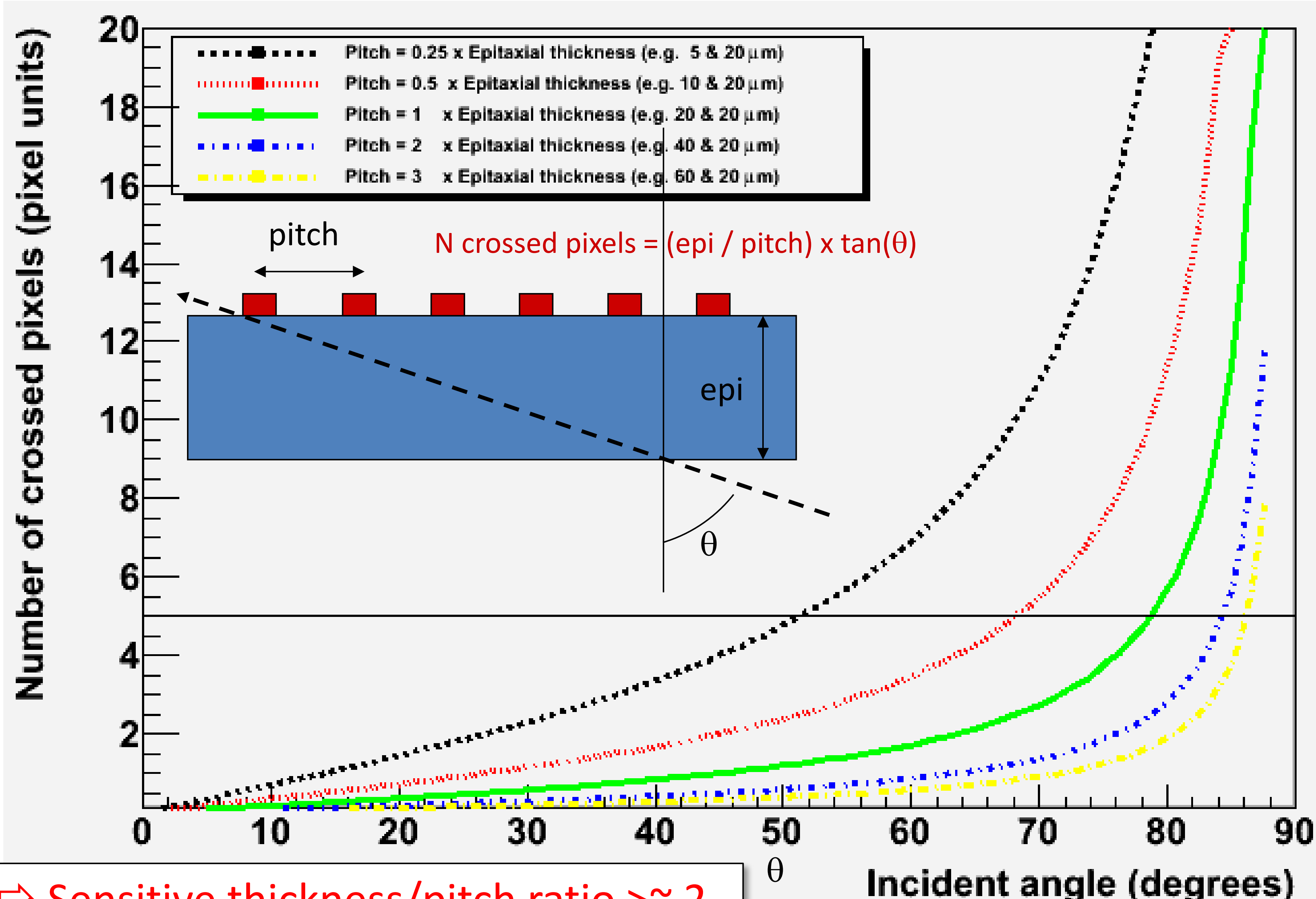
$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0\sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$



⇨ σ_{sp} ~ 3 µm ⇦⇨ pitch ~ 15-20 µm
(assuming binary output, ~20 µm epi.thickness & large depletion in 180nm tech.)

Elongated clusters: low pT tagging

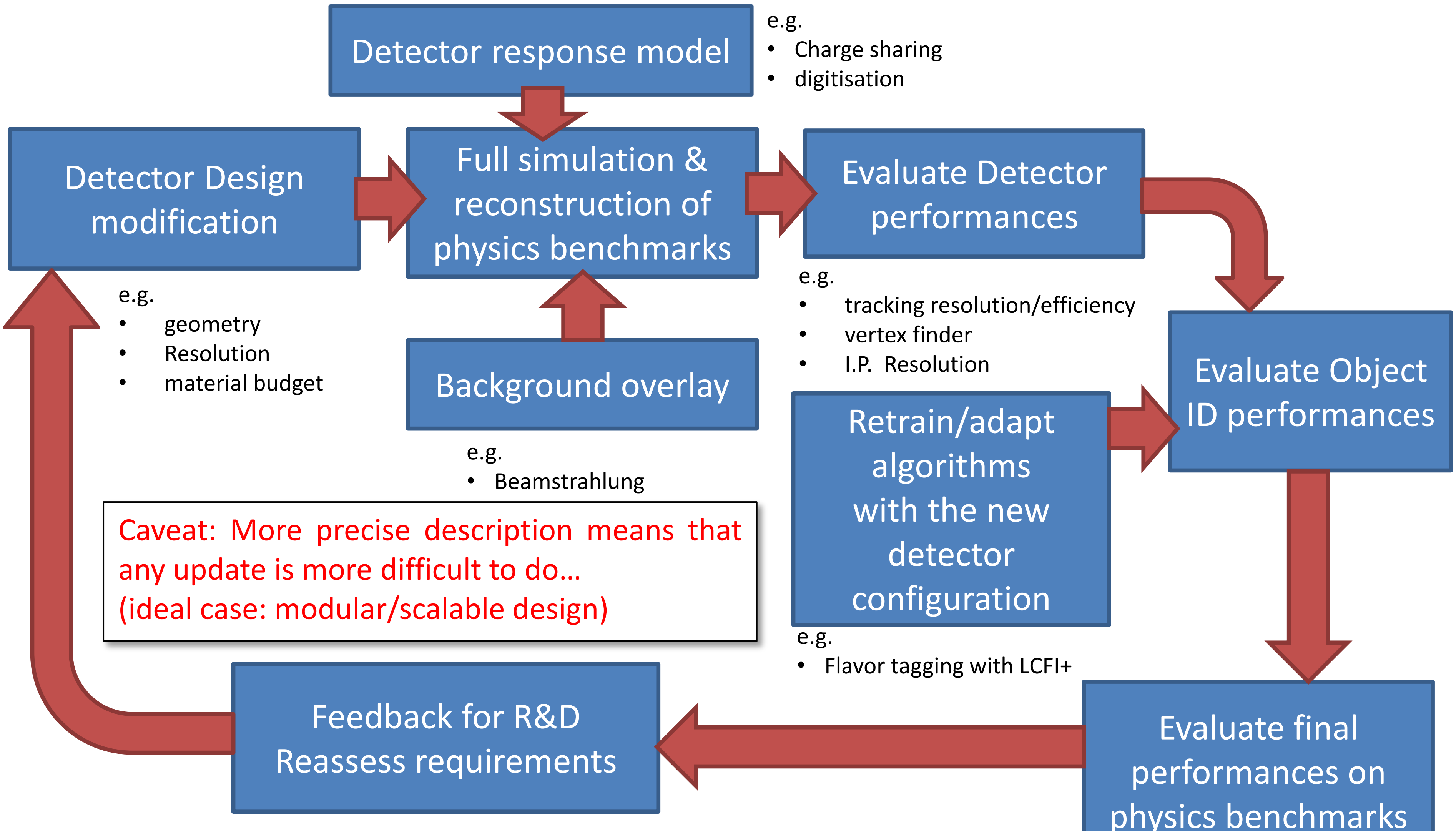


⇨ Sensitive thickness/pitch ratio >~ 2

Detector optimization and simulations

Optimization of the detector

- Example: Shall we target 18 or 22 μm pitch ?
- Caveat: One can not decouple detector optimization and algorithm optimization

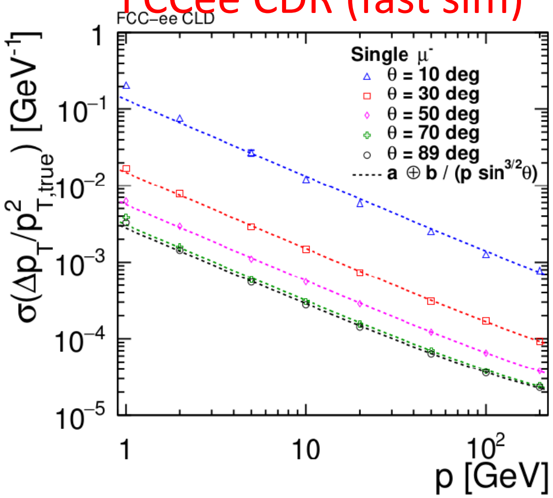


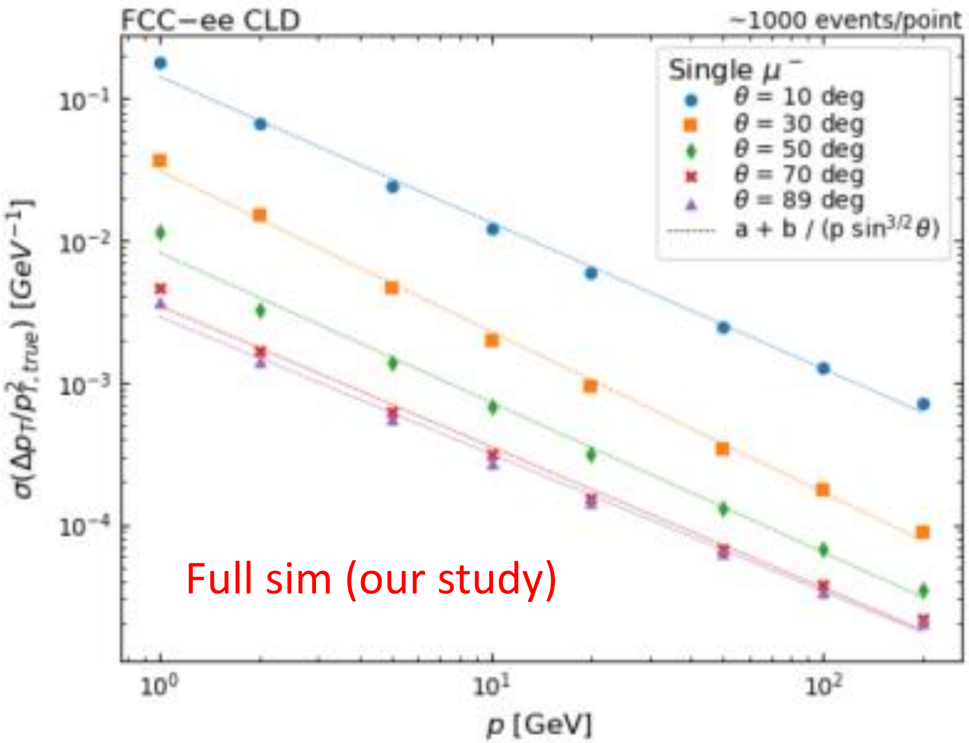
Example of detector optimization: CLD vertex/tracker

Jeremy Andrea, Auguste Besson, Ziad El Bitar, Gaelle Sadowski (PhD) (IPHC, CNRS, Strasbourg)

- Master the full simulation chain (key4hep) for detector optimisation
  - ✓ Goal: Optimisation of the Design
    - Complete physics studies (Long lived particle: HNL, etc.)
    - Object performances: Tracking, vertexing, Flavour tagging
  - ✓ Test new ideas
  - ✓ Guidelines for future R&D

FCCee CDR (fast sim)





Full sim (our study)

Full simulation chain validated

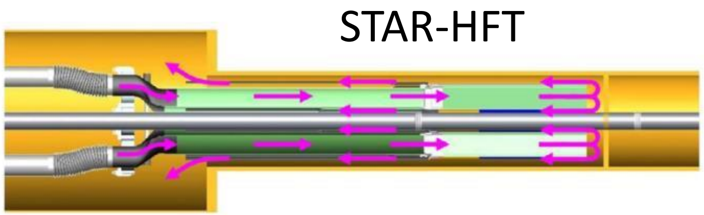
Power, Architecture & designs

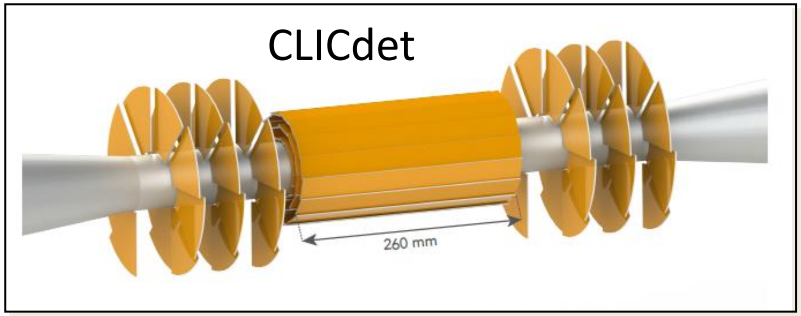
Power challenges

Power Analog $(mW/chip)$	49.22
Power Bias $(mW/chip)$	4.5
Power PriorityEncoder $(mW/chip)$	4.219
Power DigitalPeriphery $(mW/chip)$	64.27
Power PLL $(mW/chip)$	18.5
Power Serializer With Data $(mW/chip)$	86.06
Power Serializer With No Data $(mW/chip)$	0
Power LVDS $(mW/chip)$	56.4

MIMOSIS like architecture, 180 nm

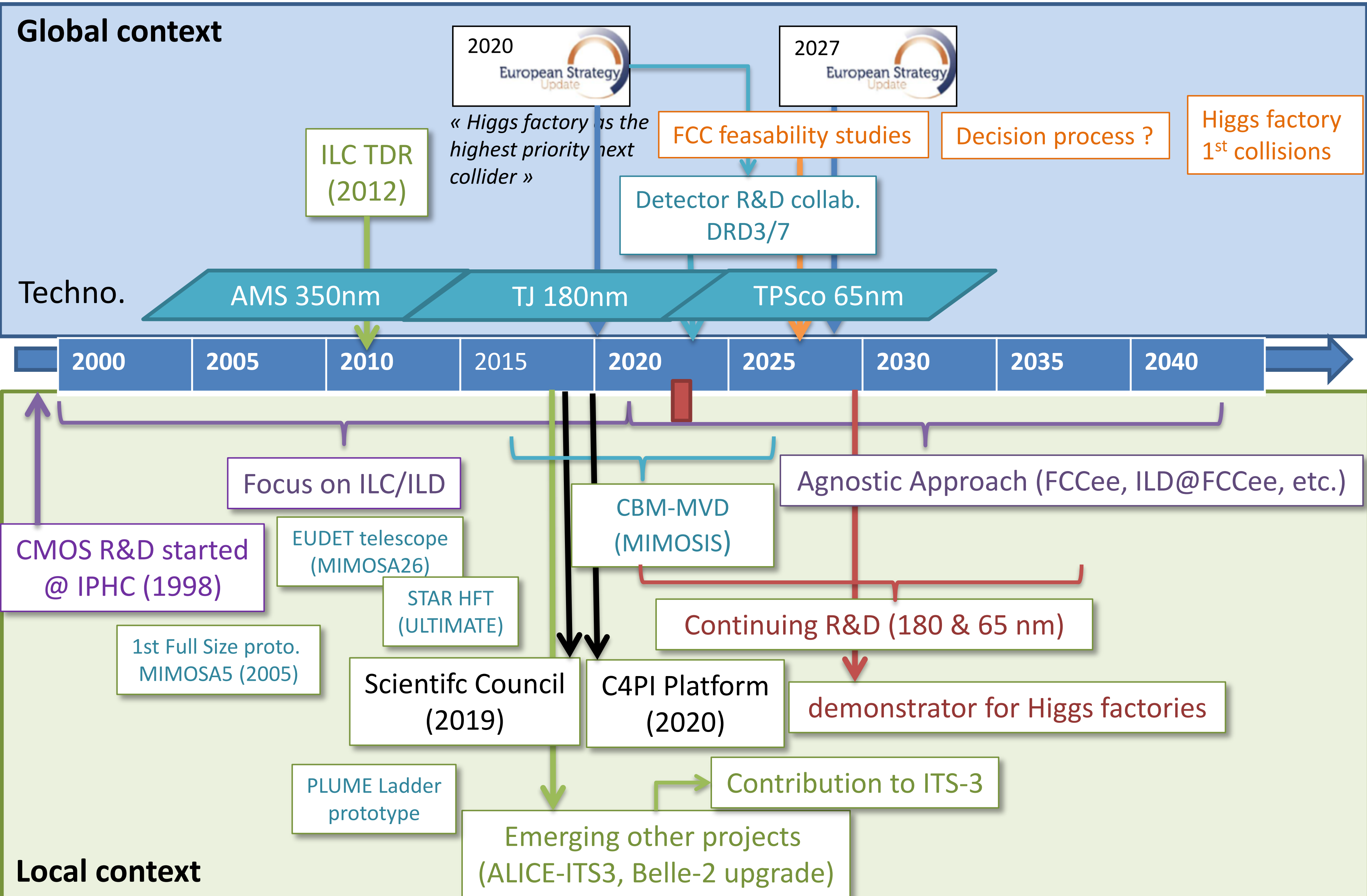
- Power is in conflict with all other parameters
- Baseline:
  - ✓ Air flow cooling only to minimize material budget
  - ✓ Up to ~ 20 mW/cm^2
    - what is the limit ? ~50 mW/cm^2 or even more ?
- Driving parameters:
  - ✓ # channels, Time resolution / data flux
  - ✓ Surface (VXD ~ 3500 cm^2 ; tracker O(10 m^2)
  - ✓ Power Pulsing (ILC/CLIC) ⇨ Constraints more relaxed w.r.t. FCCee
- The « Power paradox »
  - ✓ Small radius ⇨ Higher hit density and Power/cm^2 but small fraction of total power
  - ✓ Higher radius ⇨ less hit density but higher total power/layer
- Power sharing
  - ✓ Analog part: O(25-50%) ⇨ density of pixels, charge collection speed
  - ✓ Digital part: O(25-50%) ⇨ data flux, freq.
  - ✓ Output→DAQ: maximum flux. (25%)
- Architecture optimization is important
  - ✓ Priority encoder (limited by flux)
  - ✓ Asynchronous might be adapted (tot, etc.)
  - ✓ Etc.
- Technology feature size
  - ✓ e.g. 180nm to 65 nm: ~50% Power reduction
- Air extraction:
  - ✓ In conflict with disks and forward acceptance
    - (≠ALICE ITS2/3, Belle-2, STAR-HFT)





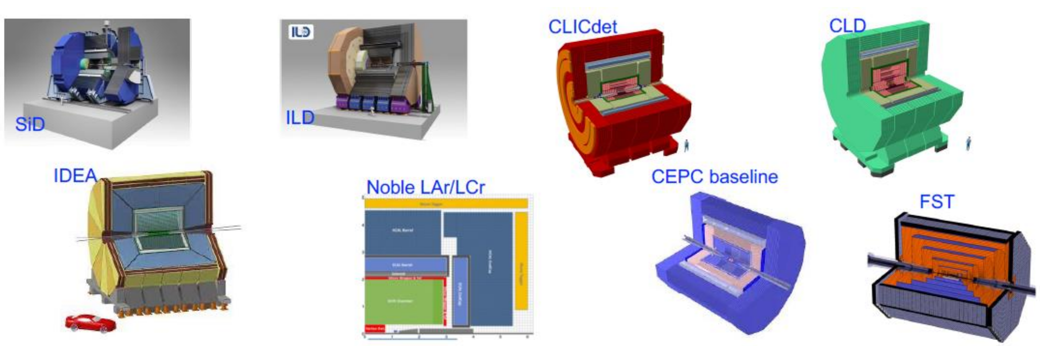
Higgs factories

Future e^+e^- collider: global and local context



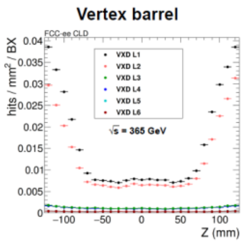
Tracking/vertexing detectors in future e^+e^- colliders

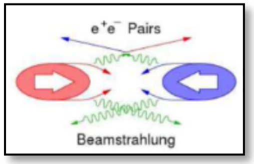
Collider	ILC		CLIC	FCCee			CEPC	
Bunch separation (ns)	330/550		0.5	20/990/3000			25/680	
Power Pulsing	yes		yes	no			no	
beamstrahlung	high		high	low			low	
Detector concept	SiD	ILD	CLICdet	CLD	IDEA	Lar	Baseline	IDEA
B Field (T)	5	3.5	4	2	2	2	3	2
Vertex	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel
Vertex Rmin (mm)	16	16	31	12	12	12	16	16
Tracker	Si-strips	TPC	Si-Pixel	Si-Pixel (+RICH ?)	DC/Si-strips	DC/Si-strips or Si-Pixels	TPC or Strips	DC/Si-strips
Tracker Rmax (m)	1.25	1.8	1.5	2.2	2.0	2.0	1.8	2.1
Disks layers	4 + 4	2 + 5	6 + 7	3 + 7	3 (150 mrad)		2+6	



(From D. Dannheim)

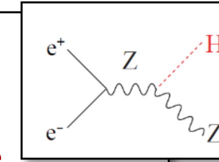
Large similarities between the concepts but also significant differences





Vertex detector requirements (ILC/FCCee)

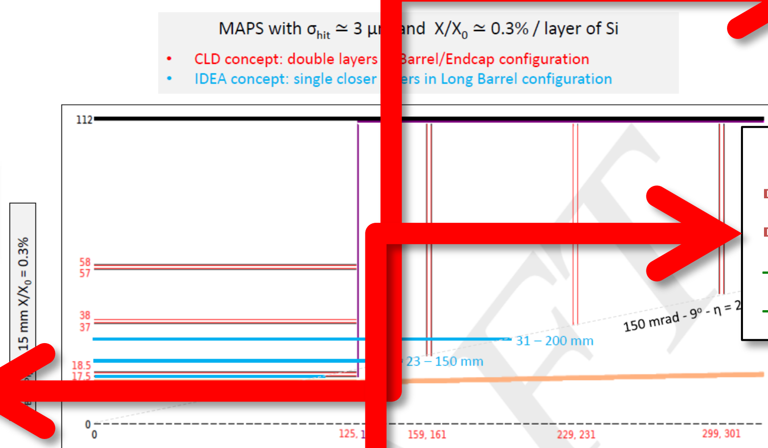
Physics
- ➩ Flavour tagging
- ➩ Low pT tracks
- ➩ Vertex/Jet charge determination
- ➩ Track seeding



Physics O(Hz/cm^2)

Beam background O(10-50 MHz/cm^2)

CLD and IDEA Vertex Detectors designs (superimposed)



(Figure: D. Contardo)

Vertex reconstruction
- ➩ granularity
- ➩ Pitch ~17-20 μm
- ➩ (σ_{sp} ~3-4 um)

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Material Budget
- ➩ ~ 0.15% X_0 / layer
- ➩ < 1% X_0 for the whole VTX
- + ~0.3 % X_0 for the beam pipe
- + 0.15% X_0 for 5 μm Gold coating

Time resolution
O(100ns-1 μs)

O(10ns)@CLIC

Low material detectors & supports structures

Power consumption
~< 50mW/cm^2

$$\sigma_{d_0} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

$a \simeq 5\,\mu m$ $b \sim 10\ \mu m.GeV$

Fast read-out & low Power Architectures (~ 20-50 mW/cm^2)

Cooling
Stiffness / Alignment

No Power pulsing @FCCee

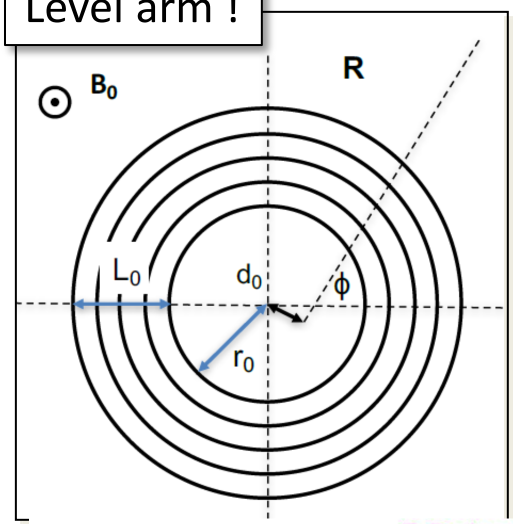
- Design: 5 single layers or 3 double layers ? Inner and outer radius ? Etc.
- R&D: ➩Keep excellent spatial resolution, low material budget, moderate Power consumption and push towards better time resolution (BX)

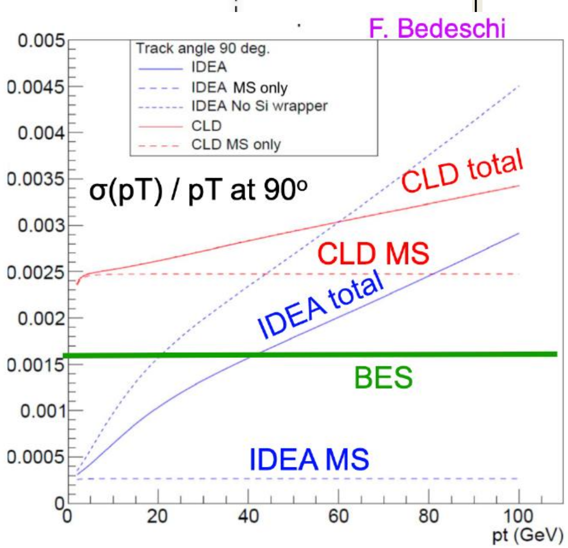
Tracker requirements

Expected performances

$$\frac{\sigma_{p_T}}{{p_T}^2} \sim 2 \times 10^{-5} GeV^{-1}$$

Level arm !





Physics

- ➪ Momentum resolution
- ➪ Tracking efficiency
- ➪ Track separation, low fake tracks
- ➪ Etc.

- Material budget vs intrinsic resolution
  - ✓ Typically σ_{sp} ~5-10 μm/layer ; material ~1-2% X_0/layer ; Power ~< 100 mW/cm^2
  - ✓ Low momentum vs high momentum
- 2 main options:
  - ✓ All silicon (CLD, CLICdet, SiD)
    - Few high resolution layers
    - Possibly timing capabilities
  - ✓ Silicon + Gazeous detector
    - TPC (ILD) / Drift Chamber (IDEA)
    - dEdx/dNdx capabilities,
    - More hits, overall less materials
    - TPC: Ion back flow issue for circular colliders
- PID Strategy to be included (RICH, timing, dEdx, etc.)

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

$$d_{tot}/X_0 = (N+1)d/X_0.$$

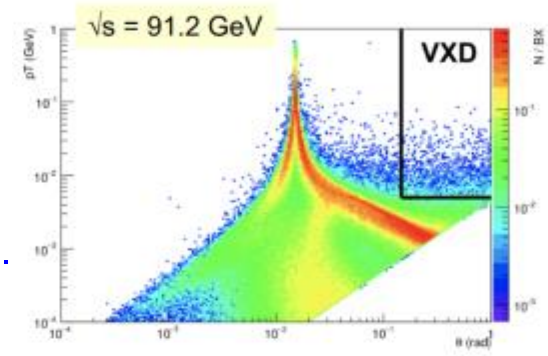
d = layer thickness, N = # layers

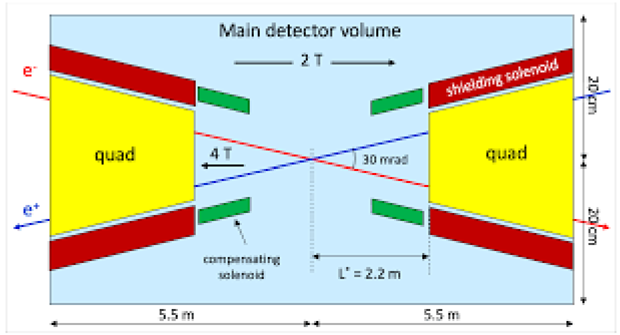
$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{0.3\beta\, B_0 L_0}\sqrt{\frac{d_{tot}}{X_0 \sin\theta}} \qquad \frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\, p_T}{0.3\, B_0 L_0^2}\sqrt{\frac{5}{N+5}}$$

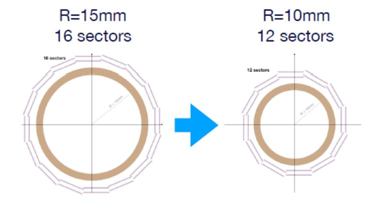
m.s. term dominates for pT ~< 100 GeV/c

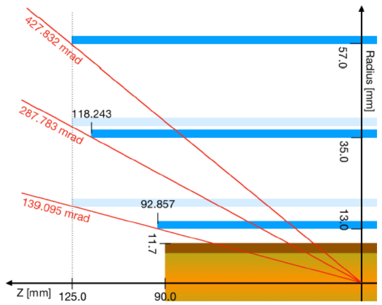
Vertex/tracking detector comments

- Particle ID has to be included in the tracker concept
  - ✓ dEdx and/or dNdx and/or fast timing
- Inner and outer radius are key factors
- Forward acceptance (e.g. asymmetry measurements)
  - ✓ Limited by MDI constraints, beam pipe, luminosity measurements, etc.
    - 30 mrad acceptance (FCCee)
- B-field
  - ✓ Limited to 2 T in circular machine (@ Z-pole)
- Beam time structure
  - ✓ Power pulsing only for linears
- Beam related Background
  - ✓ Beamstrahlung (incoherent e^+e^- pairs)
    - Occupancy driver for linears
    - Less severe for circular (⇨Rmin reduction ~10mm))
  - ✓ Synchrotron radiation (mainly circulars)
    - Possible shielding (increase beampipe material budget)
- VTX Geometry
  - ✓ Probably 5-6 layers VTX (R < 60 mm)
    - Robustness (standalone tracking)
    - low momentum tracking
    - Track seeding @ different radii
    - e.g. FIPs, highly ionizing particles, LLPs, etc.
  - ✓ « long barrel » (sticking the first measurement point to the beam pipe)





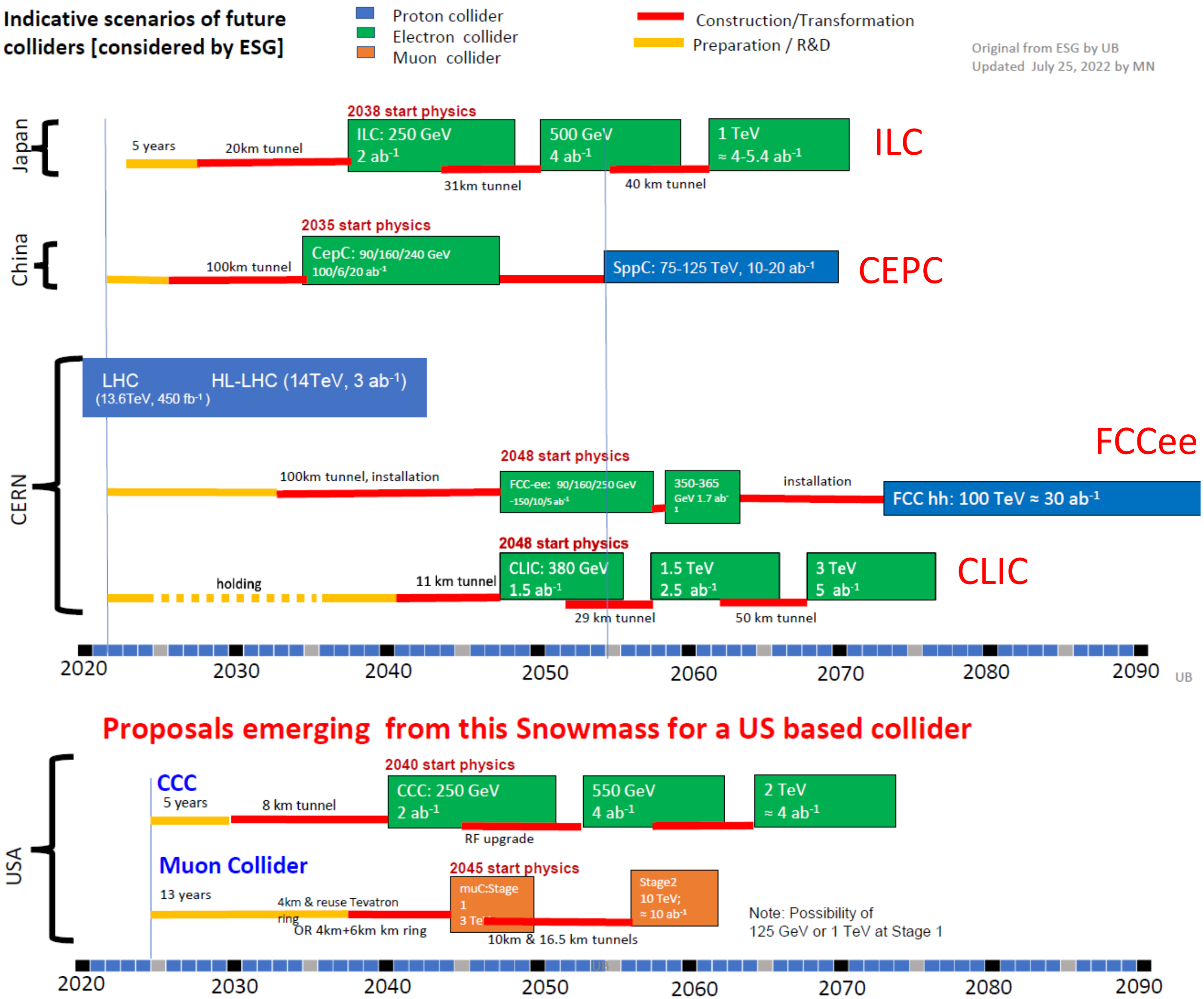




VTX/Tracking detector is highly connected to the MDI and the whole detector concept

Future e+e- colliders (« Higgs factories »)

Snowmass summary (summer 2022): https://snowmass21.org/energy/start



- Next Milestone: European Strategy Update for particle physics (~2026-27)
- Coming decade: Detector R&D programs through DRDs
- Other proposals considered (e.g. new concepts, ILC hosted outside Japan, etc.)

e+e- collider beam parameters

Linear

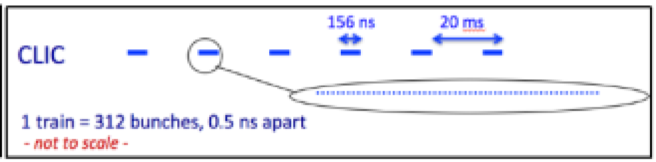
Parameter	ILC 250 GeV	ILC 500 GeV	CLIC 380 GeV	CLIC 1.5 TeV	CLIC 3 TeV
Luminosity L ($10^{34}cm^{-2}sec^{-1}$)	**1.35**	**1.8**	**1.5**	**3.7**	**5.9**
L > 99% of √s ($10^{34}cm^{-2}sec^{-1}$)	1.0	1.0	0.9	1.4	2.0
Repetition frequency (Hz)	5	5	50	50	50
Bunch separation (ns)	554	554	0.5	0.5	0.5
Number of bunches per train	1312	1312	352	312	312
Beam size at IP σ_x/σ_y (nm)	515/7.7	474/5.9	150/2.9	~60/1.5	~40/1
Beam size at IP σ_z (μm)	300	300	70	44	44

ILC: Crossing angle 14 mrad, e^- polarization ±80%, e^+ polarization ±30%
CLIC: Crossing angle 20 mrad, e^- polarization ±80%

Very small beams + high energy => beamstrahlung

Very small bunch separation at CLIC drives timing requirements for detector

Very low duty cycle at ILC/CLIC allows for:
Triggerless readout
Power pulsing



Circular

	FCC-ee Z	FCC-ee Higgs	FCC-ee ttbar	CEPC Z (2T)	CEPC Higgs
√s [GeV]	**91.2**	**240**	**365**	**91.2**	**240**
Luminosity / IP ($10^{34}cm^{-2}s^{-1}$)	**230**	**8.5**	**1.7**	**32**	**1.5**
no. of bunches / beam	16640	393	48	12000	242
Bunch separation (ns)	**20**	994	3000	**25**	680
Beam size at IP σ_x/σ_y (μm/nm)	6.4/28	14/36	38/68	6.0/40	20.9/60
Bunch length (SR/BS) (mm) Beam size at IP σ_z (mm)	3.5/12.1	3.3/5.3	2.0/2.5	8.5	4.4

Beam transverse polarisation
=> beam energy can be measured to very high accuracy (~50 keV)

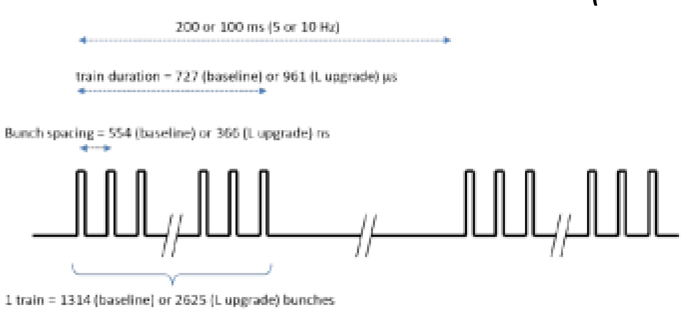
At Z-peak, very high luminosities and **very high e^+e^- cross section (40 nb)**
⇒ **Statistical accuracies at 10^{-4} -10^{-5} level ⇒ drives detector performance requirements**
⇒ **Small systematic errors required** to match
⇒ This also drives requirement on **data rates** (physics rates 100 kHz)
⇒ Triggerless readout likely still possible

Beam-induced background, from beamstrahlung + synchrotron radiation
- Most significant at 365 GeV
- Mitigated through MDI design and detector design

Modified from Lucie Linssen, ESPPU, 2019

Mogens Dam / NBI Copenhagen AIDA++ Open Meeting, CERN 4 September, 2019 6

(slide from Mogens Dam/Lucie Linssen)



FCCee Collider parameters

Updated luminosity parameters (2023):

Working point	Z, years 1-2	Z, later	WW, years 1-2	WW, later	ZH	$t\bar{t}$	
$\sqrt{s}$ (GeV)	88, 91, 94		157, 163		240	340–350	365
Lumi/IP ($10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$)	70	140	10	20	5.0	0.75	1.20
Lumi/year (ab^{-1})	34	68	4.8	9.6	2.4	0.36	0.58
Run time (year)	2	2	2	0	3	1	4
Number of events	$6\,10^{12}$ Z		$2.4\,10^{8}$ WW		$1.45\,10^{6}$ HZ + 45k WW $\rightarrow$ H	$1.9\,10^{6}$ $t\bar{t}$ +330k HZ +80k WW $\rightarrow$ H	

Table 1 The baseline FCC-ee operation model with four interaction points, showing the centre-of-mass energies, instantaneous luminosities for each IP, integrated luminosity per year summed over 4 IPs corresponding to 185 days of physics per year and 75% efficiency, in the order Z, WW, ZH, $t\bar{t}$. The luminosity is assumed to be half the design value for machine commissioning and optimisation during the first two years at the Z pole, the first two years at the WW threshold, and the first year at the $t\bar{t}$ threshold. (Should the order of the sequence be modified to either Z, ZH, WW, $t\bar{t}$ or ZH, WW, Z, $t\bar{t}$, the ZH stage would start with two years at half the design luminosity followed by two years at design luminosity, while the WW stage would run afterwards for only one year but at design luminosity.) The luminosity at the Z pole (the WW threshold) is distributed as follows: $40\,\mathrm{ab}^{-1}$ at 88 GeV, $125\,\mathrm{ab}^{-1}$ at 91.2 GeV, and $40\,\mathrm{ab}^{-1}$ at 94 GeV ($5\,\mathrm{ab}^{-1}$ at 157.5 GeV, and $5\,\mathrm{ab}^{-1}$ at 162.5 GeV). The number of WW events include all $\sqrt{s}$ values from 157.5 GeV up.

2021

parameter	Z	WW	H (ZH)	ttbar
beam energy [GeV]	45	80	120	182.5
beam current [mA]	1390	147	29	5.4
no. bunches/beam	16640	2000	393	48
bunch intensity [10^{11}]	1.7	1.5	1.5	2.3
SR energy loss / turn [GeV]	0.036	0.34	1.72	9.21
total RF voltage [GV]	0.1	0.44	2.0	10.9
long. damping time [turns]	1281	235	70	20
horizontal beta* [m]	0.15	0.2	0.3	1
vertical beta* [mm]	0.8	1	1	1.6
horiz. geometric emittance [nm]	0.27	0.28	0.63	1.46
vert. geom. emittance [pm]	1.0	1.7	1.3	2.9
bunch length with SR / BS [mm]	3.5 / 12.1	3.0 / 6.0	3.3 / 5.3	2.0 / 2.5
luminosity per IP [$10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$]	230	28	8.5	1.55
beam lifetime rad Bhabha / BS [min]	68 / >200	49 / >1000	38 / 18	40 / 18