65nm chips

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4 chips in MLR1 and 15 chips of CE65V2 in ER1

Modification	Purpose	2 Basic chips with pitch/geometry, um	Comment	Total No of chips	status
CE65V A,B,C,D	Charge collection, Pixel amplifier/buffer variants exploring: AC, DC , SF pixels	15, 25	For lab and beam test: charge collection, leakage, noise, node techno, optimization	2 basic chips and 3 techno flavors: 1) no n-implant: CE65 A, CE65 D 2) Blanket n-implant: CE65 C 3) n-implant with gaps: CE65 B	Submitted In tests

Modification	Purpose	5 Basic chips with pitch/geometry, um	Comment	Total No of chips	status
CE65V2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (AC pixel from CE65V1 is implemented)	15, 18, 22.5, 18_{hexsq}, 22.5_{hexsq}	For lab and beam test: charge collection, leakage, noise, node techno, optimization	5 basic chips x 3 techno flavors: 1) no n-implant 2) Blanket n-implant 3) n-implant with gaps)	Submitted

Minimalistic(*) lab test program continuation and for UniZH, CTU

- **Basic set of measurements and plot results:**
  - ✓ Noise: thermal noise distribution(ENC), FPN (baseline distribution)
  - ✓ Fe55 Calibration peak (from that we estimate averaged conversion factor to calibrate in electrons) with seed signals (seed in electrons)
  - ✓ Custer 3x3 (cls3, in el.) and 5x5 (cls5, in el.)
  - ✓ Charge sharing correlation plots: cls3 (in el.) vs seed(in el.)
- **Advanced measurements :** linearity, pixel-to-pixel variation, RTS, leakage current(**) -> some of them only for next CE65V2 chips

Coming actions:

- **Transfer knowledge of lab software (SB), firmware (KKJ), hardware (KKJ, SB, SS)**
- **Collection of results, carrier boards and chips available (SS, SB + all)**

- **Basic set of measurements for: CE65A, B, D , only for versions ACpix and all versions of CE65V2**
  - ✓ **At different HV voltage: 1V to 10V with step 1V**
  - ✓ **Different irradiation doses: 1e13 Neq, 1e14 Neq, 1e15 Neq (for CE65V2 only)**
  - ✓ **Different PSUB/PWELL: only for CE65V2, for CE65V1 PSUB=PWELL=0**
  - ✓ **Different temperatures: 0C, 10C, 20C**

Tests: UniZH, CTU + students (of Ziad) ??

(*) Exclude:

- **CE65C**
- **DC and SF pixel versions**
- **VSUB/PWELL <0**
- **Linearity with monochromatic X-ray of various energy, pixel-to-pixel gain variation, deep RTS study**

(**) Pixel-to-pixel variation of leakage current is ongoing (KKJ and AD), demanded (WS) input for DPTS -> optimization FE for the next ER2 run

Minimalistic(*) beam test program for CE65V1 / (will be similar for CE65V2)

- **Basic results:**
  - ✓ Resolution and Clusters
  - ✓ Detection efficiency and fake hit rate
  - ✓ Signal spectra

Coming actions: discuss (all)

- **Advanced results:**
  - ✓ Resolution, efficiency, clusters and fake hit rate with “offline” digitization to certain threshold in electrons in range from 50 to 200 e (complementary to DPTS and future MOSS)

- **For: CE65A, B, D , only for versions ACpix**
  - ✓ **At different HV voltage: 1V to 10V with step ?V -> will be more clear after lab tests**
  - ✓ **Different irradiation doses: 1e13 Neq, 1e14 Neq**
  - ✓ **PSUB=PWELL=0**

(*) Exclude:

- **CE65C,**
- **DC and SF pixel versions**
- **VSUB/PWELL <0**

HW preparation for next CE65V2

Carrier PCB design considerations:

- ✓ Learned from past experience:
  - Single ended chip output buffer for oscilloscope and then differential for PROXY board: get better freedom for feedback resistances
  - All digital inputs buffered (better on PROXY)
  - RC filters for analogue inputs
- ✓ Other changes:
  - Extra functionality (CALIB injection, windowed readout)
  - Try to combine compatibility with existing PROXY with reduced functionality (to CE65V1)
  - Possible on-board fixed biasing option to run without DAQ/PROXY

Coming actions:

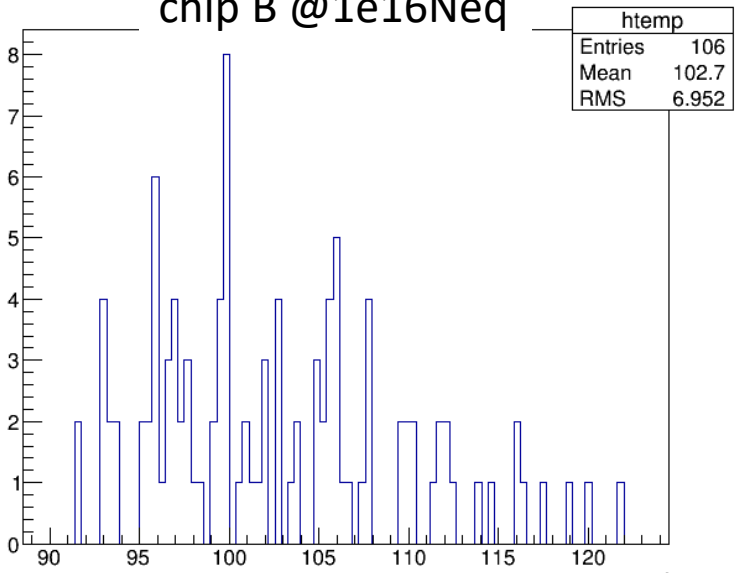
- **Carrier conceptual design, simulation (AD, consultation from KKJ +- Italy DAQ team)**
- **Carrier PCB design (AD with consultation from CI, KKJ)**
- **Existing FW DAQ and PROXY adaptation (KKJ, consultation from AD, not clear for + - Italy DAQ team)**
- **Estimate alternative to DAQ (only for lab tests): feasibility of DAQ based on Digilent Oscilloscope (AD, KKJ) -> if yes, carrier should be compatible with two systems..**

Backup slides

Actual tests (KKJ, AD): Leakage current results at T=20C

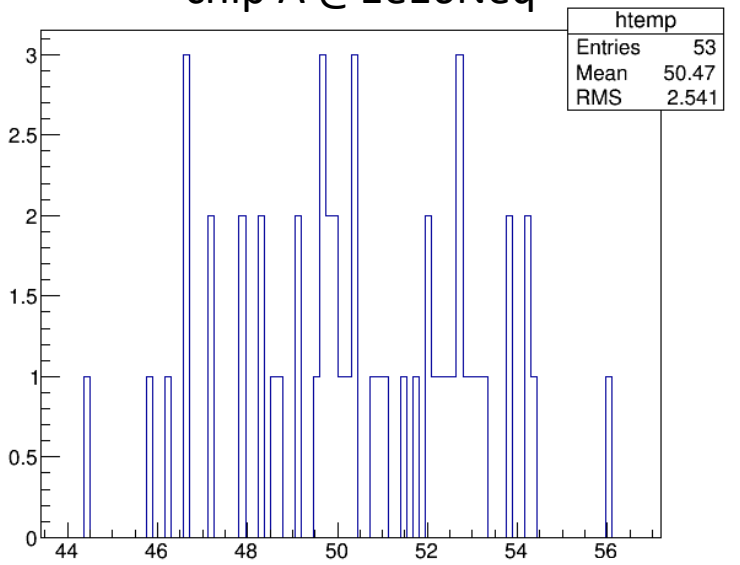
1. After 500Mrad:
   - chip B ~ 0.45 pA /pixel, peak-to-peak 0.4pA to 0.5pA
2. After 1e15Neq:
   - chip B (modified, with gaps) 22 pA /pixel, 18pA to 28pA peak-to-peak
   - chip A twice smaller, 11pA /pixel, 9pA to 14pA peak-to peak
3. After 1e16Neq:
   - chip B (modified, with gaps) 103 pA /pixel, 91 pA to 122 pA peak-to-peak
   - chip A twice smaller, 51pA /pixel, 44pA to 56pA peak-to peak

chip B @1e16Neq



pA /pixel

chip A @1e16Neq



pA /pixel

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Conclusions and perspectives

Conclusions for CE65V1:

- Served to get several results from matrix of pixels:
  - ✓ expected charge collection for standard and modified diode, capacitance 2-4fF
  - ✓ sensitive volume thickness ~11 um, and can be depleted > 3V
  - ✓ work after irradiation to 1e15 Neq, leakage <20 pA/pix (however difficult to readout)
- DAC tested and worked
- Still to do (irradiations at 1e13Neq, 1e14Neq, RTS)

To do in CE65V2: R&D for charge collecting node optimization for large stitched chips (MOSS)

- Charge collection properties:
  - ✓ Clusters, charge sharing
  - ✓ Spatial resolution, multiplicity
  - ✓ Efficiency
- More precise electrical properties:
  - ✓ Leakage current , RTS
  - ✓ Depletion, capacitance

Next CE65V3xxx with possible sub-versions

✓ **complementary study for ITS3**
which can not be all done in large scale sensors and not included in other small scale chips:

- Include/repeat similar program as for CE65V2: matrix layout geometry, pitch size variation
- Charge collecting diode size optimization: RTS, signal, efficiency
- Front end circuit: versions, optimizations, new ideas
- Digital cells optimization: leakage current evaluation, test different ideas

<= Andrei
+ Corentin (from CERN)

✓ **R&D beyond ITS3, paving new ideas for ALICE3**

- Additional small test structure of asynchronous architecture <= Jean's thesis with Frederic
- New pixel structure optimised for low gain (in view of reducing power needed for analog front-end)
  <= Andrei + PhD thesis to start in Fall 2023