Rd53B Electrical QC

COmparison of characteristics of module 20UPGR92101024

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Paris

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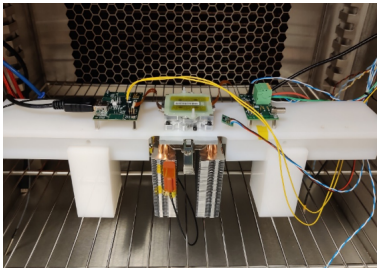
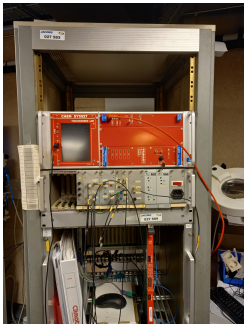
Setup

The module is powered and monitored in a climate chamber with:

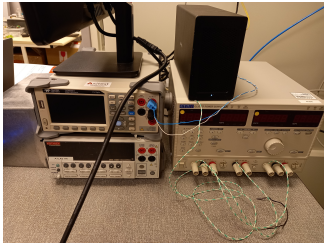
- A CAEN power supply (ps)
- A T3DMM6-5 multimeter
- PFP-KX7+ PCIe FMC card with 640 MBps YARR firmware



(a) Setup with module in climate chamber



(b) Power supply



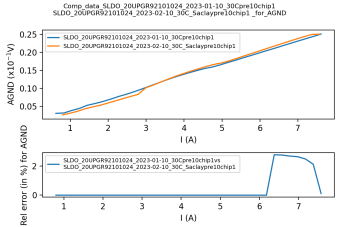
(c) Multimeter

Figure 1: Setup in climate chamber

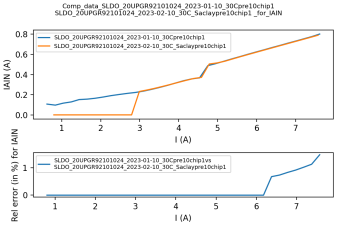
The Figure 1 shows our setup in the climate chamber. The white bridge supports the module, powering and reading cards, plus the heat exchange device.

Module 20UPGR92101024 chip 1

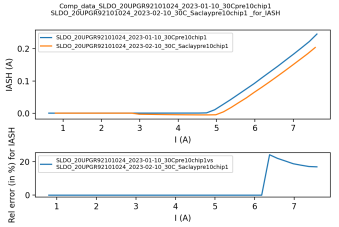
The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



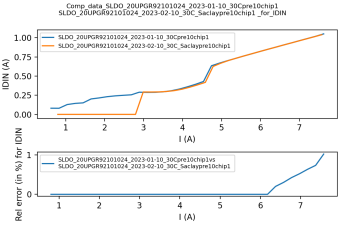
(a) AGND measurements



(b) IAIN measurements



(c) IASH measurements



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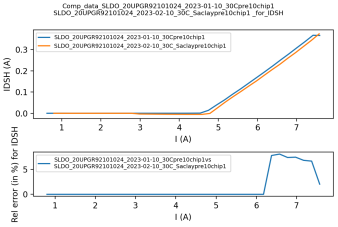
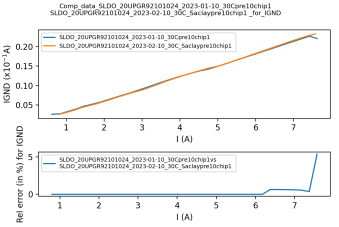


(e) IDSH measurements

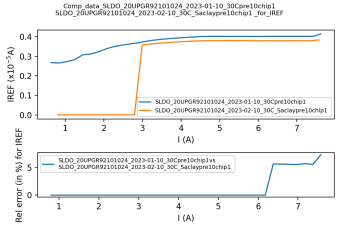


(f) IGND measurements

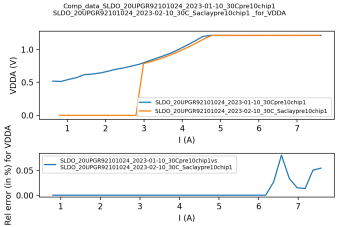
Figure 2: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 1

Module 20UPGR92101024 chip 1

The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



(a) IREF measurements



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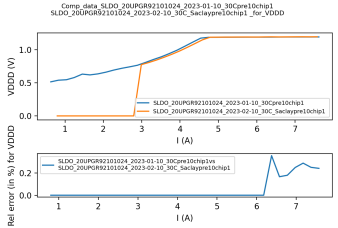
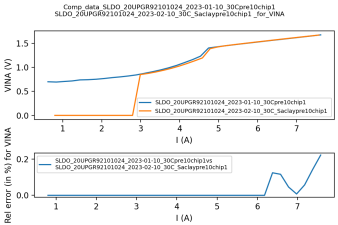


(c) VDDD measurements



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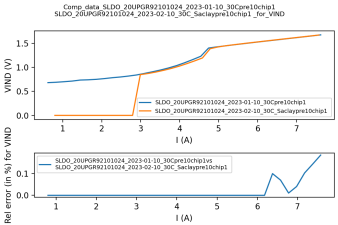

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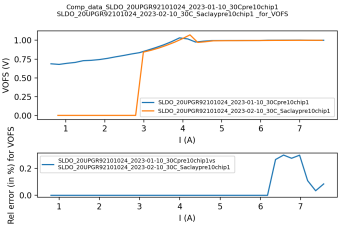
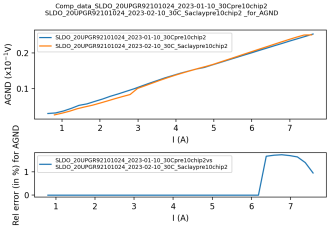


(f) VOFS measurements

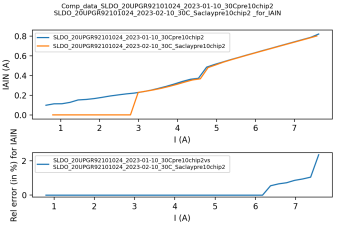
Figure 3: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 1

Module 20UPGR92101024 chip 2

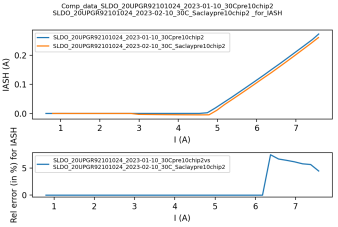
The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



(a) AGND measurements



(b) IAIN measurements



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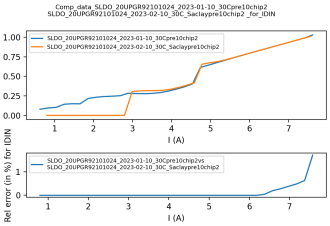

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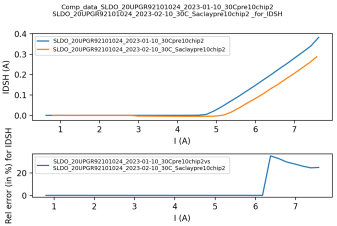

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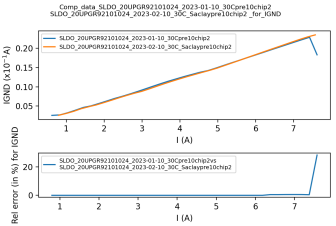
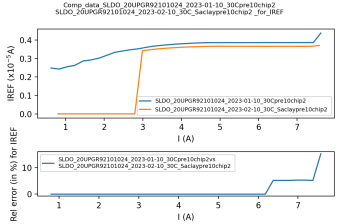


(f) IGND measurements

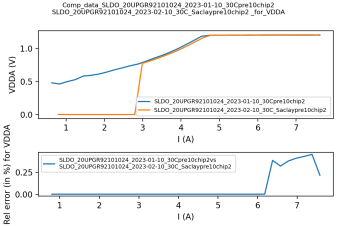
Figure 4: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 2

Module 20UPGR92101024 chip 2

The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



(a) IREF measurements



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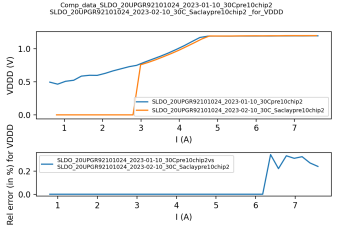

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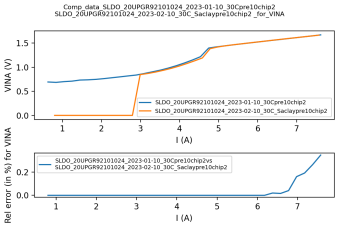
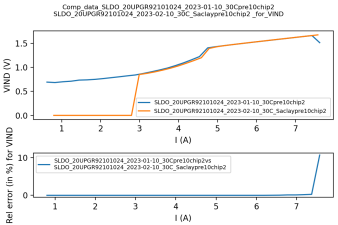
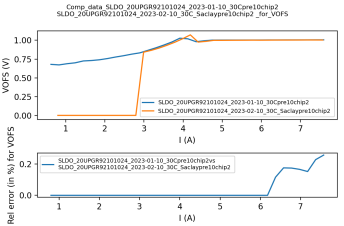


(d) VINA measurements



(e) VIND measurements

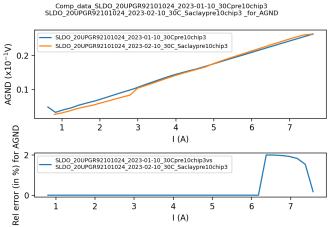


(f) VOFS measurements

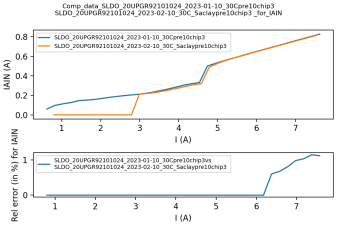
Figure 5: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 2

Module 20UPGR92101024 chip 3

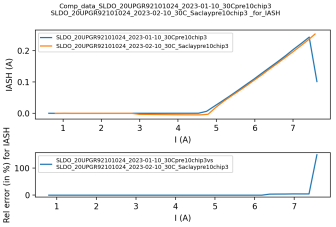
The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



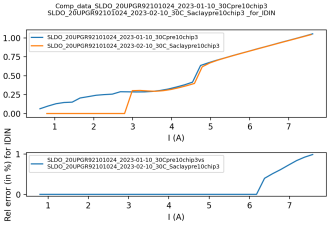
(a) AGND measurements



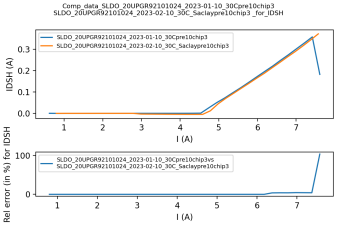
(b) IAIN measurements



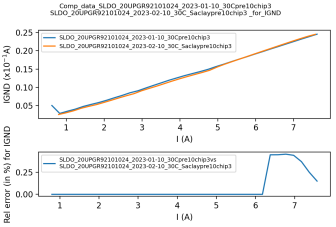
(c) IASH measurements



(d) IDIN measurements



(e) IDSH measurements

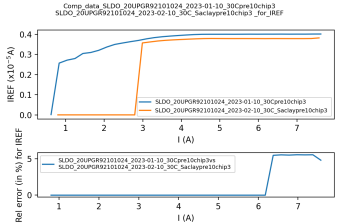


(f) IGND measurements

Figure 6: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 3

Module 20UPGR92101024 chip 3

The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



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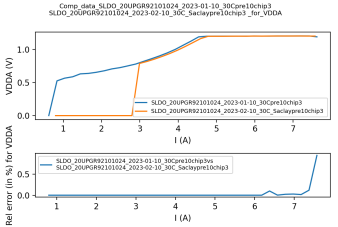
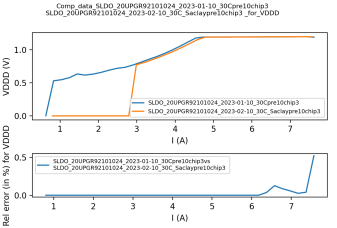
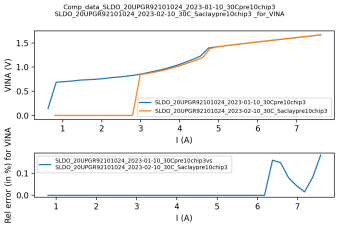


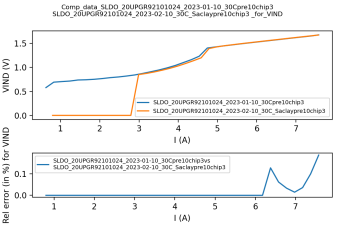
(b) VDDA measurements



(c) VDDD measurements



(d) VINA measurements



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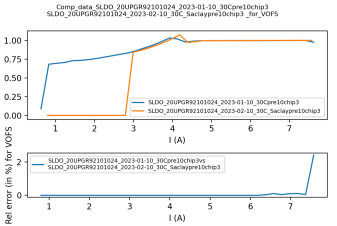
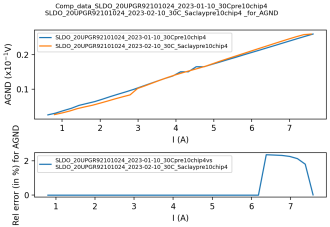


(f) VOFS measurements

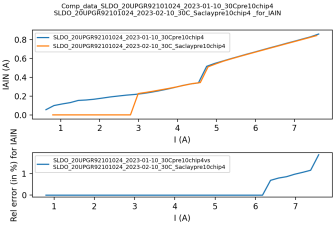
Figure 7: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 3

Module 20UPGR92101024 chip 4

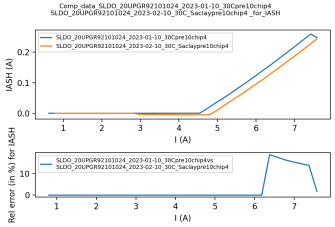
The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



(a) AGND measurements



(b) IAIN measurements



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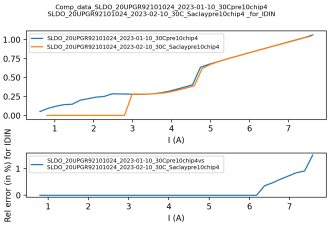

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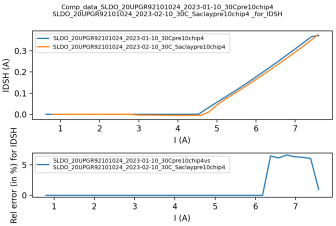
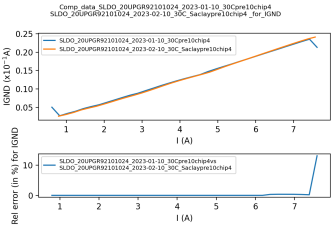


(e) IDSH measurements

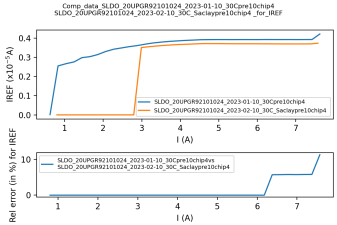


(f) IGND measurements

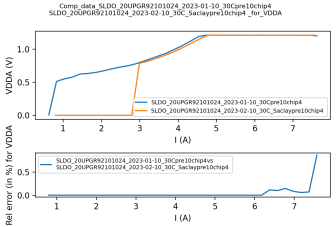
Figure 8: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 4

Module 20UPGR92101024 chip 4

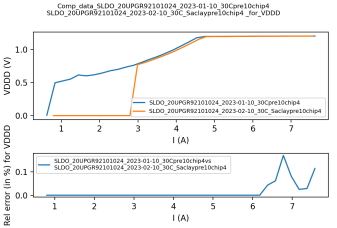
The results of test are compared by plotting them together in the same graph and by calculating the relative error over the operation region.



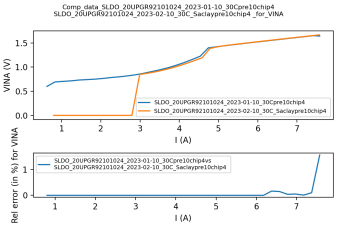
(a) IREF measurements



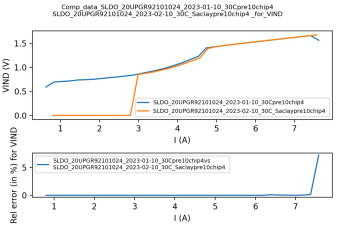
(b) VDDA measurements



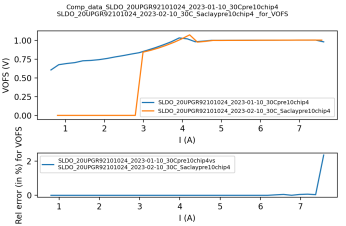
(c) VDDD measurements



(d) VINA measurements



(e) VIND measurements



(f) VOFS measurements

Figure 9: Comparison of IJCLab and LPNHE results on electrical QC of module 20UPGR92101024 chip 4

The following table presents the maximum relative error between IJCLab's results and LPNHE's ones.

20UPGR92101024	Chip 1 (%)	Chip 2 (%)	Chip 3 (%)	Chip 4 (%)
IAIN	1.48	2.35	1.15	1.87
IASH	24.22	7.43	149.74	18.84
IDIN	1.02	1.7	0.99	1.52
IDSH	8.05	35.07	104.06	6.59
IGND	5.4	28.32	0.45	13.13
IREF	7.28	15.32	5.55	11.33
AGND	2.76	1.72	2.0	2.36
VDDA	0.08	0.45	0.94	0.87
VDDD	0.36	0.34	0.52	0.17
VINA	0.22	0.35	0.18	1.55
VIND	0.18	10.72	0.19	7.21
VOFS	0.3	0.26	2.42	2.36

Comparison of results

The results are in good agreement over the working region

The relative error is never higher than 10 % , except shunt currents parameters as it is hard to monitor