CE65V2C manual[1]

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Strasbourg, November 2022

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2. Version V0.9 on 14/12/2022, A. Dorokhov, andrei.dorokhov@iphc.cnrs.fr, complete content done
3. Version V1.0 on 06/01/2023, A. Dorokhov, andrei.dorokhov@iphc.cnrs.fr, verification, consistence, corrections

Introduction

The chip CE65V2C (”C”hip ”E”xploratory ”65”nm ”V”ersion”2” ”C”harge properties) is intended for exploring charge collection properties of CMOS pixel sensors (CPS) fabricated in 65 nm technology. The CE65V2 is improved (2nd) version of the first CE65V1 exploratory chip, for which the data sheet can be found here [1]. In the first CE65V1 there are tree amplifier/buffer versions, only one (AC coupled amplifier[1]) was chosen for second chip version after tests.

The improvements in CE65V2 are made in order to allow for precise measurements of electrical properties (leakage current, depletion, capacitance) of the charge collecting diode before and after irradiation. Here is the list of additional features and improvements:

- Charge injection with external pulse
- Two extra test pixels variants in order to make accurate measurement of the input capacitance of charge collecting diode
- Programmed windowed readout: for heavily irradiated sensors one can set smaller submatrix of any size in X and Y for readout
- Separate digital and analogue power domains

The number of chip variants of CE65V1 is limited to 4, while for CE65V2 the number of variants increased in order to probe potential geometries in full scale chip (MOSS1) and beyond.

The CE65V2 chip exists in 15 variants: 5 different pixel geometries and 3 different technology options. The mechanical, electrical specifications and readout procedure are identical for all of them.

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1. Data sheet

1.1. Mechanical specifications

Chip dimensions are shown in Fig. 1.1 and bottom-left corner zoom is shown in Fig. 1.2. The chip has square size of 1.5 mm $\times$ 1.5 mm. The logo is places at the left bottom position of the chip and it contains name of the chip. The name has common part ”CE65V2C” and the part for different modifications described in details in chapter 3.2.

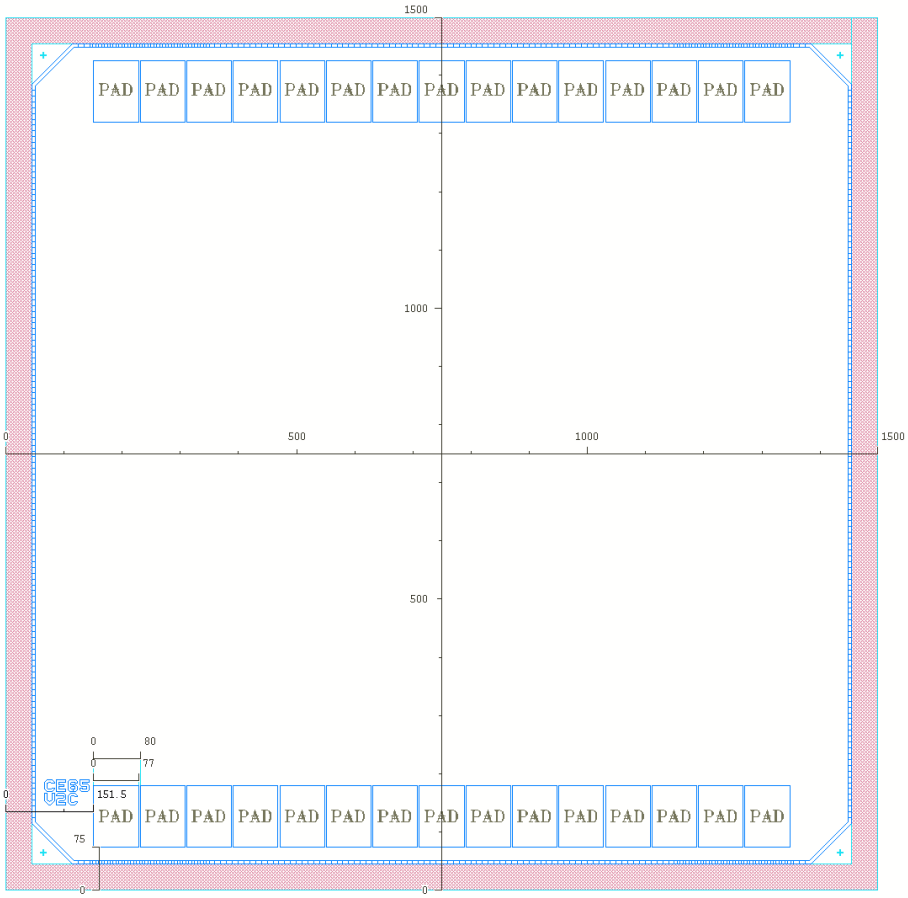

Figure 1.1. Chips dimensions in µm and common part of the logo. The name has common part ”CE65V2C” and variable part after, not shown here and described in chapter 3.2.

Due to extra functionality of CE65V2 the pad destinations and names are different from those of CE65V1. The pads are placed symmetrically on top and bottom sides of the chip.

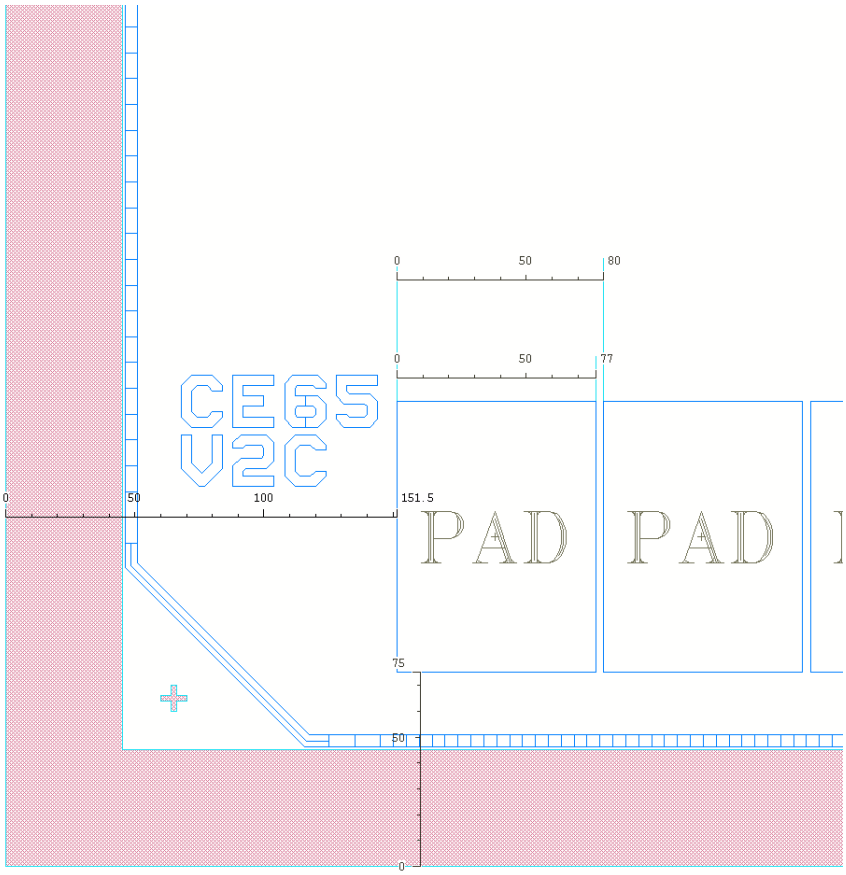

Figure 1.2. Bottom pads placements. Placement period 80µm, top pads places symmetrically from top side.

1.2. Electrical specifications

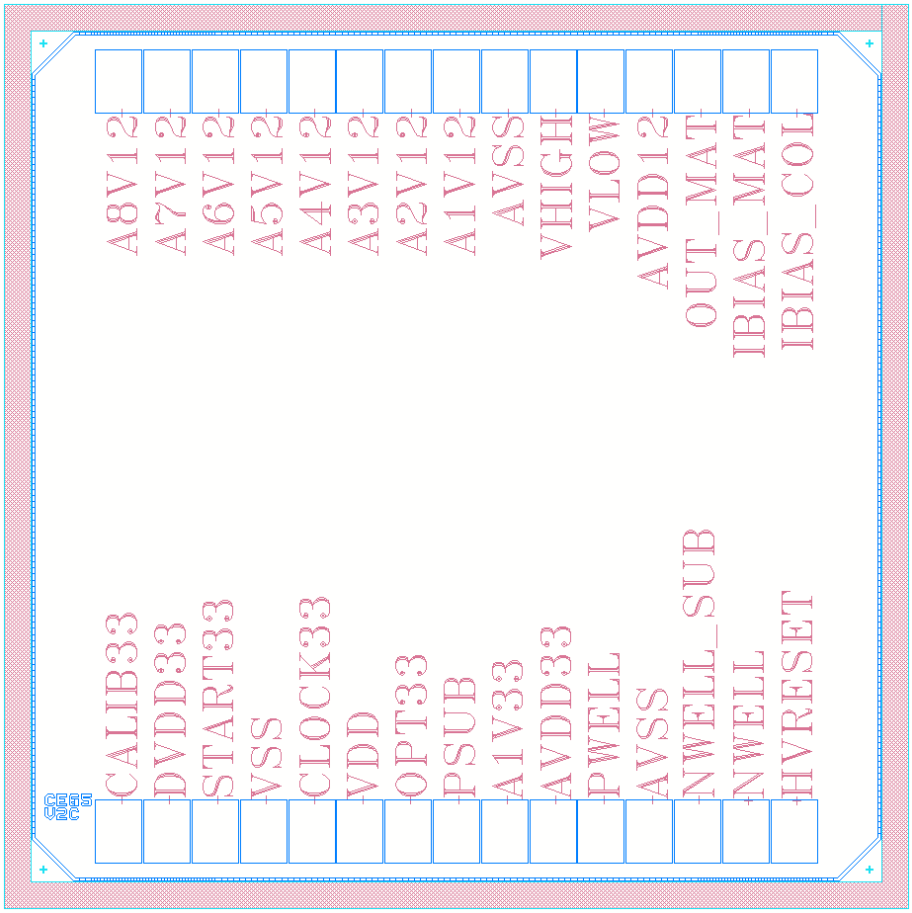

Figure 1.3. Pads: electrical connections.

The chip connections are shown in Fig. 1.3, the summary of operational conditions, nominal, maximal and minimal values are presented in Tab. 1.1. The chip has 7 power pads (0V, 1.2V, 3.3 V), 4 digital inputs pads (3.3V CMOS), 6 voltage bias pads, 3 current bias pads, one unprotected HV pad and analogue output pad. There are 8 analogue bias pads which were reserved for future use. The operating clock frequency can be up to 40 MHz.

Table 1.1. Chip connections: electrical values. Detailed description of current biasing with equivalent circuits is in section 2.5.

N	Pad name	Direction/power	Nominal, V	Min, V	Max, V	Purpose
1	CALIB33	digital input	X	0	3.3	digital control
2	DVDD33	power	3.3	0	3.3	IO power
3	START33	digital input	X	0	3.3	Digital control
4	VSS	power	0	0	1.2	digital core and IO
5	CLOCK33	digital input	X	0	3.3	digital control
6	VDD	power	1.2	0	1.2	digital core
7	OPT33	digital input	X	0	3.3	digital control
8	PSUB	bias	0	-4	0	p substrate bias
9	A1V33	current source	20µA	<100µA	3.3	bias current
10	AVDD33	power	3.3	0	3.3	analogue 3.3V
11	PWELL	bias	0	-4	0	pixels pwell bias
12	AVSS	power	0	0	3.3	analogue core
13	NWELL_SUB	bias	1.2	0	1.2	nwell bias
14	NWELL	bias	1.2	0	1.2	nwell bias
15	HVRESET	HV, unprotected	10	0	20	HV bias
16	IBIAS_COL	current sink	186µA	0	<500µA	bias current
17	IBIAS_MAT	current sink	3mA	0	<10mA	bias current
18	OUT_MAT	analogue out	∼400mV	<10mA to AVSS	1.2	output
19	AVDD12	power	1.2	0	1.2	analogue 1.2V
20	VLOW	bias	0.8	0	1.2	calibration voltage
21	VHIGH	bias	1.2	0	1.2	calibration voltage
22	AVSS	power	0	0	3.3	analogue ground
23	A1V12	bias	X	0	1.2	NC, future use
24	A2V12	bias	X	0	1.2	NC, future use
25	A3V12	bias	X	0	1.2	NC, future use
26	A4V12	bias	X	0	1.2	NC, future use
27	A5V12	bias	X	0	1.2	NC, future use
28	A6V12	bias	X	0	1.2	NC, future use
29	A7V12	bias	X	0	1.2	NC, future use
30	A8V12	bias	X	0	1.2	NC, future use

2. User Guide

2.1. Introduction and overview of chip architecture

The chip was designed in order to explore charge collection and electrical properties of the collection nodes. It has matrix of 1152 pixels (Fig. 2.1), organized in 48 columns and 24 rows. Each pixel has charge collecting node, composed of nwell/substrate diode, which is biased by HV via forward diode. There is voltage amplifier and buffer in each pixel. The schematic is similar to the improved gain NMOS amplifier, presented at [2]. Output of each pixel buffer is multiplexed by digital control to one analogue buffered chip output, that is in similar way to previous CE65V1 chip [1].

The charge collecting nodes, except those for the last column, are connected to amplifier and buffer via coupling capacitance 7.5‡ fF. The charge injection to pixels can be done by small capacitance (220‡ aF) with digital pulse "CALIB33", positive edge makes negative injection, same polarity in response from particle. The amplifier is inverting, and resulting output pulse has positive polarity.

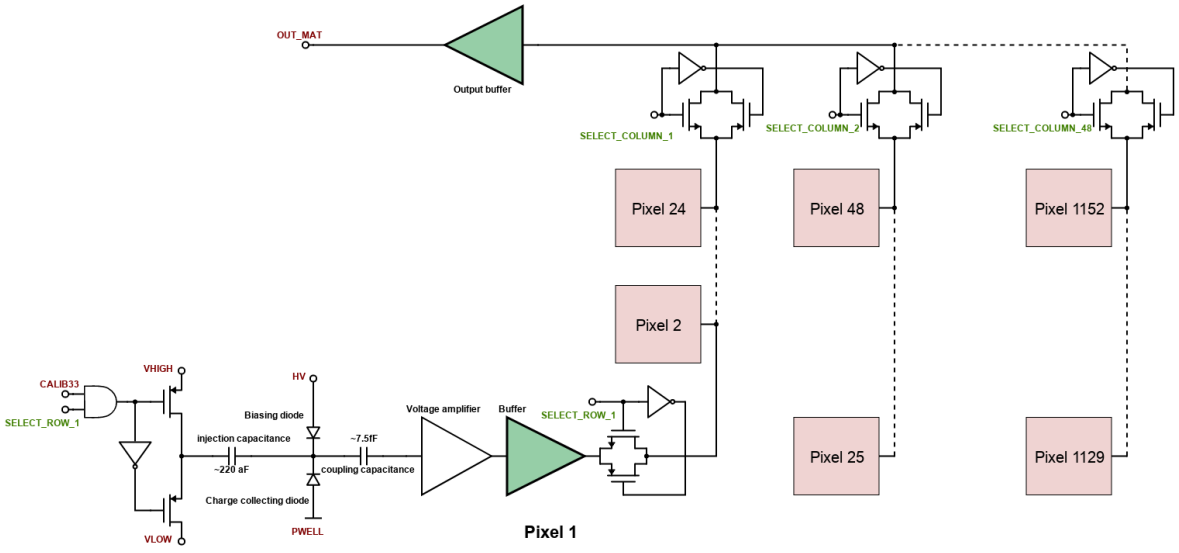

Figure 2.1. Simplified chip schematics. Red: external connections; green: internally generated.

‡Layout extracted value

In the last column the charge collecting diode connected only to the biasing diode, therefore the signal can be generated only by CALIB33 pulse.

In the first half of pixels of the last column (Fig. 2.2) the signal is generated via injection capacitance, while charge collecting diode is disconnected, hence it is possible to measure the sum of parasitic and amplifier input capacitance.

In the second half of pixels of the last column (Fig. 2.3), the injection capacitance is shorted to coupling capacitance 7.5 fF, hence it will be possible to calibrate the whole readout chain by knowing precisely the voltage of injection step. The combinations of calibration measurements with response from ^{55}Fe source will allow for precise measurements of charge collecting diode capacitance, leakage current, injection and coupling capacitance.

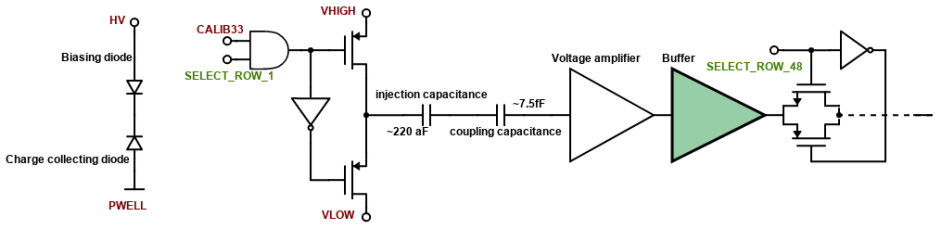

Figure 2.2. Column 48, first half (pixels 1129 to 1140), pixel schematics.

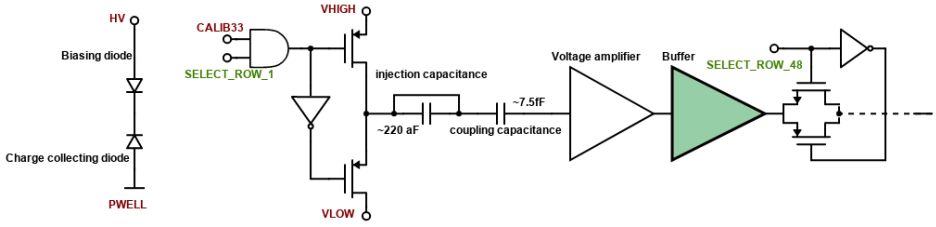

Figure 2.3. Column 48, second half (pixels 1141 to 1152), pixel schematics.

The measurements with ^{55}Fe source or m.i.p particle are performed in the rolling shutter readout way, same way as for CE65V1 chip[1]. The charge developed by particle is stored at collecting diode capacitance, the voltage difference before and after particle arrival gives the signal proportional to the charge collected by pixel (Fig. 2.4).

With digital control pulses START33 (Fig. 2.6) the first pixel is connected to the chip output and can be digitized. With digital pulse CLOCK33 one can multiplex the signal values from subsequent pixels to the chip output. That readout mode described in details in subsection 2.3.1. The response from particles can be read out for first 47 columns as last column reserved for precise calibration purposes. After 1152 clock pulses completed, which makes one readout frame, the first pixel is connected again and scan will continue in a loop with further clock pulses. The

START33 is asynchronous and has priority, which connects the first pixel to chip output. Therefore, if needed, any fraction of pixels can be scanned in a loop, however by this way it is not possible to systematically read fraction of pixels in column for a given number of columns.

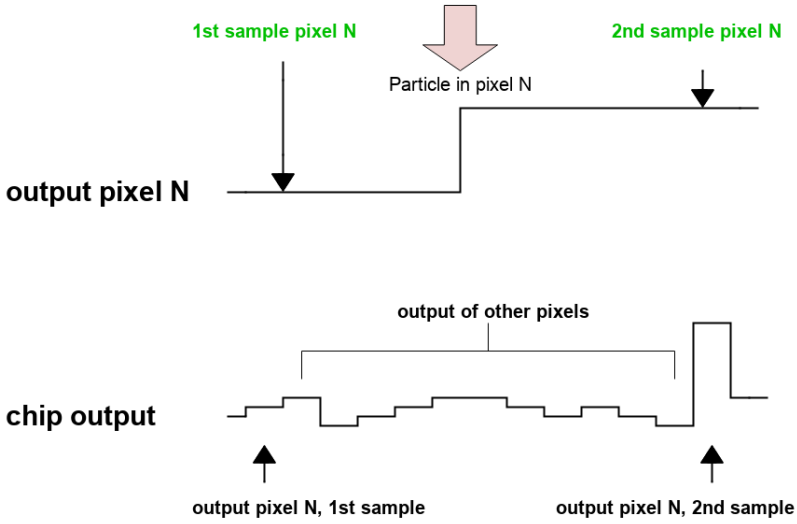

Figure 2.4. Waveforms for rolling shutter readout; top: internal output for single pixel, signal after particle, bottom: multiplexing pixel outputs to chip output.

Optional digital control OPT33 modifies the action of START33 and is used to limit the readout matrix to window mode (Fig. 2.7). Normally, when OPT33 set to high level, START33 connects pixel of first column and first row to the output, independently what was the column and row before. When it is set to logic 0, the START33 connects the pixel of first row and next column. So with subsequent clock pulses the pixel in that column will be multiplexed, even the previous column was not completely readout. Combining START33 and OPT33, and providing clock (CLOCK33) one can multiplex pixels from arbitrary rectangular window, starting from first pixel. This mode, described in details in subsection 2.3.2, should be used, if the leakage current is increased, and the charge stored in pixel diode can not be maintained for long time. Therefore, window mode can allow for evaluation of charge sharing between pixels in case the readout of full size matrix can not provide reliable data.

2.2. Biasing

For minimal chip operation, one need to set three current biases and three voltage biases, in order to inject calibration charge two more voltage biases are required. The estimated from simulation biasing values are presented in Tab. 2.1. The PSUB[‡] voltage should not be smaller then -4 Volts, and the current should be checked at lowest values. The voltage for NWELL and NWELL_SUB should be applied by resistor 10 kΩ in order to avoid excessive current due to possible punch-through to 1.2V.

During the tests bias values may be changed in order to optimize the resulting data quality. The currents may need to be increased in order to ensure good signal quality at higher clock frequencies (up to 40 MHz). The higher the currents, the large the voltage non-uniformity, so in order to optimize uniformity of the baseline the currents can be reduced. However in that case clock frequency has to be reduced.

Although the estimated values presented in Tab. 2.1 can be tried first, it is generally recommended to verify that the output waveform quality and the ADC sampling time position provide reliable data, and the biasing optimization should help to achieve good results.

Table 2.1. Initial recommended values for biasing, they may subject to change after tests

PAD	Destination	Initial recommended values	scaling to internal circuit	Internal value	Comment
A1V33	current/source	20 μA	1/20	1 μA	pixel SF bias/3.3V domain
IBIAS_COL	current/sink	100 μA	1/4	25μA	second SF bias/1.2V domain
IBIAS_MAT	current/sink	3 mA	1	3mA	output SF bias/1.2V domain
NWELL_SUB	voltage	1.2 V	1	1.2 V	connect via resistor 10 kΩ
NWELL	voltage	1.2 V	1	1.2 V	connect via resistor 10 kΩ
HVRESET	voltage	10 V	1	10 V	
PSUB	voltage	0 V	1	0 V	
VLOW	voltage	0.8 V	1	0.8 V	$>$ 0.4V, otherwise Q_{inj} not precise
VHIGH	voltage	1.2 V	1	1.2 V	Q_{inj} = (VHIGH-VLOW)*C_{inj}

In order to help designing the biasing schematics, the equivalent circuits for biasing currents and for analogue output are shown in Fig. 2.5. One can see that A1V33 required external current sink, while IBIAS_COL and IBIAS_MAT require current sources.

[‡]Negative voltage with respect to VSS

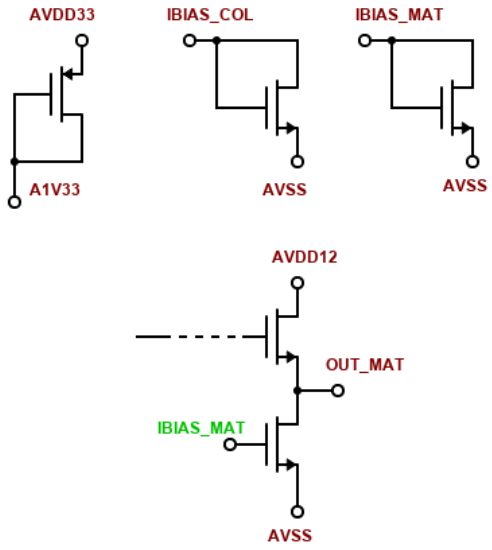

Figure 2.5. Equivalent circuits: top - for bias currents, bottom - chip output buffer.

2.3. Readout operation modes

2.3.1. Full matrix readout mode

This mode use to multiplex pixels in a sequence shown in Fig. 2.6 with CLOCK33 ans START33 pulses. Optional controlling OPT33 should be kept high. Only one START33 needed at the beginning, then after pixel 1152, the pixel 1 is connected and sequence continues in a loop. However not harmful to repeat START33 at the time of every 1st pixel. The sequence can be interrupted any time by START33: pixel 1 will be connected, then multiplexing goes through pixels until START33 is activated again. By this way one can readout a part of the matrix.

2.3.2. Windowed readout mode

In order to cope with increased leakage current and hence loose of the signal, one can define any window in matrix, starting from pixel 1. The OPT33 signal propagate the START33 and hence reset multiplexer to the first pixel. If OPT33 is low, the START33 resets the multiplexer to beginning (bottom pixels in matrix in Fig. 2.6) of next column. So every column read out only partially if START33 arrives before 24 clocks of CLOSK33. An example of 3x3 window readout is shown in Fig. 2.7.

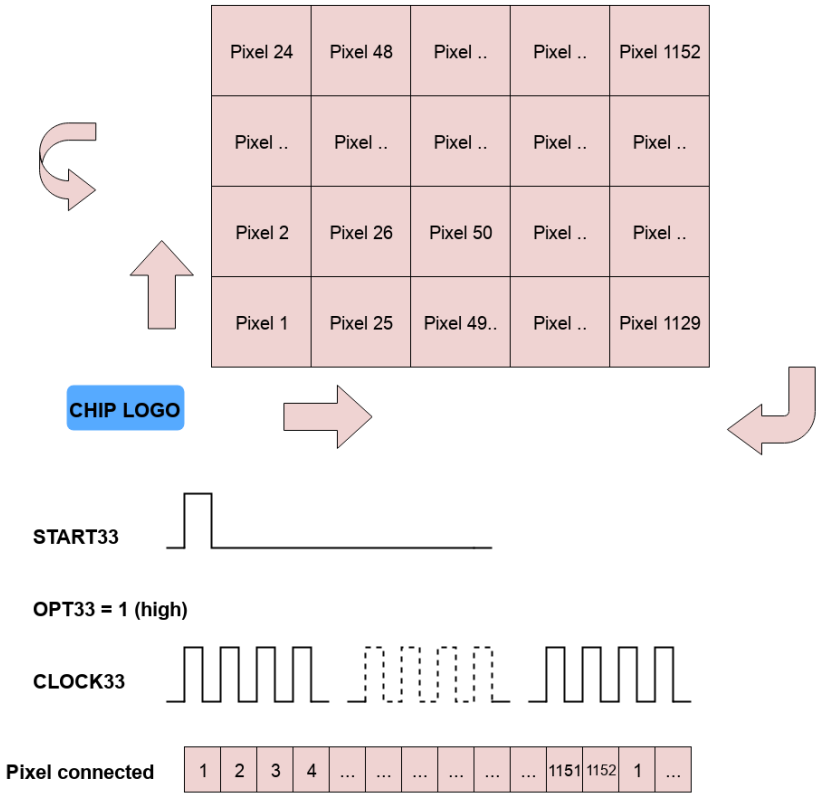

Figure 2.6. Rolling shutter readout mode: readout sequence, pixel order in matrix and related chip logo position are presented.

2.3.3. Electronic calibration

Electronic calibration is done by pulse CALIB33. The positive edge of CALIB33 will switch the input of calibration capacitance from VHIGH to VLOW voltage potentials, so charge collection diode will receive negative charge, i.e. similar polarity as from real particle.

One has to select pixel by using START33, OPT33 and CLOCK33 signals as described in 2.3.1 or 2.3.2. Then the charge can be injected and corresponding output signal can be measured, as shown in Fig. 2.8. One should note, that the calibration pulse is propagated to whole row to which the selected pixel belongs to. So best way is to select pixel for longer time with increased clock period and then calibrate pixels one by one as shown in Fig. 2.8.

2.3.4. Extra calibration features

For the last column, as it was described in 2.1, the only the electronic injection can be done, the way described in 2.3.3, as the charge collecting diode is completely disconnected.

For the pixels from 1129 to 1140 the injection is done via the injection capacitance to the AC

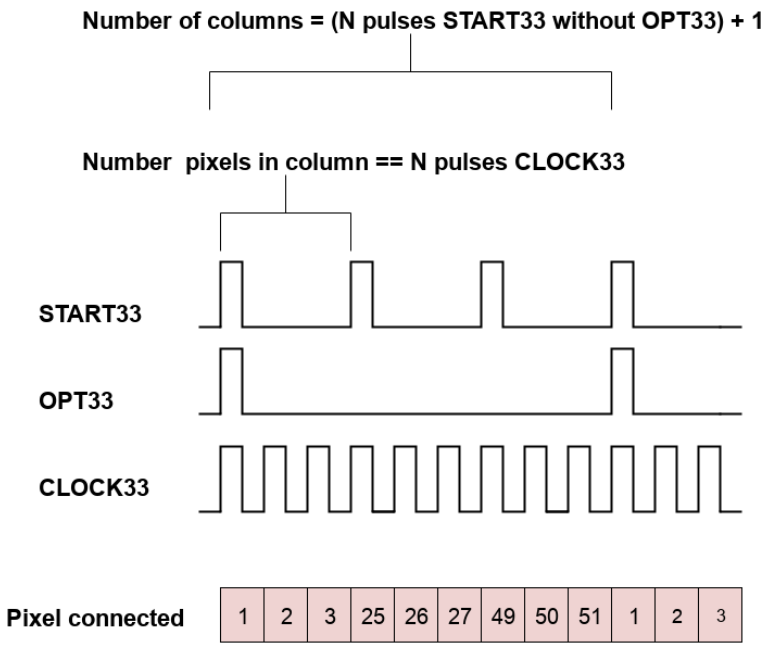

Figure 2.7. Windowed readout mode: in this example 3 x 3 pixels matrix is readout. The pixel number geomertical positions are in figure Fig. 2.6.

coupling capacitance connected to the amplifier input.

For the pixels from 1141 to 1152 the injection capacitance is shortened and injection pulse is applied directly to the AC coupling capacitance ad the to the input of the amplifier, hence one can calibrate the readout chain, knowing the injected pulse amplitude.

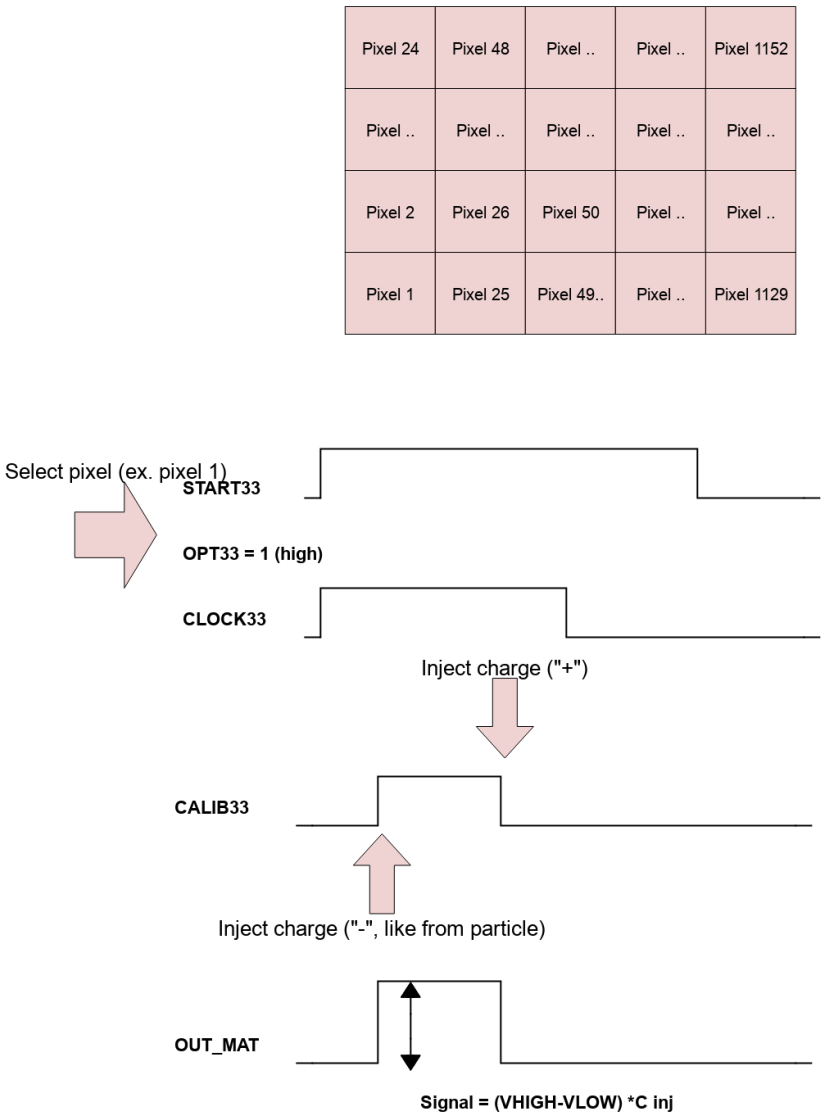

Figure 2.8. Calibration with electronically injected charge.

3. Chips variants reference guide

3.1. General description

The CE65V2 exist in 15 variants: 5 pixel/matrix geometry options each implemented in 3 technology options. Each variant can be distinguished by logo. The logo contains four lines of text, example in Fig. 3.1. The first line is common for all chips: " CE65". Second line has common part "V2C", acronym of second "V"ersion, exploration of"C"harge collecting properties. Technology option is encoded in last letter of the second line, there are tree options: "N"o option, "B"lanket and "G"ap. Third line is pitch size in µm, there are three pitches: 15µm, 18µm and "22p5µm" for 22.5µm. Fourth line contain either "SQ" or "HS" letters, for "SQ"uared or "H"exagonal "S"quared positioning of pixels in matrix.

The pitches of 18µm and 22.5µm squared design are identical to those in MOSS1 chip.

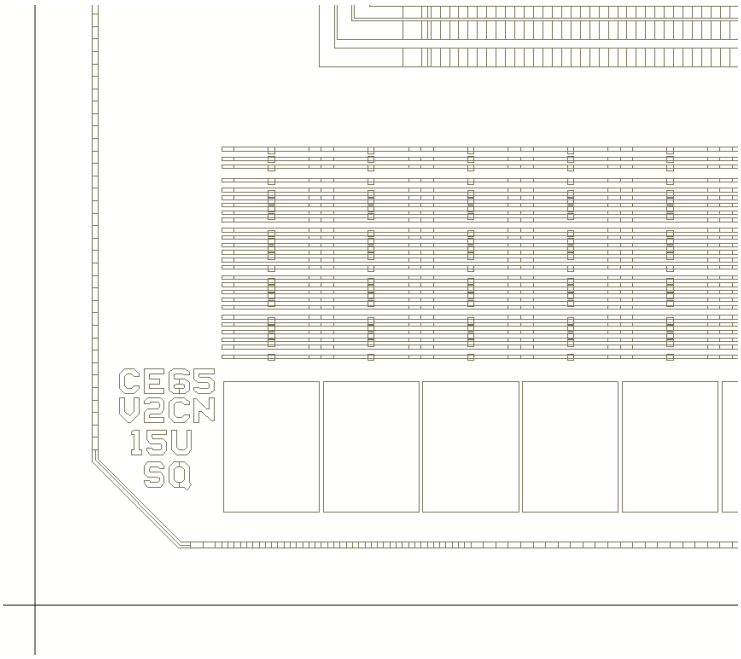

Figure 3.1. Example of chip logo: CE65V2 chip for "C"harge study, "N"o techno option, 15 µm pitch, "SQ"uared design.

3.2. Pixel variants

In the figures 3.2, 3.3 3.4, 3.5 3.6 the simplified matrix layout is presented. The position of first pixel with respect to the bottom left edge of the chip is shown, only first three rows and three columns are shown in the figures.

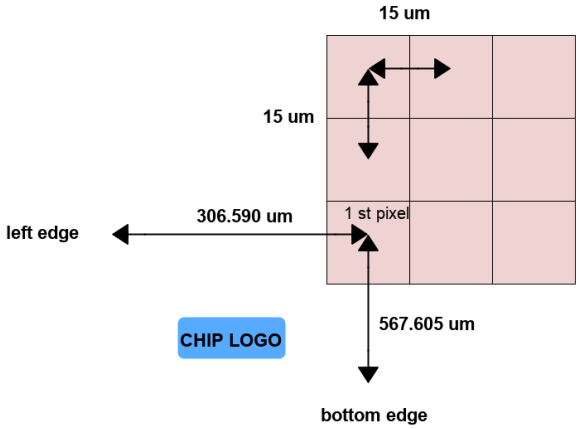

Figure 3.2. 15 µm pitch squared design.

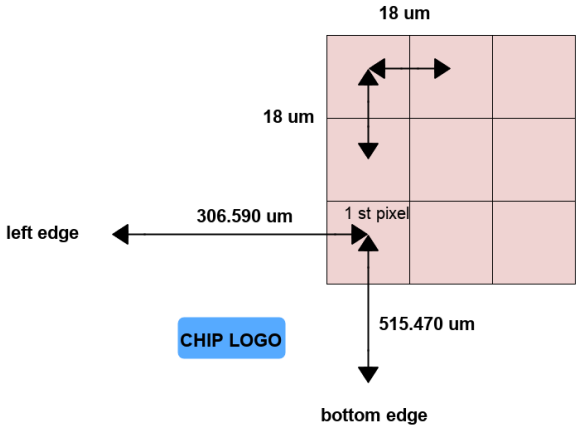

Figure 3.3. 18 µm pitch squared design.

3

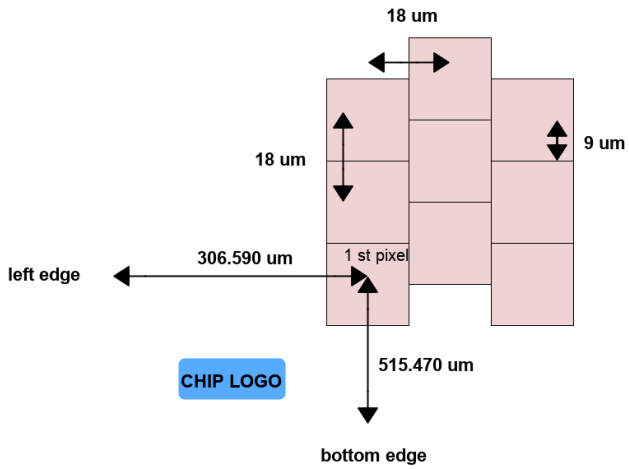

Figure 3.4. 18 μm pitch hex-squared design.

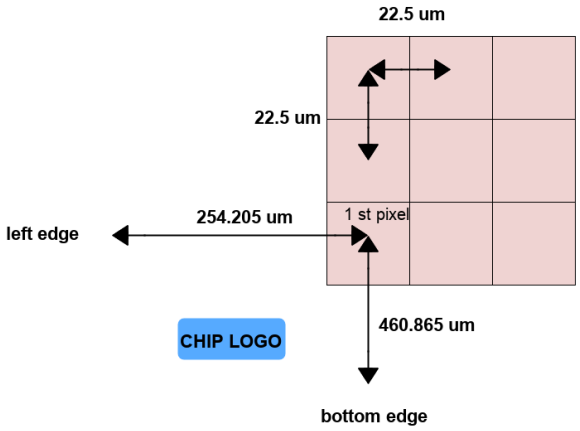

Figure 3.5. 22.5 μm pitch squared design.

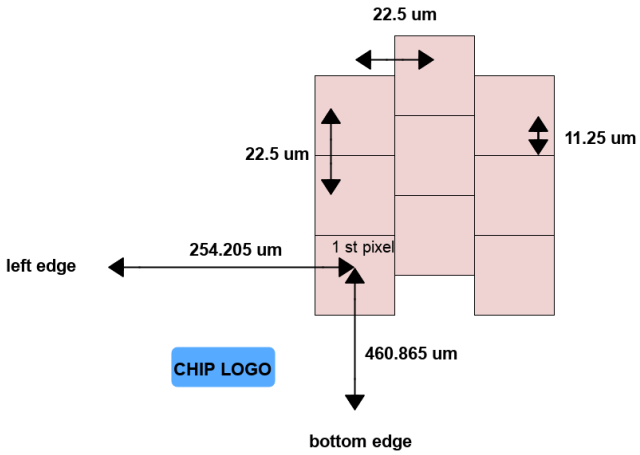

Figure 3.6. 22.5 μm pitch hex-squared design.

Bibliography

[1] CE65 (V1) manual at: "https://espace.cern.ch/ep-project-rnd-tpsco65/Shared Documents/MLR1/Datasheets/MLR1_CE65_datasheet_v1.1.pdf"

[2] A. Dorokhov, NMOS-based high gain amplifier for MAPS. VIth International meeting on front end electronics for high energy, nuclear and space applications, Perugia, Italy, 17- 20 May 2006

A. Simulations

This should be covered in a separate Application Note, as may contain details of technology, and also subject of change/modification and new requests during tests.