Small scale test chips in65 nm technology

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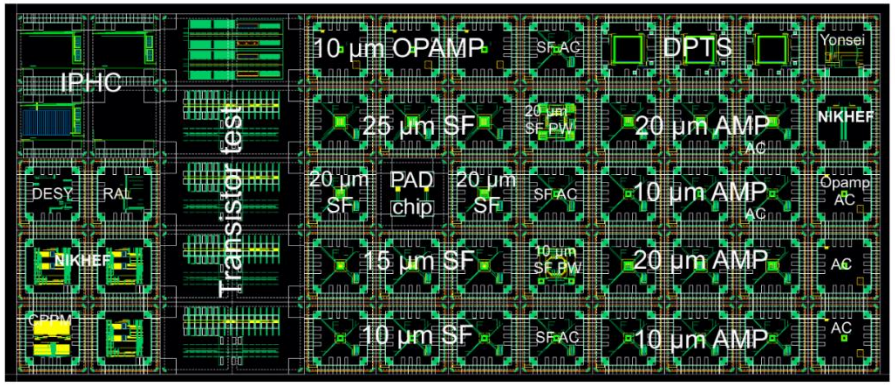
on behalf of C4Pi and PICSEL,
IPHC, Strasbourg
17/01/2023

Contributions of C4Pi and PICSEL to 65nm technology R&D



- IPHC: rolling shutter larger matrices, DESY: pixel test structure (using charge amplifier with Krummenacher feedback, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures
- Transistor test structures, analog pixel (4x4 matrix) test matrices in several versions (in collaboration with IPHC with special amplifier), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.

mlr1 run, W.Snoeys, WP1.2 meeting, 12/2020

2020 ->

1. CE65V1 ("C"hip "E"xploratoire): exploratory chip using matrix of pixels(64x32 and 48x32), output is multiplexed to one analogue channel (matrix rolling shutter readout mode):
   - 4 chips CE65V1: A,B,C,D -> Different pitch (15 and 25 um), different sensing node flavor
   - DAC prototypes
2. APTS (AA) : design in-pixel amplifier for 12 chips APTS (analogue pixel test structure: small matrix 4x4 with parallel readout designed by CERN)
3. Chip carrier PCB design and production
4. Tests and analysis

ER1 submission: small chips

Received, still digesting

- H2M
- 3 test chips from NIKHEF
- 1 test chip from RAL
- 2 test chips from DESY
- 15 test chip from IPHC (CE65v2)
- 2 SEU test chips from INFN Bari (final)
- 1 test chip from SLAC
- 1 test chip from CPPM
- Ported Transistor Test Structures, APTS SF and OA, and DPTS

20220601 | EP R&D WP1.2 Report | Monolithic Sensor Development 5

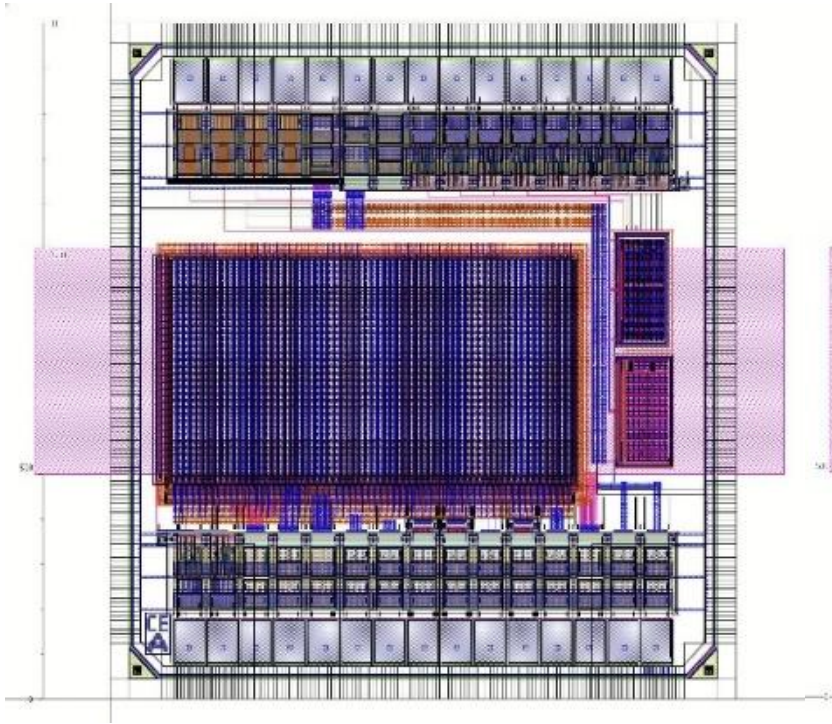
ER1 run, W.Snoeys, WP1.2 meeting, 06/2022

2022 ->

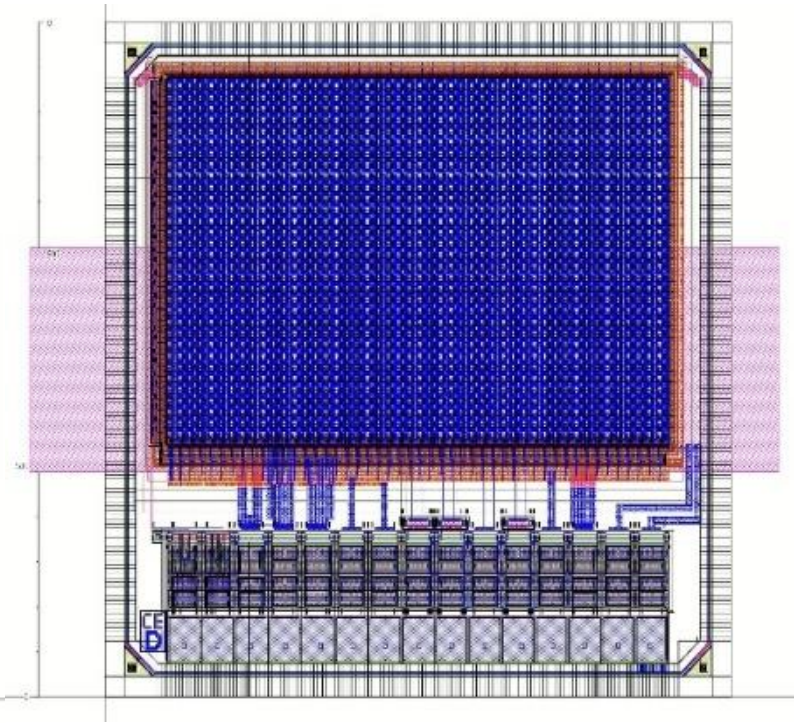
1. CE65V2 second version with enhanced testing capability: matrix of pixels(48x24), output is multiplexed to one analogue channel -> 15 chips CE65V2:
   - Different pitch (15, 18, 22.5 um)
   - Square or (nearly) hexagonal matrix layouts
   - Different sensing node flavor
2. 3 chips CE65 from 2020 (A,B,C) ported to new metal stack
3. Contributions to MOSS and MOST (stitched sensors)
4. Expected: Chip carrier design and production
5. Expected: Tests..

Family of CE65_xx (1.5mm x 1.5mm) chips

2020/21

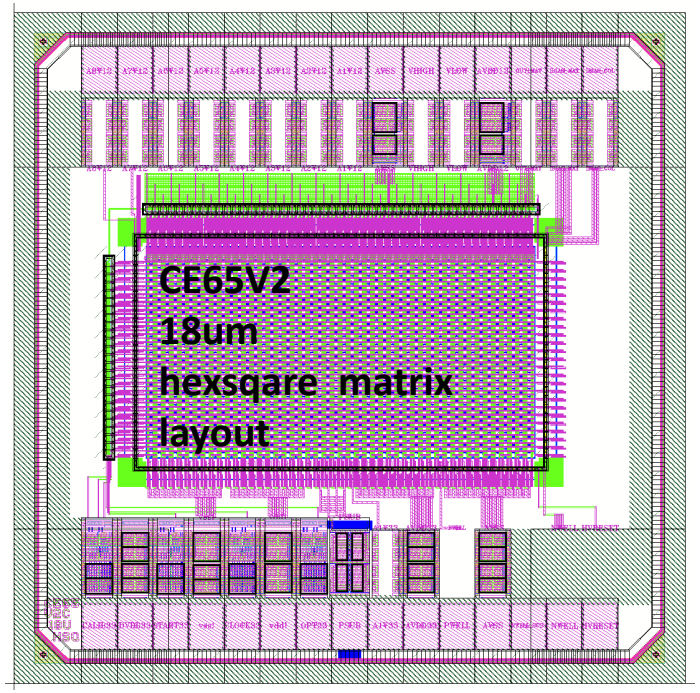


CE65V1 (A,B,C flavor, all 15 um pitch)



CE65V1 (D, 25um pitch)

2022



- ✓ In total 4 chips: each matrix has tree pixel amplifier/buffer types (ACampl, DCampl, SF) + DACs in some chips -> first try with 65nm…

- ✓ In total 15 chips with different pitch, matrix layouts and pixel flavor, each matrix has only one AC ampl type

CE65V2 in ER1

CE65V2_xx (1.5mm x 1.5mm), 15 chips in process of submission in ER1 run

Versatile* exploratory chip using matrix of pixels (48 col x 24 row) output is multiplexed to one analogue channel (matrix rolling shutter readout mode, can be read completely or in arbitrary size "window" mode):

- ✓ share common pads structure, carrier and proxy boards
- ✓ 4 power domains: 3.3V analogue, 1.2 analogue, 3.3 digital, 1.2 digital
- ✓ 3.3 analog and 1.2 analog share same ground AVSS
- ✓ 3.3 digital and 1.2 digital share same ground DVSS
- ✓ one column reserved for precise charge collecting diode measurements

Power:

- digital (3.3V IO/1.2V CORE): DVDD33, DVDD12,DVSS
- analogue (3.3V): AVDD33, AVSS
- analogue (1.2V): AVDD12, AVSS

2 digital input pulses (3.3V): clock, start, calib, opt

5 unprotected pads: HVRESET, NWELL ,NWELL_SUB, PWELL, PSUB

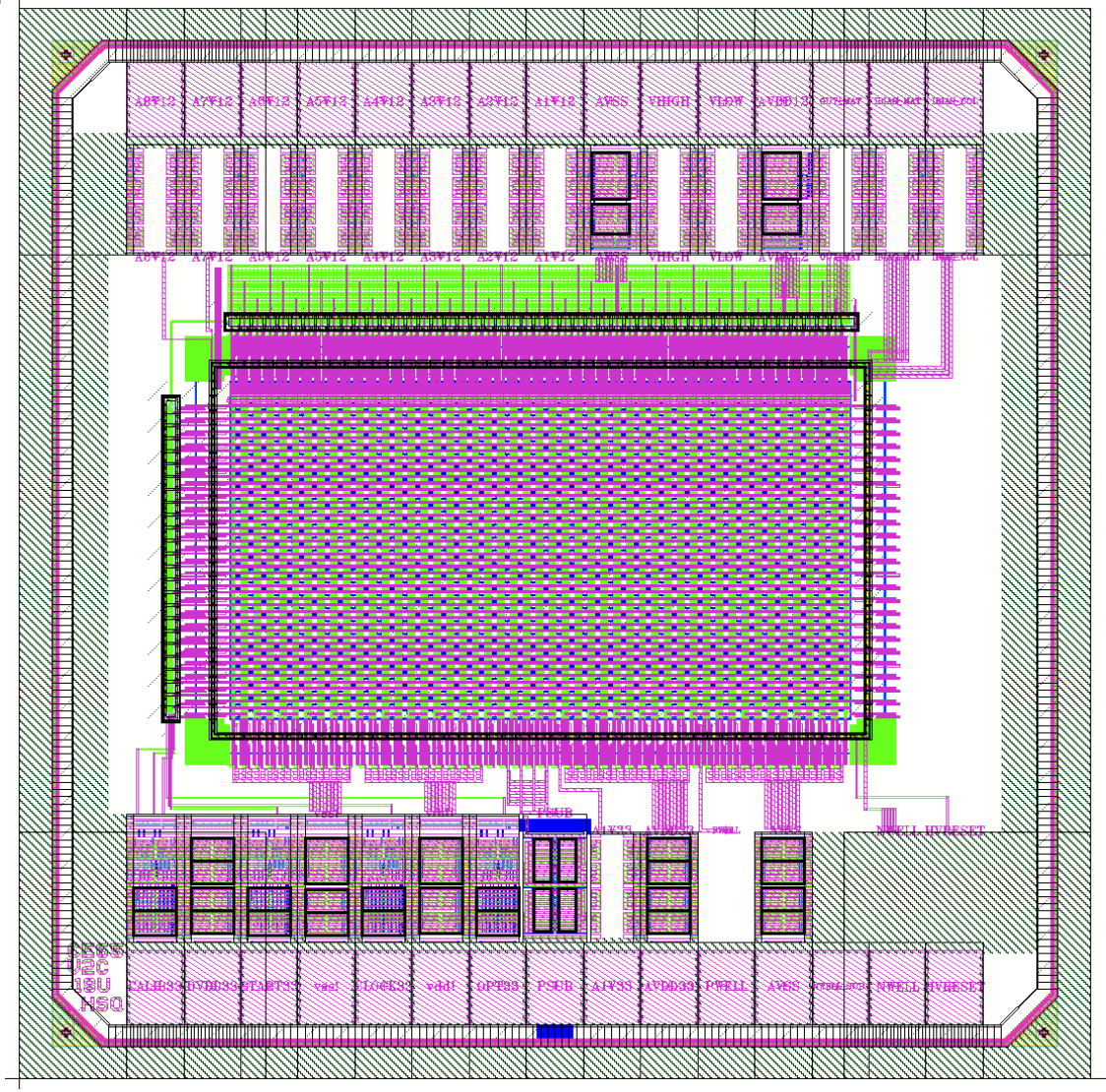
Output is in 1.2V analogue domain

2 calibration voltages: VHIGH, VLOW

2 biases for output buffer

9 biases for pixel front-end:

- 8 X 1.2 analogue biases (reserved for future use for more complex FE)
- 1 x 3.3 analogue biases

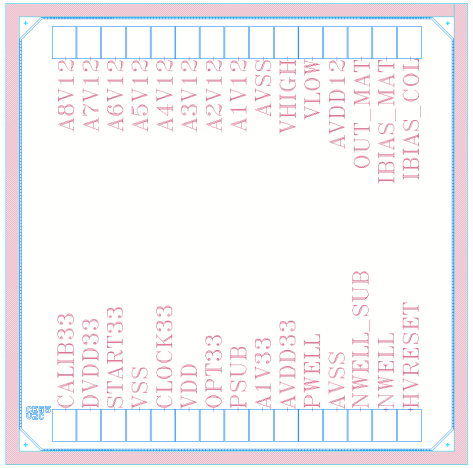


(*) instead of pixel can be any small structure for tests

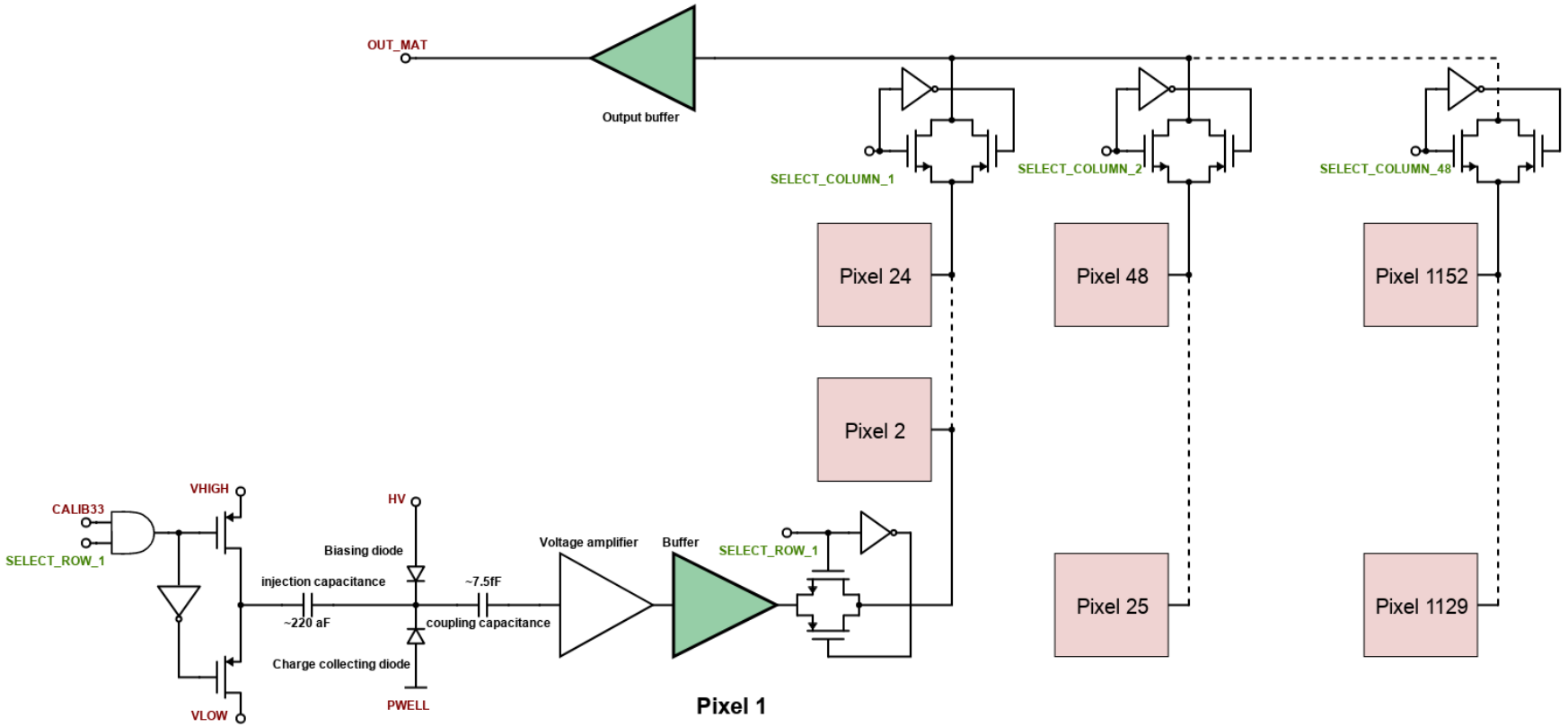
15 chips of CE65V2 in ER1

Modification	Purpose	5 Basic chips with pitch/geometry, um	Comment	Total No of chips	status
CE65V2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (AC pixel from CE65V1 is implemented)	15, 18, 22.5, 18_{hexsq}, 22.5_{hexsq}	For lab and beam test: charge collection, leakage, noise, node techno, optimization	5 basic chips x 3 techno flavors: 1) no n-implant 2) Blanket n-implant 3) n-implant with gaps)	Submitted

CE65V2C conceptual design



CE65V2C

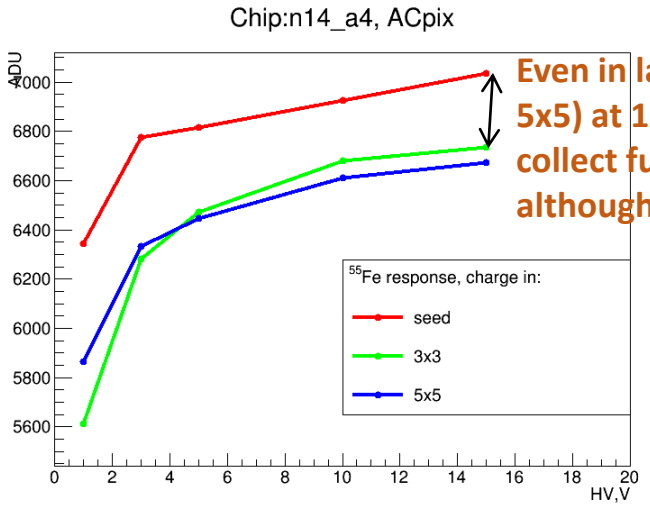


Versatile chip: in this version pixels are multiplexed to analogue output, but instead of pixel can be any block to test it systematically

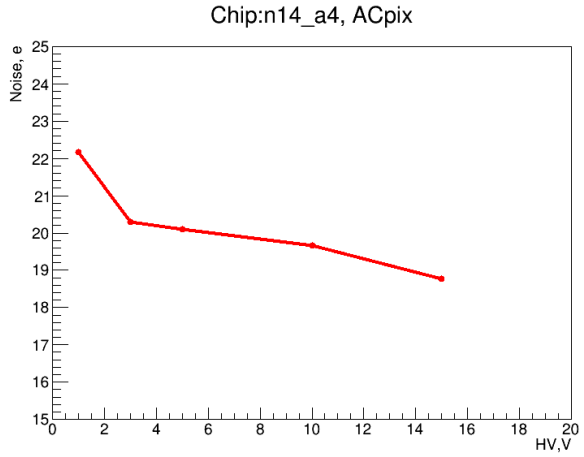
Recall some results from previous CE65

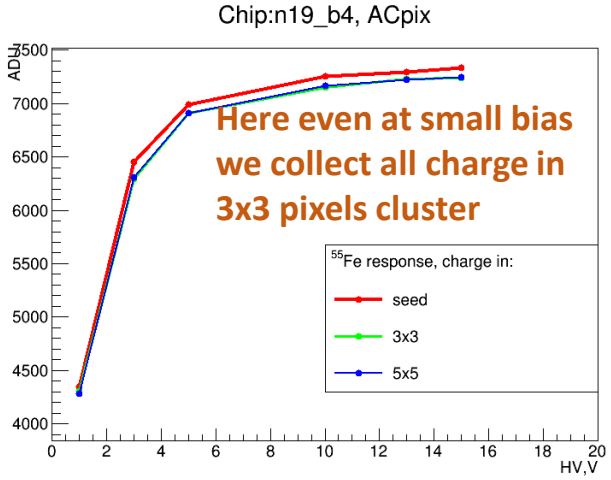
Lab tests: standard (a4) vs modified (b4) diode charge collection efficiency for AC pixel, measured with Fe55

Standard, split4



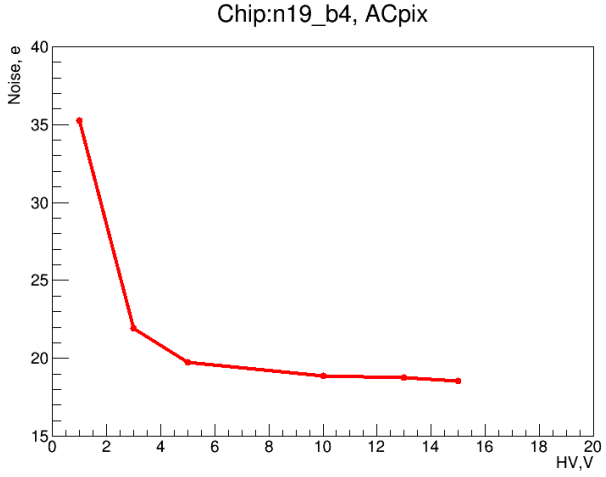
Even in large cluster (up to 5x5) at 15V we do not collect full charge, although still up to 95%





Here even at small bias we collect all charge in 3x3 pixels cluster

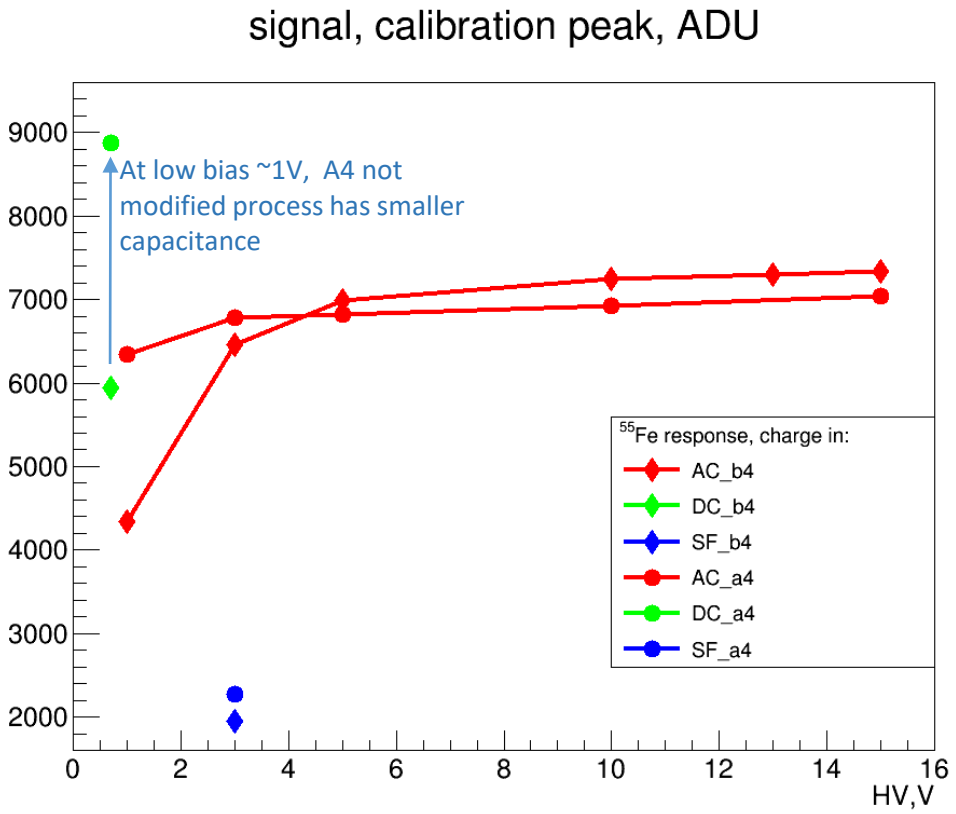
Modified (gaps in n- layer), split4

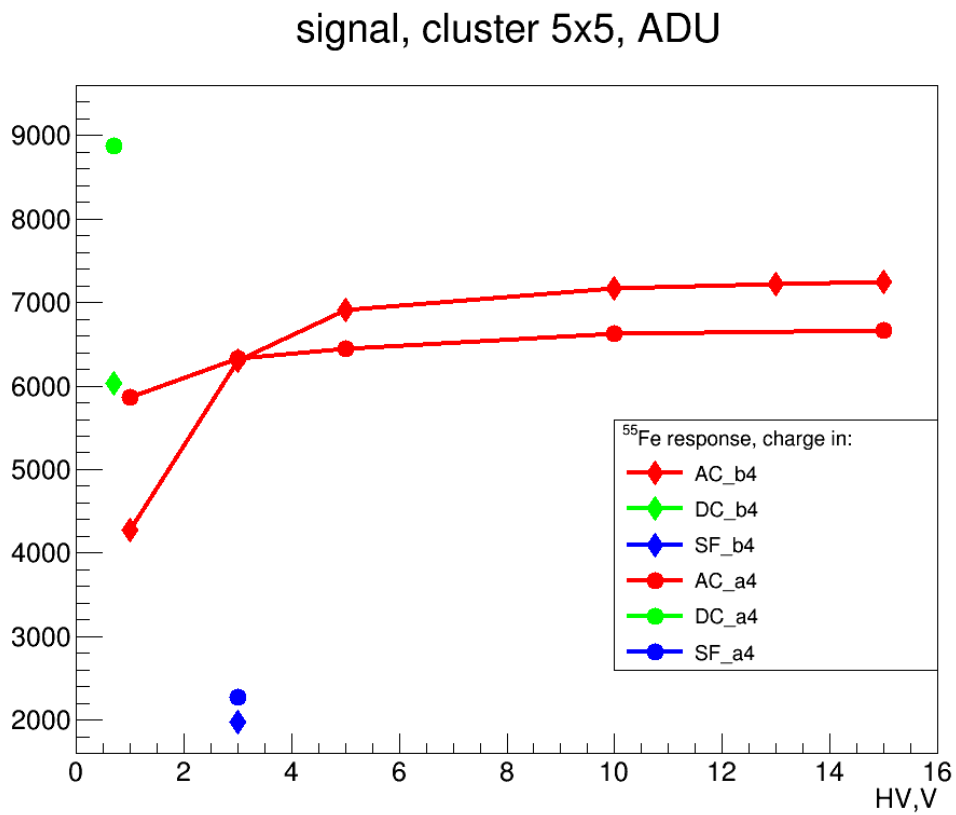


Observations

- modified diode has better collection efficiency: even at small voltages, charge localized in one seed pixel
- ENC is comparable, although at low voltage standard diode has smaller ENC -> related to diode capacitance increase due to depletion -> next slide

Lab tests: charge collection efficiency standard (a4) vs modified (b4) diode : AC, DC and SF sub-matrixes, measured with Fe55

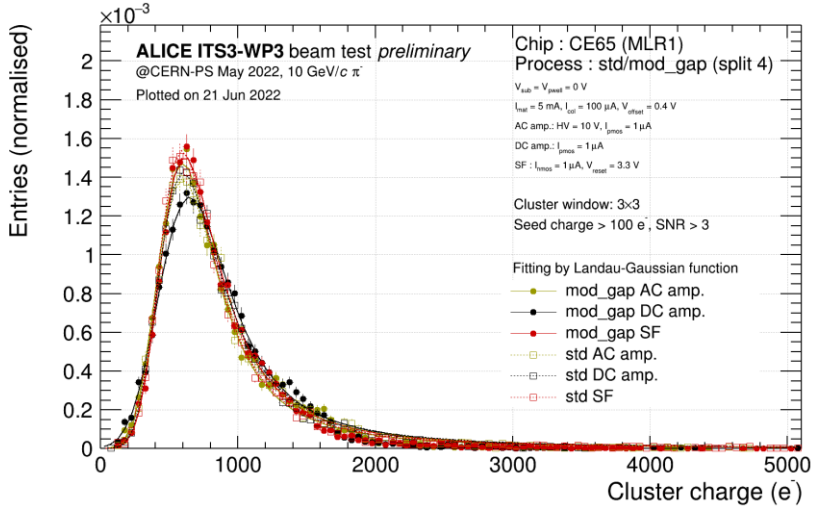




Observations:

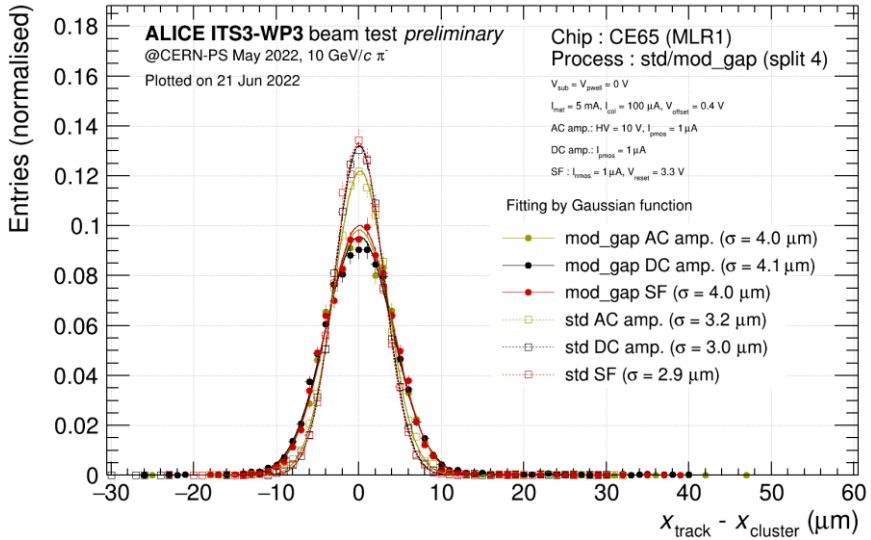
- Depletion of standard diode is easier and starts at ~1V
- Extra parasitic capacitance for AC diode is significant ~x2 of diode capacitance
- At > 3 V bias voltage, both standard and modified diodes are depleted
- Amplifier increases the signal by factor of ~3

Beam tests



- Seed pixel identified with charge > 100 e- & SNR>3
- All pixels within 3x3 range associated to cluster
- Only clusters associated with tracks & away from sub-matrix edge

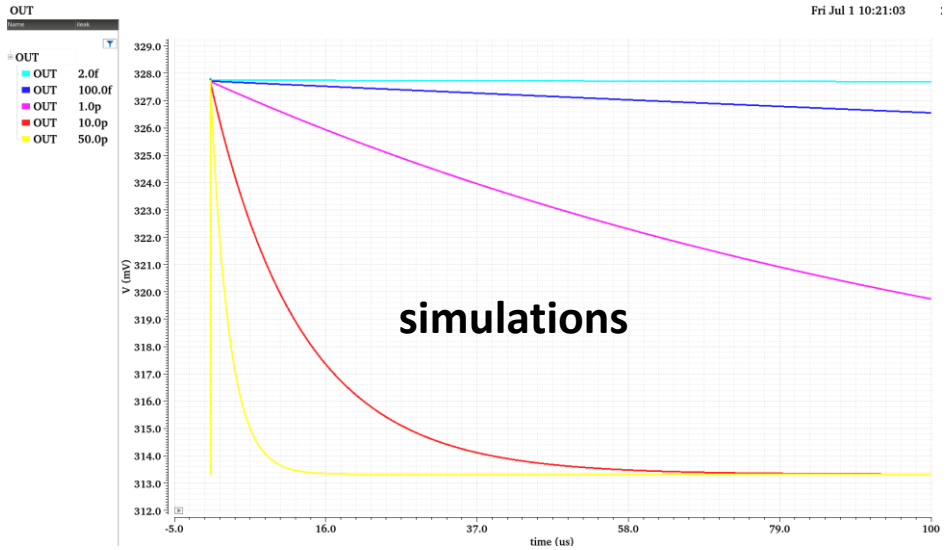
1. Collected charge in cluster is independent of diode modification, compatible with Landau*Gaussian with ENC ~15 e-
2. Thickness of sensitive volume ~11 µm



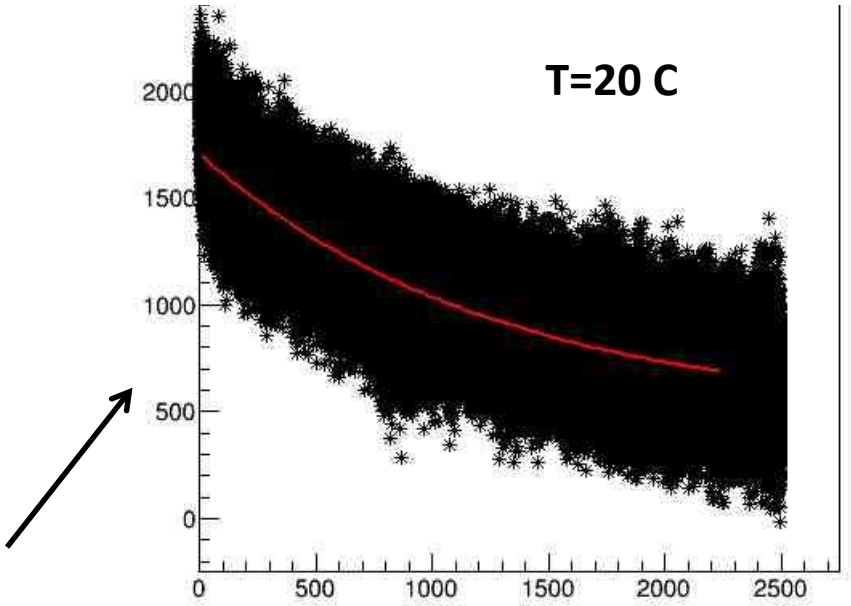
Residual decreased by ~1 µm for standard diode -> coherent with Fe55 tests: larger spread and hence cluster size lead to better spatial resolution

Leakage current

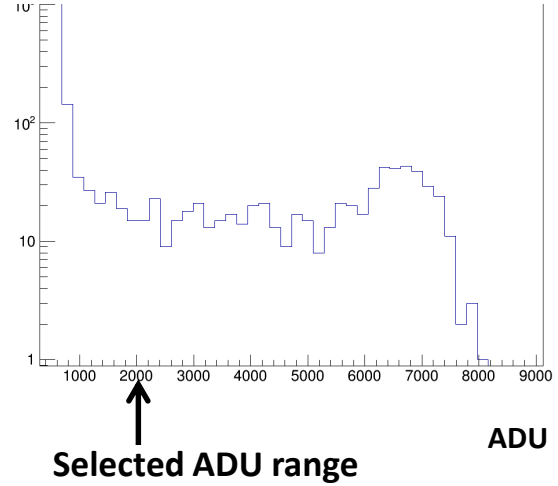
Waveforms at different leakage currents: 2fA, 100fA, 1pA, 10pA, 50pA



Superimposed one pixel waveforms, sample-to-sample noise is significant, so fit all point



Example of seed pixel, 1e15 Neq/cm2, 10 pixels, T=6C



Measurements (at stabilized T=20C):

1) Select pixel
2) Record selected 100 pulses from Fe55 with amplitudes in range 1800-2200 ADU, to be sure there are no saturation in readout, also to have small amplitudes (linear response)
3) Fit with exp + baseline and calculate leakage using layout extracted input capacitance (3.8 fF for AC and 2.5fF for SF pixels)
4) Repeat over pixels (can be very long ~1 day for matrix)

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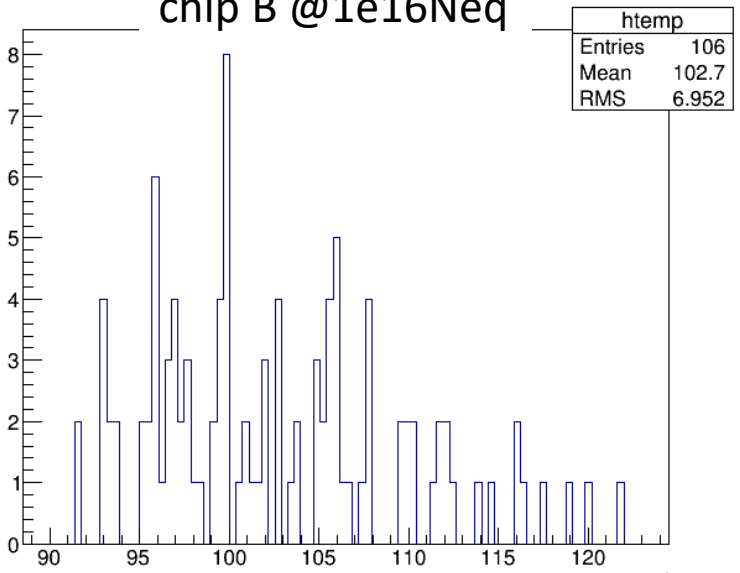
Leakage current results at T=20C

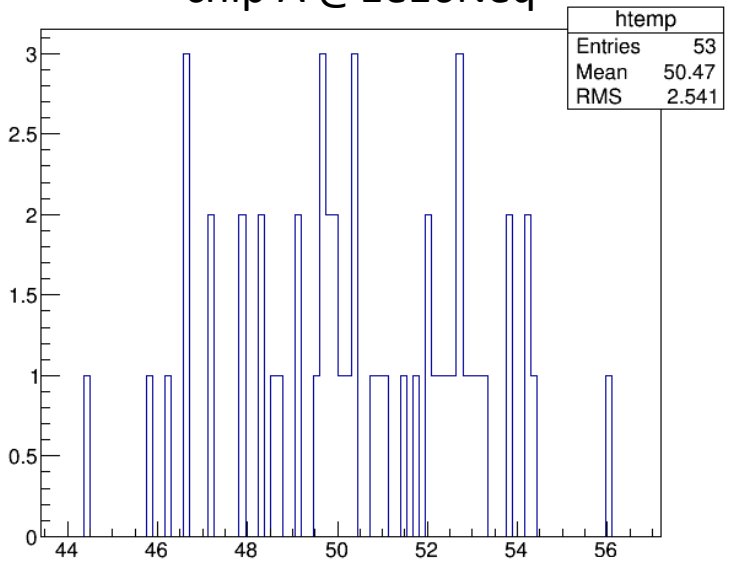
1. After 500Mrad:
   - chip B ~ 0.45 pA /pixel, peak-to-peak 0.4pA to 0.5pA
2. After 1e15Neq:
   - chip B (modified, with gaps) 22 pA /pixel, 18pA to 28pA peak-to-peak
   - chip A twice smaller, 11pA /pixel, 9pA to 14pA peak-to peak
3. After 1e16Neq:
   - chip B (modified, with gaps) 103 pA /pixel, 91 pA to 122 pA peak-to-peak
   - chip A twice smaller, 51pA /pixel, 44pA to 56pA peak-to peak

chip B @1e16Neq



pA /pixel

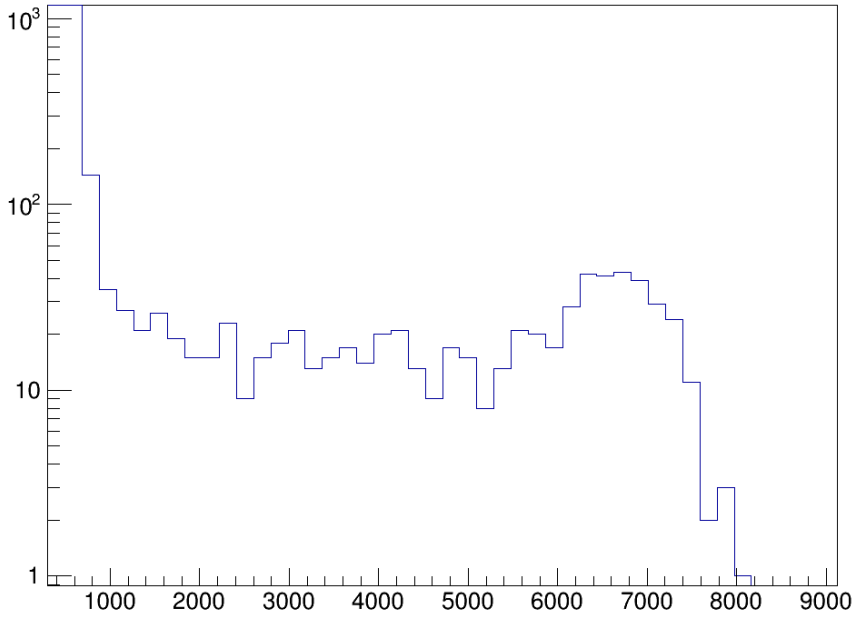
chip A @1e16Neq



pA /pixel

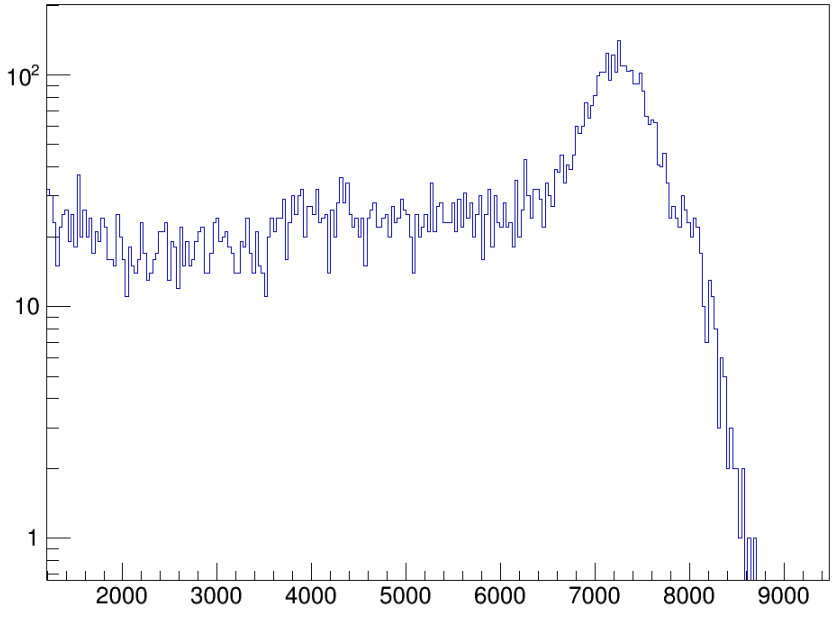
Irradiated chips, charge collection, calibration peak Fe55

Seed pixel, 1e15 Neq/cm2, 10 pixels, T=6C



ADU

Seed pixel, Non- Irradiated



ADU

At low temperature and taking only 10 pixels to speed up the readout we mitigate the effect of not complete signal due to specific readout problem and one can conclude:

The calibration peak seems to be not changed after irradiation up to 1e15Neq for these tests, for 1e16Neq seems to be very difficult to measure due to rapid discharge

Conclusions and perspectives

Conclusions for CE65V1:

- Served to get several results from matrix of pixels:
  - ✓ expected charge collection for standard and modified diode, capacitance 2-4fF
  - ✓ sensitive volume thickness ~11 um, and can be depleted > 3V
  - ✓ work after irradiation to 1e15 Neq, leakage <20 pA/pix (however difficult to readout)
- DAC tested and worked
- Still to do (irradiations at 1e13Neq, 1e14Neq, RTS)

To do in CE65V2: R&D for charge collecting node optimization for large stitched chips (MOSS)

- Charge collection properties:
  - ✓ Clusters, charge sharing
  - ✓ Spatial resolution, multiplicity
  - ✓ Efficiency
- More precise electrical properties:
  - ✓ Leakage current , RTS
  - ✓ Depletion, capacitance

Next CE65V3xxx with possible sub-versions

✓ **complementary study for ITS3**
which can not be all done in large scale sensors and not included in other small scale chips:

- Include/repeat similar program as for CE65V2: matrix layout geometry, pitch size variation
- Charge collecting diode size optimization: RTS, signal, efficiency
- Front end circuit: versions, optimizations, new ideas
- Digital cells optimization: leakage current evaluation, test different ideas

<= Andrei
+ Corentin (from CERN)

✓ **R&D beyond ITS3, paving new ideas for ALICE3**

- Additional small test structure of asynchronous architecture <= Jean's thesis with Frederic
- New pixel structure optimised for low gain (in view of reducing power needed for analog front-end)
  <= Andrei + PhD thesis to start in Fall 2023

Merci de votre attention!