ITS3 IPHC Meeting – Sensor Developments

Gianluca AR, Walter S

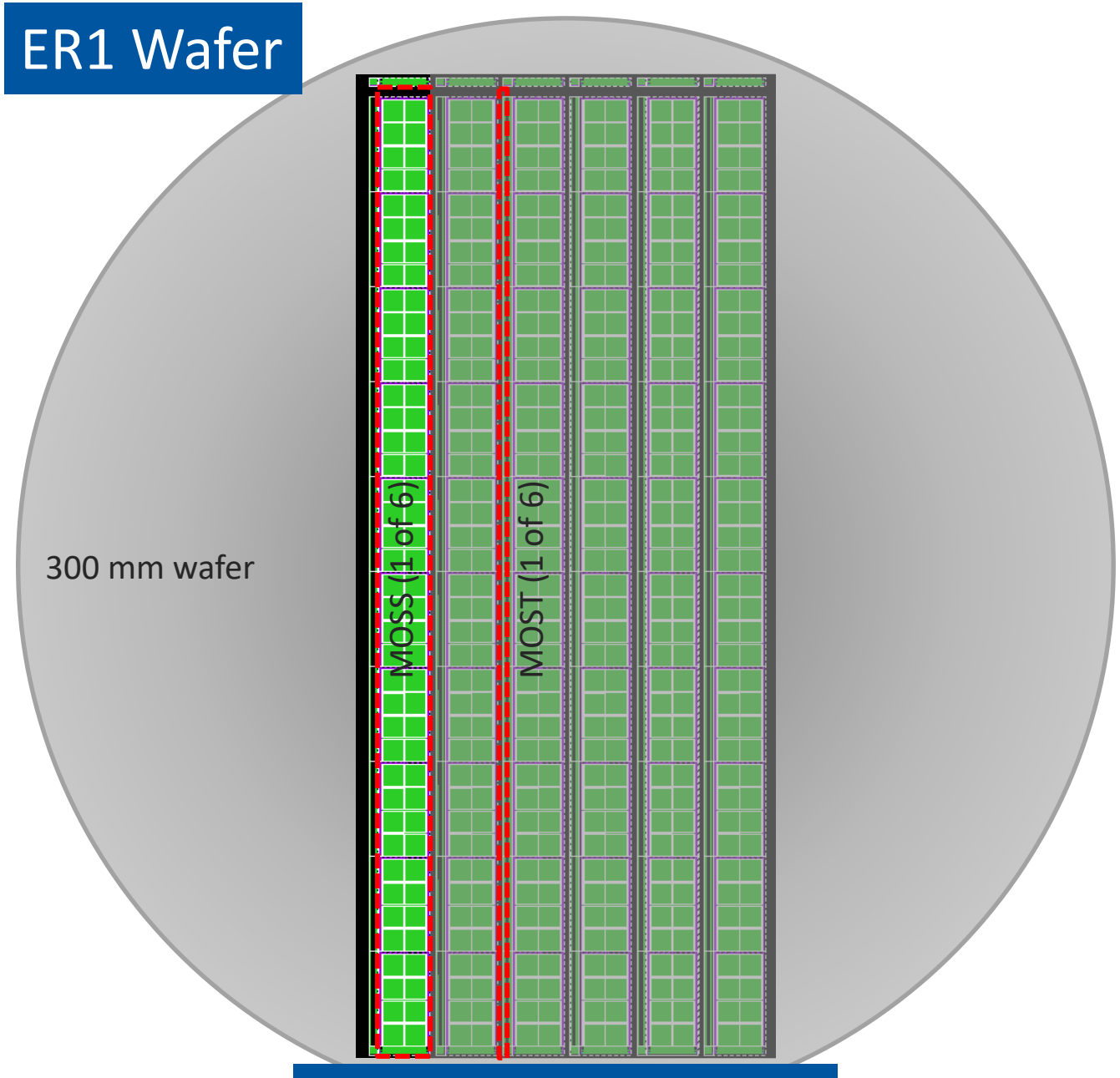
Outline

ER1 Submission

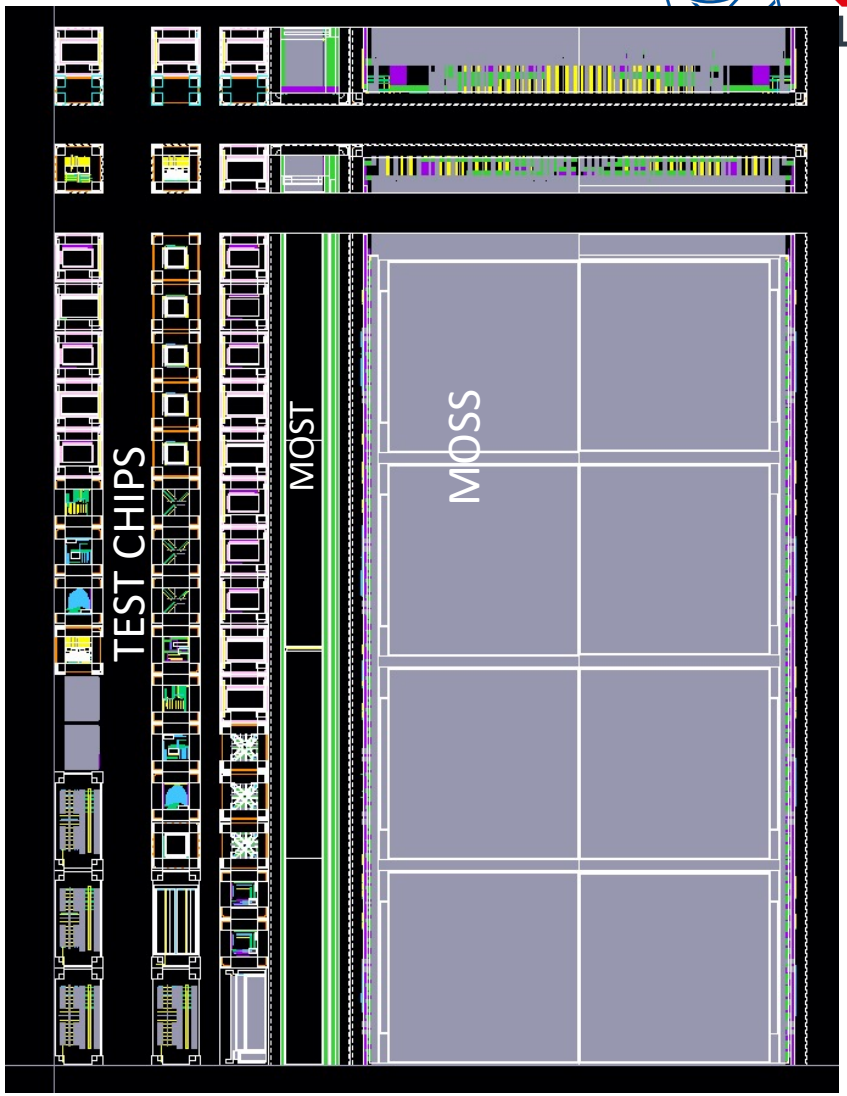
EP R&D WP1.2 new phase

Concepts for the ER2 stitched sensor

ER1 Wafer



6 MOSS and 6 MOST per Wafer



51 instances of Test Chips per Reticle

ER1 Tape-Out

24 Sept	WK38	**ER1 MOCK submission**	Known DRC violations and residual issues.
6 Oct	WK40	MOSS design release	Density and residual DRCs on MOSS fixed.
31 Oct	WK43	MOST design release	Density and residual DRCs on MOSS fixed.
4 Nov	WK44	Chiplets design release	Various density issues on multiple chips.
14 Nov	WK46	**ER1 TRUE tape-out**	Extensive and intensive checks on full wafer gds and virtual dicing.
1 Dec	WK48	Submission of modified implant geometry	Split on gaps in the buried low-dose n-type layer.
5 Dec	WK49	Mask views available	Foundry.
11 Dec	WK49	Mask views approved	By us (via a slow remote GUI only inspection tool).
12 Dec	WK50	**Mask fabrication STARTED**	
23 April 2023	WK16	Expected wafer shipment date	

Last plenary
14 Oct

- Wafers production plan
  - 18 wafers with ER1 base mask set
  - 6 wafers with variant mask (split) concerning the *buried n-type implant*
    - Removed in MOST. Increase of gap width in APTS, DPTS, MOSS pixels

EP R&D WP1.2 enters **Phase III.A**

ER1 completes WP1.2 Phase II and starts Phase III.A

Scope

Development and design

Stitched sensor chip MOSS2 targeting all ITS3 requirements and functions

Pixel development structures compatible with MOSS2

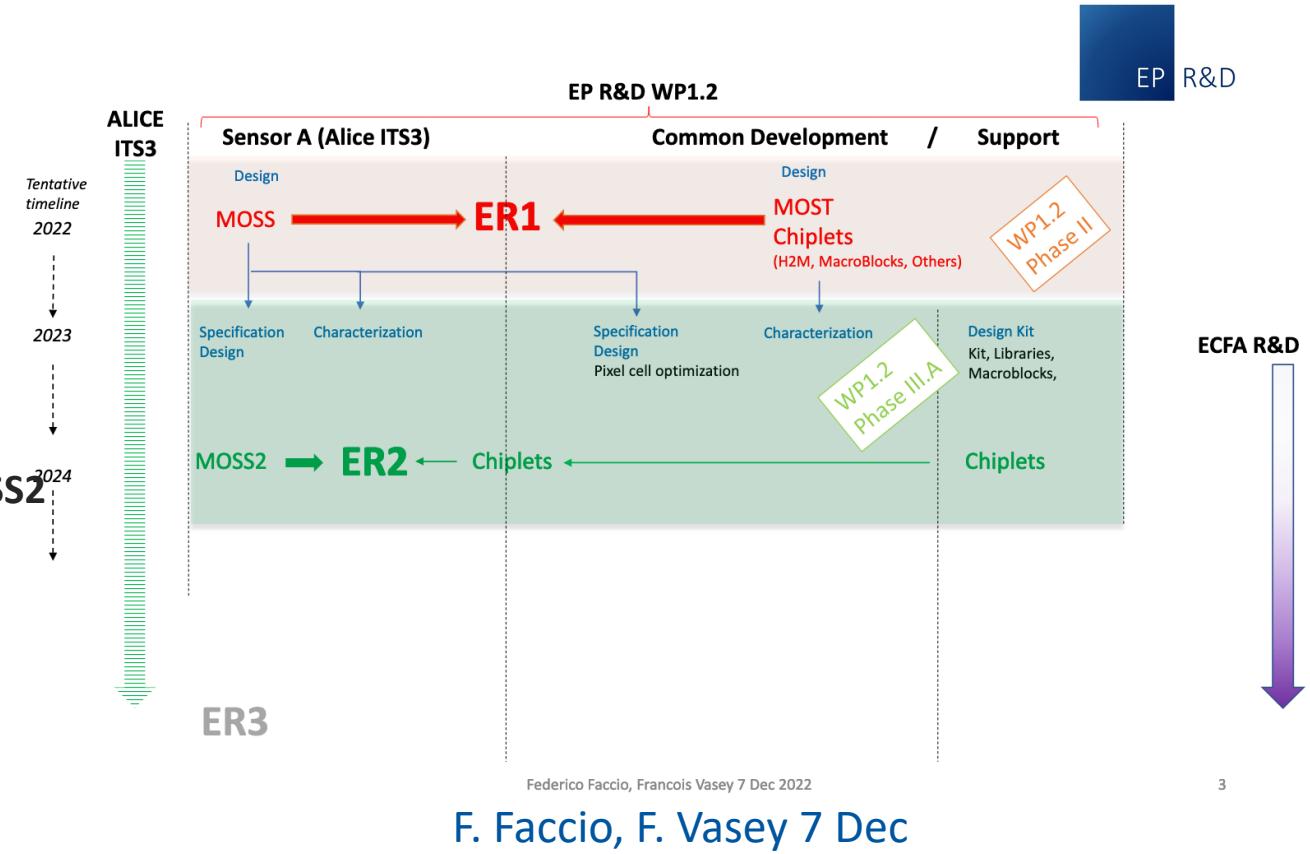
Macro blocks and cell libraries for ER2

Characterization

ER1 sensors and chips

Timeline

Dec 2022 -> Q1-2024 (**ER2** submission)



F. Faccio, F. Vasey 7 Dec

Outlook EP R&D WP1.2 **Phase III.B**

Split of ITS3 final sensor design cycle

Design for ER3 submission of the final chip planned to be in the scope of ALICE ITS3

Tentative timeline
2022
2023
2024

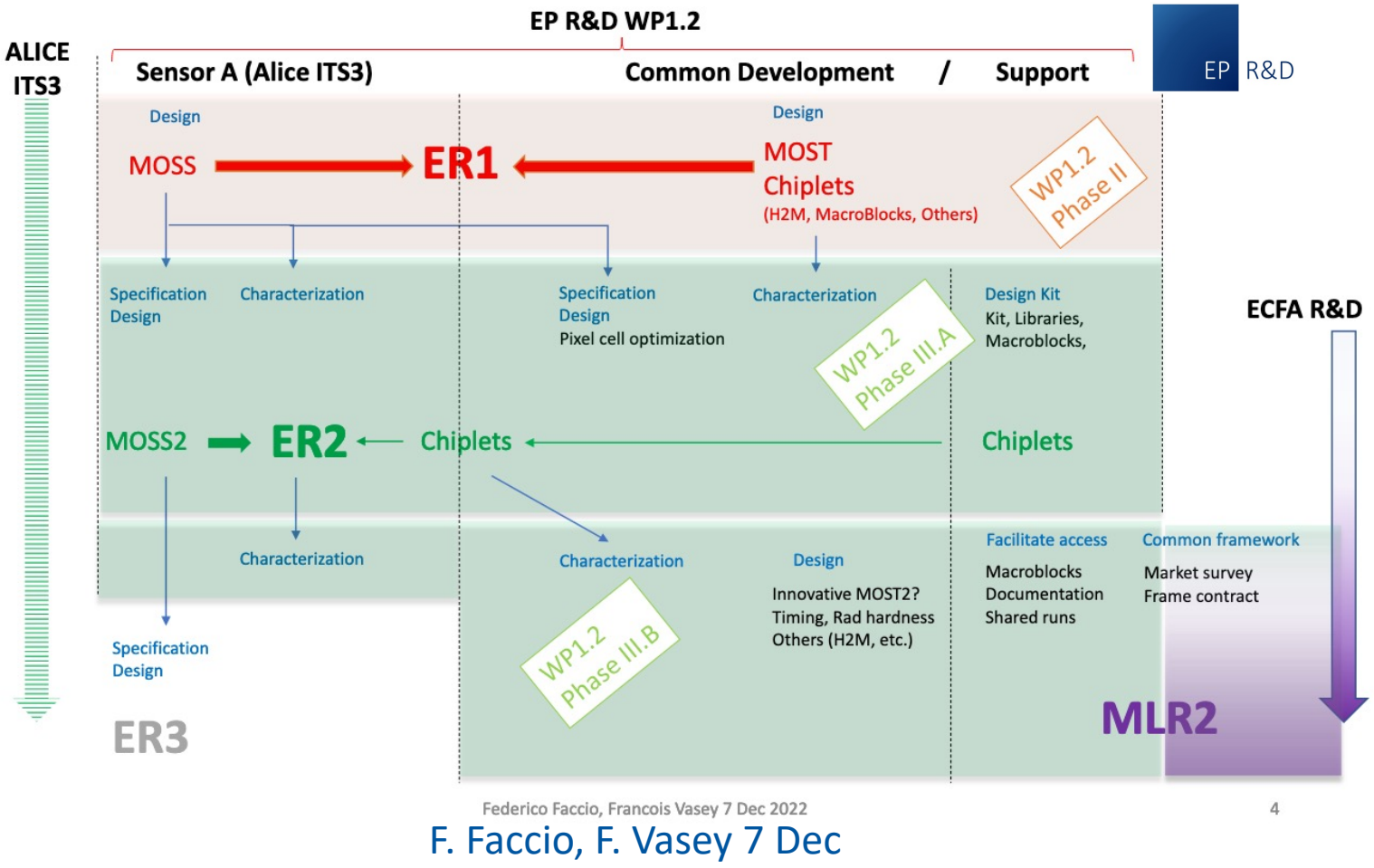
Phase III.B scope

Characterization of ER2 designs

Developments from ER1 (timing, radiation hardness, H2M)

Timeline

Q2 2024 -> **MLR2** submission



F. Faccio, F. Vasey 7 Dec

Structured as Collaborating Activities

Sensor A – ITS3

Gianluca

Developments

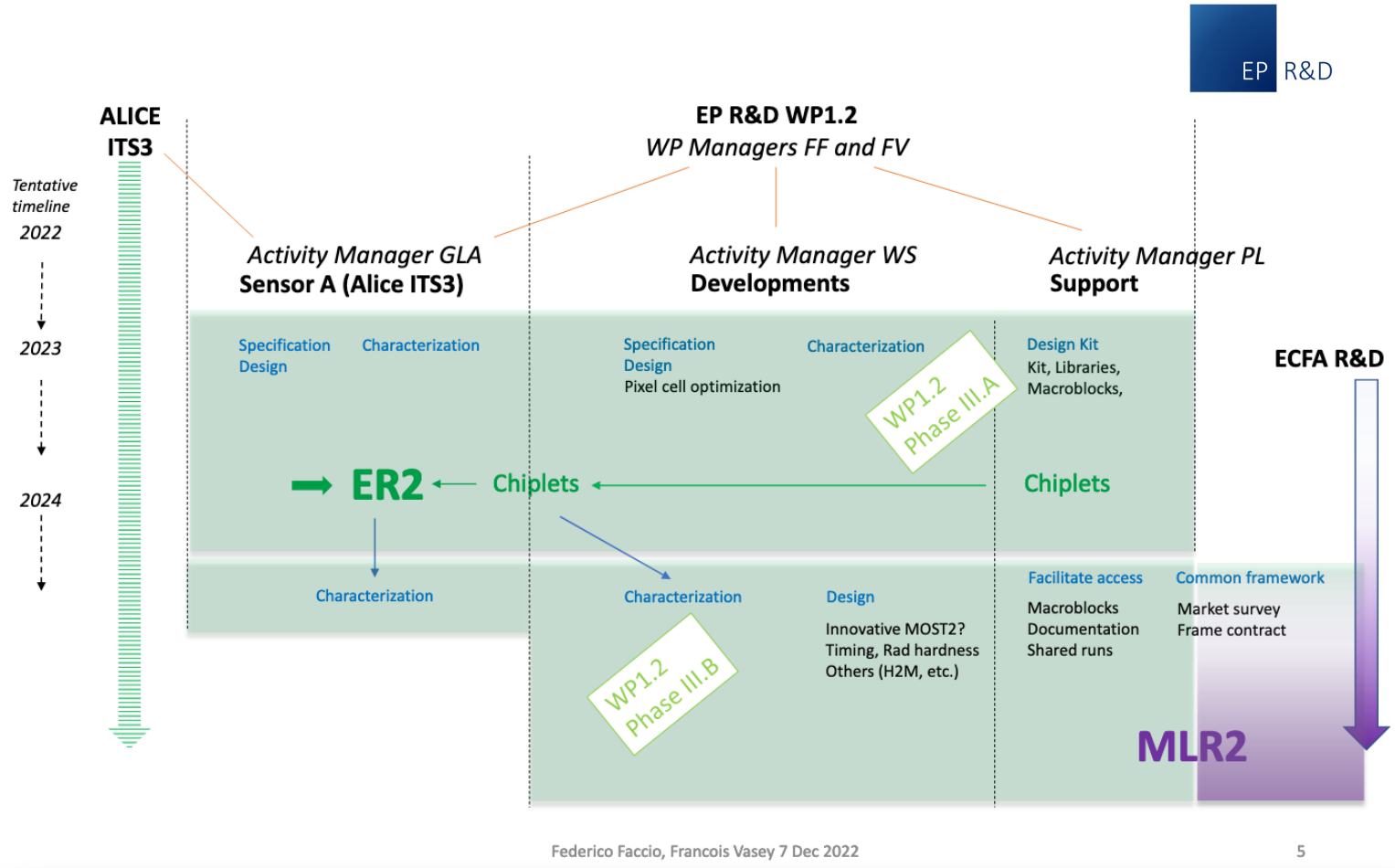
Walter

Support

Pedro

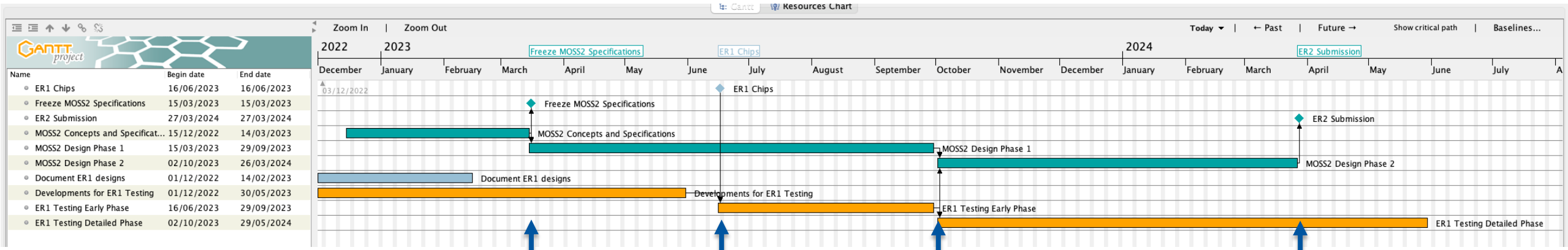
WP1.2 Coordination

F. Faccio (ESE-ME SL), F. Vasey (ESE GL)



F. Faccio, F. Vasey 7 Dec

Outlook WP2



Freeze MOSS2 Specifications

ER1 chips

First results ER1 chips

ER2 Submission

ER2 STITCHED SENSOR

MOSS2 Design Concepts and Specifications

Next stitched sensor chip is **not** a direct evolution of MOSS +/- MOST

- Goals are different
  - MOSS and MOST are true exploratory designs for proof of principles and learning methodology and yield
  - MOSS2 is the **first attempt to cover ITS3 requirements**
- Existing circuits need substantial redesign
- New features to be added

Studies and discussions started

- Architectural options
  - Identifying requirements, trade-offs, MOSS/MOST commonalities, differences
- Gathering lists of design questions and development needs
  - Plan to assess and address them by simulation studies in Jan-Feb
- First look into early simulations of readout capabilities and requirements
- Started identifying areas of responsibility and discussing design assignments

Power distribution

Power distribution remains **major challenge**

- IR drops
- Investigate additional metal and redistribution layer options
- Carefully looking into power domain partitioning and on-chip power regulation
  - Could allow to cope with IR drops, but llarger thermal dissipation
- Promote power to top concern for every block specification, design, validation from the beginning

Yield and DFM

Yield remains **major unknown**

- Keep improving design for yield
- Explored in ER1, compromised in certain design blocks
- Need to handle yield more quantitatively and systematically in ER2
  - Use the available tools (interesting early stage exploration from Frederic)
  - Seek data from foundry
  - Further develop Custom Design rules

Major themes

Leakage

MOSS and MOST analysis revealed large potential impact of leakage currents

Can break power budget for digital consumption. Also affects analog biasing

Early studies of Leonardo, Thanu. Simulations on Digital Pixel by Geun Hee

Limits density of transistors and gates

Needs consideration from early stages

Recent updates

Detailed studies of sub-threshold conduction leakage

Activity recently resumed, Geun Hee, Gianluca, Szymon, Frederic

Identifying mitigation techniques to keep the leakage under control

MOSS2

Concept

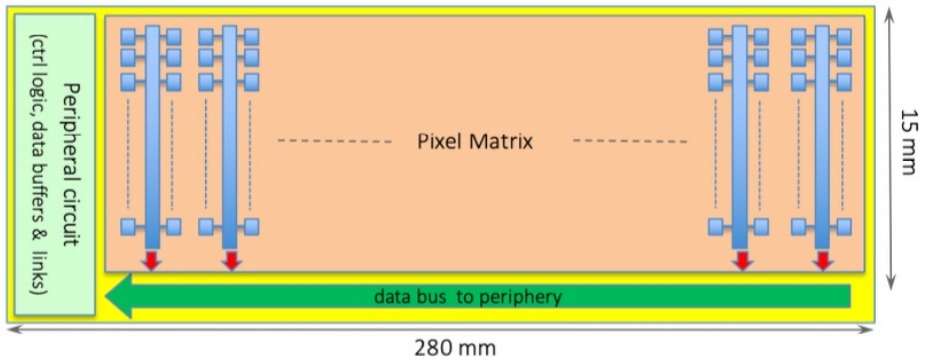
Use stitching to implement ***abutted arrays of sensors on the same die***

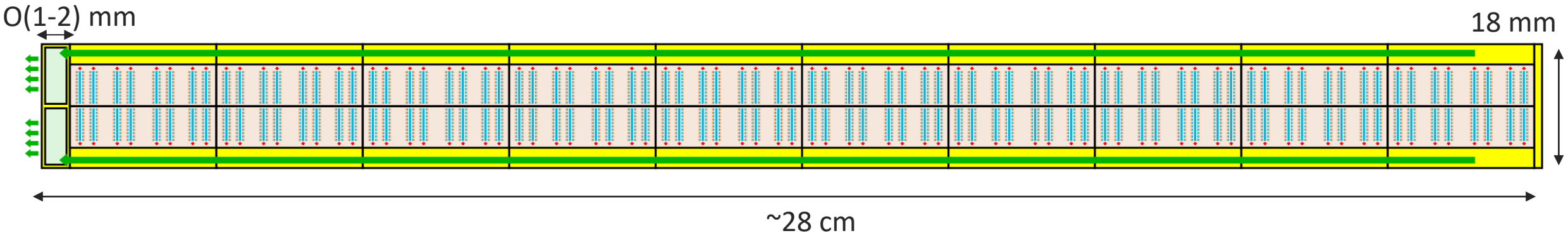
Include know-how from ALPIDE, MLR1, MOSS and MOST and other designs

Two peripheral regions on the long edges

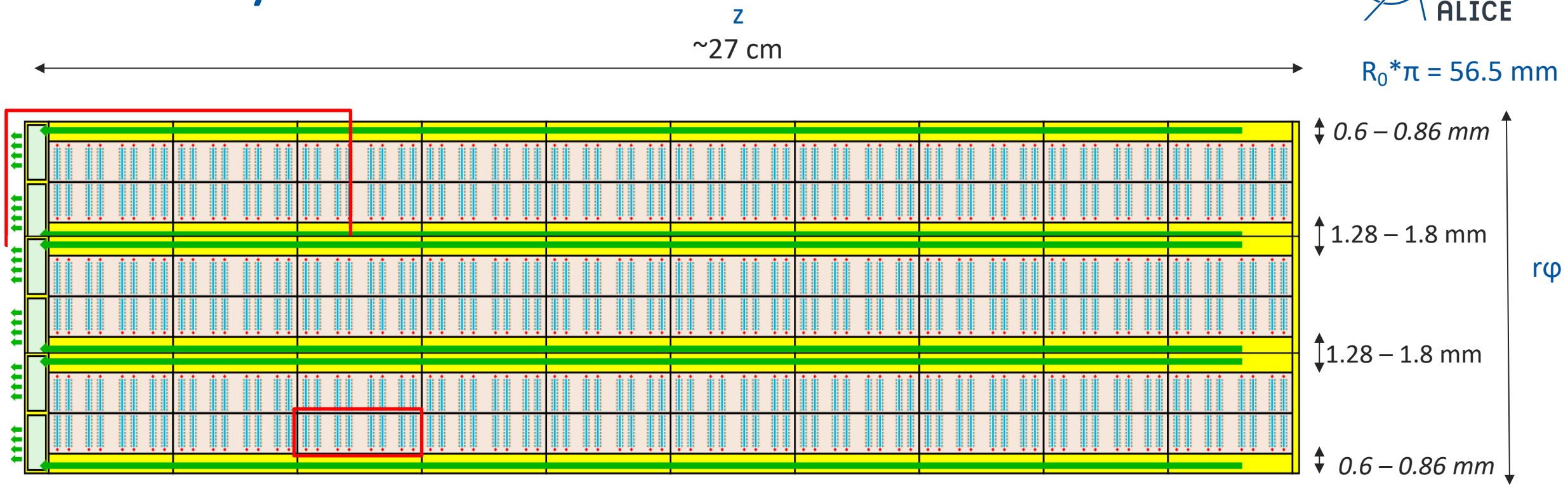
Data collected in long edge peripherys and transmitted at high rate over on-chip fast data busses (concept 1)

ITS3 Letter of Intent





Half Layer 0

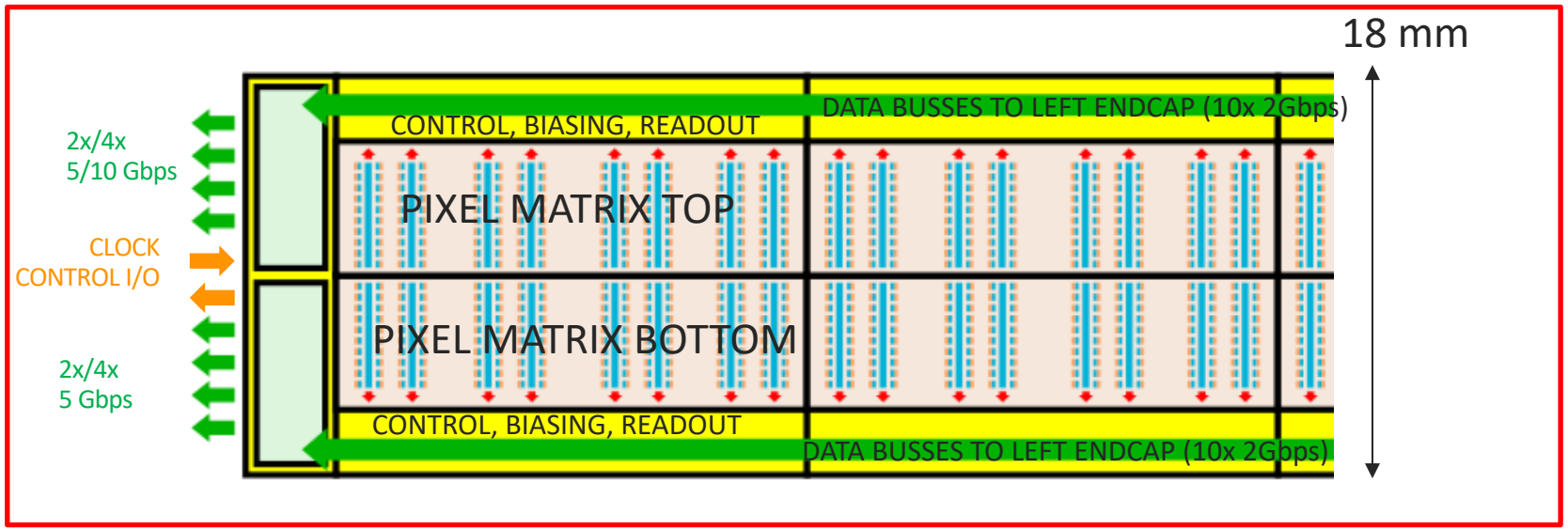


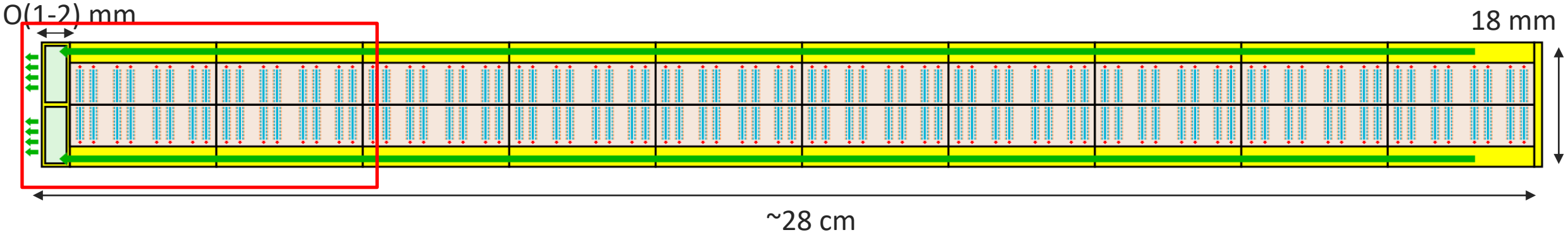
60 Sensitive Units

Non sensitive peripheral regions: 3.76 – 5.32 mm

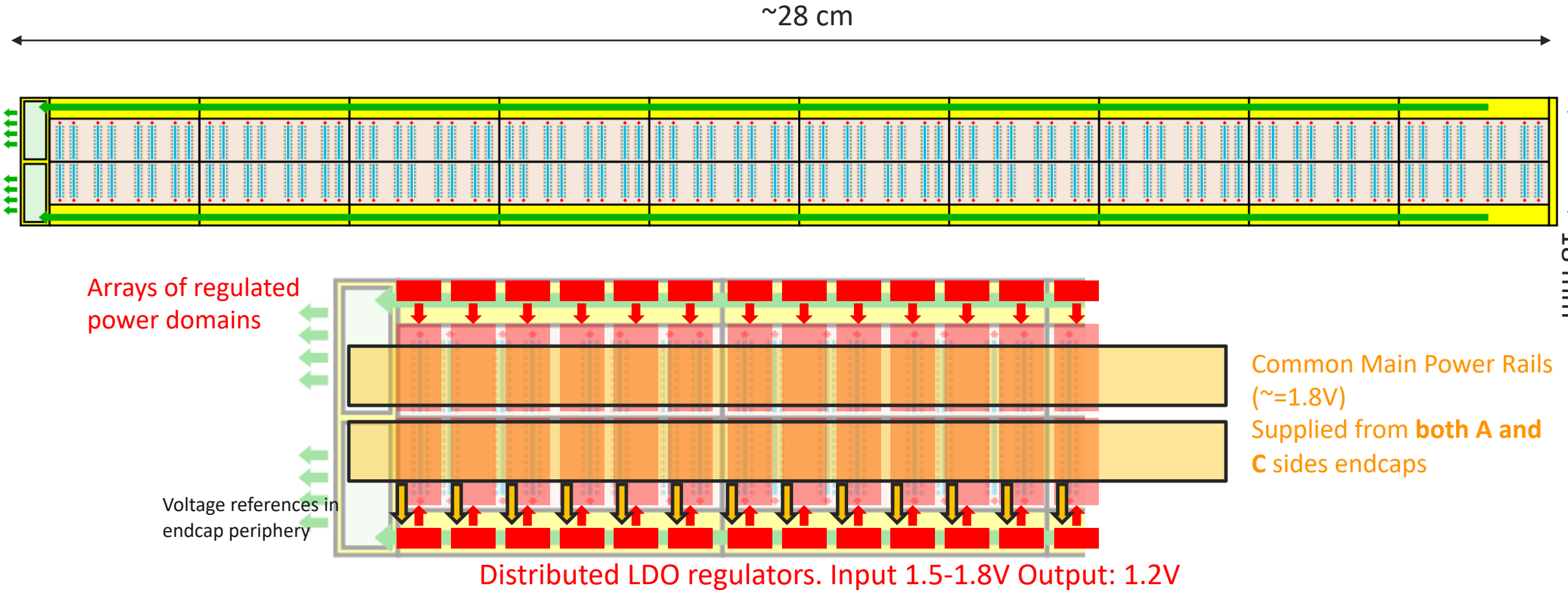
6.7% – 9.5%

Stitched backbone busses and fast serial outputs



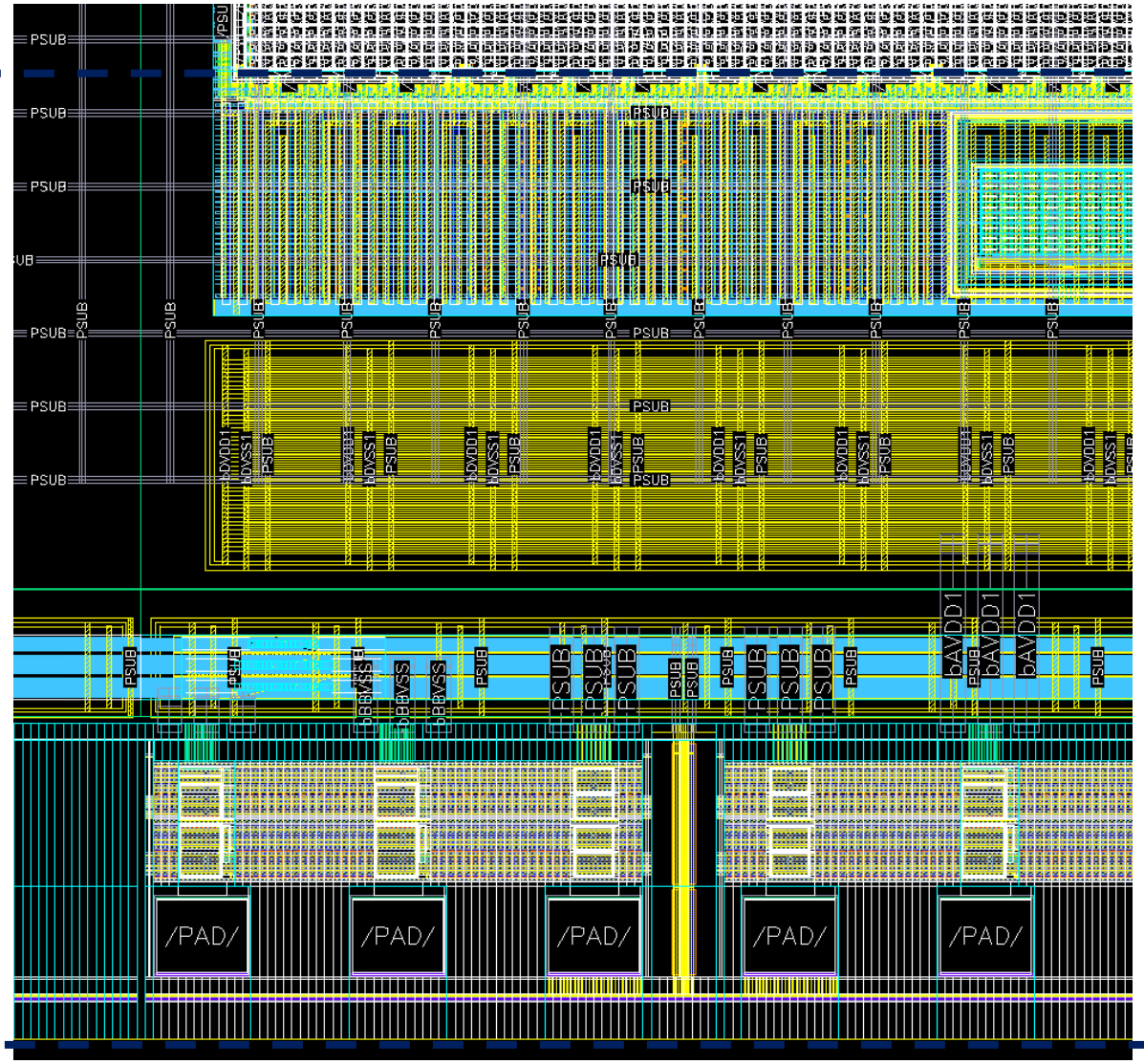


On-chip power regulation



Very preliminary concepts, many questions to study.
If power density stays below 15 mW/cm^2 then effective *total* ~= 20 mW/cm^2

Periphery developments



MOSS

~1180 um

DAC and Biasing
300 um

Digital Periphery
350 um

Backbone
170 um

PAD Ring
360 um

45 um

MOSS2

640 - 900 um

150 - 240 um

200 - 300 um

80 - 100 um

210 - 260 um

Regulators in place of pads?

Scribe center

Summary and Outlook

ER1 tape-out DONE. Production started

ETA: May 2023

Need to prepare for timely testing

Documentation of ER1 chips, developments of test infrastructure and test plans

Starting new sensor design phase

ALICE ITS3 Sensor Development framed in EP R&D WP1.2

Started capturing and categorizing ideas and questions to study (Jan-Feb)

Review and freeze major chip specifications by mid-March 2023 (Review)

REFERENCE MATERIAL

MOSS Matrix readout power densities

7 Summary of power values for the modeling of MOSS macros consumption

The following tables provides a summary of the key figures calculated in the other sections to provide a reference for the power analysis on the MOSS chip design.

For hit rate dependent figures, a particle hit flux of $\Phi = 2.2\,\mathrm{MHz/cm^2}$ is assumed.

Pixel Matrix only
[mW/cm²]

Analog Power Density ($\mathrm{mW/cm^2}$)	Pitch 18 µm	Pitch 22.5 µm
Static	11	7
Pixel hits	0.001	0.001

Digital Power Density ($\mathrm{mW/cm^2}$)	Pitch 18 µm	Pitch 22.5 µm
Leakage (typ.)	0.48	0.31
Leakage (abs. max.)	25	16
Pixel hits	0.004	0.004
Strobe (100 kHz)	0.163	0.120
Readout (to periphery)	0.025	0.025

Most pessimistic leakage scenario
Analysis needed

MOSS2 *new* features

On chip power regulation of sub-regions and common power rail

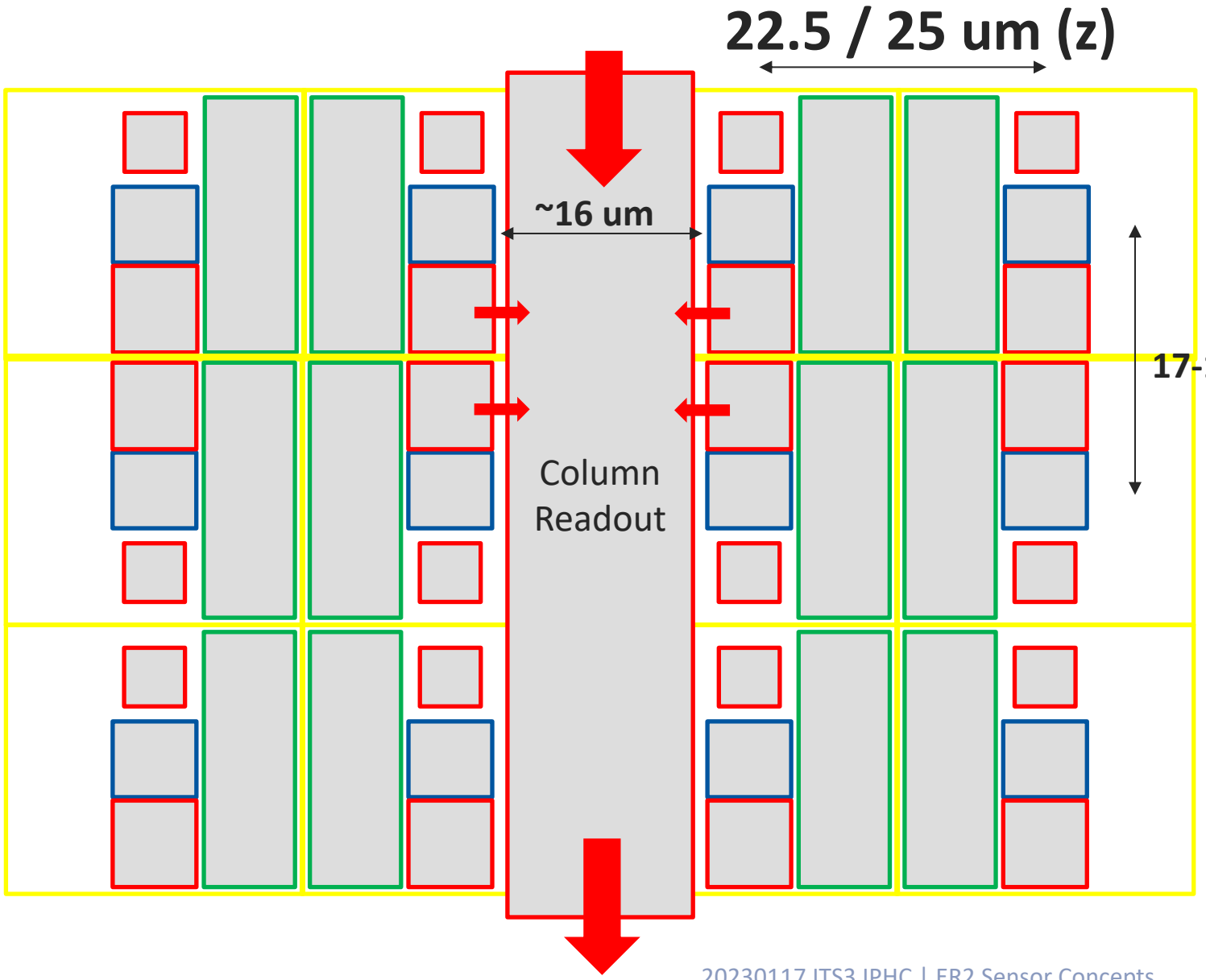
High speed differential on-chip backbone busses

High speed output links in endcap

Differential I/Os

ADC, Temperature sensors

Evolution of matrix readout



Column Drain Readout

Hit pixels transmit their address on 9 bits shared bus one at the time

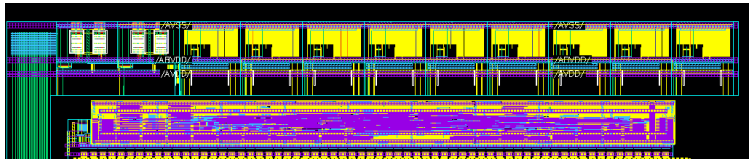
Token transfer down the column

Estimated signalling routes in 16 µm

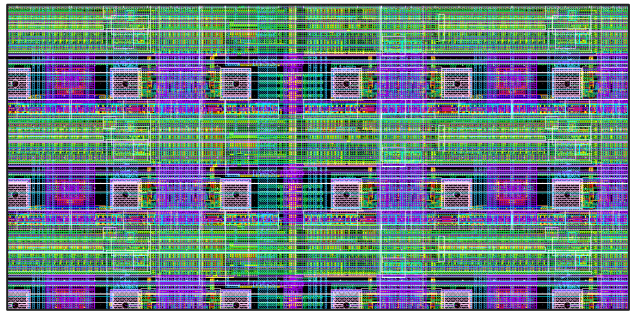
(x4 widening) 16 routes M2, 8 ? routes M4

(x3 widening) 22 routes M2, 11 ? routes M4

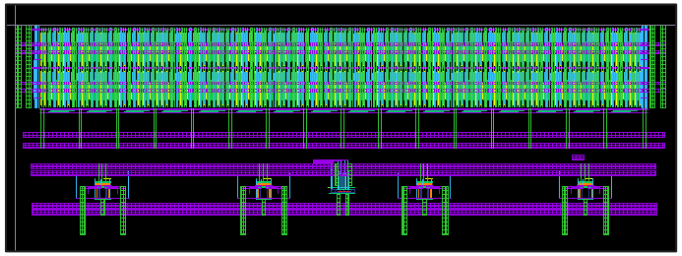
MOST layout snapshots



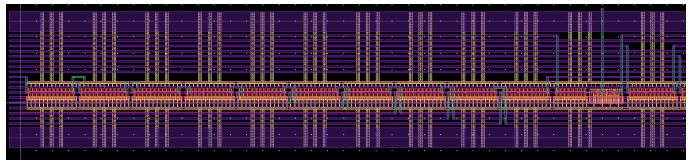
Detail of the top periphery (biasing generation, slow control, test pulsing)



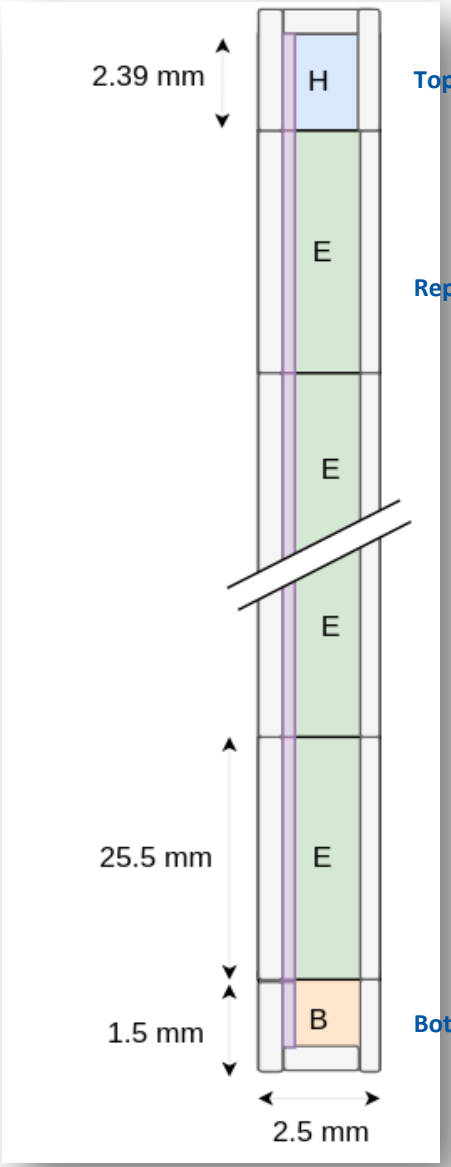
Detail of the pixel matrix



Detail of the bottom periphery core with the 4 CML outputs

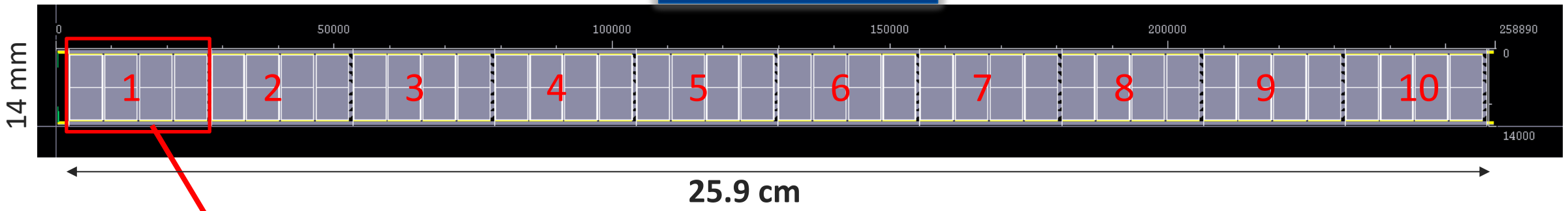


Detail of the stitched backbone buffers



MOSS layout snapshots

6.72 Mpixels



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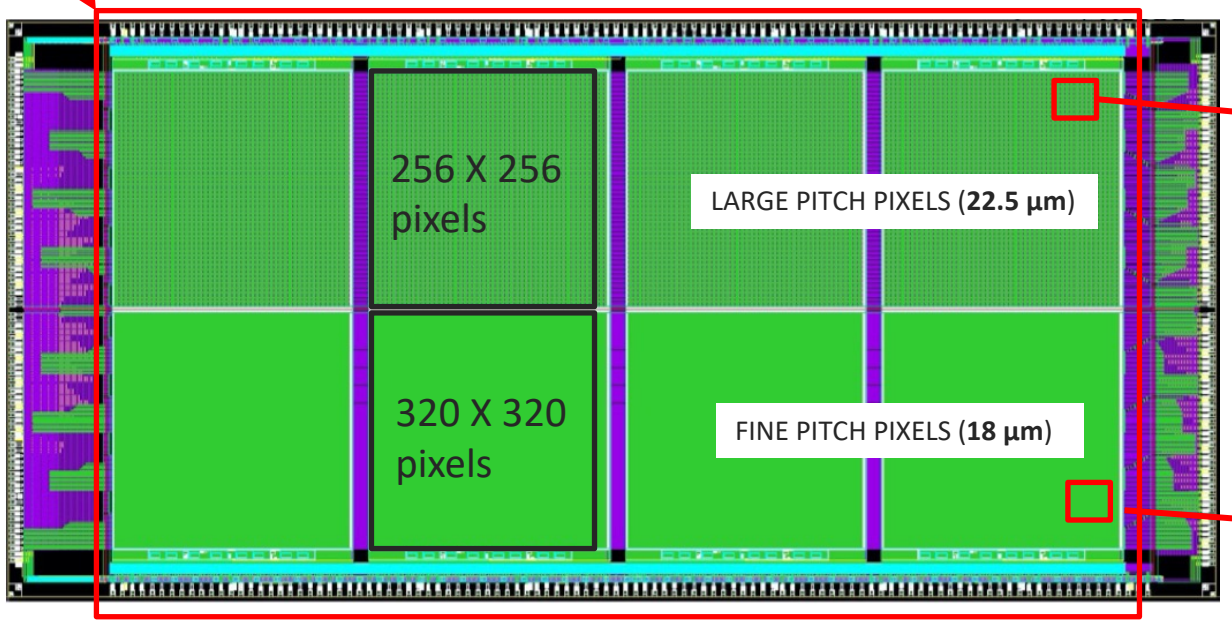
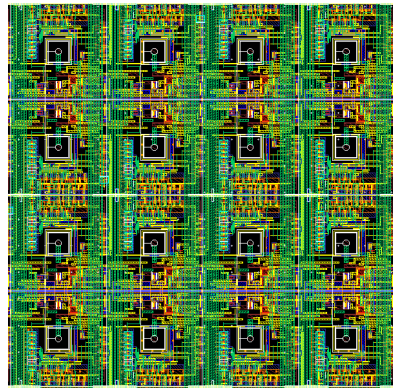
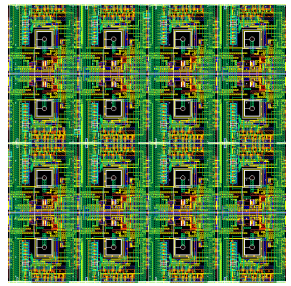




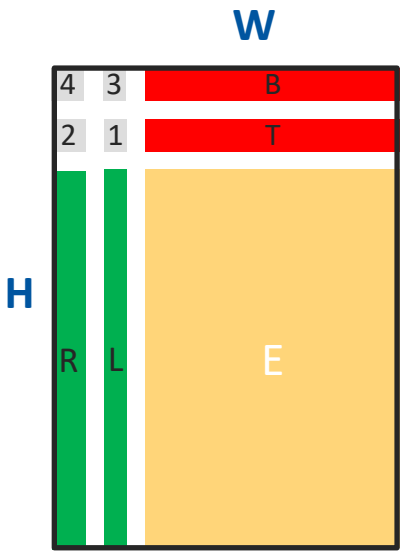
Pitch 22.5 µm



Pitch 18 µm

Towards ER1 – Stitching Interlude

Design Reticle (typ. 2×3 cm)



Circuits on wafer