HKROC: an integrated front-end ASIC to readout photomultiplier tubes for large neutrino experiments

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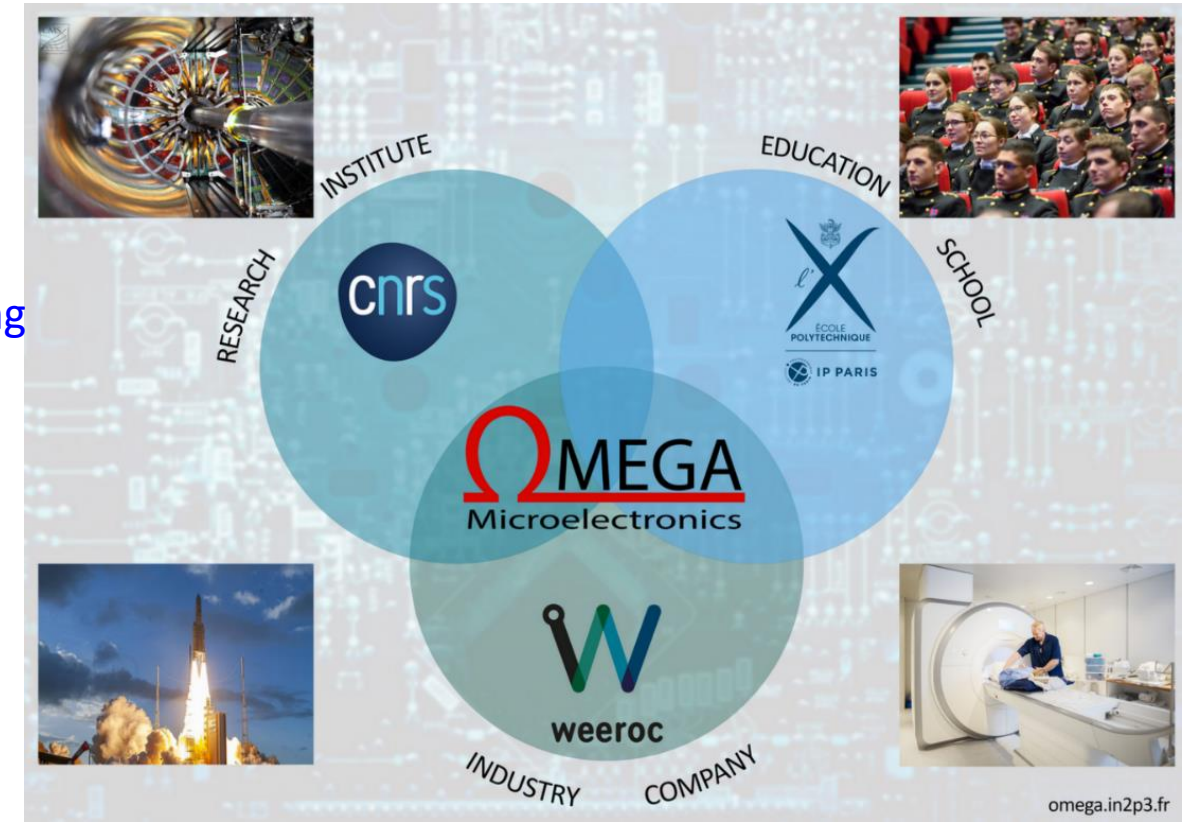
Organization for Micro-Electronics desiGn and Applications

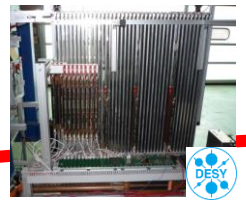
OMEGA Microelectronics Laboratory

- National Micro-electronics design center to address readout electronics needs for instrumentation in Particle and Astroparticle Physics
- 12 CNRS staff engineers, highly specialized in low noise, rad-hard, high speed mixed-signal readout ASICs
- Location at Ecole Polytechnique provides strong links with teaching and industrial partners in Advanced Technologies
- OMEGA major realizations in a nutshell
  - First readout chip for PM multi-anodes (OPERA_ROC 2003)
  - First readout chip for SiPM (FLC_SiPM 2005)
  - First readout chip with digitization for imaging calorimetry (SKIROC2 2010, HGCROC2 2019)
  - First readout chip with digitization of LGAD diodes for picosecond timing measurements (ALTIROC1 2018)

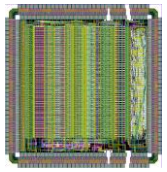


ASICs produced and installed on detectors since 2006

Omega

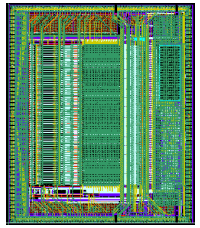


MAROC3

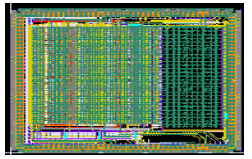


2006

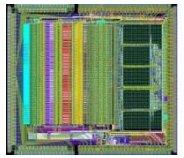
SKIROC



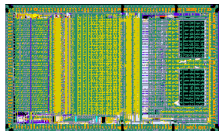
SPIROC



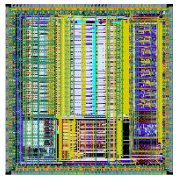
MICROROC



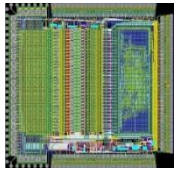
HARDROC



SPACIROC



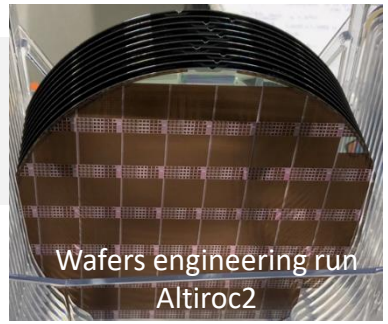
PETIROC



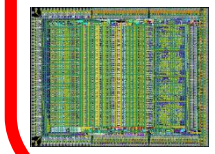
9 engineering runs in 9 years :

AMS SiGe 0,35um 2014, 2016, 2018

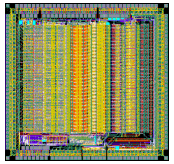
TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



TRIROC

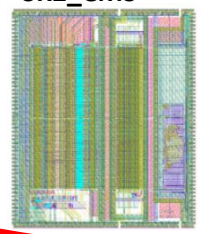


CITIROC

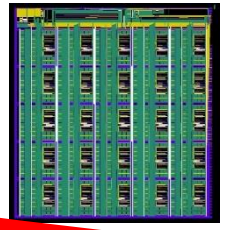


CATIROC

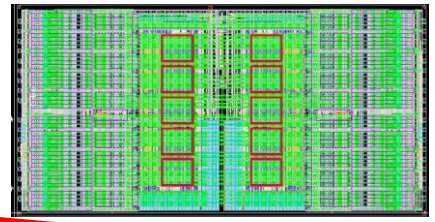
SK2_CMS



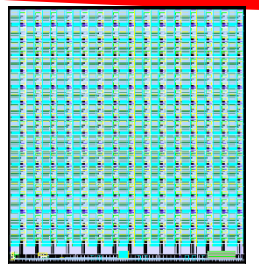
ALTIROC1



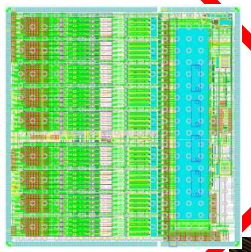
HGCROC



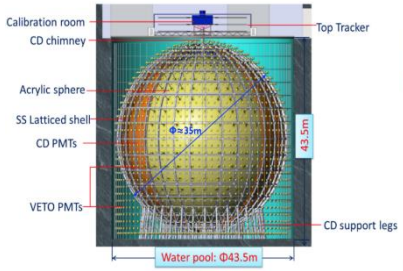
ALTIROC2



HKROC



2023



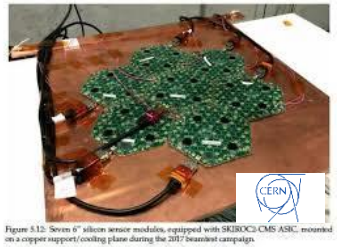
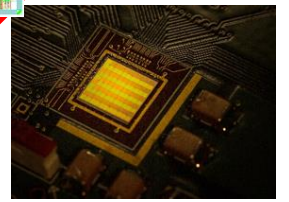


Figure 5.12: Seven 6" silicon sensor modules, equipped with SKIROC2-CMS ASIC, mounted on a copper support/cooling plane during the 2017 beamtest campaign.



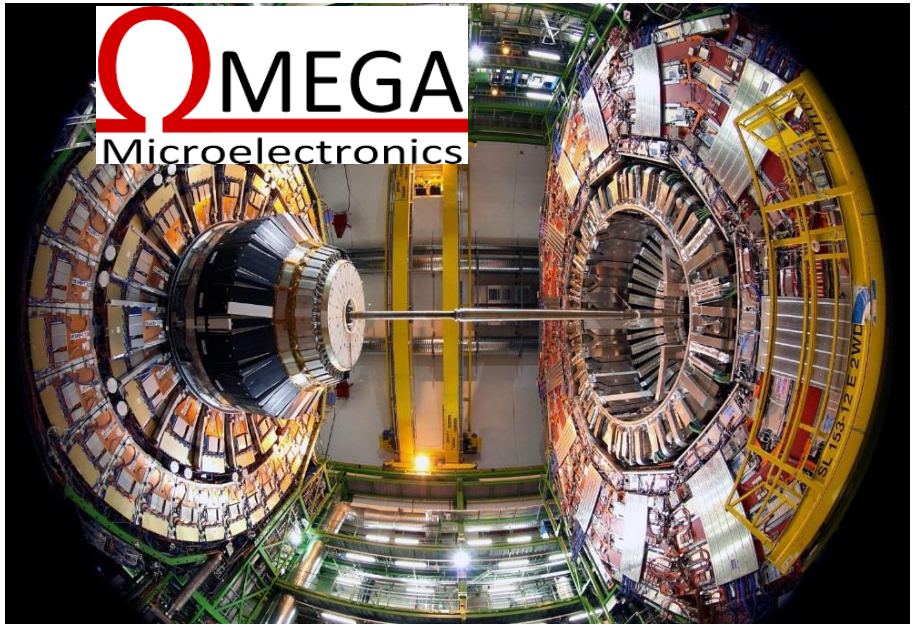
From HL-LHC to the HKROC ASIC

HGCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year
Project started in **2017**



HKROC was developed in
6 months

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

New preamplifier
New digital processing

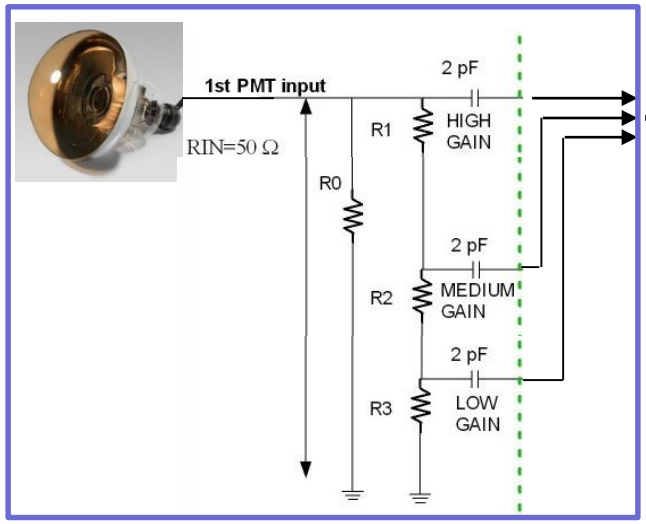
HEP trend => imaging calorimetry

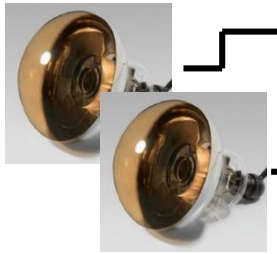
- ❑ High number of channels
- ❑ Charge and precise timing (<50 ps)
- ❑ Low power + System-On-Chip

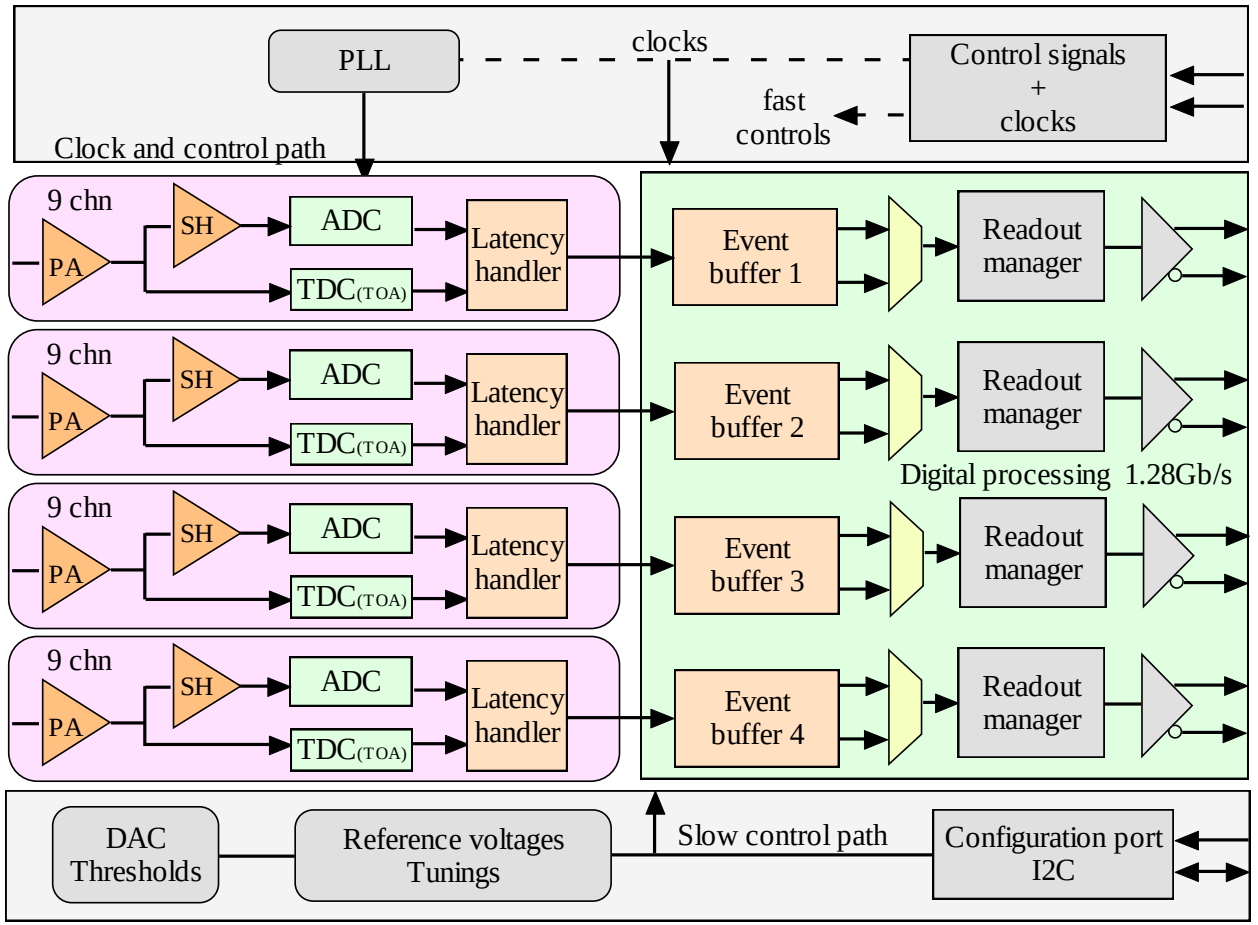
Based on HGCROC, HKROC-based electronics will provide a versatile, low-power and fully integrated solution for large neutrino experiments

HKROC main features

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Or 36 PMTs with one gain



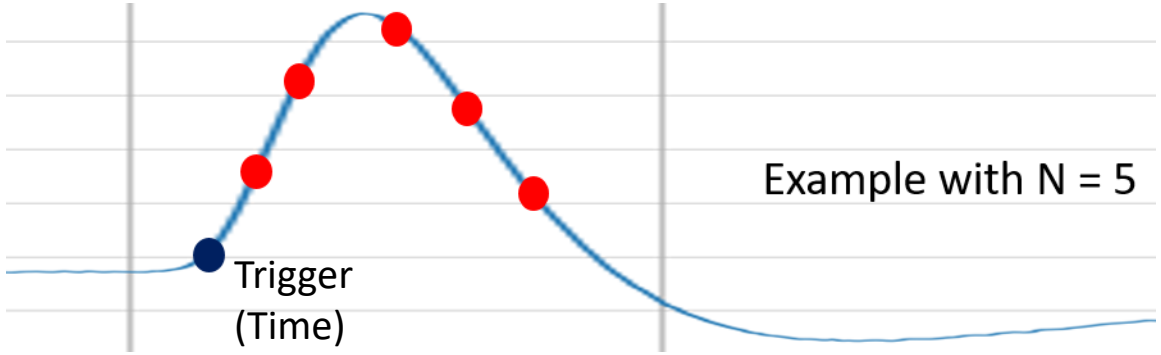




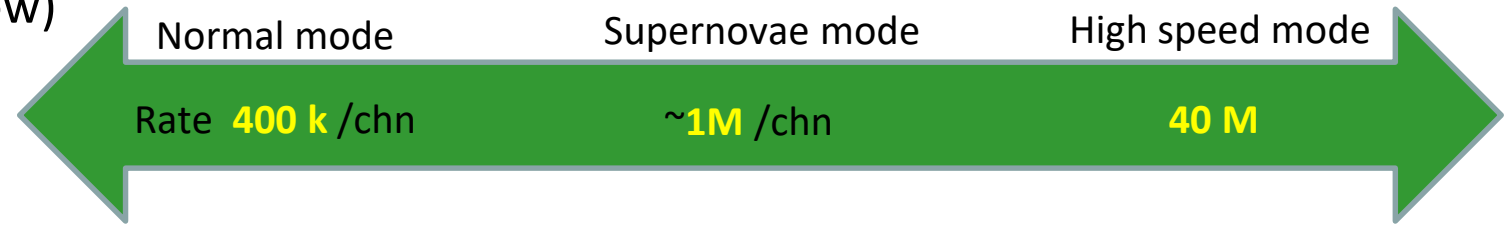
- ASIC in TSMC 130 nm node
- Low power: 10 mW per channel
- Large charge measurement with 3 gains (up to 2500 pC)
- Integrated timing measurements (25 ps binning)
- Readout with high speed links (1,28 Gb/s)
- HKROC is a waveform digitizer with auto-trigger

HKROC: waveform digitizer with auto-trigger

- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA
    - 5% resources of a modern XILINX FPGA



- When using 3 gains / PMT (high, medium, low)
  - Hit rate capability up to 400 kHz / PMT
  - Increased up up to 1 MHz by focusing on high gain
    - Dynamic selectable by the user
  - Average values only limited by readout speed



HKROC can accept consecutive events (separated by ~30 ns)

Internal HKROC memory writing is without dead time

Readout speed is only limited by serial link bandwidth (average values above)

Timeline and hardware

HKROC0
2021/12

HKROC0-BGA
(x80) - 2022/06

HKROC1b-BGA
(x80) - 2022/12

HKROC production
(x4000) - 2023/04

HKROC-based acquisition system paper
2023/09

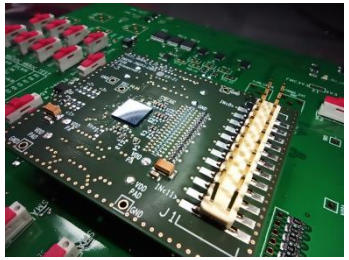
Mezzanine daughter board

Acquisition board

Acquisition board with reconstruction

2023/06

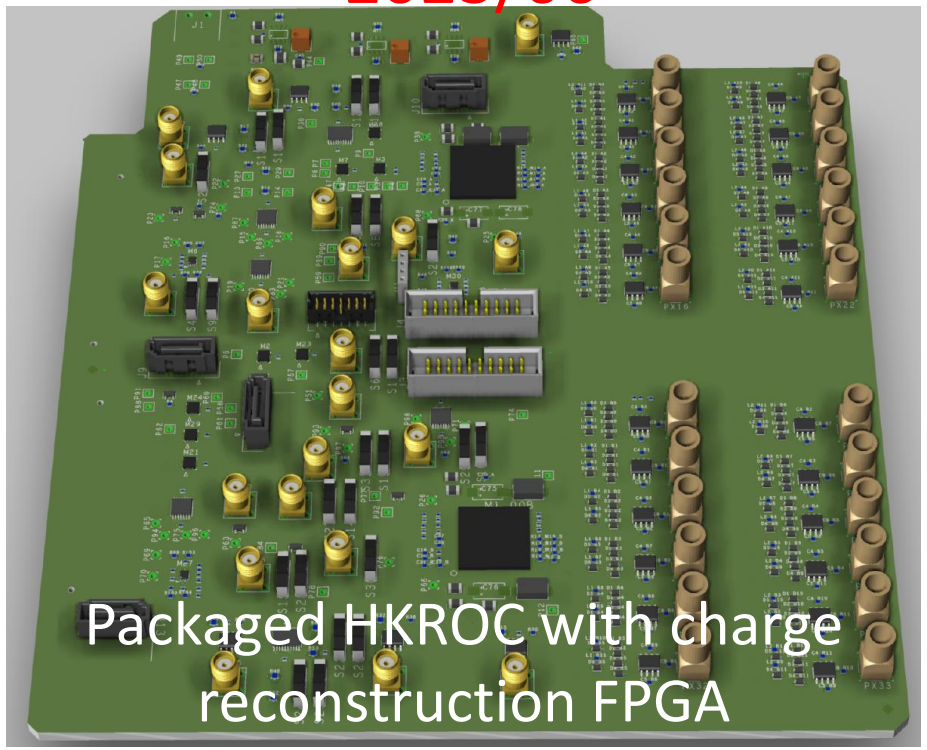
2021



Naked HKROC on mezzanine

2022

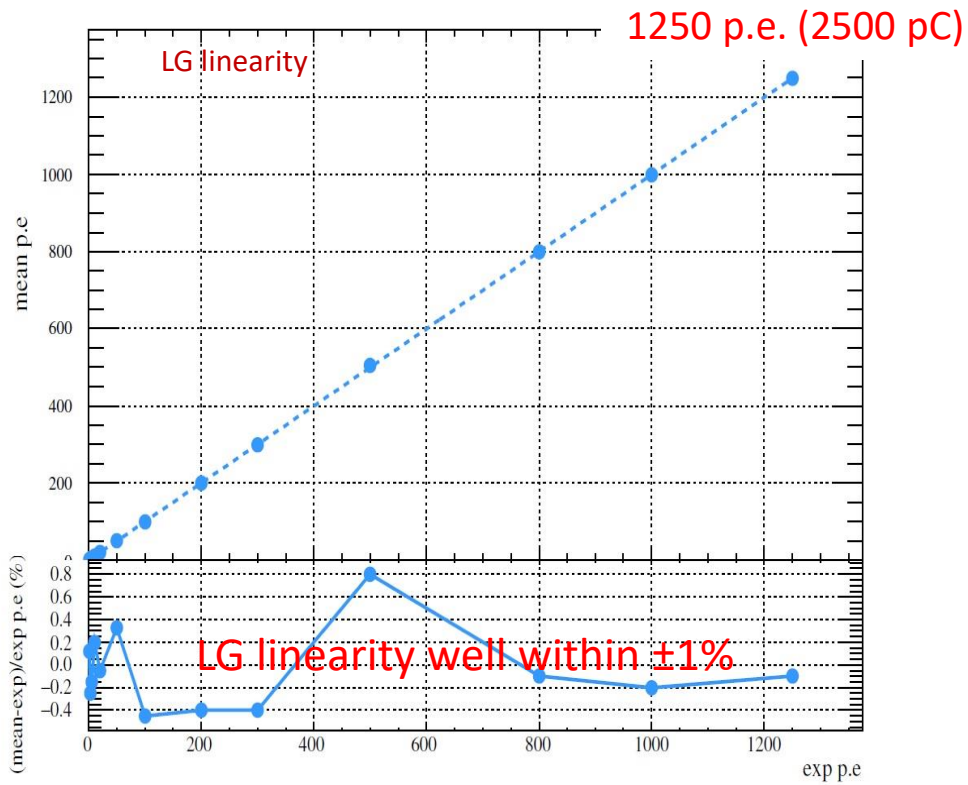
Packaged HKROC with acquisition board

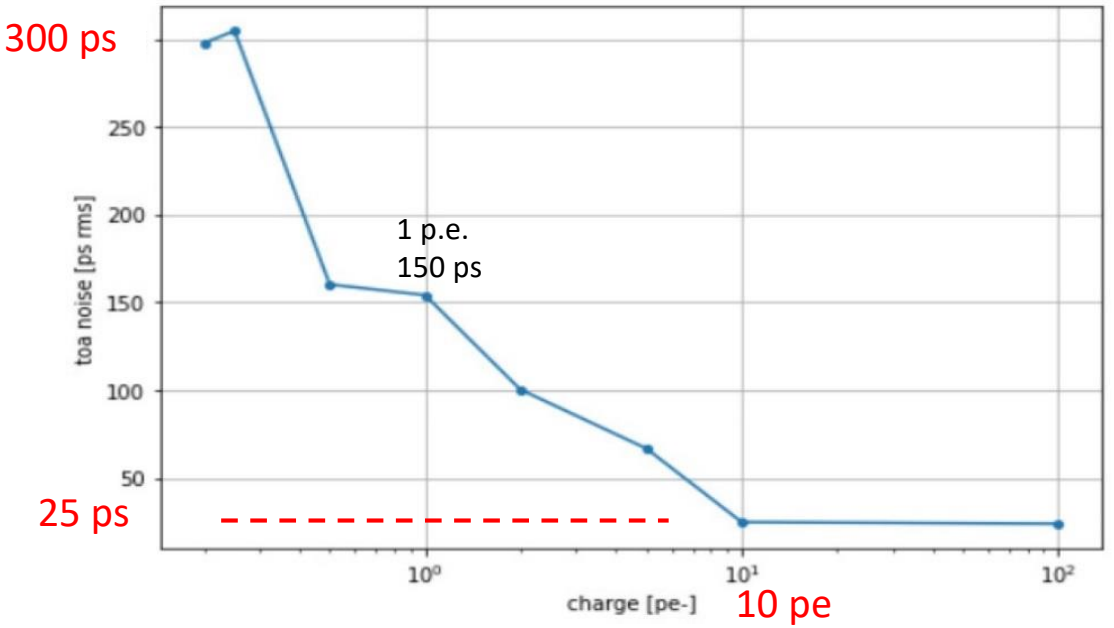


Packaged HKROC with charge reconstruction FPGA

Main experimental results with HKROC0 – Charge and Time

- Measurement with the full chain (analog + digital and reconstruction)
  - Signal auto-triggered with threshold





Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC) across the 3 gains**

TDC characterization with **1/6 p.e. threshold**

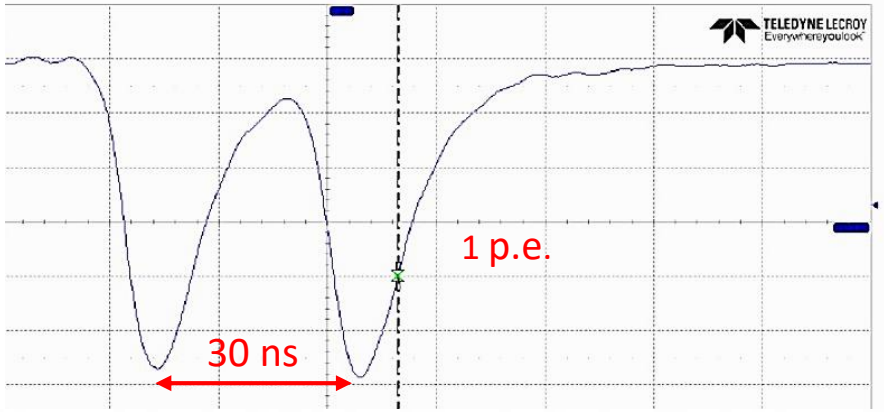
TDC resolution :

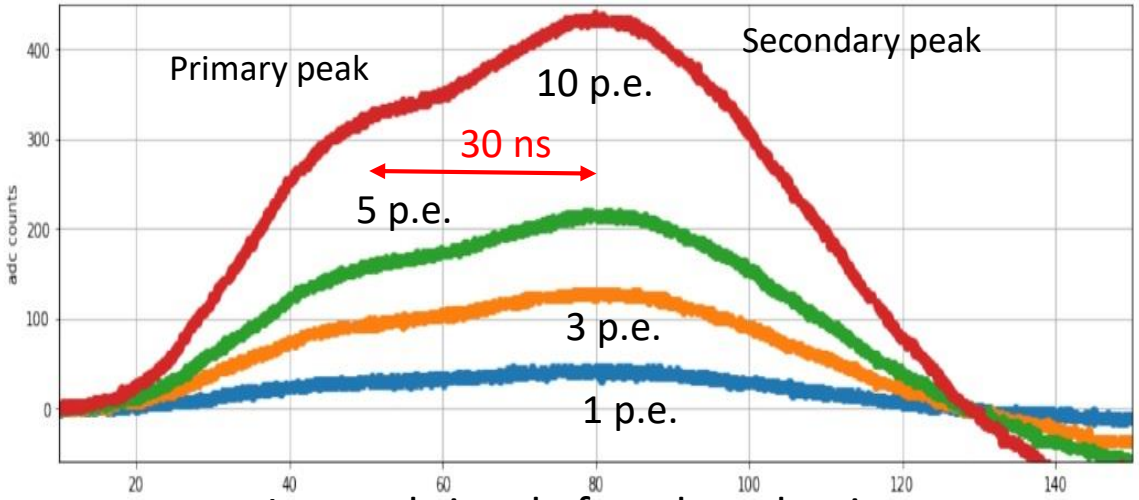
150 ps rms @ 1 p.e

≤ 25 ps rms @ 10 p.e

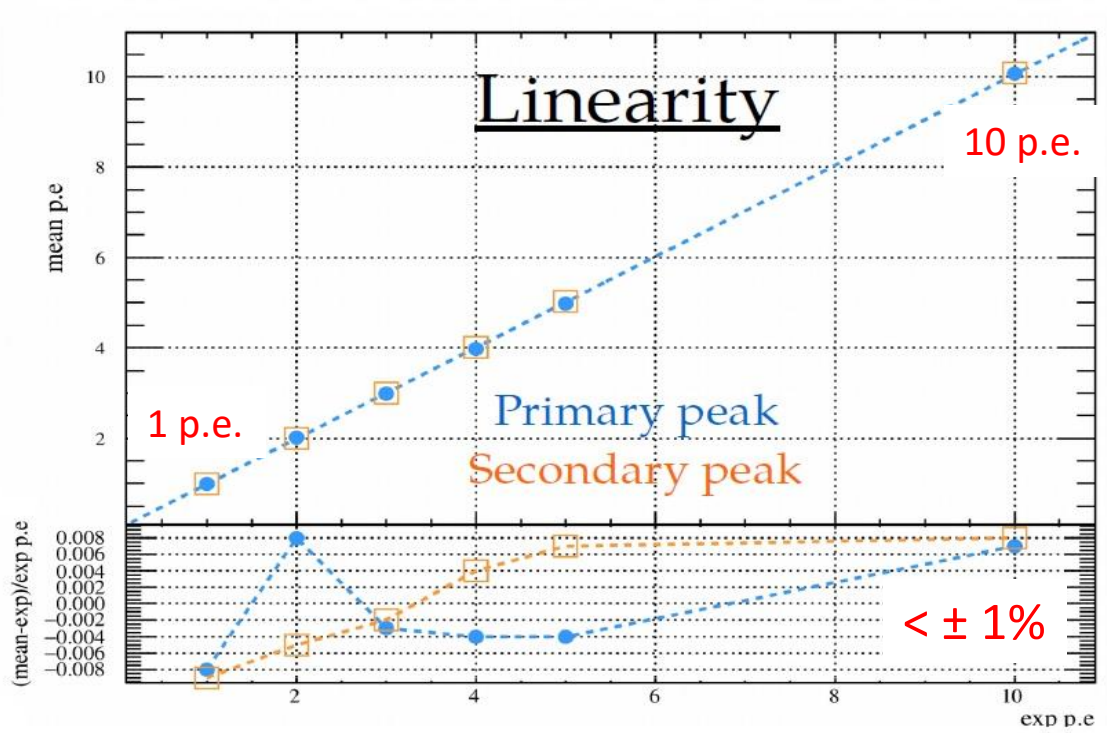
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)





Internal signal after slow shaping



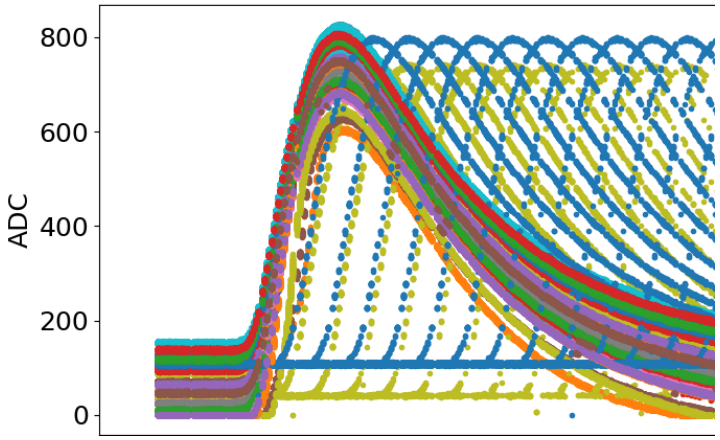
Charge reconstruction algorithm of the two peaks

Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

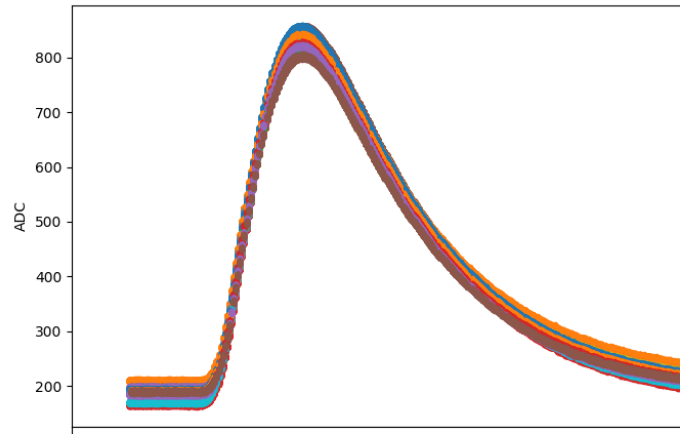
Improvements with HKROC1b - Yield and crosstalk

HKROC0 ADC yield was > 95%

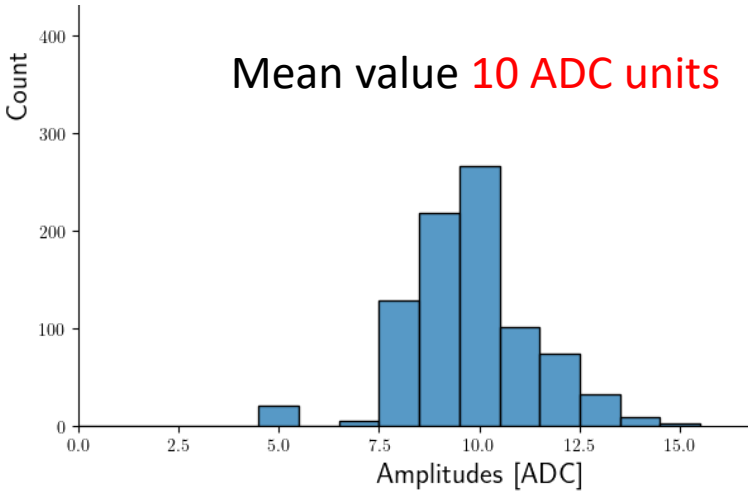


CMS-HGCROC improvement included in HKROC1b ADC

HKROC1b, 100% operating channels



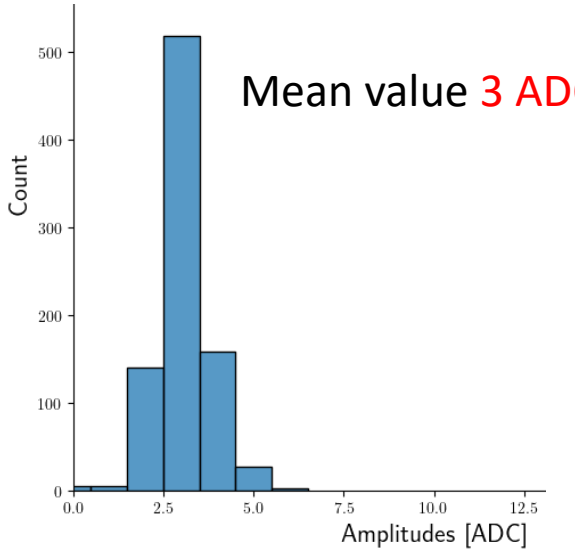
HKROC1b measurements



Mean value 10 ADC units

Reduction of the crosstalk of large signal on other channels

Reduction of x3
(1 pe is ~ 30 ADCu)



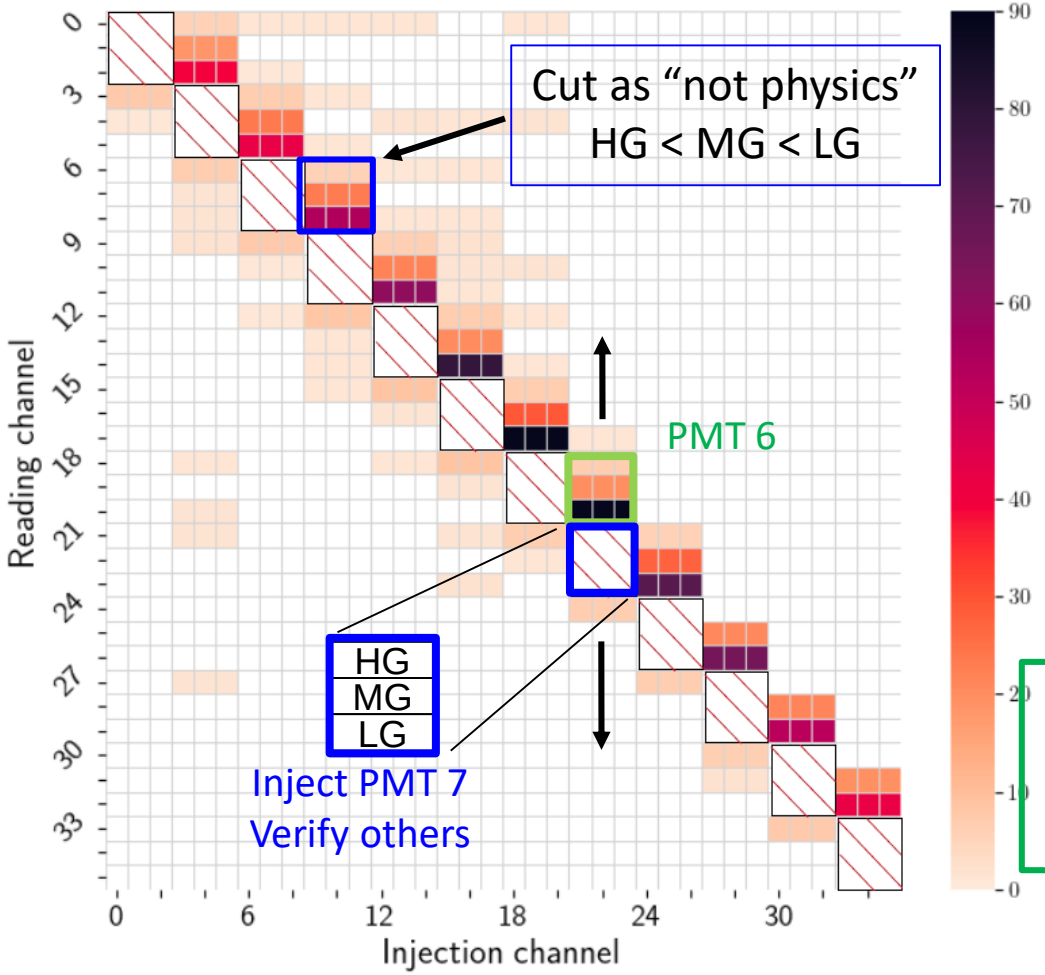
Mean value 3 ADC units

Acquisition board improvements

- Coupling map by injecting large charge (> 900 pe)
  - Importance of electronics board stackup
  - Huge work on the PCB with focus on suppressing HG coupling

Coupling fully cut thanks to HG "immunity" to crosstalk (veto)

Board v1 (Mezzanine) [ADC units]

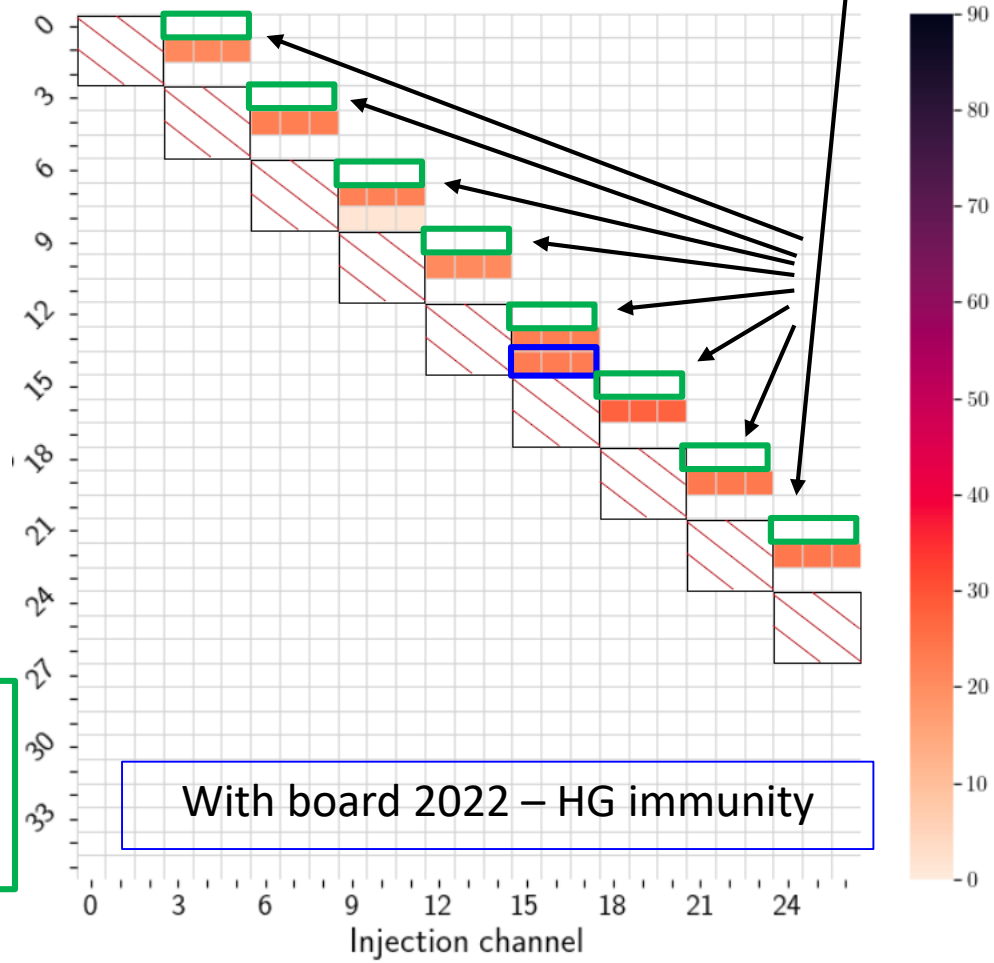


Acq. board 2022:
3 PMT gains split into 2 layers

HG and LG immunity to coupling

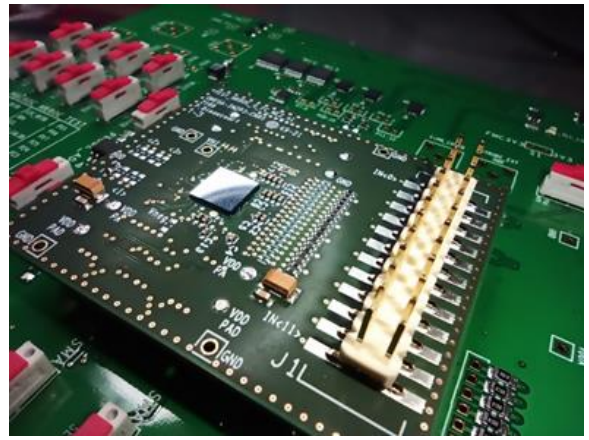
Acq. board 2023:
3 PMT gains split into 3 layers

Board v2 (BGA) [ADC units]

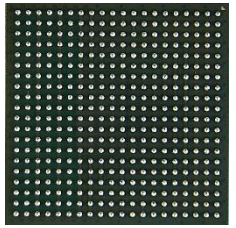


Conclusion

- HKROC is a versatile ASIC able to readout PMT
  - Time measurement with a precision < 50 ps
  - Charge measurement with a linearity of 1% (up to 2500 pC)
  - Low power consumption (10 mW per channel, 30 mW if three gains used)
  - Hit rate up to ~40 MHz with an average from 100k to 1M (fast mode)



- Production is booked for April (quantity > 4000).
  - Packaged is a BGA with 0.8 mm pitch (400 balls)



- Provide a full HKROC-based solution (ASIC + board) to the community
  - Auto-triggered waveform digitizer
- Paper will be published will all the measurements and possibilities

HKROC0 2021/12 → HKROC0-BGA (x80) - 2022/06 → HKROC1b-BGA (x80) - 2022/12 → HKROC production (x4000) - 2023/04 → HKROC-based acquisition system paper 2023/09

Mezzanine daughter board

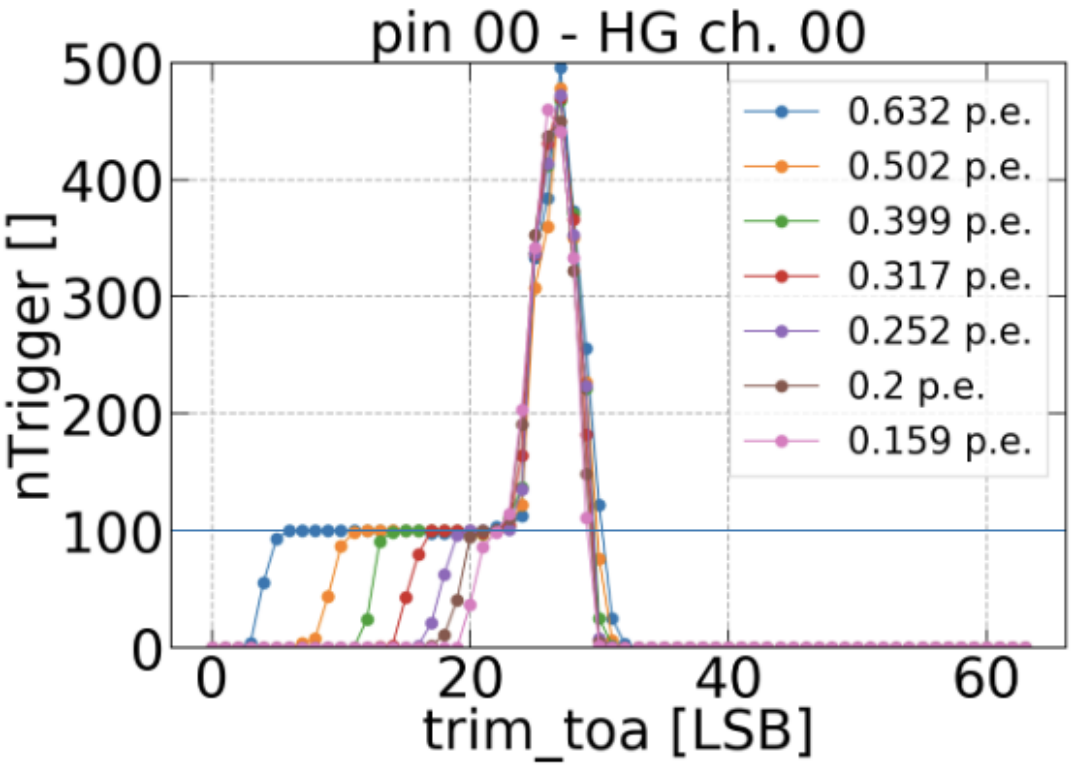
Acquisition board

We are here

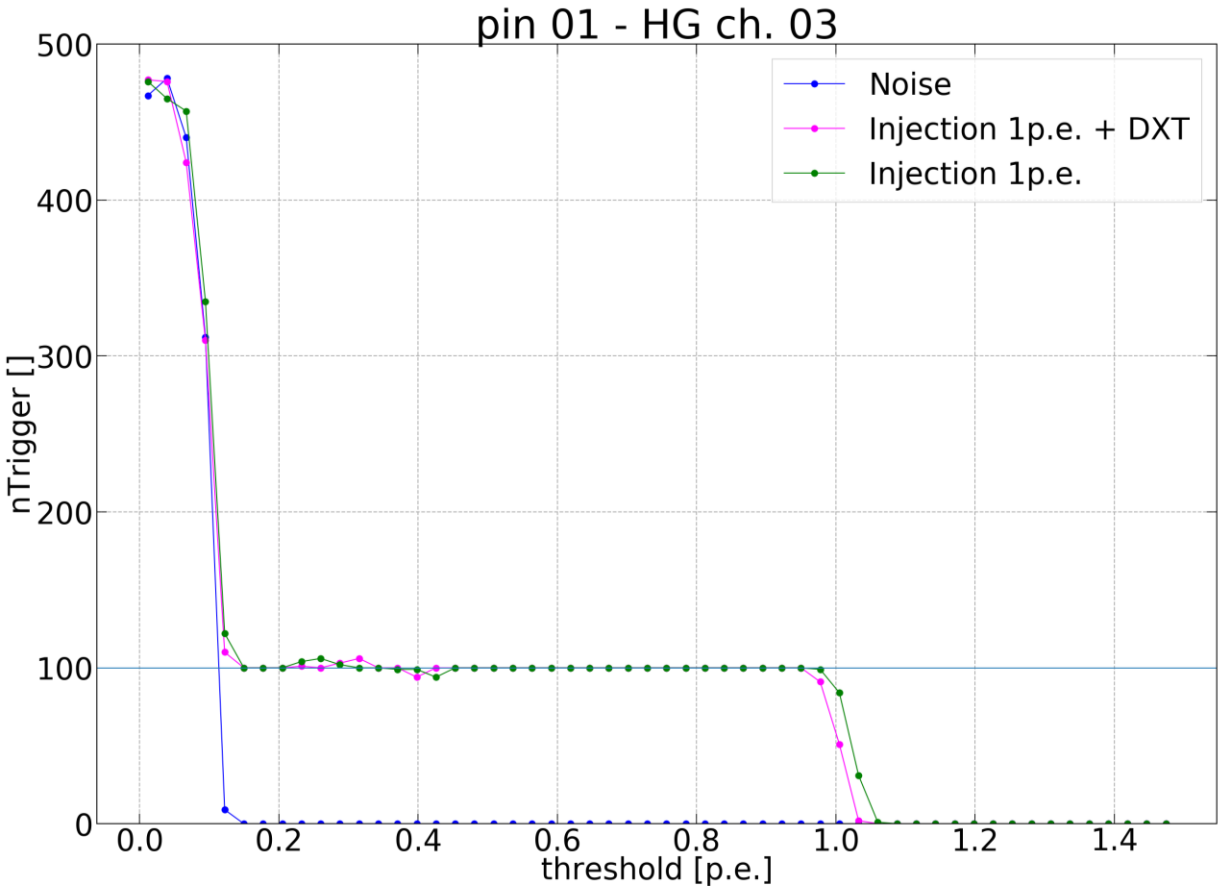
Acquisition board with reconstruction

Backup

Threshold measurements with HKROC1b



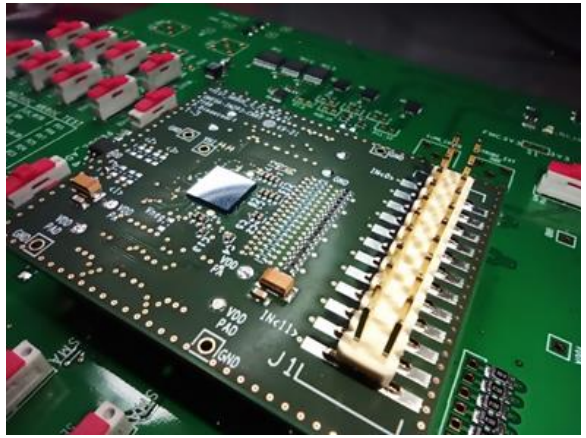
Minimum threshold of 1/6 pe



1 pe trigger efficiency with 1000 pe in another channel

Conclusion (not done yet)

- The **HKROC first version** has been submitted to **TSMC** in **August 2021** and **received** in **January 2022**.
- **HKROC performance** fits well for the HyperK experiment:
  - 90 % for **1/5 p.e (0.4pC)** events ;
  - Charge linearity **< ±1%** from 1 to 1250 p.e ;
  - Charge resolution **< 0.1 p.e** @≤ 10 p.e
  - TDC resolution : **150 ps** @1 p.e; ≤ 30 ps @ 10 p.e
  - Hit rate : **950 kHz** in SN mode

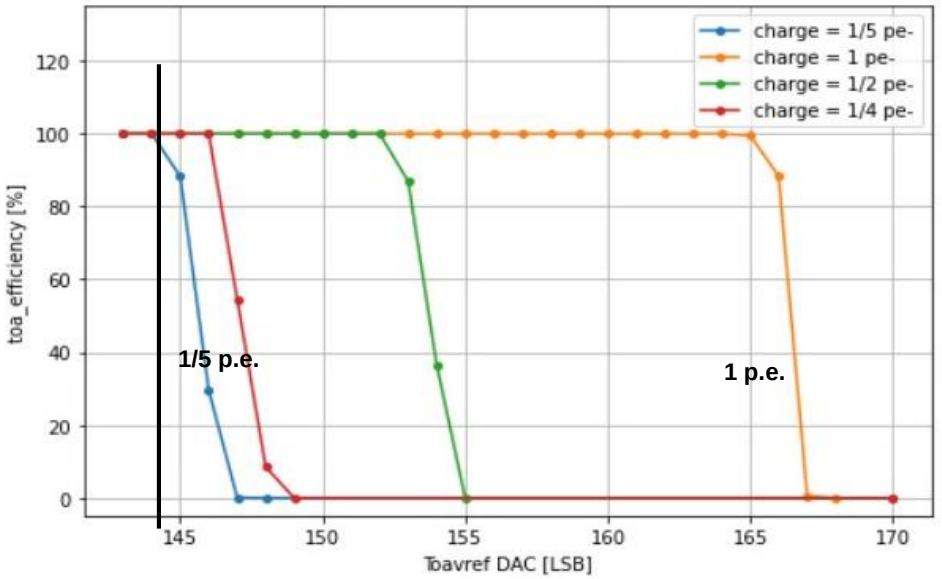


- A “pre-production” version of the ASIC HKROC (**HKROC V2**) was submitted in July 2022 to fix few minor bugs (crosstalk; …) and will be tested at the end on this year

- Current version is mounted on board through a flip-chip process but **1000 HKROC** will be packaged in **17x17 BGA package** with 400 balls (0.8 mm) and to be received in October 2022.

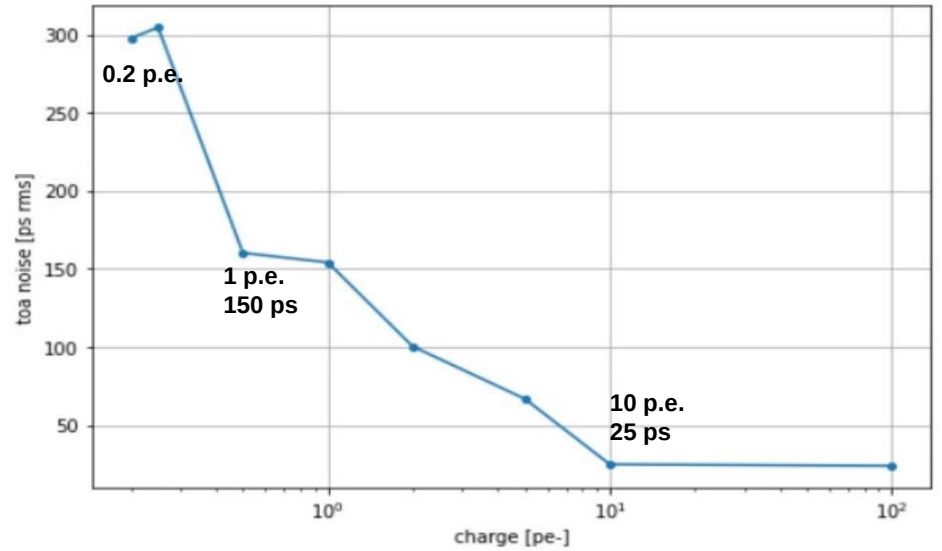
HKROC0 Trigger measurements

The HyperK specifications require the trigger **threshold** to be set at **1/6 p.e (330 fC)**



- **Hit efficiency : 90 % for 1/5 p.e events (400fC)**

  ~100 % if ≥ 1/4 p.e
- Extracted **threshold** value corresponding at **1/6 p.e**
- **Very low noise** : < 1 Hz **(0 noise hit in 10s @ 1/6 of p.e.)**



TDC characterization with **1/6 p.e. threshold**

TDC resolution :

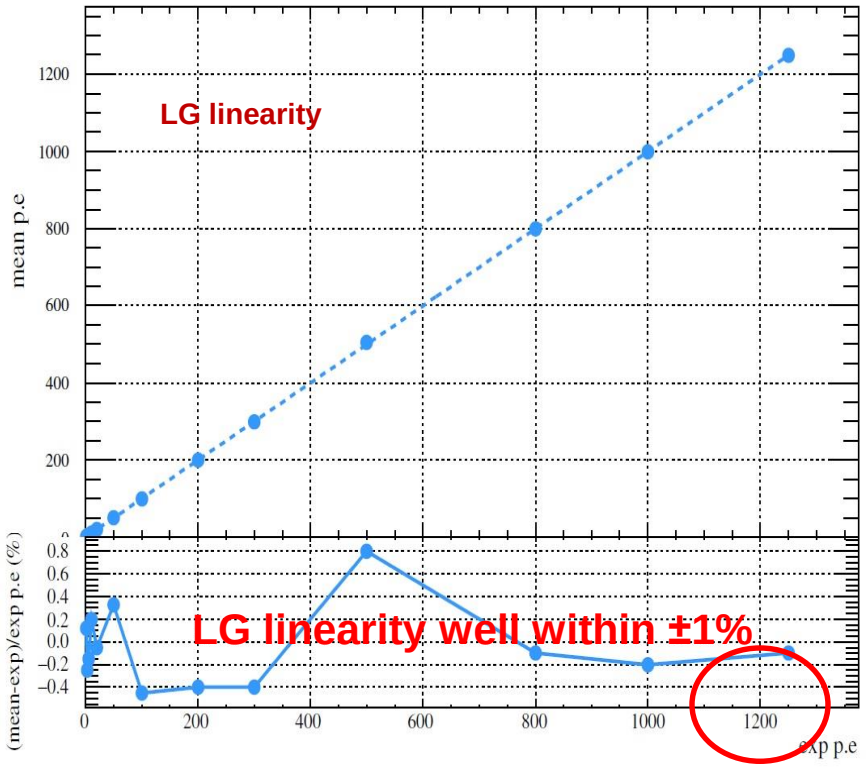
150 ps rms @ 1 p.e [300 ps required]

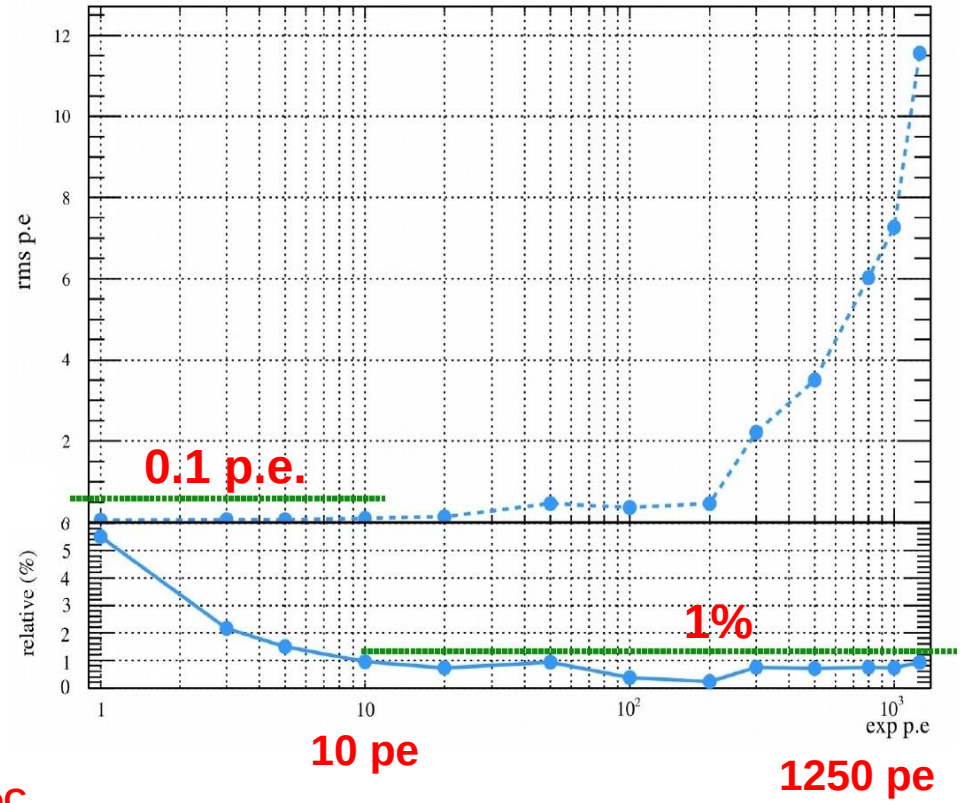
≤ 25 ps rms @ 10 p.e [200 ps required]

- Excellent agreement with HK requirements

HKROC0 Charge measurements

The **whole** acquisition **chain** is tested:
The signal is **amplified**, **auto-triggered** and **converted** by the internal **ADC**.





HG, MG and LG tested!!

Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

The charge measurements Fulfill the HK requirements!!!

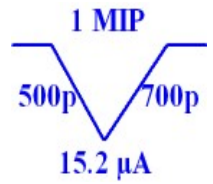
Charge resolution :

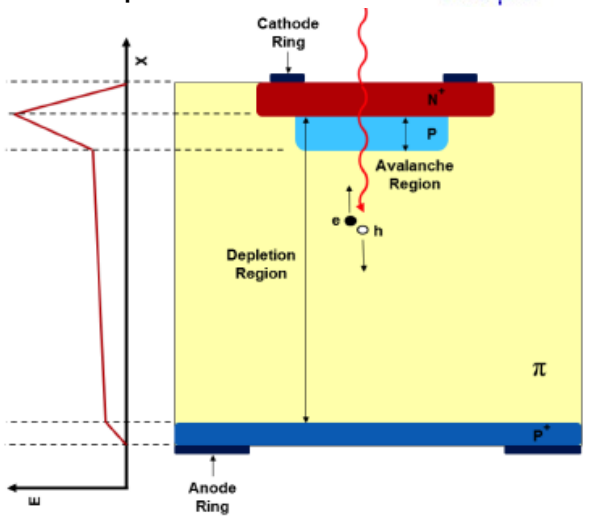
< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

High Granularity Timing Detector in HL-LHC

LGAD sensor
1.3 x 1.3 mm^2
Thickness = 50 µm
Cd = 4 pF



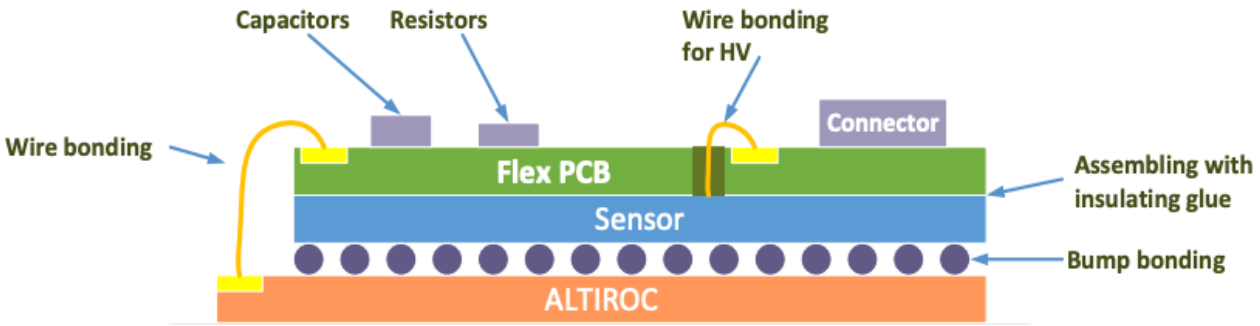


ASIC'S REQUIREMENTS

225 channels
Minimum charge : 2 fC
Charge dynamic : up to 100 fC
Noise : < 0.5 fC or 3 ke^-
Cross-talk : < 2 %
Timing precision : 35 ps for 10 fC
(per hit) 70 ps for 4 fC

Calibration LGAD-like injection :
Range : 0 – 100 fC
Rise time : 0.5-1.5 ns

Luminosity : Number of hits per bunch crossing for 2 time windows



Talk on the long Flexible Printed Circuits from Marisol Robles Manzano on Thursday, 9h20

TOA TDC
Resolution : 20 ps
Measurement window : 2.5 ns
Conversion time : < 25 ns

TOT TDC
Resolution : 120 ps
Dynamic range : 20 ns
Conversion time : < 25 ns

Radiation tolerance
TID : 2 MGy w/SF=2,25
NIEL : 2.5 10^{15} n_{eq}/cm^2 w/SF=1.5
SEE : 10^{15} n_{eq}/cm^2 w/SF=1.5
SEU rate : < 5 % per hour

ASIC power dissipation < 1.2 W
Per channel :
Analog very front-end : < 2 mW
TDC : 0,5 mW at 10 % occupancy
Digital : < 2 mW

ATLAS HGTD: ALTIROC ASIC

- **ALTIROC (**Atlas Lgad Timing Integrated ReadOut Chip)
  - Design under OMEGA responsibilty - Collaboration CERN Geneva, LPCF Clermont-Ferrand, IFAE Barcelona, SLAC Stanford, SMU Dallas
  - 20 ps timing silicon timing detector for jet identification and pileup rejection

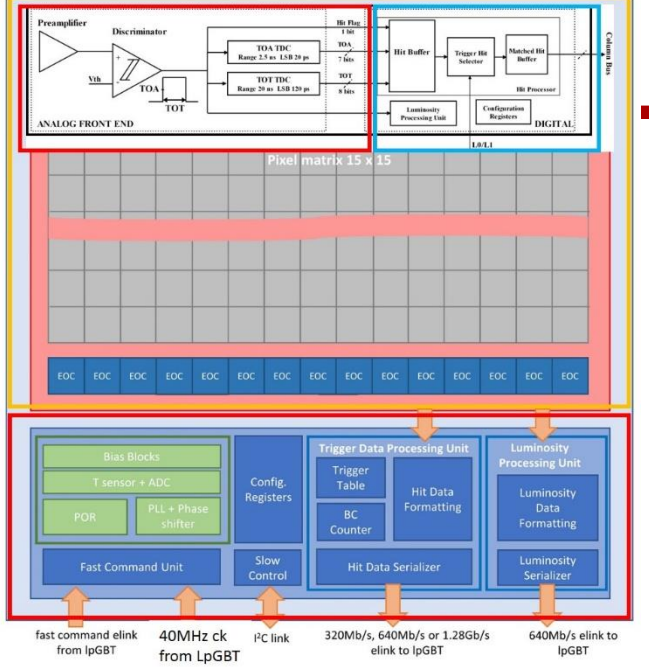
  ⇒ Pixel ASIC for precise timing measurements
    - **Qmin/Cd ~ 500 µV** with **Cd ~4 pF** (1300 x 1300 µm2) and **Vth min= 2 fC** to be compared with other timing ASIC for which Qmin/C > 2 mV with Cd ~ 50 fF (50 x 50 µm^2) and Vth min = 0.1 – 0.2 fC

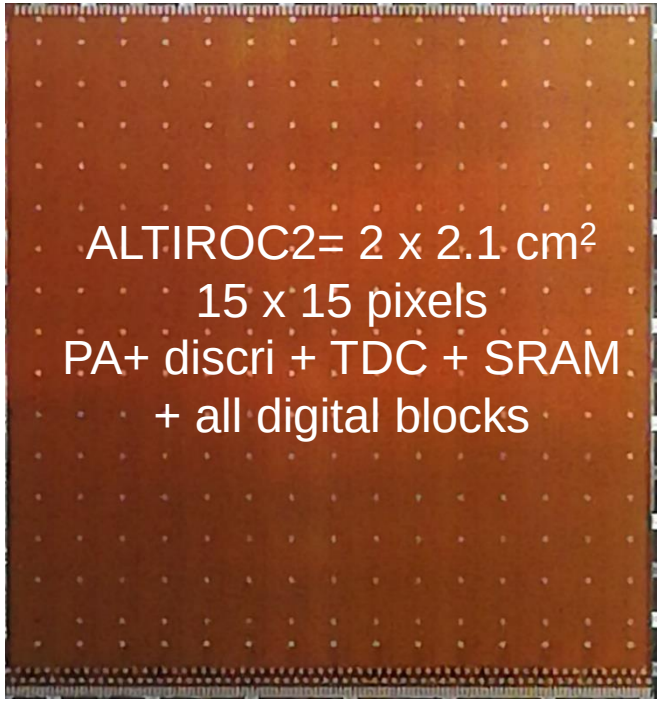
  ⇒ Mix of requirements specific to calorimetry and some of the requirements specific to pixel ASICs for trackers

  ⇒ Mix of Analog on Top design for the floorplan and analog performance + Digital on Top design for digital part (70% of the ASIC)

  - ALTIROC2 : first 225 channels full matrix LGAD readout chip with **1 GHz** preamplifier **4 pF** detector capacitance = **new territory in HEP**

- See details in https://indico.cern.ch/event/1127562/contributions/4904499/attachments/2511666/4317317/ALTIROC2_ATLAS_HGTD.pdf

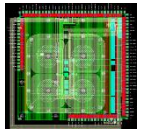




ALTIROC GENEALOGY

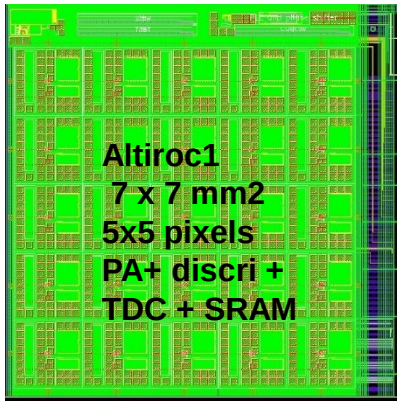
TSMC 130nm

2016-2017



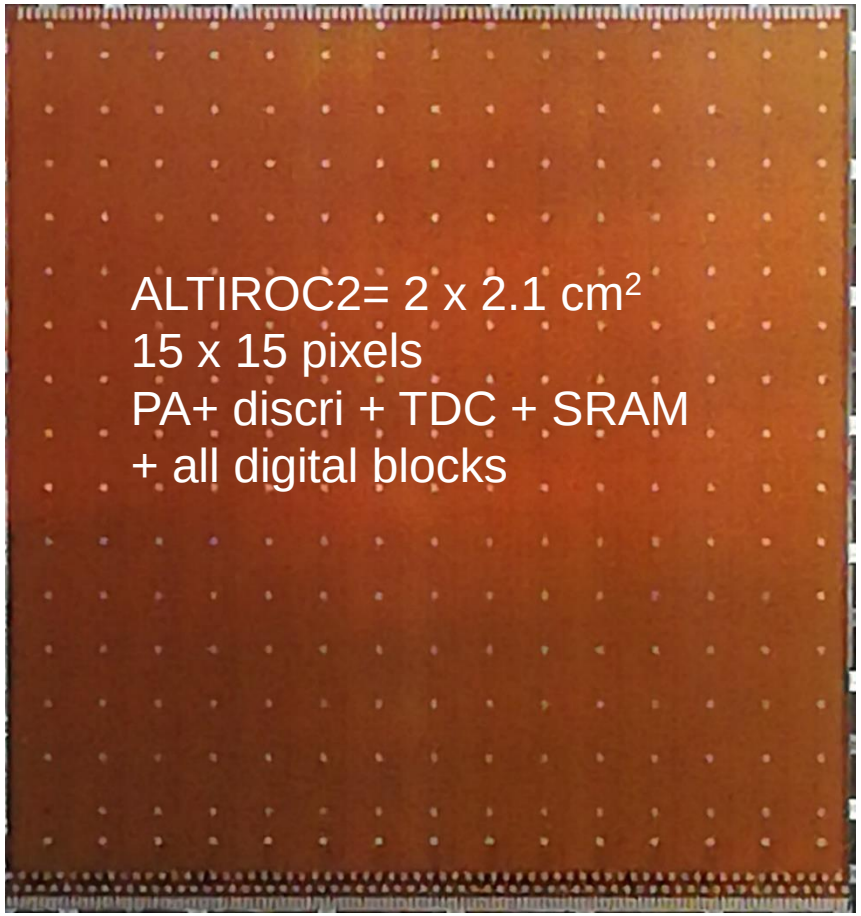
Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

2018-2019



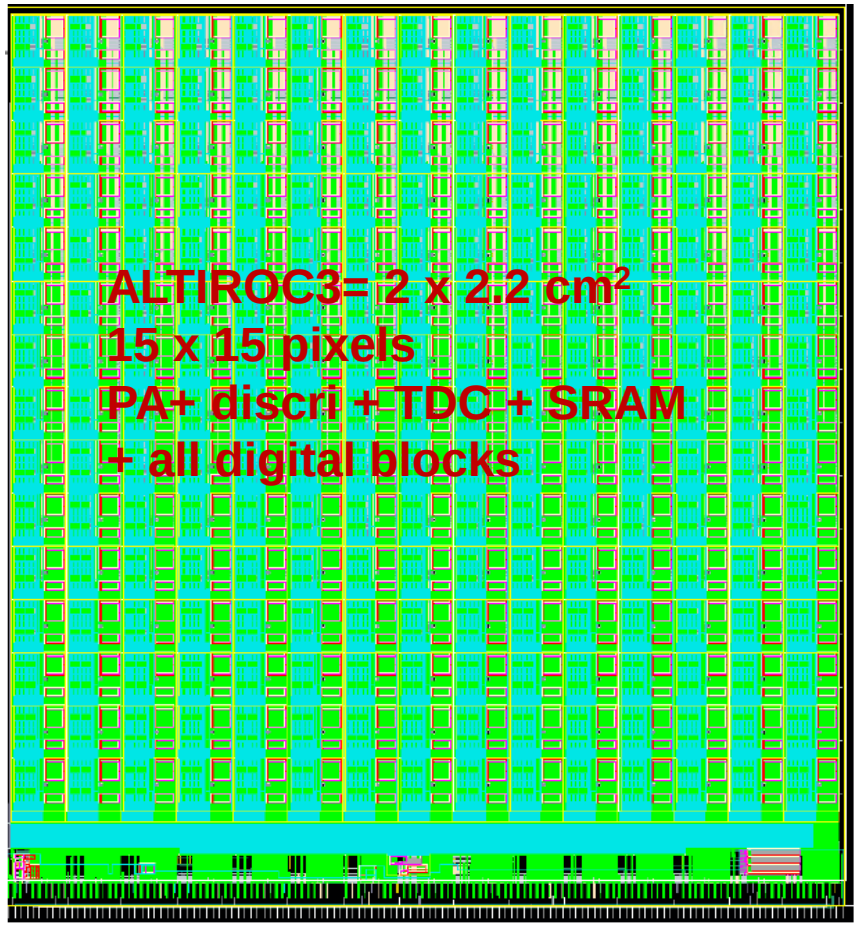
Altiroc0 and 1:
No digital,
To validate the FE part at system level
(= ASIC bump-bonded onto a sensor)

2019-2021



ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

2021 - 2022



ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

Summary of the HKROC0 performances

Item measured	Performances
Trigger efficiency at 1/6 p.e.	$> 90\%$ for 1/5 p.e signals 100% for $\geq 1/4$ p.e signals
Trigger noise at 1/6 p.e.	< 1 Hz (No trigger observed in 10 s)
TDC resolution	150 ps at 1 p.e, 70 ps at 5 p.e, 25 ps > 10 p.e Validated with PMT
Charge linearity	$< 0.5\%$ in high & medium gain channels $< 1\%$ in low gain channel up to 1250 p.e Validated with PMT
Charge resolution	< 0.1 p.e for signals up to 10 p.e $< 1\%$ beyond 10 p.e signal Validated with PMT
Dead-time & pile-up	≤ 30 ns for two signals of same amplitude ≤ 30 ns for a prompt ≤ 5 p.e and secondary of 1 p.e < 1 μs for a prompt signal ≤ 850 p.e and secondary 1 p.e
Maximal hit-rate w/ 100% eff.	415 kHz in normal mode 950 kHz in SN-mode Potential extension beyond to be studied.
Cross-talk	Hit probability in neighbouring channel of a 1250 p.e signal is $< 0.1\%$ *Note that cross-talk found at ASIC level, but cut by FPGA. Identified and will be removed in ASIC v2.*
Maximal hit-rate w/ 100% eff.	415 kHz in normal mode 950 kHz in SN-mode Can be extended even beyond for v2.
Temperature dependency	mean time $\Delta T = 17.5$ ps/°C rms time $\Delta T \leq 1$ ps/°C mean charge $\Delta Q = 0.1\%$/°C (no correction) charge variation has no dependency
Power consumption (W)	≤ 6.6 W for 24 PMTs
Resistance to HV	Received 1,000 2000 V discharge from PMT-base Unprotected ASIC received 7×10^{10} 7V injections (> 500 yrs of HK) without any impact on performances Validated protection circuit itself saturates signals > 7 V to 7 V.
Failure rate / year	ASIC failure $\leq 0.03\%$

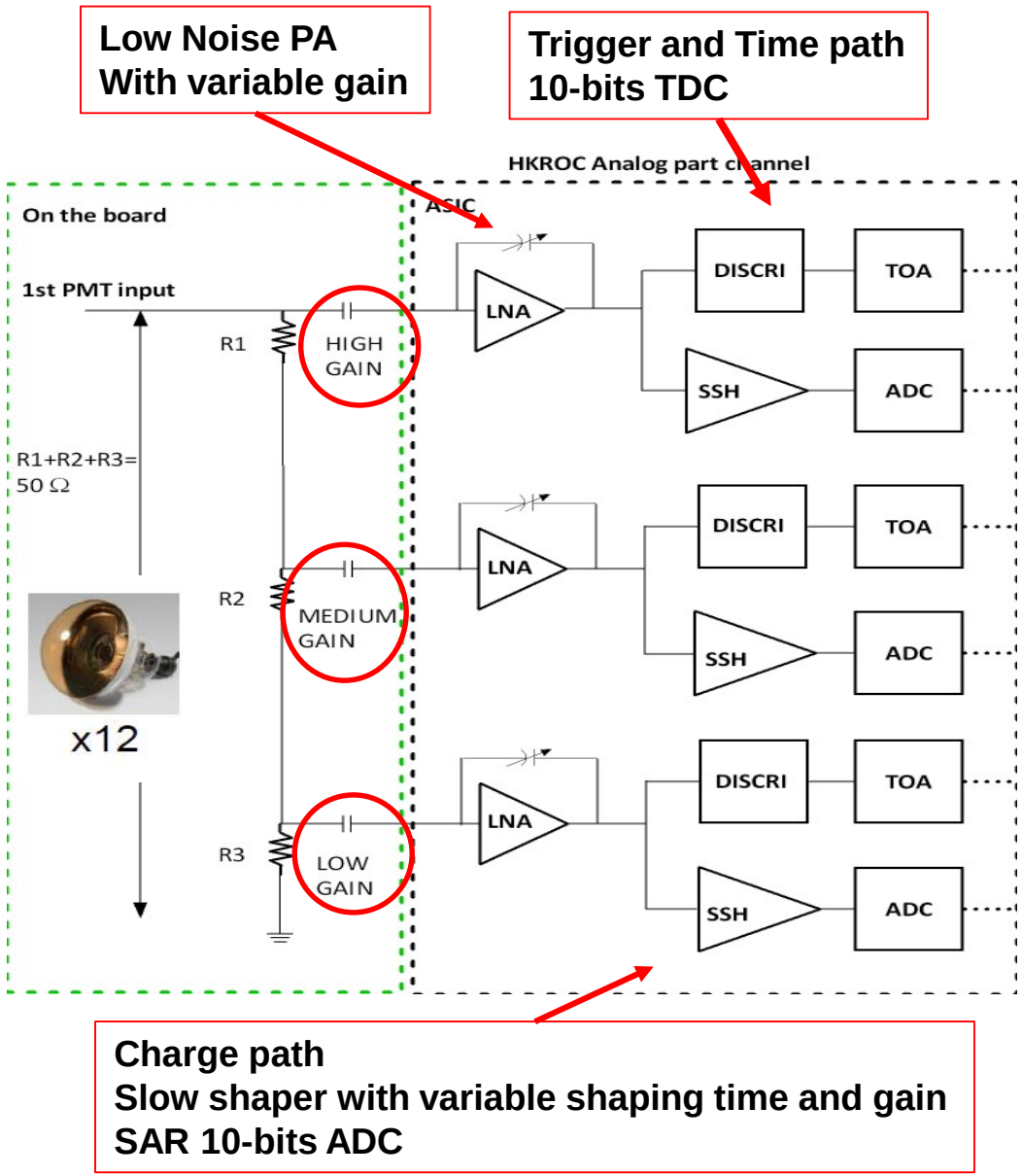
HKROC0 perf.

Min requirements	
Discriminator **threshold**	**1/6 p.e.** (**0.33 pC**)
Charge linearity	1% for 1 p.e. to **1250 p.e.** (**2 pC to 2500 pC**)
Charge resolution	**0.1 p.e. for < 10 p.e.** (**0.2 pC** for Q< 20 pC) **Better than 1% for >10 p.e.** (1% for 20 pc)
Maximum **hit rate**	**1 MHz/ch** **For close Supernova**
Timing resolution	**300 ps for 1 p.e.**(2 pc) **200 ps for > 6 p.e.** (12 pC)

To extend the charge dynamic range:

1 PMT channel connected

to **3 HKROC channels**

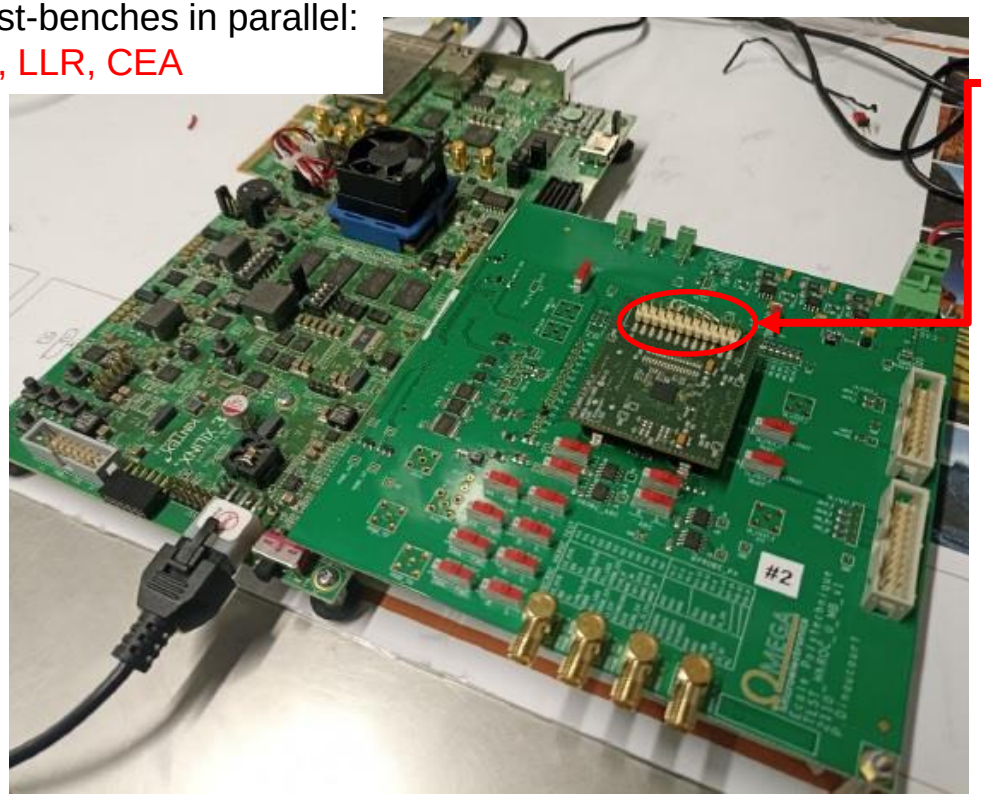


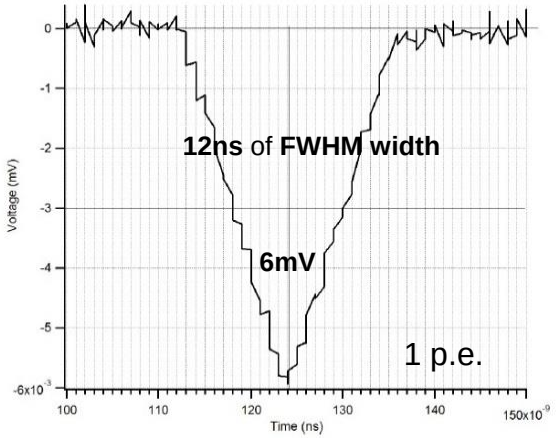
HKROC testbench

HKROC has been received in **January 2022**

A dedicated **test-board** used to test the ASIC performances. It is placed on a **mezzanine board mounted** directly through a **flip-chip process**. The mezzanine is mounted on a **mother board** that is connected to a test board " **Xilinx Kintex UltraScale FPGA KCU**"

Three test-benches in parallel:
OMEGA, LLR, CEA



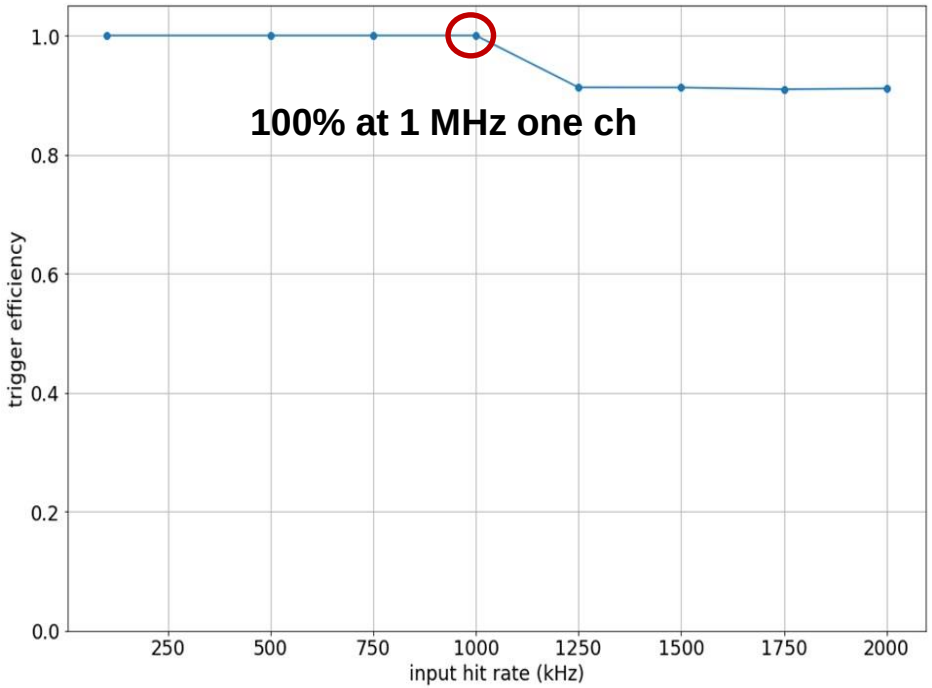


ASIC Power Consumption: 40 mW/PMT
Board Power Consumption: 3.2 W

HKROC Trigger rate measurements

FAST hit rate (~ 1MHz) required for close Supernova signals (~ 1 p.e.)

Normal mode:

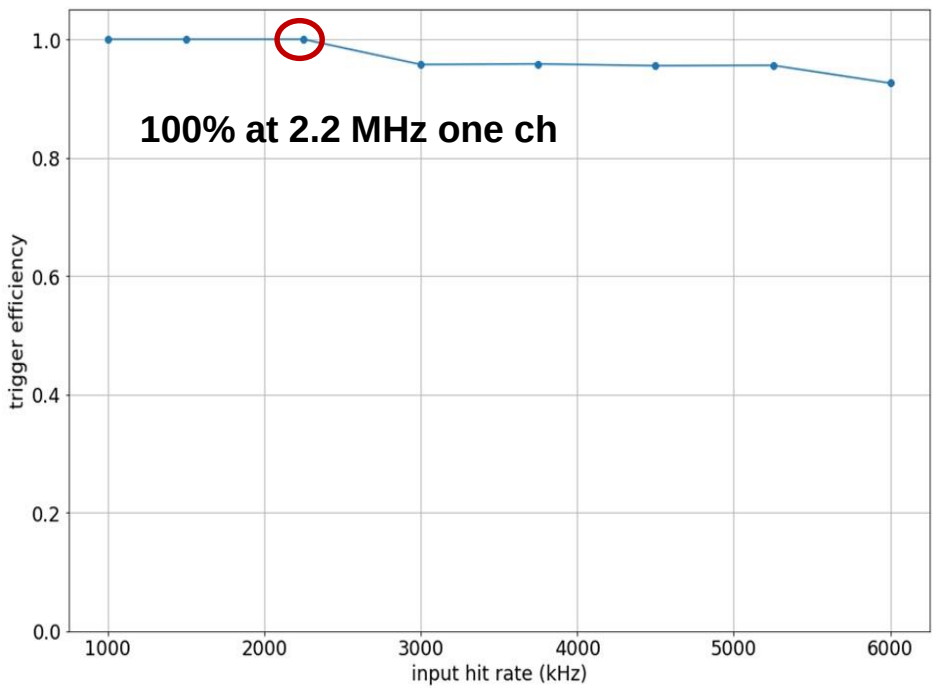


1 PMT channel →

3 HKROC channels tested in Normal Mode:

100% Trigger efficiency up to **415 kHz 3 chs**

Super Nova mode



1 PMT channel →

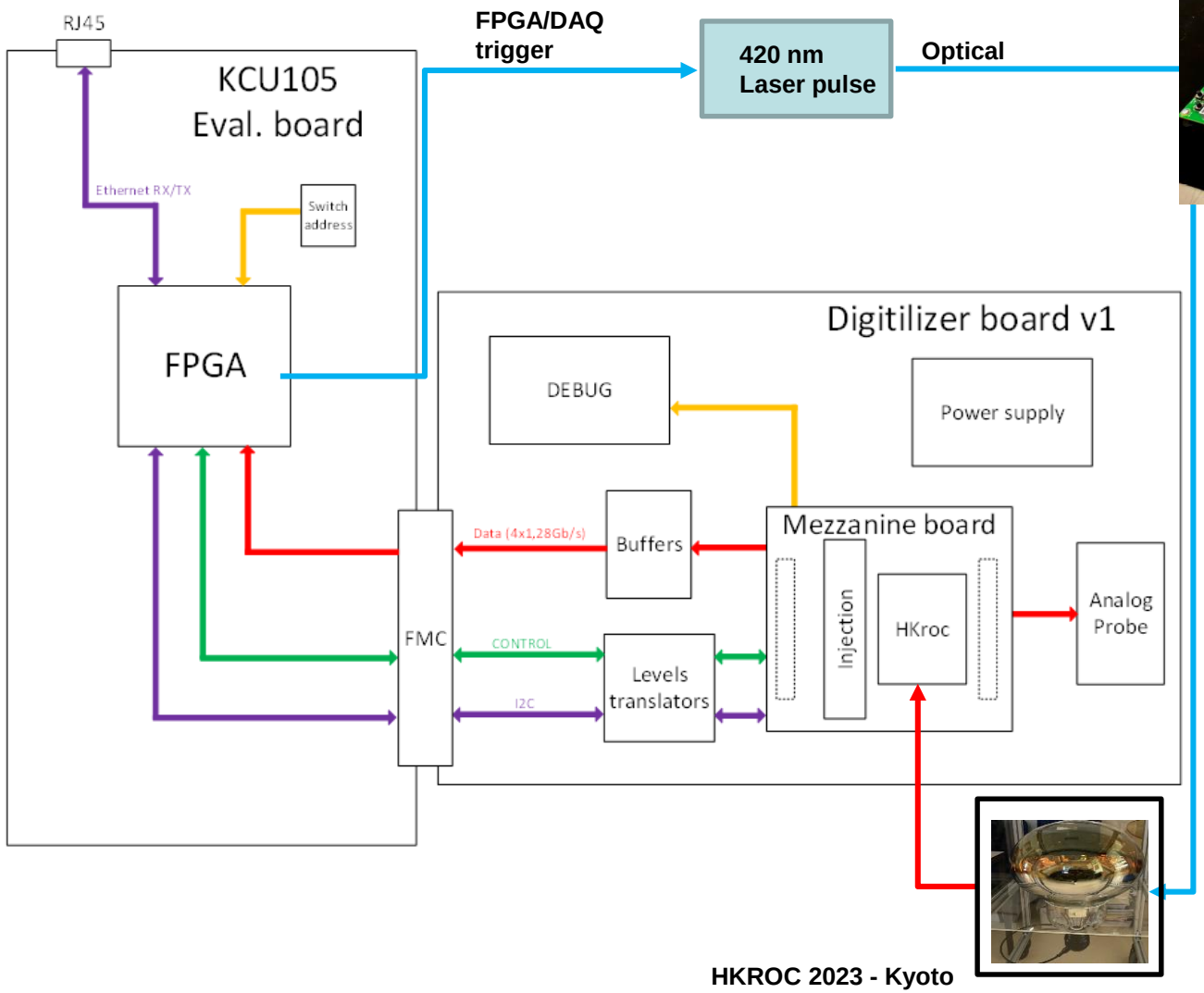
3 HKROC channels tested in SuperNova Mode:

100% Trigger efficiency up to **950 kHz 3 chs**

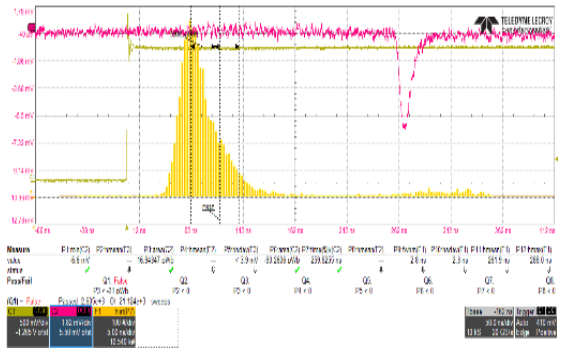
The HKROC saturation naturally appears when the chip internal memory is full. The chip has one independent memory for each read-out link at 1.28 Gb/s, which gather 3 PMTs.

PMT testbench

Connected Hamamatsu R12680 PMT to HKROC illuminated by a PILAS 402 nm laser diode



- PMT HV set to have the 1 p.e peak amplitude at -6 mV
- Charge calibrated
- TTS : FWHM= 2.8 ns, σ= 1.2 ns



PMT measurements

Trigger time distribution for events having charge ≤ 1.5 p.e : FWHM of **2.6 ns**

- **Excellent agreement with the 2.8 ns found for the PMT only**
- Digitizer does not degrade the PMT time resolution !

The charge **linearity** is **≤ ±1%**

Exact same behavior than with the function generator.