Hyper-Kamiokande

Time Synchronization Scheme for the Hyper-Kamiokande experiment

IN2P3-IRFU-INFN

25/10/2022

Context

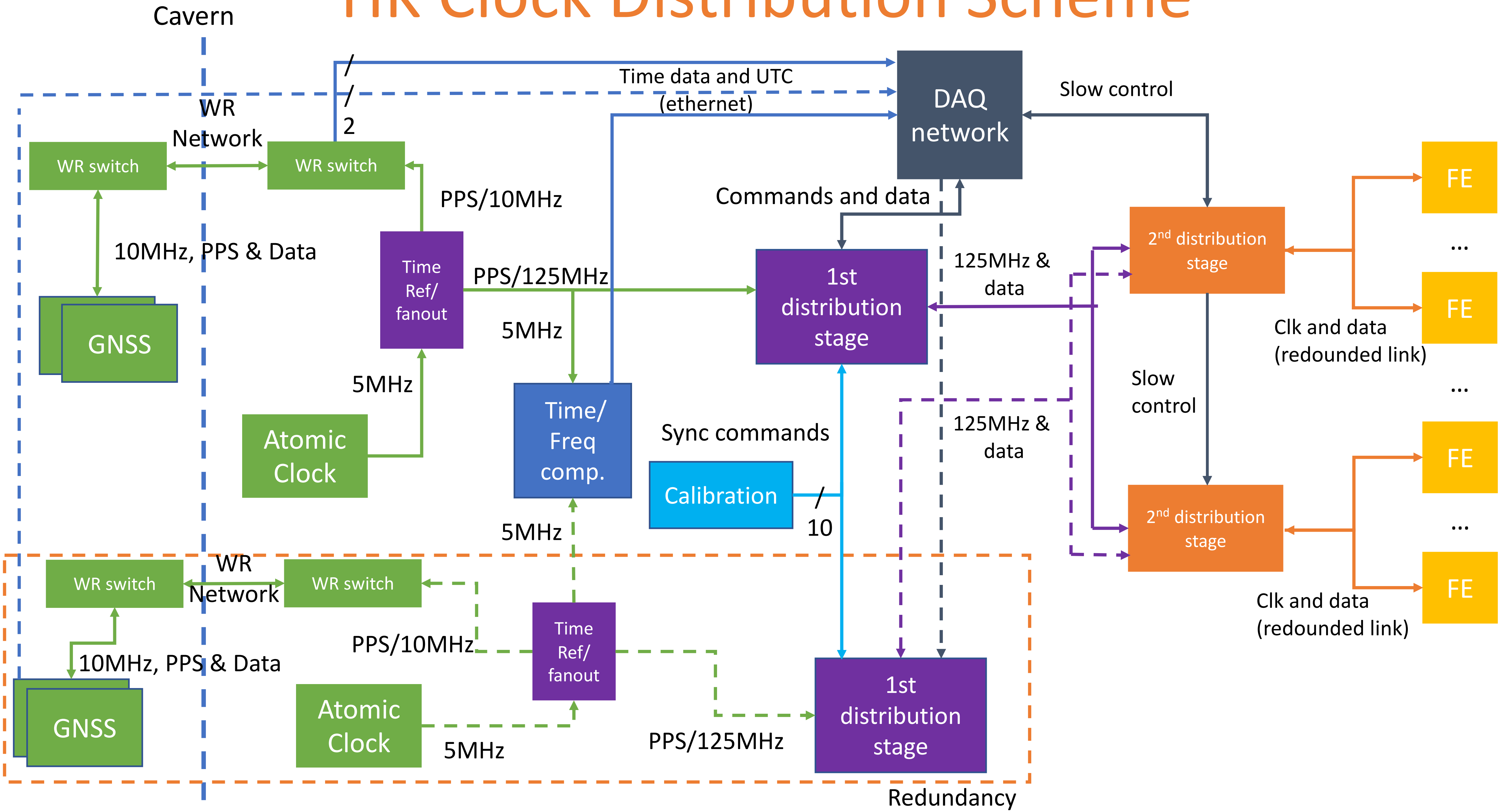
LPNHE, CEA and INFN have joined forces to design a full time distribution scheme that has been submitted to the international collaboration in April 2022. The group will be in charge of its construction, commissioning and maintenance.

The proposal envisions to provide a system that fulfills the needs of the HK far detector. Possible synergies could be found with the time generation system at JPARC, the Intermediate Water Cherenkov detector and the future ND280 upgrades (when integrated in HK).

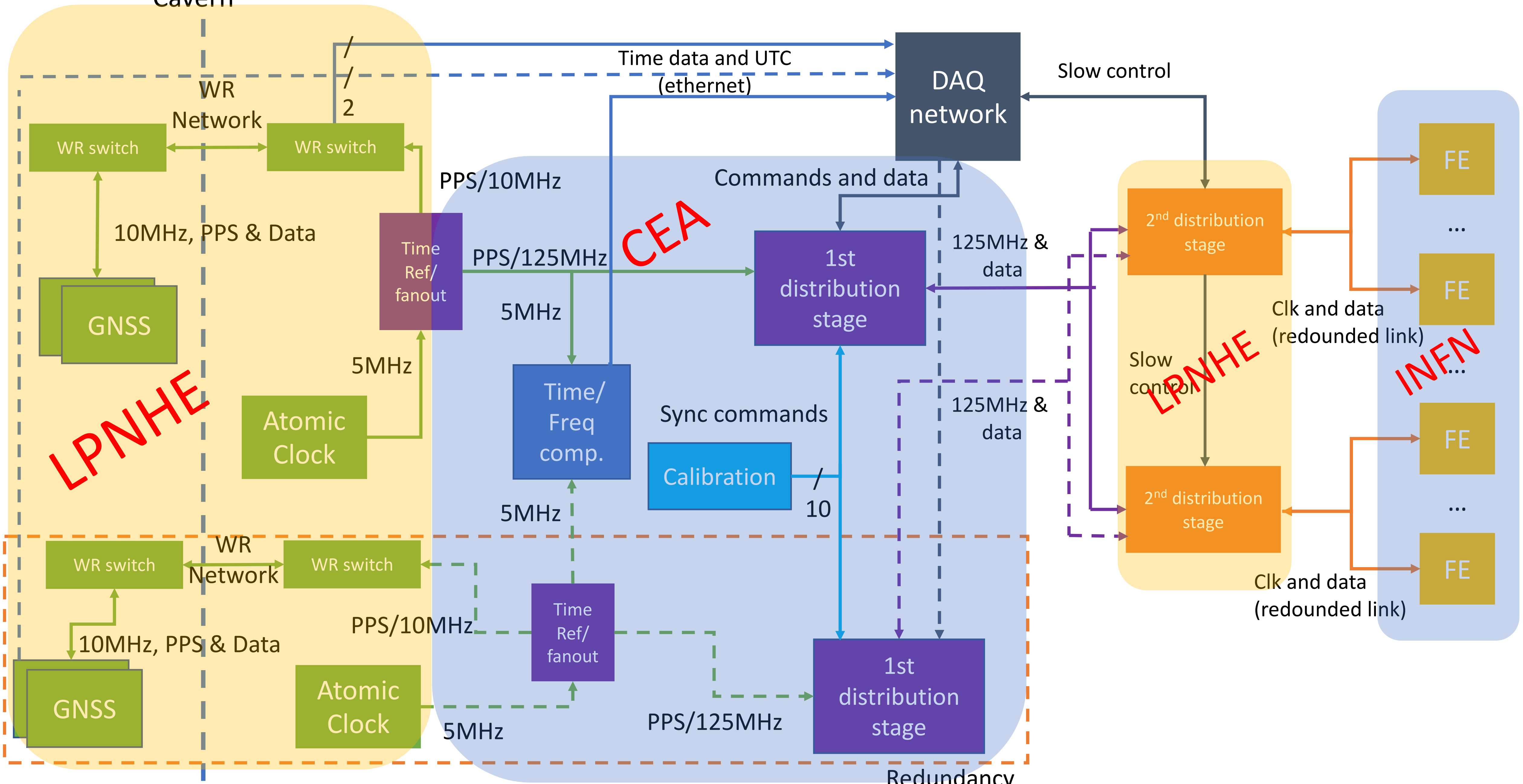
To conceive this proposal, an intense and fruitful R&D campaign has been carried out. The designed time distribution system meets all the far detector requirements.

This program takes advantage of the experience that group members have acquired in designing similar systems for other experiments and of a very fruitful collaboration with the SYRTE lab (Observatoire de Paris) responsible for the French UTC implementation.

HK Clock Distribution Scheme



HK Clock Distribution Scheme



The Clock Generation & UTC Conceptual Scheme

- The local time is generated (by a precise atomic clock) in the form of 5MHz (HK local time).

- The time reference point custom board receives this frequency, generates a local PPS and distributes them to the GNSSs and the first distribution stage. It has extra ports to compare the main and spare base cadence.

- The first distribution stage produces the clock which is sent via the second stage to the FE.

- The events will be tagged with the HK local time and converted in UTC by the DAQ. A correction algorithm will be applied to compensate the atomic clock drift.

Time Base and UTC Characterization

All the main chain components have been purchased and an extensive test campaign has been performed to precisely characterize the proposed scheme

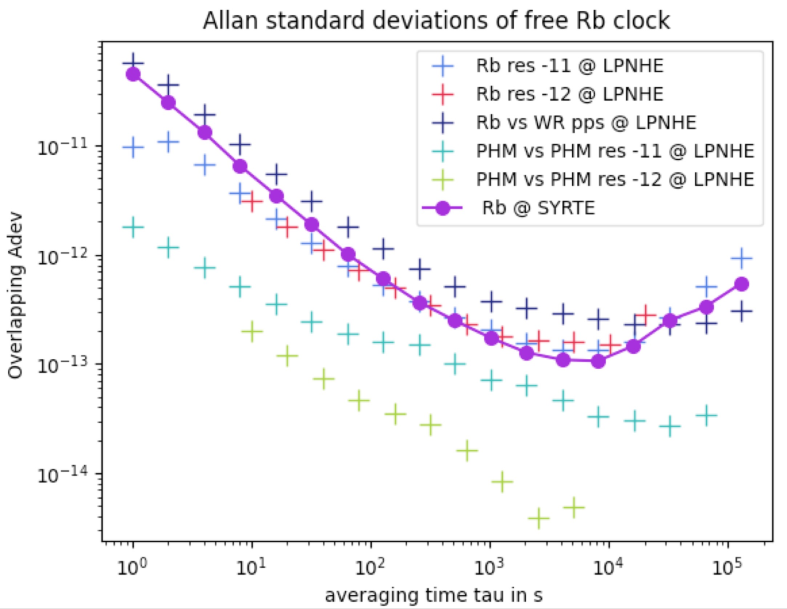
At LPNHE we have:

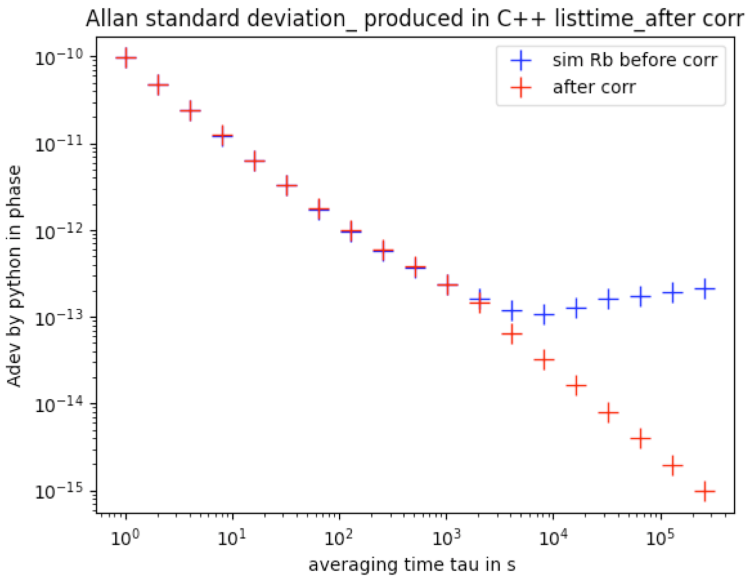
- 2 SRS SF725 Rubidium atomic clocks
- 2 Septentrio PolaRx5TR receivers + antennas
- 2 clock and Frequency counter Keysight 53220
- 1 PH1008 Passive Hydrogen Maser Atomic clock

We have also a copy of the UTC(OP) PPS and 10MHz clock sent via white Rabbit link from the SYRTE laboratory (where it is produced). This is very important time reference for comparative analysis.

Work performed by M. Guigue, L. Mellet and V. Voisin

Time Base and UTC Characterization Results and correction studies





Measured performances of the atomic clocks and GNSS receivers

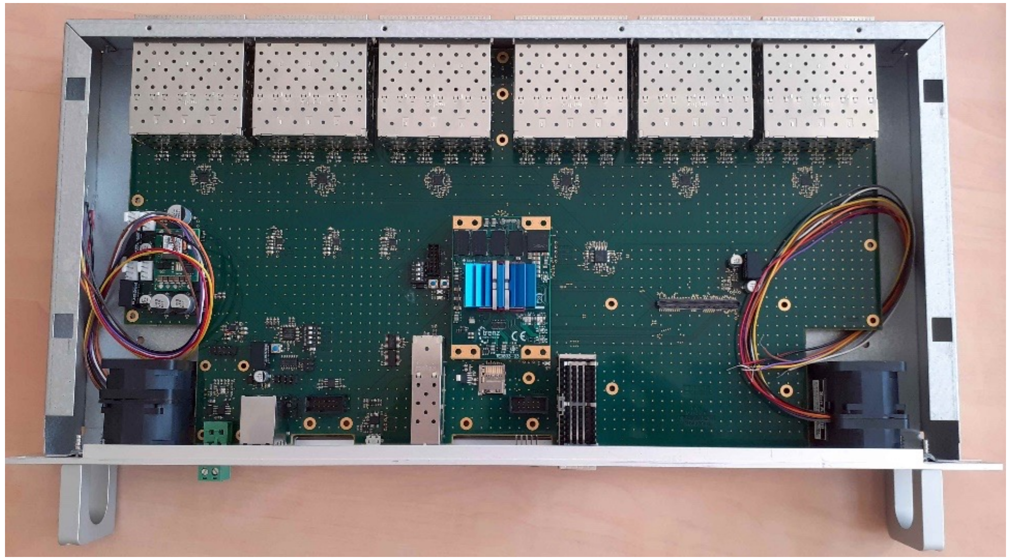
Simulated stability of the local time base after UTC conversion and correction

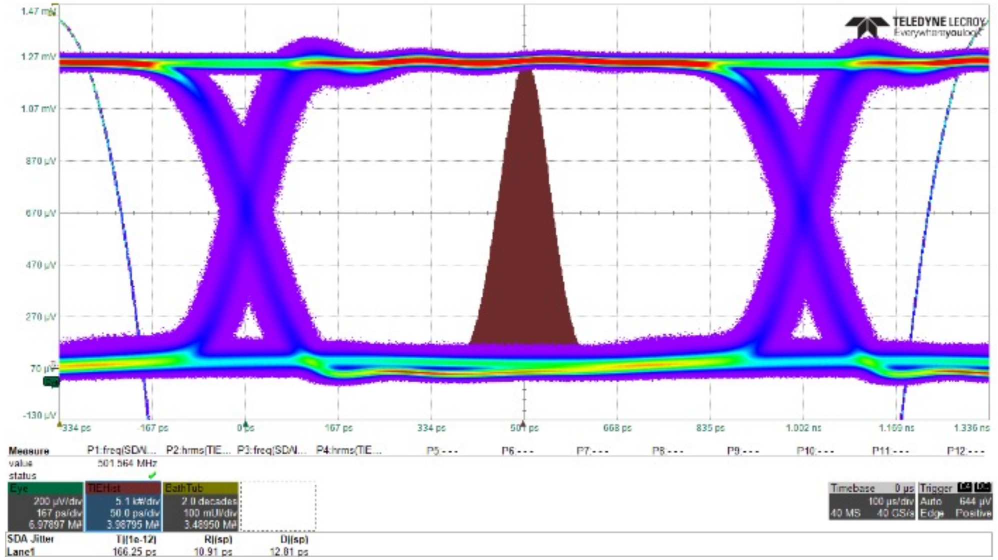
- The work on the correction algorithm is progressing and we are planning to test it on real data in the next 6 months.
- Tests at HK and JPARC site are under discussion. We hope to perform them by March 2023.
- The local time base to UTC and JPARC site expected uncertainty is about 10 ns (100 ns required).

- More detail in the L. Mellet talk https://hkdbweb.in2p3.fr/doc/meetingfiles/A00004681/Clockstudies_HKpremeeting.pdf

Work performed by M. Guigue, L. Mellet and V. Voisin

First Clock Distribution Stage Board Demonstrator





Principles

- Generic board for R&D on clock distribution based on Trenz SoC with Xilinx UltraScale+ FPGA
- Command interpreter on SoC (bare metal, Linux in final system) + Gbit Ethernet link to control PC
- Mezzanine card interfaces to external reference master clock

Optical out – 1 Gbps data mode

- Rj = 11 ps and Dj < 13 ps

Current results

- 48 TX ports tested in pure clock distribution mode, modulated clock mode and classical serial data transmission. Runs up to 1 Gpbs and shows low jitter Rj typ. ~10 ps Dj typ. <20 ps
- Stability of input to output latency at level of 10 ps after board power cycling, and comparable stability of relative phase alignment between different optical outputs
- 48 RX ports tested for 125 MHz clock feed back reception. Logic based on DDMTD technique being implemented to measure stability of distributed clock via round-trip latency monitoring

Work performed by CEA-IRFU D. Calvet and E. Molina

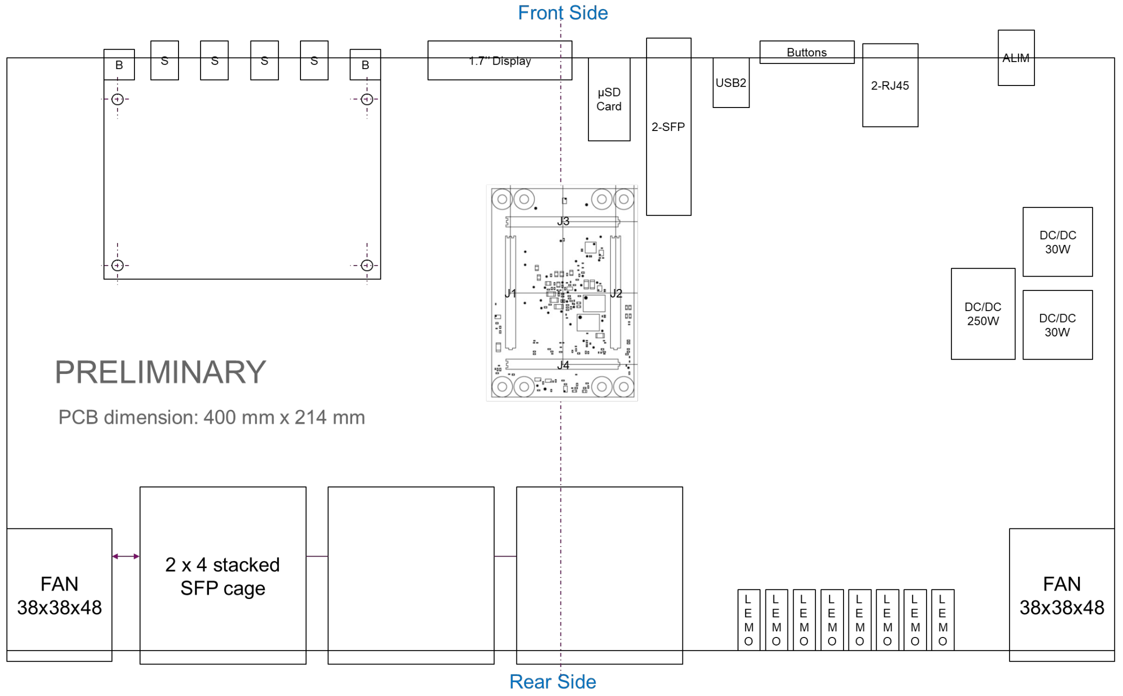
First Clock Distribution Stage Board Next Steps

48-port demonstrator – exploitation

- Continue firmware/software functionality developments and device characterization
- Incorporate clock mezzanine card – production suffered delays; board now expected mid-nov
- Validate specific blocks and various concepts as much as possible

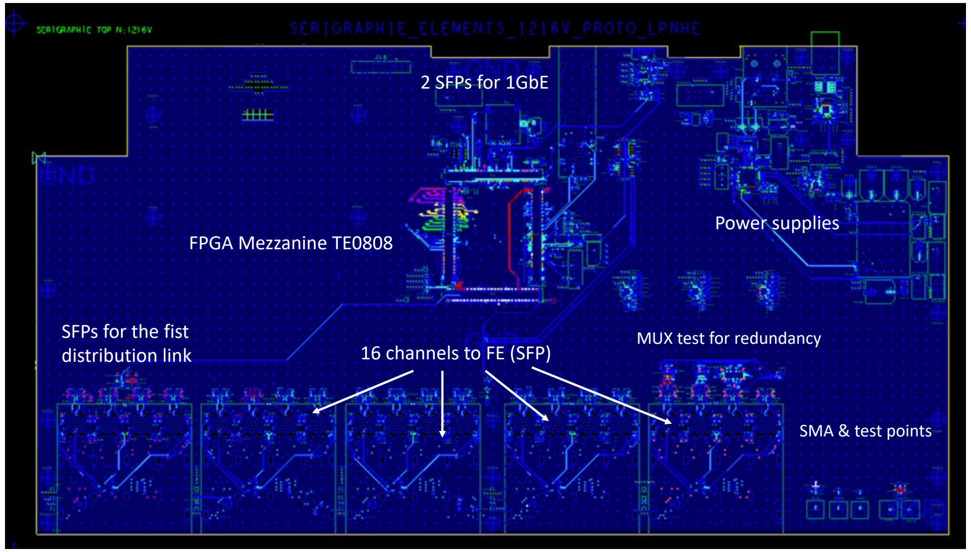
1st stage clock distributor prototype – in design

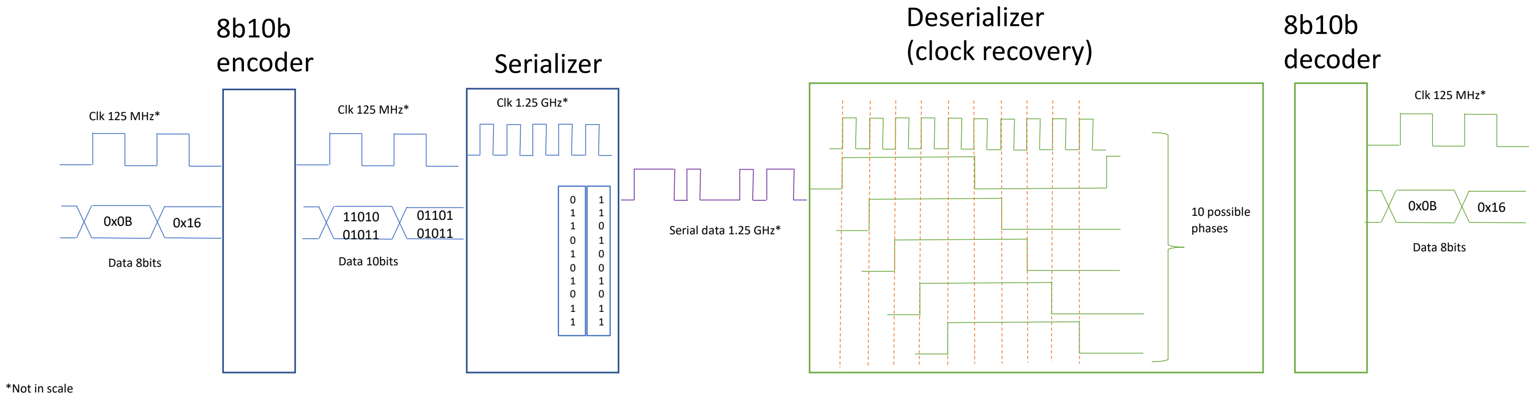
- Same concept architecture as 48-port prototype and re-use of many of its validated parts.
- Lower density of 24-ports allowable by the use of passive optical splitter in the TX direction and because only a small fraction of 2nd stage distributors will have a return optical link to the 1st stage



Work performed by CEA-IRFU D. Calvet and E. Molina

Second Clock Distribution Stage Board Concept

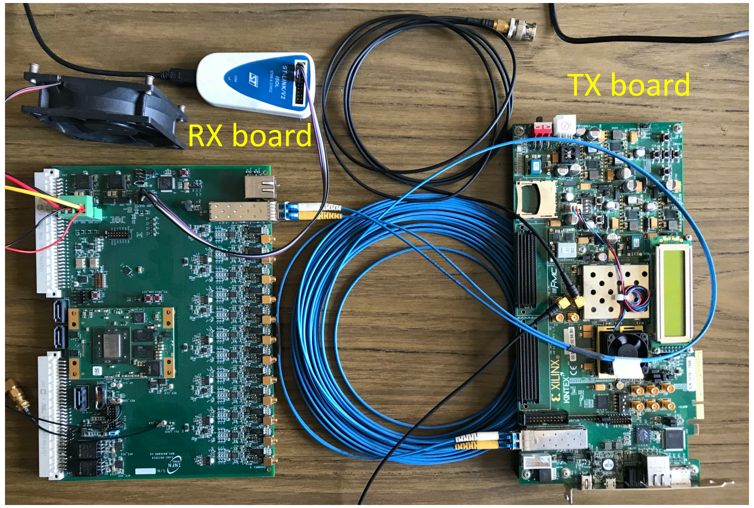


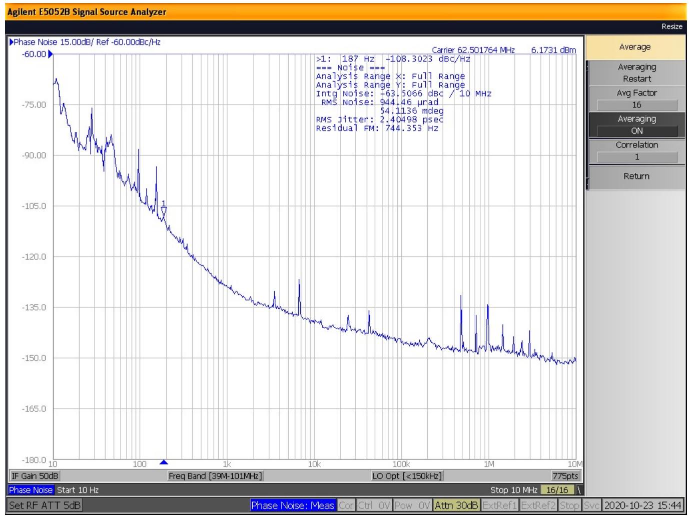


- The board receives the clock from the first stage and transmits the it to the time distribution endpoint in the front-end embedded into data via optical fiber.
- The main element is an FPGA with embedded processors mounted on Trenz module TE0808.
- It runs a custom firmware and software working under a Linux OS (Debian).

Work performed by LPNHE (s. russo and E. Pierre)

Second Clock Distribution Stage Board
Tests and Next Steps





Jitter measured at the Endpoint = 2.4ps

- Clock and data distribution have been tested with EVBs and already available boards. The jitter at the endpoint has been measured at 2.4 ps (requirement 100 ps) after a PLL jitter cleaner.
- The firmware and software development continues on EVB and it will be ported on the first prototype as it arrives. The porting time will be very short due to the high compatibility of the two systems.
- Tests will be then performed against the DPB prototypes already in our possession (thanks to C. Toledo and M. Ziembicki)

- To absorb long delay on procurement a tender for the final production mezzanine purchase has been done. The process will be finalized by mid November.

Work performed by LPNHE and INFN (s. russo and F. Ameli)

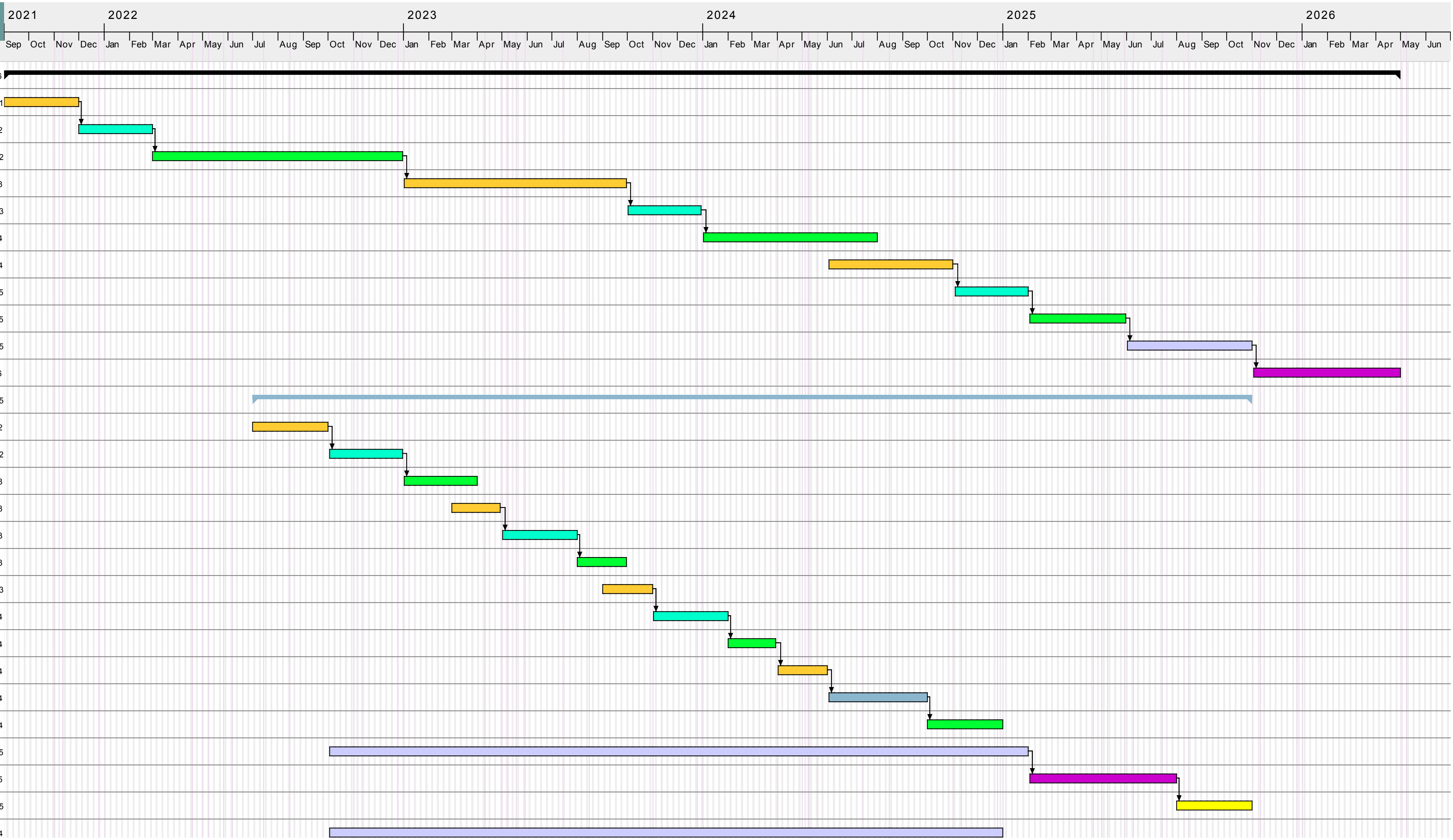
Time Distribution Endpoint

- The time distribution endpoint will be embedded in the Data Processing Board.
- We support the DPB development providing firmware/hardware IPs and components.
- A full chain composed from the second distribution stage, the DPB and digitizer will be installed at CERN as soon as a suitable space will be available (negotiations started).
- To absorb long delay on procurement a tender for the final production SFP transceivers purchase has been done. The process will be finalized by mid November.

Work performed by LPNHE and INFN (s. russo and F. Ameli)

Time Distribution Schedule

Name	Begin date	End date
1st Stage Clock Distributor	9/1/21	4/30/26
48-port clock distributor prototype - design	9/1/21	11/30/21
48-port clock distributor prototype - production	12/1/21	2/28/22
48-port clock distributor prototype - test	3/1/22	12/30/22
1st Stage Clock Distributor prototype - design	1/2/23	9/29/23
1st Stage Clock Distributor prototype - production	10/2/23	12/29/23
1st Stage Clock Distributor prototype - test	1/2/24	7/31/24
1st Stage Clock Distributor final - design	6/3/24	10/31/24
1st Stage Clock Distributor final - production	11/4/24	1/31/25
1st Stage Clock Distributor final - test	2/3/25	5/30/25
Contracting & component procurement	6/2/25	10/31/25
Production (6 units min.)	11/3/25	4/30/26
2nd Stage Clock Distributor	7/1/22	10/31/25
2nd Stage Clock Distributor Prototype #1 design	7/1/22	9/30/22
2nd Stage Clock Distributor Prot...	10/3/22	12/30/22
2nd Stage Clock Distributor Prototype #1 test	1/2/23	3/31/23
2nd Stage Clock Distributor Prot...	3/1/23	4/28/23
2nd Stage Clock Distributor Prot...	5/2/23	7/31/23
2nd Stage Clock Distributor Prot...	8/1/23	9/29/23
2nd Stage Clock Distributor Final Prototype design	9/1/23	10/31/23
2nd Stage Clock Distributor Fina...	11/2/23	1/31/24
2nd Stage Clock Distributor Final Protype test	2/1/24	3/29/24
2nd Stage Clock Distributor design finalization	4/2/24	5/31/24
2nd Stage Clock Distributor Pre-production	6/3/24	9/30/24
2nd Stage Clock Distributor pre-...	10/1/24	12/31/24
2nd Stage Clock Distributor Contract & Procurment	10/3/22	1/31/25
2nd Stage Clock Distributor Mass...	2/3/25	7/31/25
2nd Stage Clock Distributor Mass...	8/1/25	10/31/25
Time Distribution Endpoint procurment	10/3/22	12/31/24



The work is on schedule. The production is expected to be concluded in time for the assembly and commissioning in Japan

Summary

- A great synergy and collaboration has been established between IN2P3, CEA, INFN.
- The full time distribution scheme has been designed.
- Test and characterization campaigns on different subsystems have been carried out.
- First prototypes have been designed and are ready/fabricated now.
- The system will be tested together with the DPB and digitizer soon

Clock Generation & UTC - Connections

- The local time is generated (by a precise atomic clock) in the form of 5MHz in synch to each other (HK local time).

- The time reference point custom board receives the frequency, generate a local PPS and distributes them to the GNSSs and the first distribution stage. It has extra ports to compare the main and spare base cadence.

- GNSSs use the input cadence to sync the outputs and have a reference frequency more stable than the internal oscillator

Clock Generation & UTC - Connections

- 2 GNSSs receivers (connected to the same antenna) get information from the satellites and measure the time distance between the local PPS and UTC.
- The result of this measure is sent to DAQ and used to transform the local tag to UTC
- The DAQ monitors the status of the GNSSs and select which one to use

Clock Generation & UTC - Redundancy

- The full chain (atomic clock, GNSSs (x2), and first distribution stage) is replicated for redundancy
- Having a total of 4 GNSS receivers will allow the DAQ to identify if one is malfunctioning . Extra different brands receivers will be also used.
- The time distance between the 2 chains will be constantly measured and the result sent to DAQ. This info will be used in case of switch from one chain to the other

Clock Generation & UTC - Reliability

- Scheduled interventions on components will be performed to reduce the risk of failures
- A third atomic clock will be available at far detector site and periodically turned on. It will serve as cold spare used if the main or the hot spare needs maintenance
- All the atomic clocks will be measured against the so-called travelling station every 3 / 4 years.
- The GNSS receivers will be changed before the end of life.
- The maintenance cost needs to be included in the budget request

Septentrio PolaRx5TR calibration

Our receiver (RINEX name: LPN1) was calibrated against one at Observatoire de Paris (OP73) in turn calibrated against a travelling station from Bureau International de Poids et de Mesures (BIPM, responsible of defining UTC). OP73 is then a so-called level 1 receiver and LPN1 has been calibrated as a level 2.

The receiver internal delays were measured for both GPS and Galileo constellations.

The combined uncertainty of the LPN1 station hardware delays calibration is 4 ns. This is the conventional uncertainty applied after a “direct calibration” in the TAI system.

Septentrio PolaRx5TR calibration

The two tables correspond to GPS (P1 and P2 codes) and Galileo (E1 and E2a) codes.

Receiver	Reference	MJD of Measurement	REFDLY	CABDLY	P1 DLY	TDEV	P2 DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	29.500	NC	26.300	NC
LPN1	OP73	59508 – 59514	88.3	127.1	25.832	0.024	22.871	0.022

Receiver	Reference	MJD of Measurement	REFDLY	CABDLY	E1 DLY	TDEV	E5a DLY	TDEV
OP73	Ref	59508 – 59514	85.2	129.6	31.700	NC	31.300	NC
LPN1	OP73	59508 – 59514	88.3	127.1	28.242	0.040	25.431	0.034

The values will be configured in the receiver and a correction will be applied to the UTC time. Mixing the two constellations' data will be done to provide the UTC time.

Time Base and UTC Characterization

The work on the time base characterization continues and an extensive test campaign is ongoing (thanks mainly to Lucille Mellet, Vincent Voisin and Mathieu Guige).

Most of the results are summarized here:

https://indico-sk.icrr.u-tokyo.ac.jp/event/7332/contributions/22011/attachments/20557/26254/LPNHE_timingsystem_R%26D.pdf

I give just a quick recap:

Kind of Test Performed

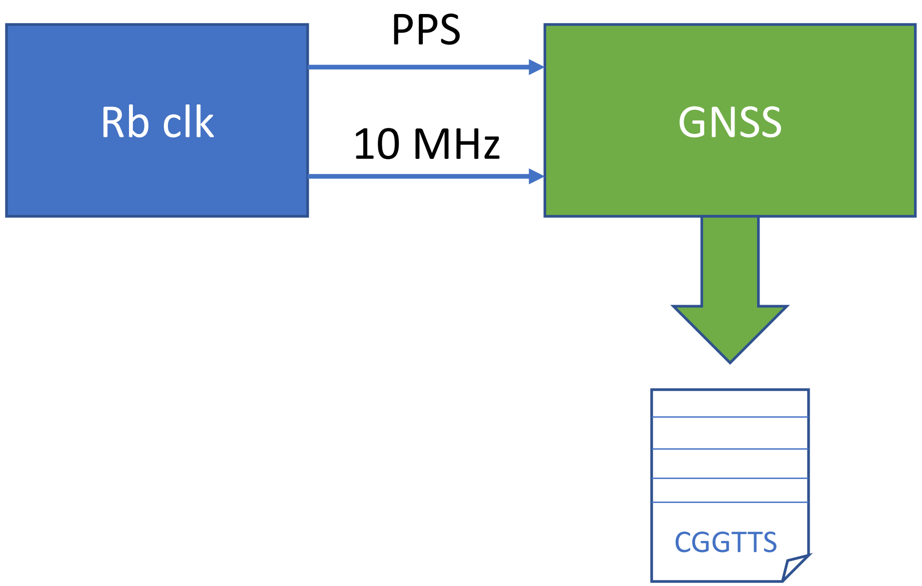
We basically perform 2 kind of tests:

- Local time base characterization. Test our proposed concept on real hardware

- Time transfer via common view: a method to measure two local time bases using the GNSS data. This method is implemented using the files published regularly by UTC(k) labs (Syrte in our case).

Local Time Base Characterization

For this test we use 1Rb clock sending 1 PPS and 10 MHz clock to the Spetentrio receiver. Thanks to the time transfer algorithm, we can estimate the drift of our local time base with respect to GNSS time (only GPS in this case)

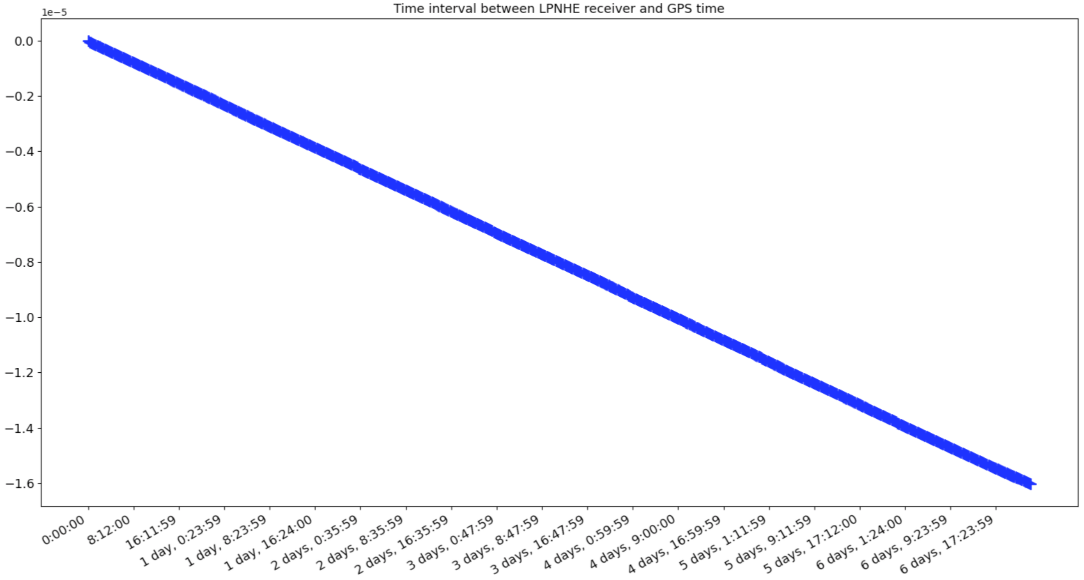


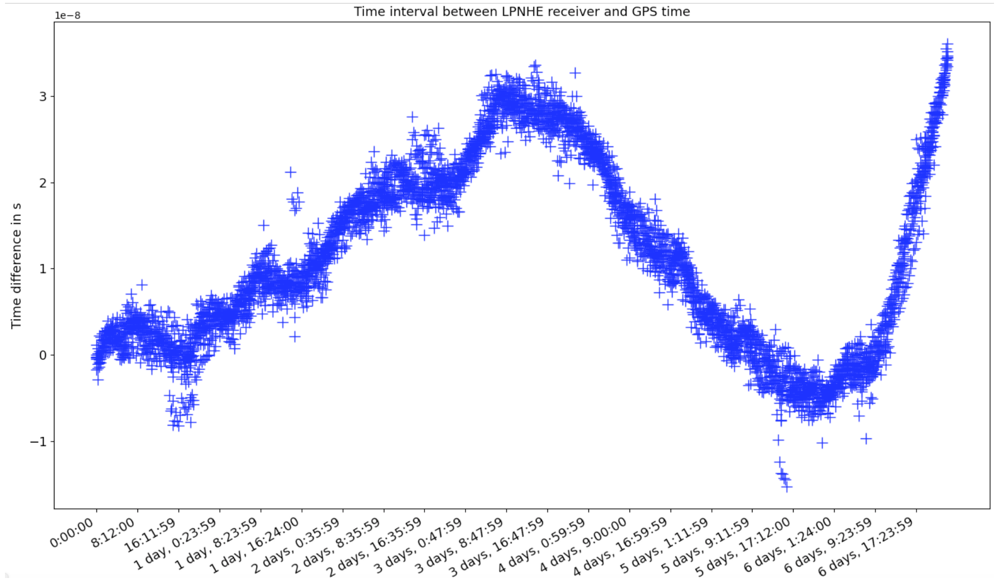
CGGTTS file with time distance
Between local time and GPS time

```
CGGTTS   GENERIC DATA FORMAT VERSION = 2E
REV DATE = 00-00-000
RCVR = PolaRx5TR (5.3.2)     SN3222543
CH = 80
IMS = PolaRx5TR
LAB = LPNHE
X = 4201670.132 m
Y = 172825.507 m
Z = 4779558.436 m
FRAME = ITRF
COMMENTS = LS=18; ElMask=0deg;
INT DLY = 25.8 ns (GPS P1),  22.9 ns (GPS P2)     CAL_ID = Calibration at OP vs OP73
CAB DLY = 505.0 ns
REF DLY = 0.0 ns
REF = SRS
CKSUM = 0b
```

SAT	CL	MJD	STTIME	TRKL	ELV	AZTH	REFSV	SRSV	REFSYS	SRSYS	DSG	IOE	MDTR	SMDT	MDIO	SMDI	MSIO	SMSI	ISG	FR	HC	FRC	CK
			hhmmss	s	.1dg	.1dg	.1ns	.1ps/s	.1ns	.1ps/s	.1ns		.1ns	.1ps/s	.1ns	.1ps/s	.1ns	.1ps/s	.1ns				
G02	FF	59693	001800	780	452	2678	6018322	-271	-513936	-272	13	61	114	3	102	13	102	13	10	0	0	L3P	6E
G04	FF	59693	001800	780	166	700	1219828	-282	-513956	-249	39	13	281	99	134	6	134	6	30	0	0	L3P	7C
G05	FF	59693	001800	780	183	3026	279947	-180	-513955	-194	43	80	257	-89	139	-78	139	-78	31	0	0	L3P	E7
G06	FF	59693	001800	780	351	2017	-3291323	-407	-513924	-267	25	35	141	27	125	25	125	25	19	0	0	L3P	A6
G07	FF	59693	001800	780	625	1419	-3723689	-282	-513929	-272	15	17	91	-5	82	6	82	6	12	0	0	L3P	68
G09	FF	59693	001800	780	505	677	2902993	-274	-513932	-248	13	73	105	11	76	-5	76	-5	9	0	0	L3P	69
G16	FF	59693	001800	780	118	411	4432147	-121	-513927	-158	42	51	387	16	78	-82	78	-82	27	0	0	L3P	98
G20	FF	59693	001800	780	460	3001	-5670792	-232	-513930	-234	22	25	113	-13	89	-22	89	-22	18	0	0	L3P	A5
G29	FF	59693	001800	780	76	3256	4549643	-265	-513933	-306	45	31	577	14	122	28	122	28	32	0	0	L3P	A2
G30	FF	59693	001800	780	430	1808	4737062	-227	-513927	-243	11	69	119	-17	108	-25	108	-25	9	0	0	L3P	BC

Local Time Base Characterization

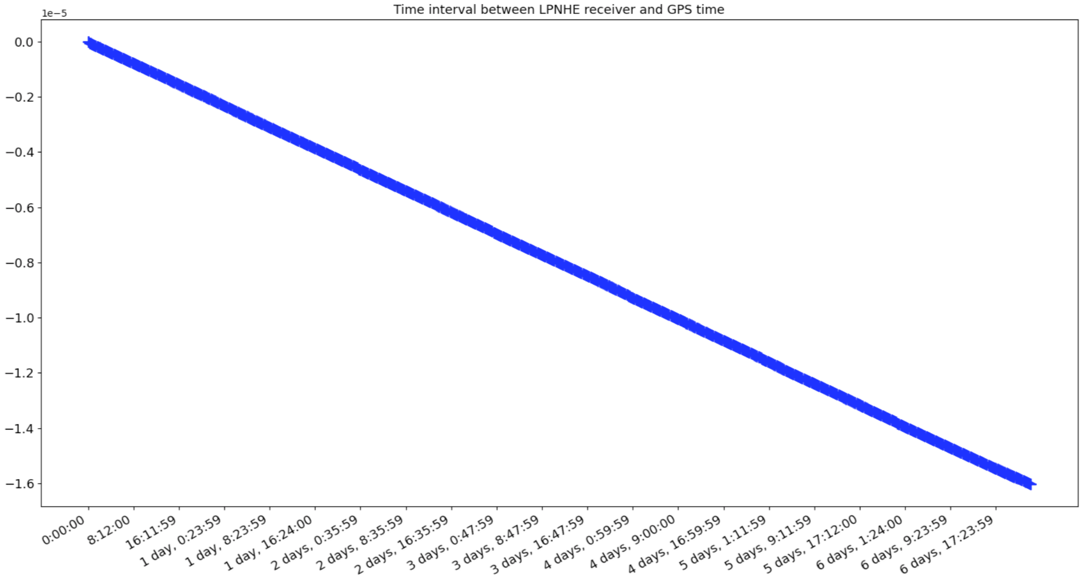


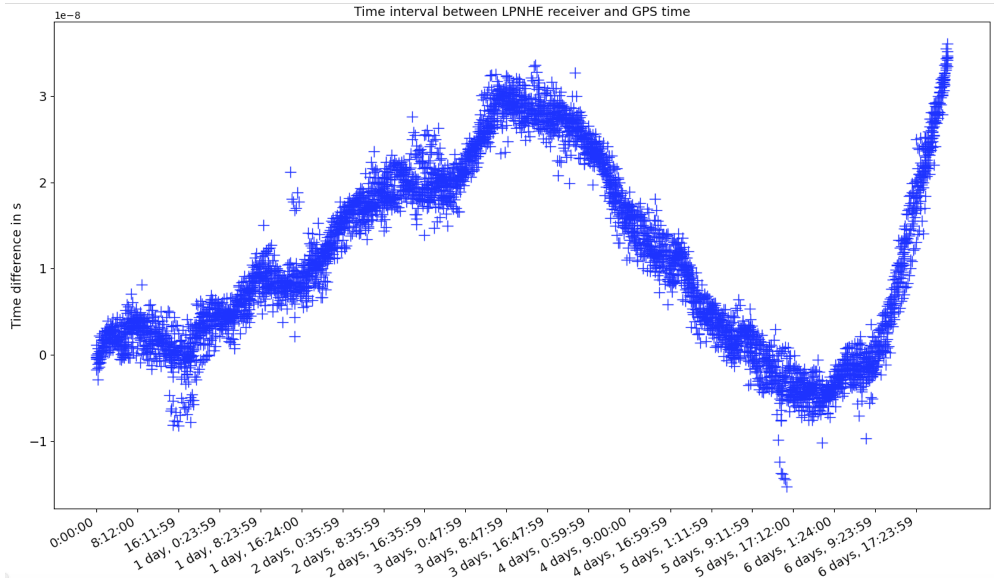


The “raw” plot (left), as produced from the receiver, shows a liner drift, as expected for the Rb clock. Once removed we can see that the clock “noise”.

(from Lucille’s talk cited before)

What Do We Do With It?

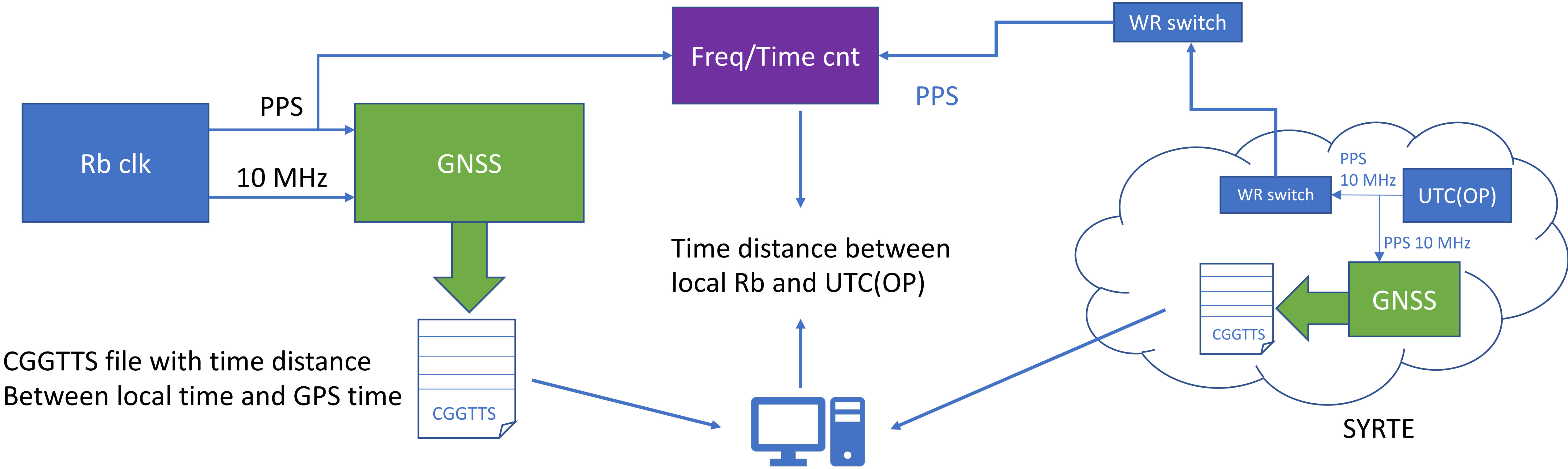




Extracting the drift from the left plot will allow us to precisely correlate the local time base (used to time tag the events) to GNSS time. Once done we can calculate the uncertainty on it (right plot). In this case is about 4 ns over 6 days (random walk).

(from Lucille's talk cited before)

How Accurate Is This Method?



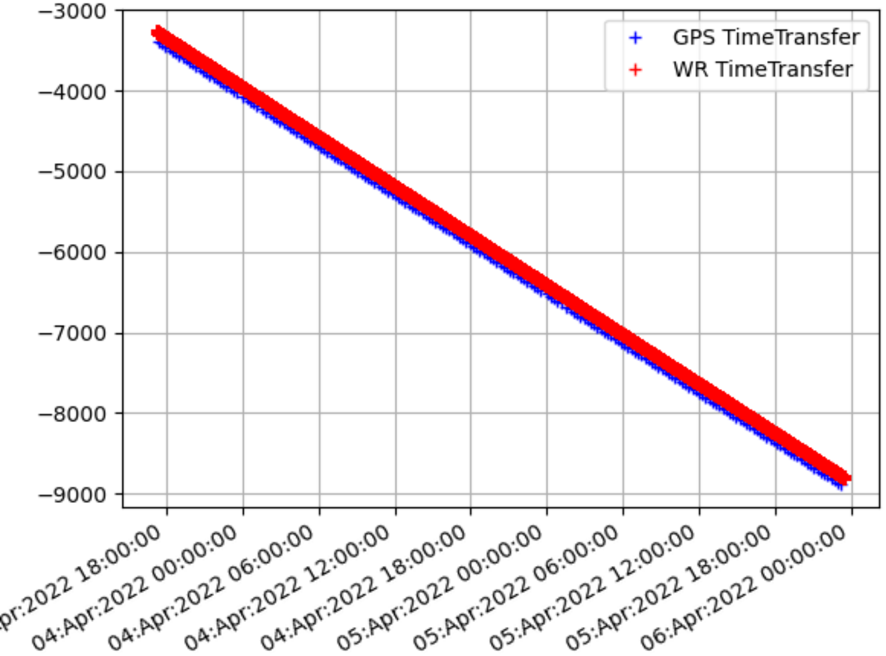
To evaluate our drift estimation method, we have done the following measure:

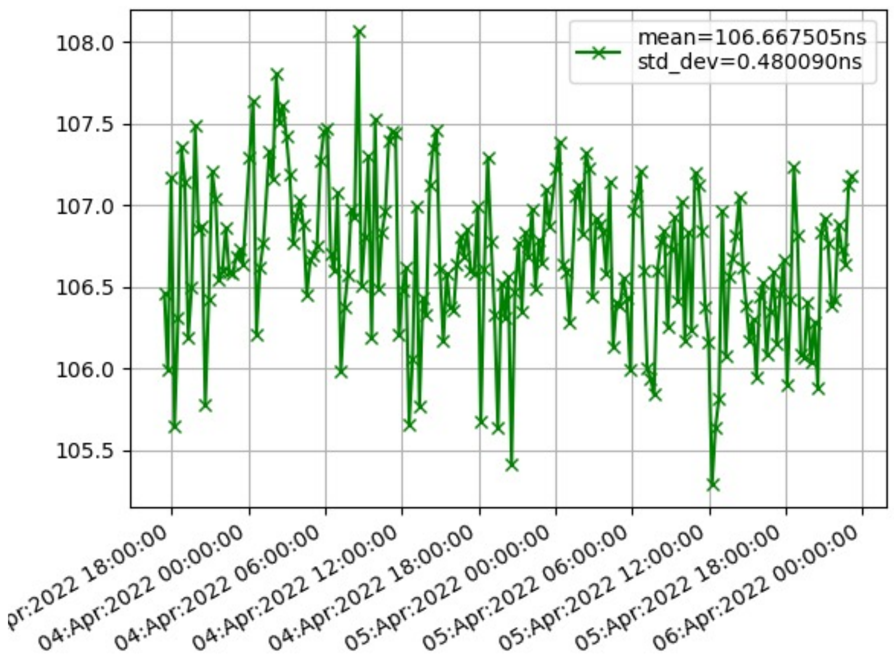
- We have created a CGGTTS form the GNSS steered by Rb clock (as before).
- Then we have used the time transfer technique to measure the time distance between our Rb clock to SYRTE UTC(OP) via common view method.
- Finally, we have compared this time distance with the one measured via the counter.

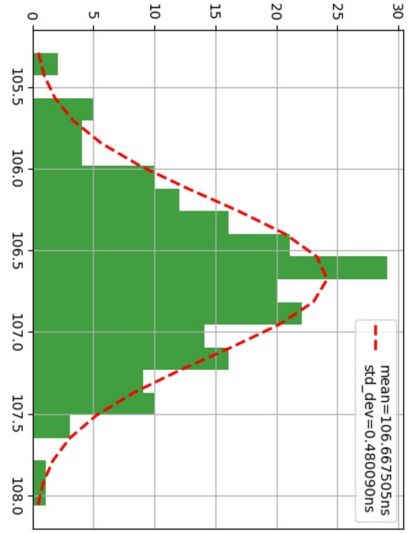
Vincent Voisin work

How Accurate Is This Method?

Time distance between local Rb and UTC(OP): Common view vs White Rabbit







Local time base/ UTC(OP)
Via common mode (blue)

Local time base/ UTC(OP)
Via white rabbit (red)

(same slope as before)

Common view method/WR
method difference
+/- 3 ns max

Histogram of the difference
Sigma = 0.48 ns

3 days of data. X axis: local time Y axis: ns

Vincent Voisin work