« Projet émergent » AC-LGAD

CEA Saclay/Irfu/
Département d'Electronique des Détecteurs et d'Informatique pour la Physique (DEDIP)

Organization for Micro-Electronics desiGn and Applications, Ecole Polytechnique, Palaiseau

Objective: Development of an **ASIC prototype**
EICROC0
able to readout a new generation of silicon sensors:
AC-LGAD
(Low-Gain Avalanche Diode)
for the future **Electron Ion Collider** (EIC) **Roman Pots**

- **Context, requirements / specificities**
- **Activity report**
- **Budget report**
- **Summary / perspectives**

Dominique Marchand (IJCLab) on behalf of the AC-LGAD project team

Electron Ion Collider (EIC)

Unique oppotunity to access/probe/image/quantify/qualify
the **gluonic, valence and sea quark content** of hadrons (low x)

- Dynamic of quark - gluon confinement
- Nucleon detailed comprehensive 3D-tomography
- Missing gluon contribution to nucleon spin and mass

And many more!

Expression of Interest supported by French theorists and experimentalists

~ 2034
Brookhaven National Laboratory

electrons (10 - 18 GeV, **~70 %** polar.)
⇒ **protons** (275 GeV, **~70%** polar.)
or
⇒ **ions** (light - deuterium - to heavy - Au, Pb, U)

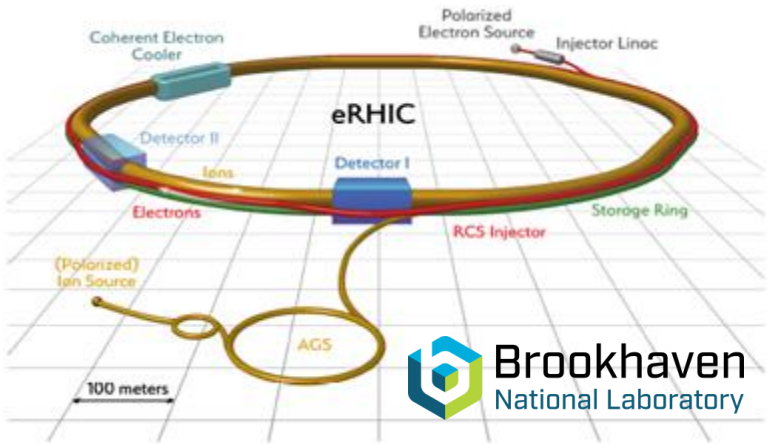
- ✶ Variable center-of-mass energies:
  20 - 100 GeV [140 GeV]
- ✶ High collision $\mathcal{L}$ **$10^{33\text{-}34}$** $cm^{-2}\ s^{-1}$
- ✶ **1 (2) interaction point(s)**

Complementarity
Jlab, LHC

Our main interest:
Exclusive Reactions
(*e.g.* Deep Virtual Compton Scattering, DVCS)

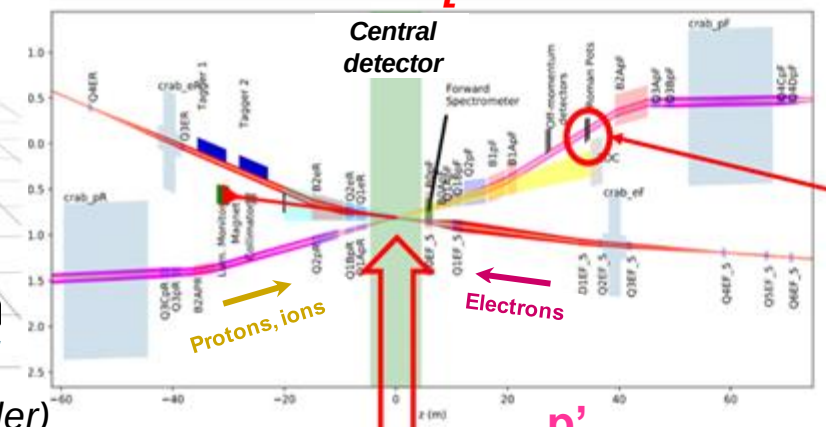
2103.05419 (March 2021)
Nucl. Phys. A 1026 (2022) 122447

electron Proton Ion Collider (ePIC) experiment: Roman Pots



Based on RHIC (Relativistic Heavy Ion Collider)

[Far-forward detectors]

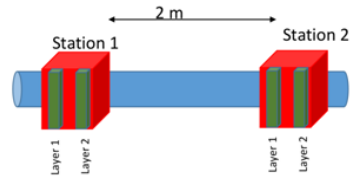


protons / ions

Momentum & Timing

Roman Pots **located ~30-40 m from IP**

2 stations of 2 layers each

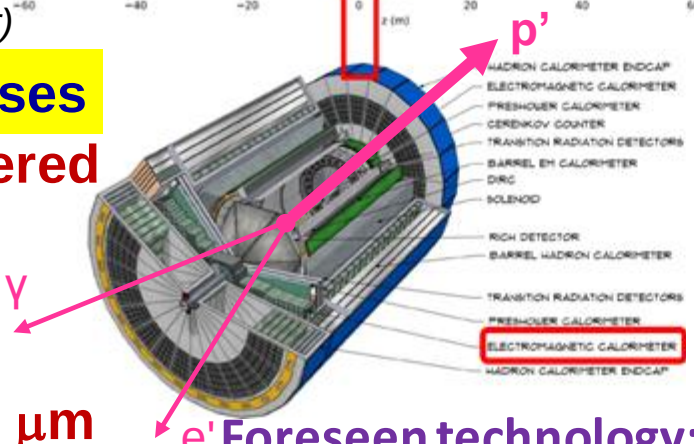


Exclusive & diffractive processes

Requirements on **forward scattered particles detection**:

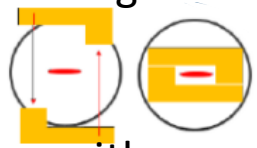
- at very small angle **< 5 mrad**
- time resolution **~30 ps**
- spatial resolution better than **50 μm**

to achieve a P_T resolution better than **10 MeV/c**



Roman Pots:

- Detector system surrounding the beam axis (a few mm)
- Placed in vacuum
- Holding silicon detectors with associated front-end electronics



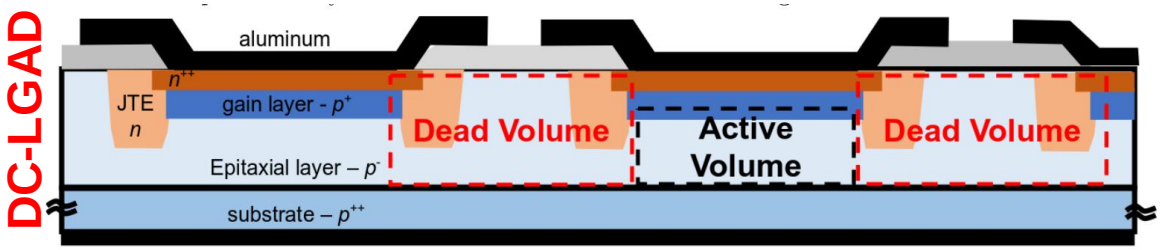
Foreseen technology: **new generation of pixellated LGAD**

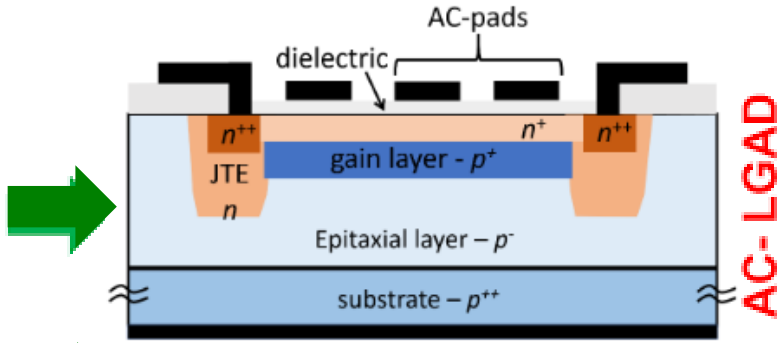
➡ **AC-LGAD**

associating good timing AND tracking capabilities

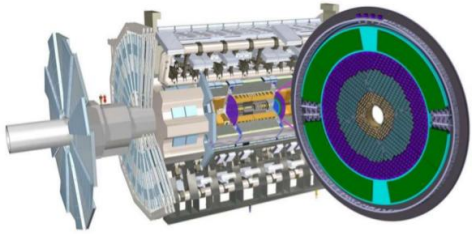
Low Gain Avalanche Diode (LGAD)

- Silicon sensors fabricated in a thin (≈50 µm) high resistive p-type substrate
- Charge gain (up to 100) to achieve very high timing resolution (20-30 ps)
- The size of the pads must be larger than the substrate thickness to achieve a uniform amplification
  → limitation for fine pixelation (< 1 x 1 mm²)





1D (timing) → **4D** reconstruction (timing & position)



ATLAS EXPERIMENT

Upgrade phase II **High Granularity Timing Detector (HGTD)**

- ➢ AC-LGAD sensors include metal electrodes placed over a thin insulating at a fine pitch, signals are induced capacitively.
- ➢ Insensitive area (edges) could be minimized
- ➢ Charge sharing → barycenter computation

- ➢ Based on pixellated **DC**-LGAD 4 x 2 cm²
- ➢ Pixel size: 1.3 x 1.3 mm²

"Fabrication and performance of AC-coupled LGADs", G. Giacomini *et al.*, JINST 14 (2019) 09, P09004,ArXiv: 1906.11542

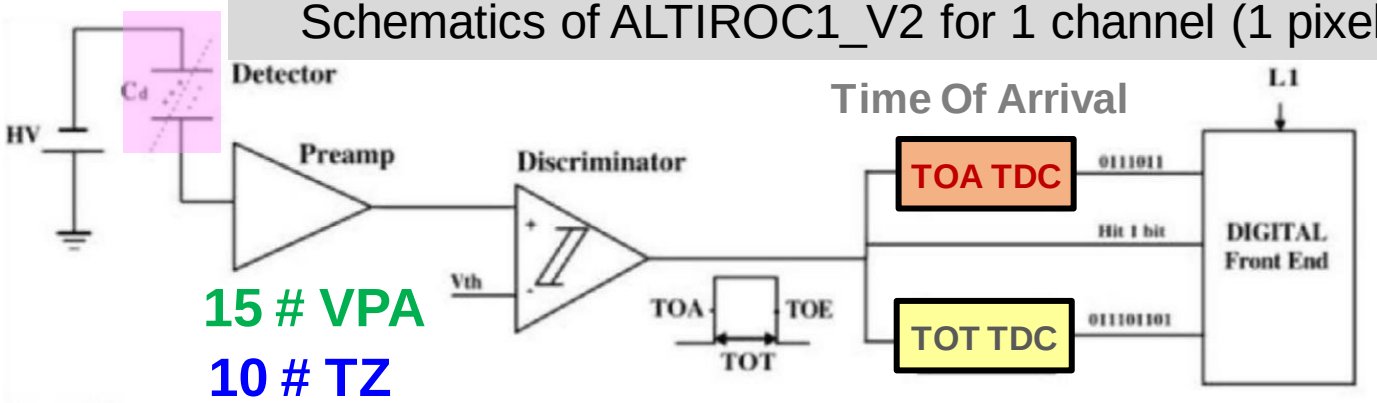
BROOKHAVEN NATIONAL LABORATORY

ALTIROC: **A**TLAS **L**GAD **T**iming **I**ntegrated **R**ead **O**ut **C**hip
[technologie CMOS 130 nm (TSMC)]

designed and characterized by OMEGA and IJCLab

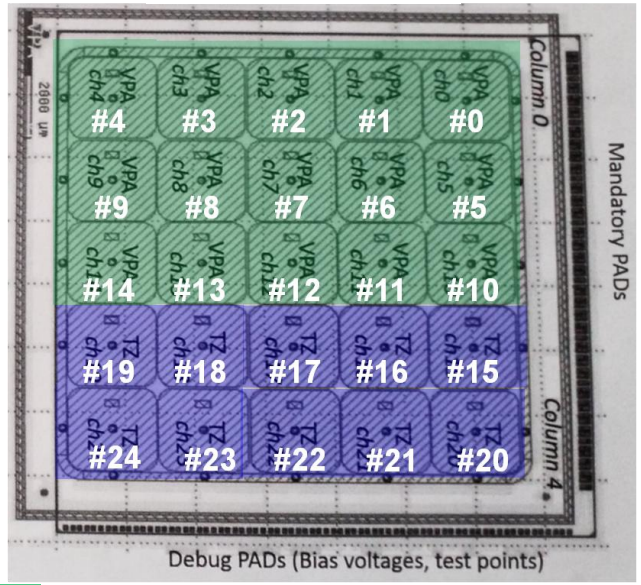
Existing ASIC to read DC-LGAD
Goal ~30 ps time resolution
ALTIROC3 (full size: 225 channels) tested under beam, oct. '21

Schematics of ALTIROC1_V2 for 1 channel (1 pixel)



(TDC: Time-to-Digital Converter)

ALTIROC1_V2 channel mapping
(25 channels)



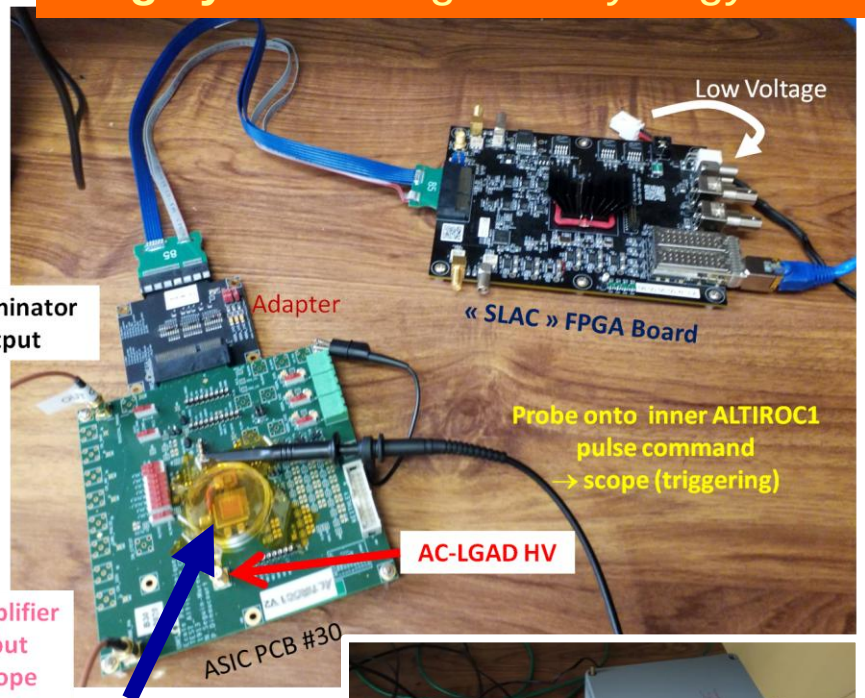
\# Voltage PreAmplifier (VPA)

\# TransImpedance PreAmplifier (TZ)

"Performance of the Front ASIC for picosecond precision time measurements with LGAD sensors", C. Agapopoulou, C. La Taille, L. Serin *et al.*, JINST, 2020, 15 (07), pp.P07007.

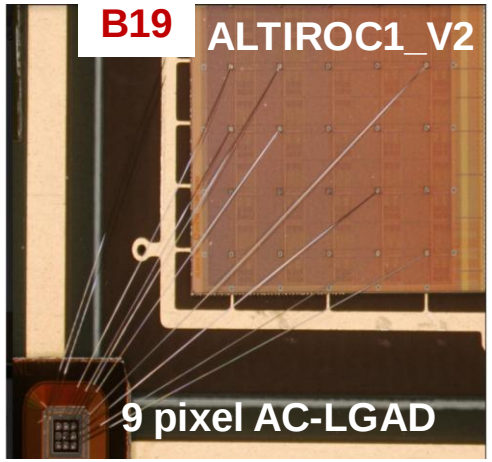
ATLAS/HGTD test bench: ALTIROC1+ AC-LGAD (3x3 pixels)

Largely benefitting from synergy with ATLAS/HGTD IJCLab team: expertise and testbench setup

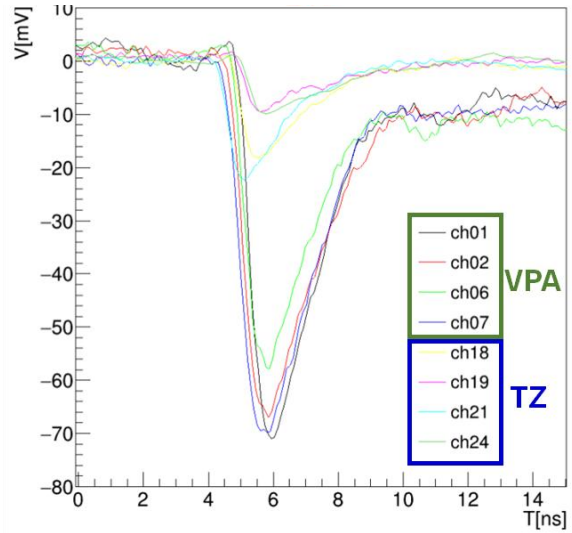


AC-LGAD prototype wire-bonded to ALTIROC1_V2 by **BNL team**

Sept. '21 - Jan. '22



HV: -160V (I ~68nA), DAC Pulser ~ 8 fC

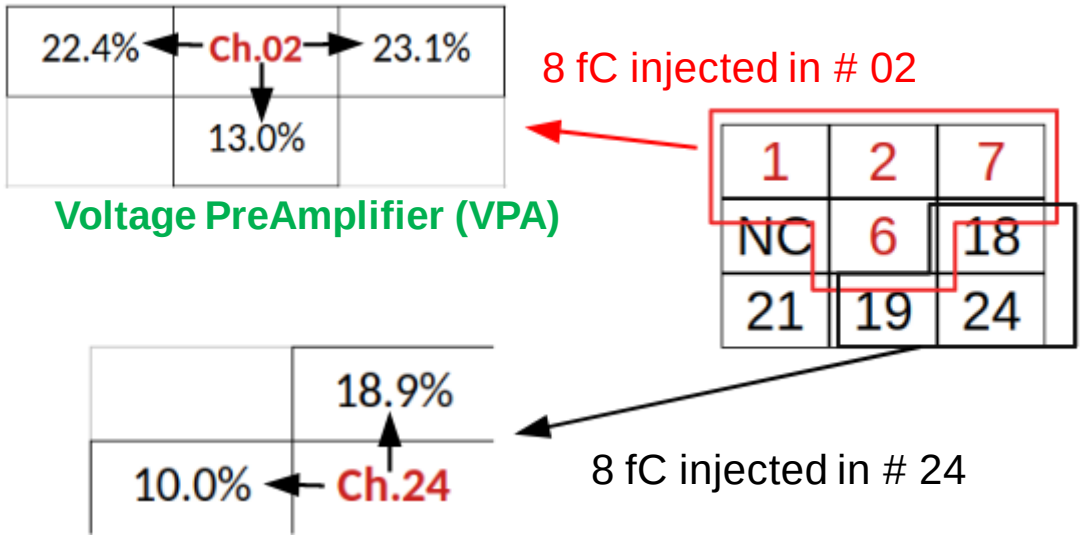


- Corrected LSB (Least Significant Bit) for each TDC channel is ~30ps
- The average jitter for each channel is ~15-20ps
- Connected TDC channel performances uniform
- Study of PA amplitudes versus injected charge
- Lowest detectable charge 2.5 fC

Studies of charge sharing: measurements

Objective: evaluation of charge sharing among adjacent pads / pixels

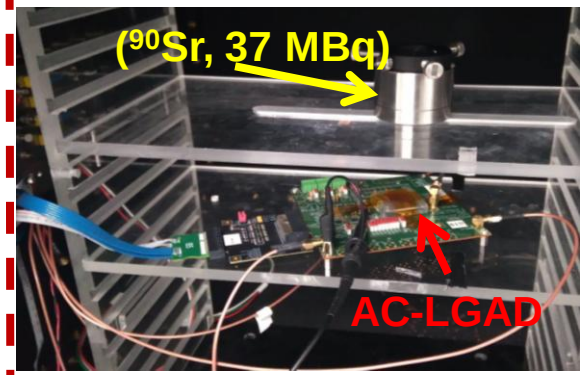
➢ Through charge injection (8 fC)



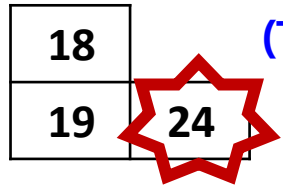
Charge sharing among neighboring pads (cross talk):
~ 15%

➢ Exposing AC-LGAD to a beta source

At IJCLab Semi-conductor and instrumentation technological platform (PSI)



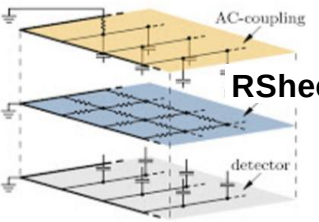
- AC-LGAD HV = -170 V
- Beta source ~5 cm above
- Whole system in black box



Charge sharing among neighboring pixels (# 18 & 19):
~30% w.r.t. # 24 (highest amplitude)
includes cross talk between pads and suffers from *ALTIROC1* TDC (TOT) discriminator signal distortion (earlier observed by ATLAS/HGTD team)

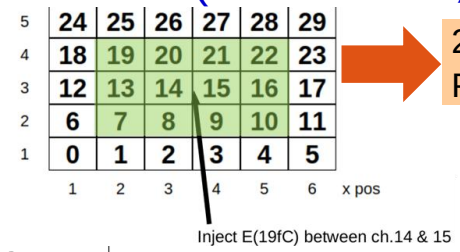
Studies of charge sharing: simulation and measurements

Synergy IJCLab ATLAS/HGTD , JLab/EIC and OMEGA teams

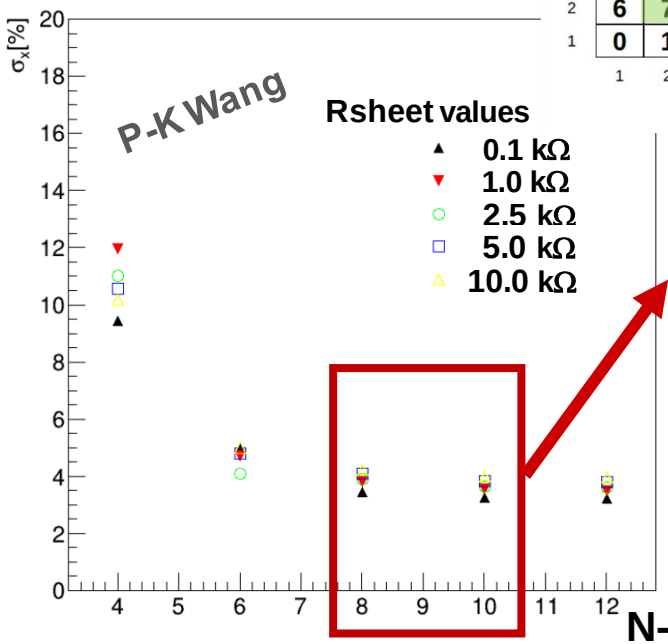


Objective: evaluation of achievable spatial resolution taking into account charge sharing between neighboring pads/pixels including smearing (Landau) +1-4 mV noise and considering **N**-bit ADC (**N**=4-12), P-K Wang

➢ Electronics Model (M. Morenas, OMEGA): 5x6 pads, TZ, several Rsheet values considered



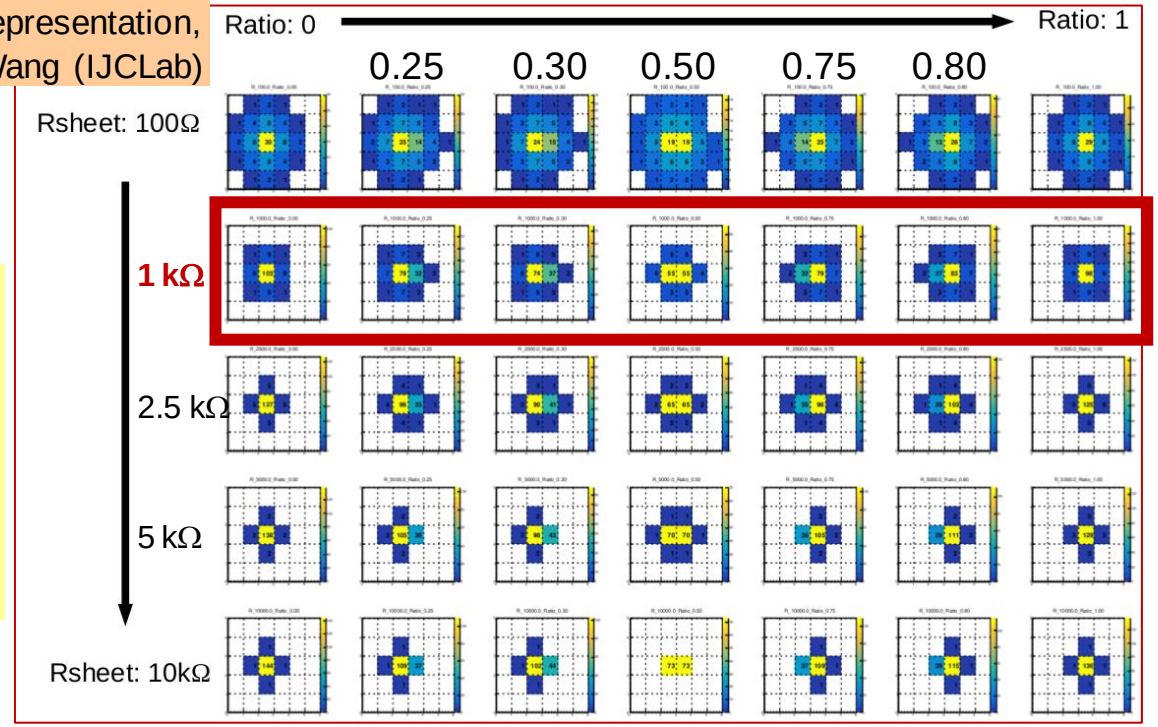
2D-Representation, P-K Wang (IJCLab)



8 and 10-bits ADC

σ_x ~ 4% (pixel width=0.5 mm)

⇔ ~20 μm



EICROC0 design

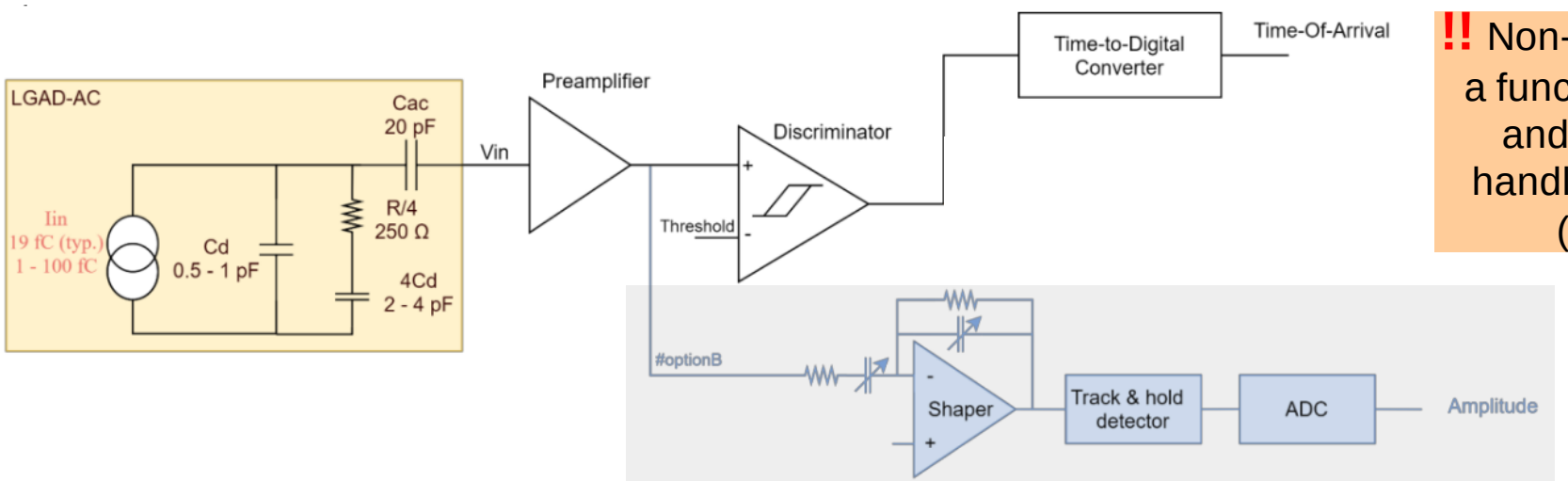
Requirements:

- pixel size **0.5 x 0.5 mm²** (HGTD 1.3x1.3 mm²)
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1mV/channel**

EICROC0 design:

- TZ Preamplifiers from ALTIROC (ATLAS/HGTD, OMEGA)
- TDC from HGCROC (CMS/HGCal, CEA/Irfu/DEDIP)
- 8 bit ADC for time-walk correction (AGH Krakow, adapted from HGCROC)

Schematics for 1 channel (1 pixel)



!! Non-linear behavior of **TOT** as a function of deposited charge and low discri threshold to handle small energy deposits (neighboring pixels)

Time-walk correction:
amplitudes
of **central hit pixel**
+ neighboring pixels required

ADC: next EICROC iteration will include a lower power consumption ADC (~1 mW/channel) designed at **IJCLab**

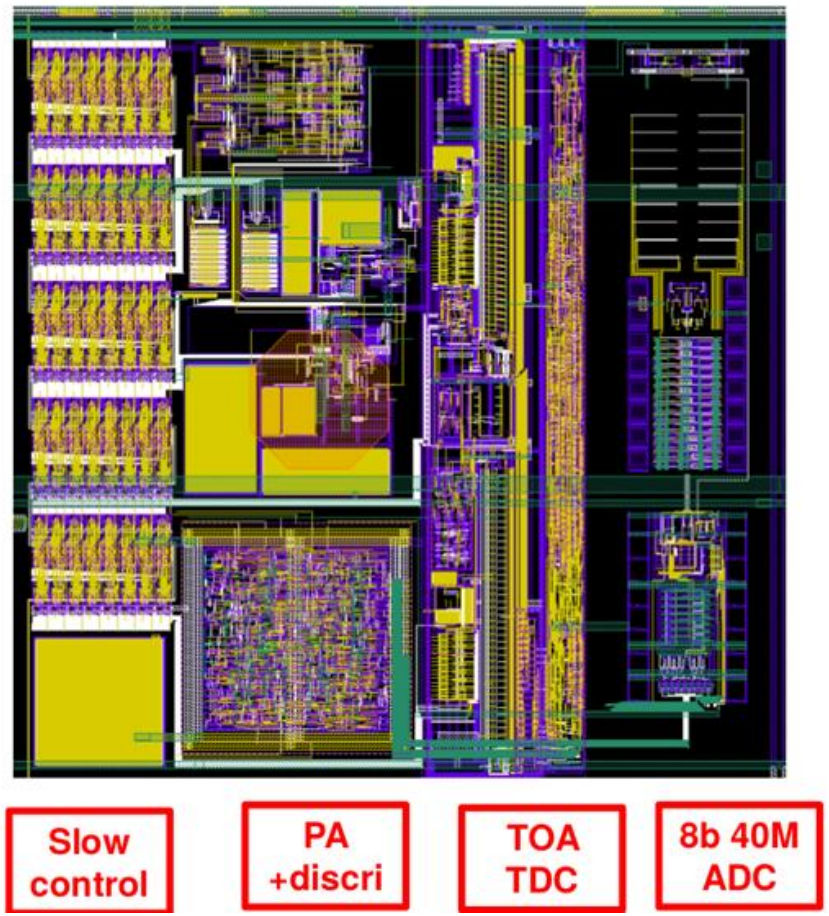
EICROC0: 1 pad (500 x 500 µm²) overview

- High speed TZ PA and discriminator (from ALTIROC)
- I²C slow control (from CMS HGCROC)
- 8 bits 40 MHz ADC (adapted from HGCROC 10 bits ADC, M. Idzik *et al.*, AGH Krakow)
- Digital readout FIFO (depth 8, 200 ns)
- 10 bits **TDC** (TOA) designed by **CEA Irfu/DEDIP**:

  HGCROC TDC (1 mm x 120 µm):
  - spatially adapted to fit in a pad of 0.5 x 0.5 mm²
  - optimization in terms of dynamic range and resolution (10 ps rms) as well as power consumption
  - common block for calibration of all TDC channels

✸ <u>5 slow control bytes/pixel:</u>
- 6 bits local threshold
- 6 bits ADC pedestal
- 16 TDC calibration bits
- Various on/off and probes

EICROC0 layout (1 pad = 1 channel)

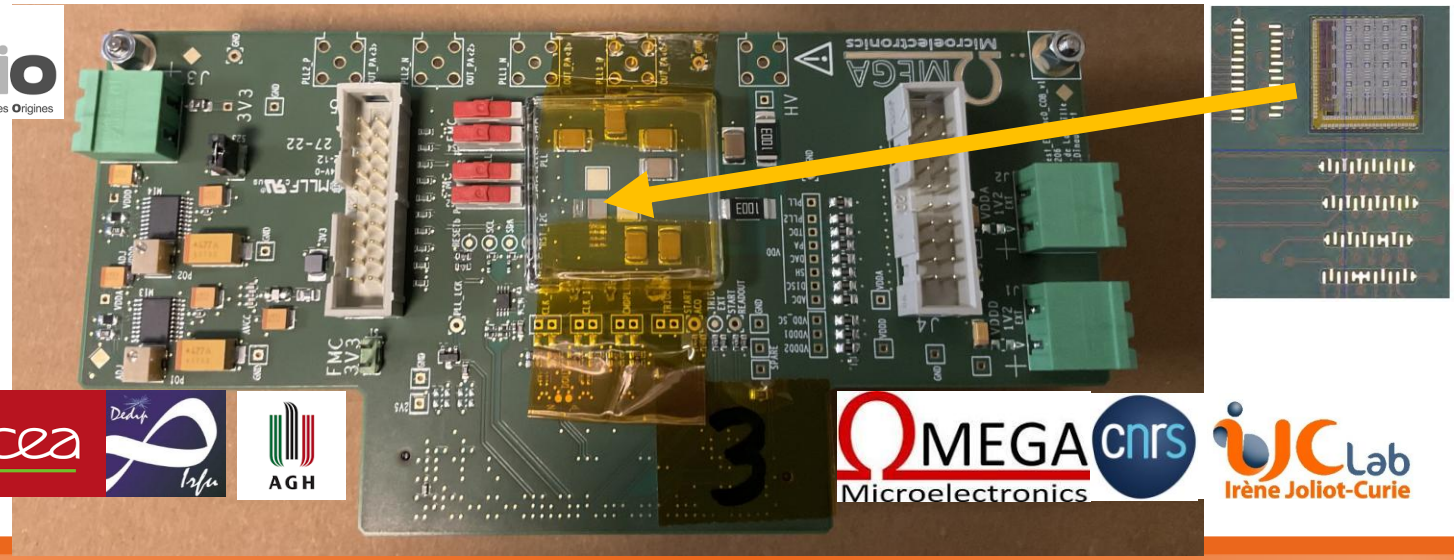


EICROC0: EIC 4x4 AC-LGAD readout test chip

- submitted through a Multi Project Wafer (130 nm CMOS technology) in March ’22
  Delivered end of July ‘22
- **Test board** (PCB) designed by OMEGA, 10 pieces **delivered end of July ‘22**
  - test board cabling by IJCLab
- **Wire-bonding of EICROC0 to test boards** by BNL collaborators
- Delivery of 3 test boards to IJCLab in **Oct. ‘22**

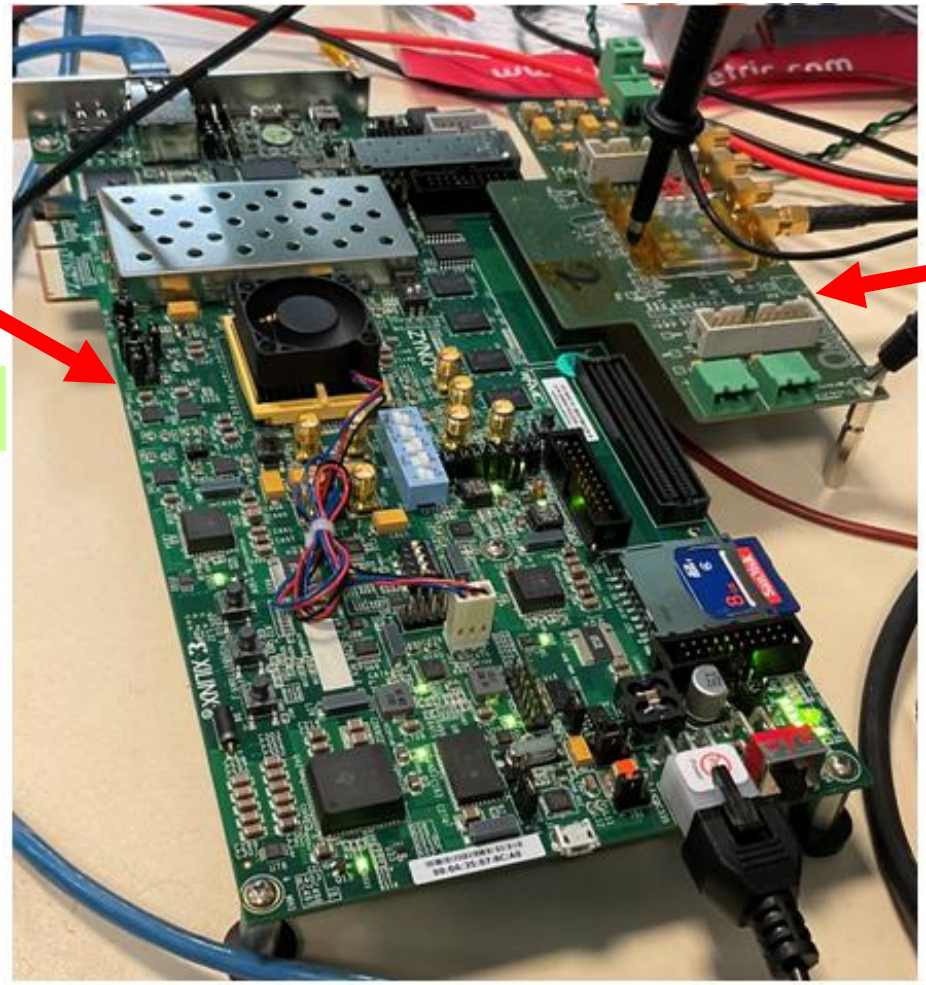
- **Interface board** (Xilinx ZC 706): firmware / software developments (A. Ba & B.Y. Ky, IJCLab)

EICROC0
Test board



EICROC0 Test Bench at IJCLab

- installed in an electronic test room (IJCLab, building 102)



Test bench finalization under progress

- ✓ I^2C communication
- ✓ Data stream written/read
- ✓ EICROC0 DC levels
- ✸ EICROC0 command pulse signal under investigation

Next step:

EICROC0 channel by channel electronic response characterization (PA, TDC, ADC, LSB & jitter evaluation, cross talk)

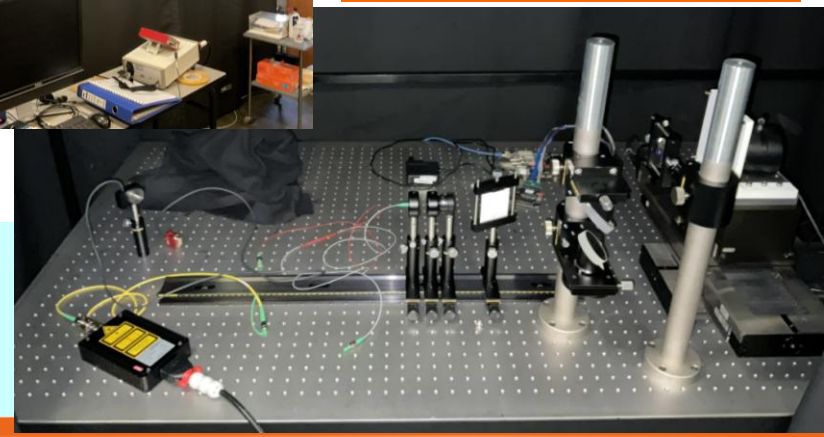
AC-LGAD Project: budget report

« Electronics »:

- Contribution to EICROC0 Multi Project Wafer
- Manufacturing of 10 test boards + purchase of components and cables
- Purchase of 2 Xilinx ZC 706 interface board
- Purchase of a dedicated high performance Lecroy oscilloscope Lercoy Waverunner 9254 2.5 GHz, 20 Gs/s, 4 channels

Dedicated infrared test bench setup at IJCLab:

- Purchase of all the required material:
  - IR laser λ=1050 nm, optical fibers + splitter
  - optical alignment elements: mirrors, lenses, visible/IR camera,
  - power meter,
  - safety equipment: curtains, IR glasses,



Largely benefiting from synergies among IJCLab departments and from BNL expertise

to be exploited to characterize the response of (ASIC+AC-LGAD) systems, complementary to measurements with a β source

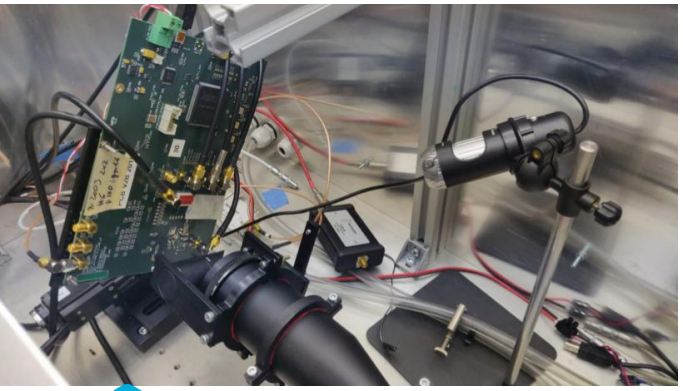
AC-LGAD project: perspectives

- EICROC0 electronic response and performance characterization,
- EICROC0 + AC-LGAD (4x4 pixels) sensor electronic response characterization,
- Characterization of the response of [EICROC0 + AC-LGAD (4x4 pixels) sensor] exposed to a physical source (IR laser, β source, particle beam)

➢ optical **IR laser test bench** operation at IJCLab: → **signal sharing, time and space**

Characterization of the response of ALTIROC1_V2 + AC-LGAD sensor (3x3 pixels)

⇨ Comparison with (AC-LGAD + ALTIROC0_V2B) measurements performed at BNL

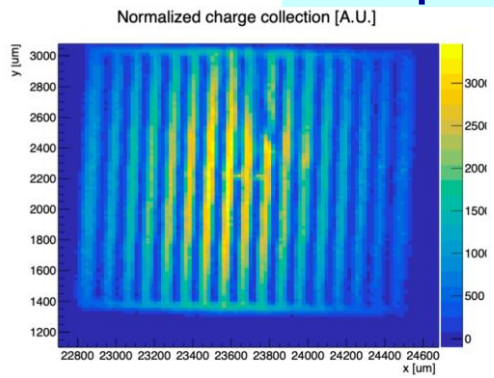


Brookhaven National Laboratory

Scanning-Transient Current Technique (TCT) using IR laser

AC-LGAD strips

Colour indicates integral charge of the signal peak from the ALTIROC analog output



"Signal formation and sharing in AC-LGADs using the ALTIROC0 front-end chip", G. D'Amen et al., arXiv:2209.07329 [physics.ins-det], JINST **17** P11028 Nov. 2022

AC-LGAD Project Summary 2021 - 2022

- Characterization of the system (AC-LGAD + ALTIROC1_V2) exploiting ATLAS/HGTD test bench (electronics response signal to an injected charge)
- Evaluation of the charge sharing ratio among neighboring pads / pixels:
  - measurements based on ALTIROC1 injected charge
  - measurements with a β source
- Development of a full simulation to evaluate spatial resolution from signal sharing including digitalization in the context of a 8/10 bits ADC
  ⇨ ADC with 8 bits sufficient to achieve 20 μm spatial resolution.

Studies presented at the EIC User Group Early Career Workshop 2022, July 24-25 (CFNS Stony Brook University, USA), "Simulation and instrumentation for the Roman Pot in the future Electron-Ion Collider", Pu-Kaï Wang (PhD, IJClab)

- Design/layout of EICROC0 : submission within a MPW in March '22 (delivered July '22)
- Test board designed, manufactured (10 pieces) and cabled
- EICROC0 wire-bonded onto test boards by BNL collaborators, available at IJCLab: Oct. '22
- EICROC0 electronic test bench being finalized
- IR laser test bench close to be operational

- Weekly IJCLab meetings
- Monthly IJCLab - Irfu - OMEGA meetings
- Monthly BNL- IJCLab - Irfu - OMEGA meetings
- Weekly EIC LGAD meetings

Fruitful tight collaboration between all involved partners

The design of the first optimized ASIC (EICROC0) dedicated to AC-LGAD sensor readout funded by P2IO positioned the French community in the forefront of this promising new technology with multiple applications in particle physics and beyond.
Visible role within the EIC international community.

IN2P3 Scientific Council (27/10/22): *for information* « EIC Project: scientific challenges and project presentation », Carlos Muñoz Camacho (IJCLab)

- contribution to EIC AC-LGAD R&D consortium: FY2022 report & FY2023 proposal
- R&T project proposal submitted in Oct. 2022 (duration 3 years, 20 k€ / year)
- **?** 2023 ANR: submission of a pre-proposal (PRC: IJCLab, CEA Irfu/DEDIP, OMEGA, *BNL*): « CD_4D-TrACE » [Chip Design for 4D-Tracking with AC-LGAD for EIC], 4 years design of EICROC full size (32 x 32 pixels)

The AC-LGAD Team

- Abdourahmane Ba
- Beng Yun Ky
- Carlos Munoz Camacho
- Dominique Marchand
- Emmanuel Rauly
- Jean-Jacques Dormard
- Laurent Serin
- Ana-Sofia Torrento
- Pu-Kaï Wang

- Florent Bouyjou
- Eric Delagnes

- Christophe de la Taille
- Nathalie Seguin-Moreau
- Maxime Morenas
- Pierrick Dinaucourt

Thank you

- Alessandro Tricoli
- Gabriele Giacomini
- Gabriele D'Amen