Future Ultra-Light Pixelated Tracking Devices

M. Winter (IJCLab-Orsay) **on behalf of DESY-IPHC-GSI-IJClab (DIGI) coll.**

(DMlab Annual meeting – DESY – 12 Decembre 2022)

Contents

SOURCES: PLUME coll., Nucl. Instr. Meth. A650 (2011) 208-212;
CREMLInplus EU project (WP-7), H2020-INFRASUPP-2018-2020;
ALICE coll, CERN-LHCC-2019-018 / LHCC-I-034;
R. Brenner et al., CERN-LHCC-2017-002 ; LHCC-I-028
C. Garuglio (ITS-3), Forum on Tracking Detector Mechanics, 2021
M. Mager, CBM-MVD workshop, https://indico.gsi.de/event/15130/, 15-16/09/2022
F. Carnesecchi, Vertex-22 workshop, 23-28/10/2022

DESIGN PARAMETRES GOVERNING DETECTOR PRECISION

- **Spatial resolution and (passive !) Material budget**

- **Sensor level:**
  - pixel dimensions (both directions)
  - sensor thickness: sensitive volume ($\Rrightarrow$ signal amplitude), read-out circuitry ($\Rrightarrow$ monolithic !)
  - pixel charge sharing
  - charge digitisation: power driver $\Rrightarrow$ minimise !
  - time resolution / read-out speed: power driver $\Rrightarrow$ compromise !
  - data flow: power driver ($\Rrightarrow$ in-pixel signal discrimination)

- **System integration (services)**
  - mechanical support
  - cooling system: driven by sensor power ($\equiv$ read-out architecture)
  - cables (powering, slow control, signal read-out): governed by sensor power ($\equiv$ read-out architecture)
  - overlap between neighbouring detector modules

OBJECTIVES & APPROACH

- **Technological goal:** achieve new standards in charged particle vertexing and tracking

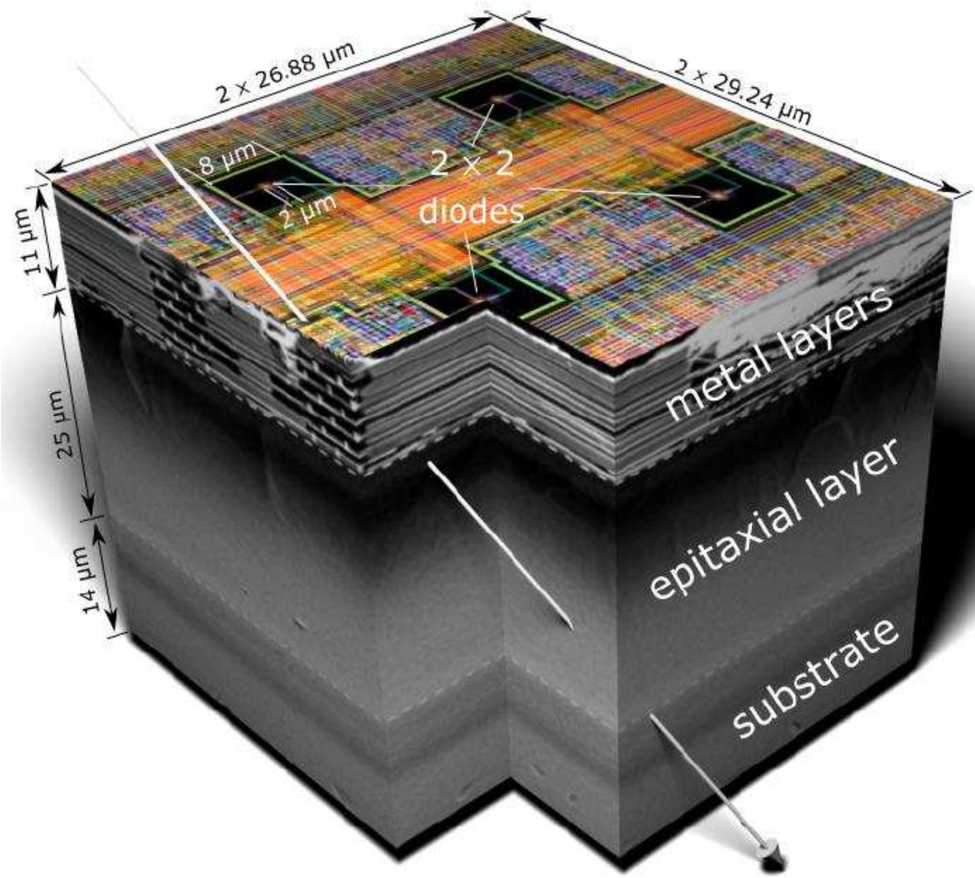
- **Detection performance top priority:** granularity & material budget $\Rrightarrow$ precision
  - exploit thinned, highly pixelated, CMOS Pixel Sensors (CPS) and the evolution of CMOS industry (feature size $\Rrightarrow$ pixel size and micro-circuit density, stitching $\Rrightarrow$ large sensors)
  - exploit new materials and forefront of industrial techniques (thermo-mechanics, electronics)
  - investigate new concepts: ”unsupported” & double-sided detection layers, wireless short range signal transmission, etc.
  - develop accurate simulation software of CMOS sensor response and reconstruction algorithms

- **Exploit common requirement priorities addressed by Helmholtz & IN2P3 groups involved in:**
  - heavy-ion and hadron physics experiments (ALICE/LHC, CBM/GSI, etc.)
  - e+e- collider experiments (future Higgs factory, BELLE-II upgrade, etc.)

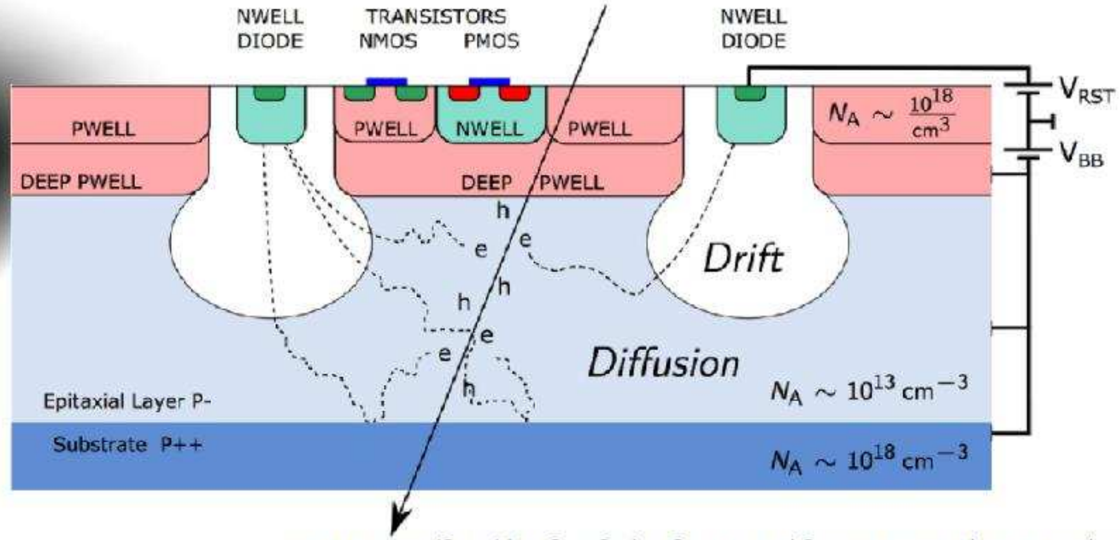
- **Exploit common interests with semi-conductor detector R&D at large:**
  - pp collider expts (HL-LHC, ...): common CMOS techno., sensor simulation & track reconstruction software
  - multi-purpose (transversal) R&D programmes addressing subatomic physics and its spin-off applications (EURIZON, AIDAinnova, ECFA detector R&D, etc.)

CMOS PIXEL SENSORS

ALPIDE
Technology



- **Process:** Tower Semiconductor 180 nm CIS
  - deep p-well to allow CMOS circuitry inside matrix
  - reverse-substrate bias
- **Detection layer:** 25 µm high-resistive (>1 kΩcm) epitaxial layer
- **Thickness:** 100 µm (OB) or 50 µm (IB)

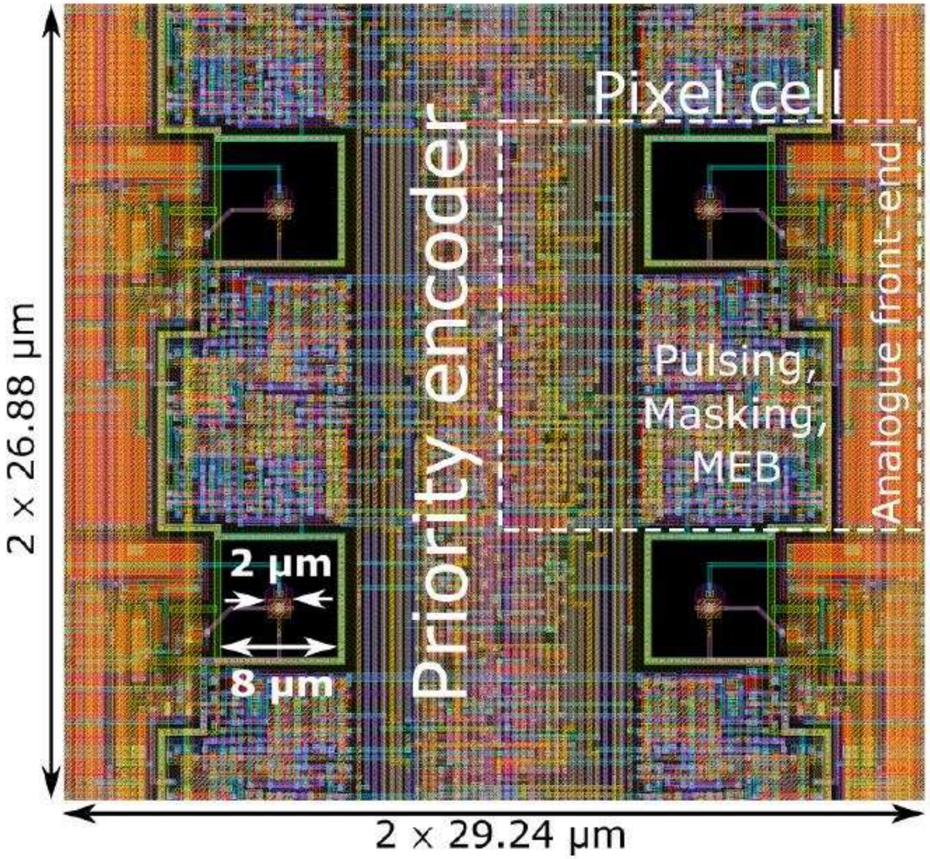


Magnus Mager (CERN) | ALICE ITS3 / ALICE 3 tracker | CBM-MVD retreat | 16.09.2022 | 6

IN-PIXEL CIRCUITRY

ALPIDE

Pixel functionality



- **Front-end:**
  (9 transistors, full-custom)
  - continuously active
  - shaping time: < 10 μs
  - power consumption: 40 nW
- **Multiple-event memory:** 3 stages
  (62 transistors, full-custom)
- **Configuration:** pulsing & masking registers
  (31 transistors, full-custom)
- **Testing:** analogue and digital test pulse circuitry
  (17 transistors, full-custom)
- **Readout:** priority encoder, asynchronous, hit-driven

O(200) transistors / pixel (wrt. 3T/4T)

SUPPRESSED MATERIAL BUDGET

ALICE

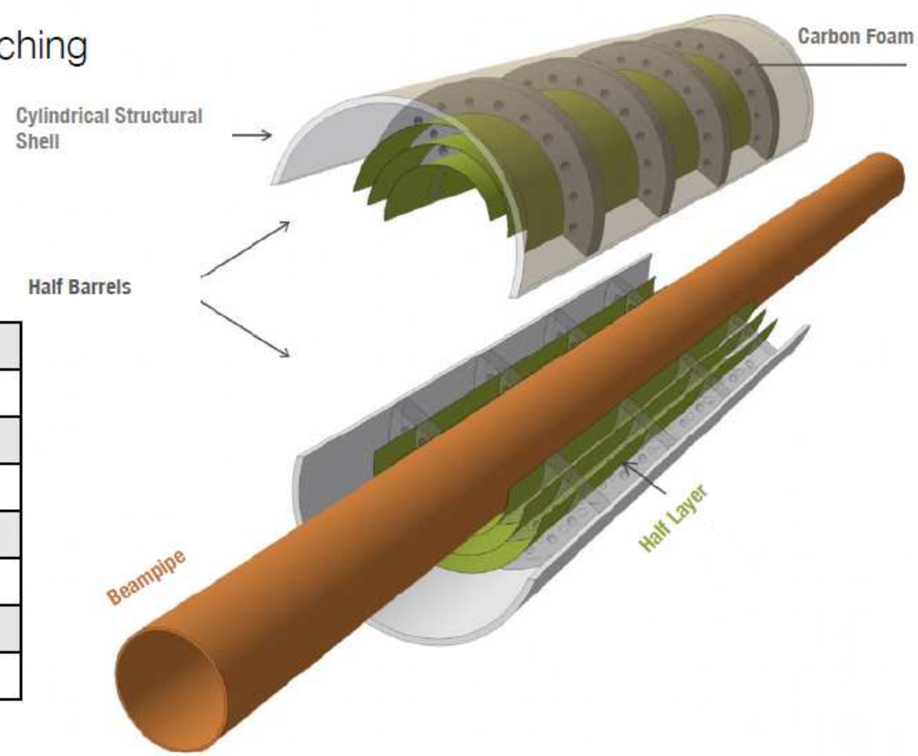
ITS3: 6 truly cylindrical wafer-scale MAPS

From 432 to 6 bent sensors

Detector concept

Key ingredients:
- **300 mm wafer-scale MAPS sensors**, fabricated using stitching
- **thinned down** to 20-40 μm, making them flexible
- **bent** to the target radii
  (L_0 23 mm → 18 mm, **closer** to the interaction point thanks to the new beampipe at 16 mm)
- mechanically held in place by carbon foam ribs

Beampipe inner/outer radius (mm)	16.0/16.5		
Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18	24	30
Length (sensitive area) (mm)	300		
Active area (cm^2)	610	816	1016
Pixel sensors dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O(10x10)		



Key benefit:
- extremely **low material budget**: 0.02-0.04% X_0 (beampipe: 500 μm Be, 0.14% X_0)
- **homogeneous** material distribution: negligible systematic error from material distribution

F.Carnesecchi, 25th October 2022, VERTEX, ALICE ITS3

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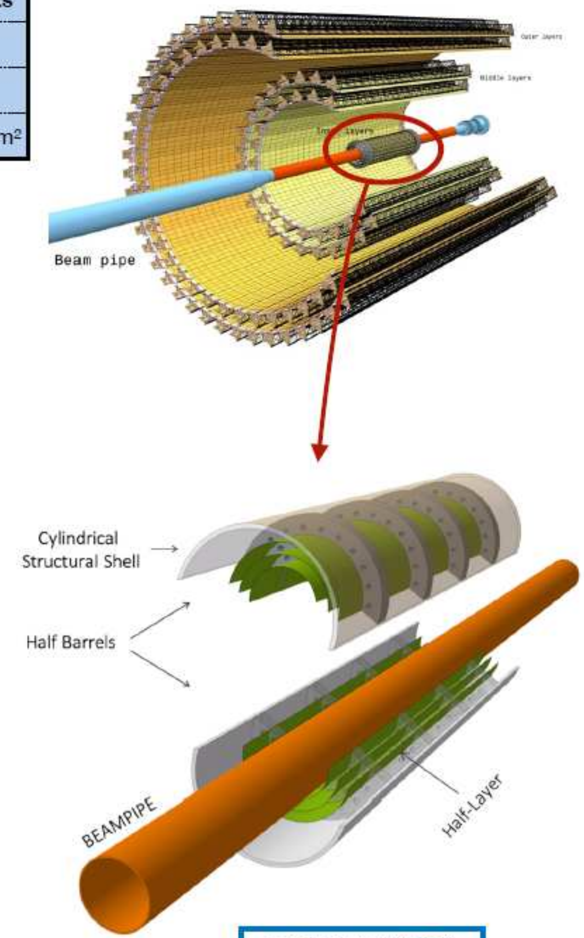
I. Sanna, 7th December 2022, WP1 meeting

ALICE ITS3

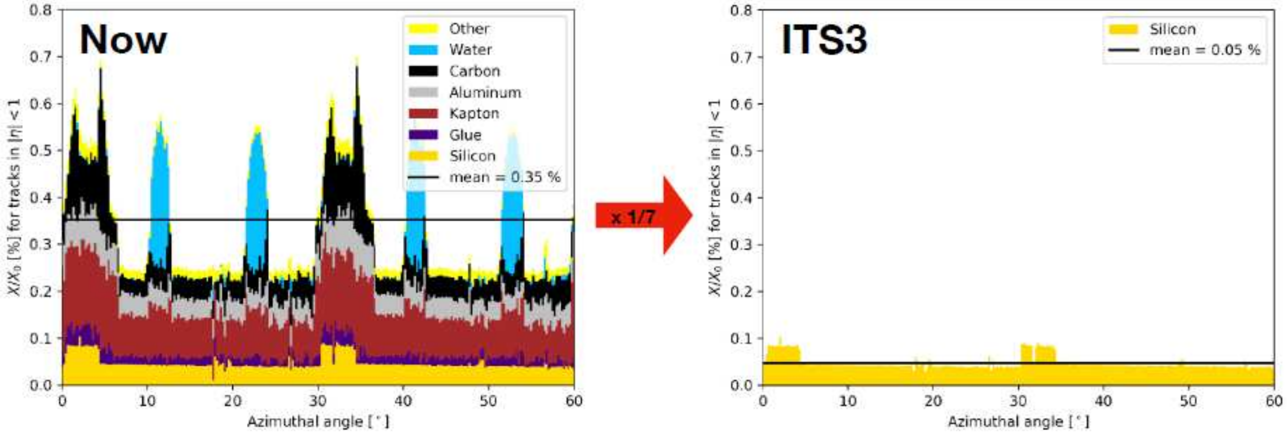
	ALICE ITS3 requirements
Pixel size (μm^2)	O(10x10)
Power consumption	< 20 mW/cm^2
Radiation hardness	10 kGy + 10^{13} 1MeV n_{eq}/cm^2



Letter of Intent: CERN-LHCC-2019-018

Replacing the 3 innermost layers with new ultra-light, truly cylindrical layers:

- Reduced material budget (from 0.35% to 0.05% X_0)
- Closer to the interaction point (from 23 to 18 mm)
- Improved pointing resolution



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CYLINDRICAL LAYERS: MAIN R&D TOPICS

ALICE

ITS3: 6 truly cylindrical wafer-scale MAPS

R&D roadmap and challenges

Outline

Air for cooling
Thermal test ongoing

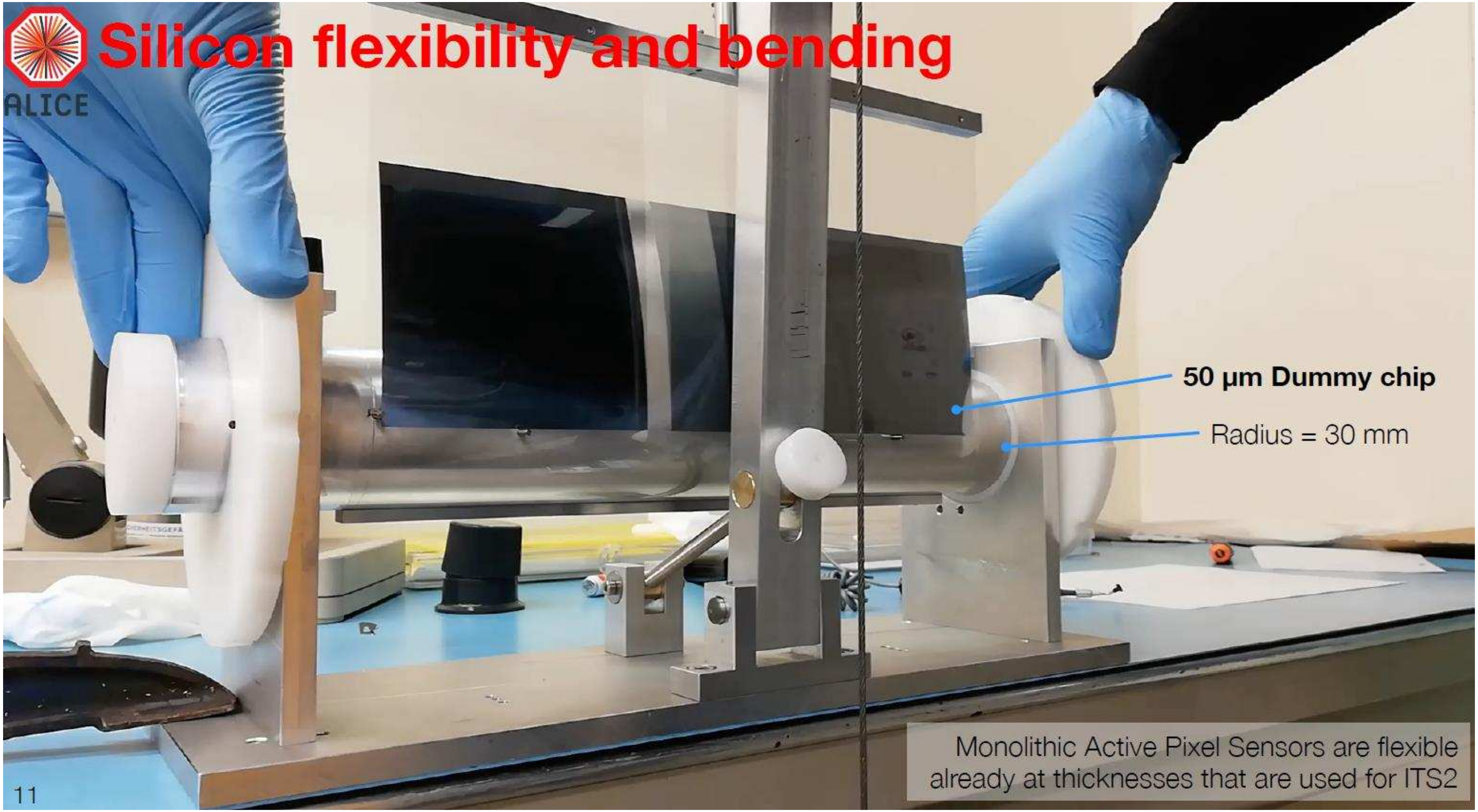
Support with Carbon foam ribs and handling ultra thin structures
Development of procedures to handle large thin chips and mechanical concept to hold thin sensors "without" material

Silicon flexibility and bending: ultra-thin, bent Monolithic Active Pixel Sensors
Performance of bent silicon at different target radii: 18 mm, 24 mm, 30 mm

Sensor design: 65 nm CIS process of TPSCo for tracking detectors
Charge collection efficiency, detection efficiency, radiation hardness

Stitching of wafer scale-chips
In chip power and signal distribution

CYLINDRICAL LAYERS: SENSOR BENDING



3 CYLINDRICAL LAYER INTEGRATION WITH FOAM SPACERS

ALICE

Silicon flexibility and bending

Mechanical mockup of 3 truly cylindrical dummy layers
Radii: 18 mm, 24 mm, 30 mm

Final aim → turn these **dummy silicon** chips into a true single die monolithic pixel sensor

F.Carnesecchi, 25th October 2022, VERTEX, ALICE ITS3

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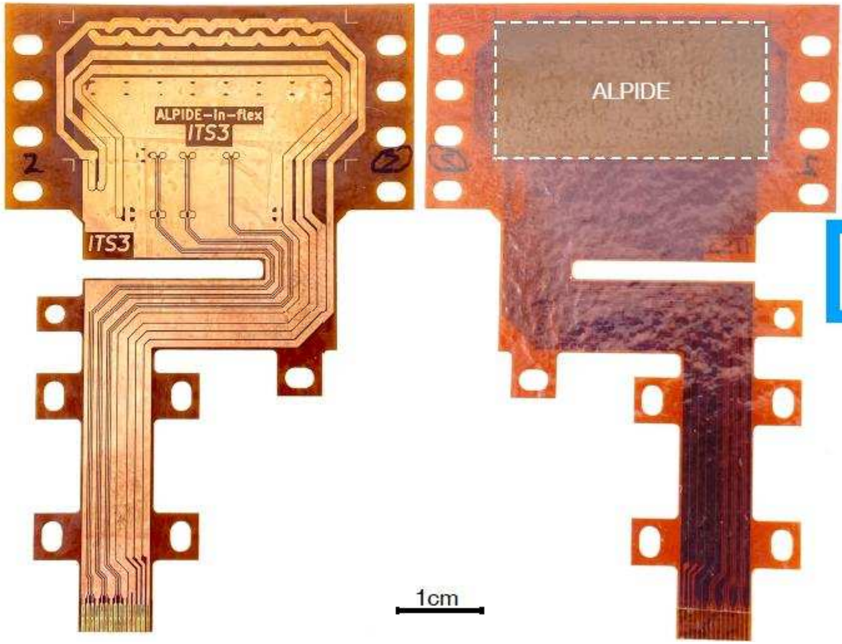
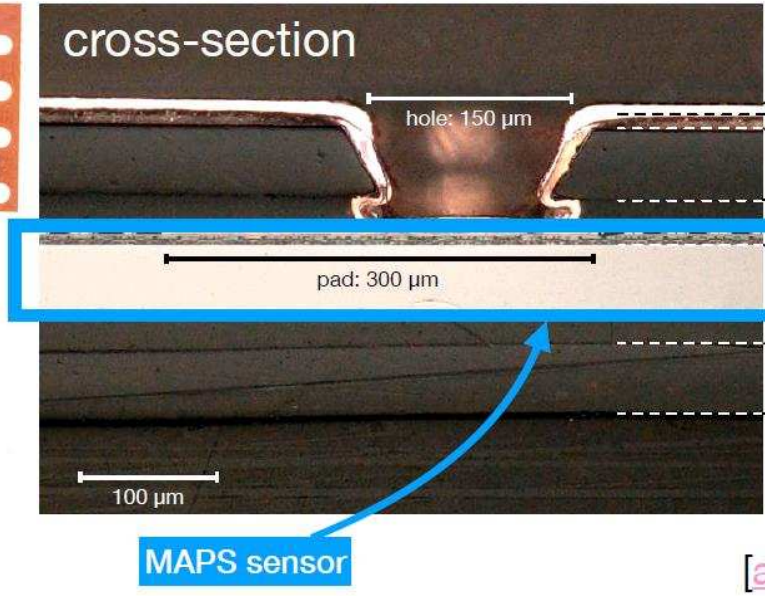
INNOVATIVE LAYER CONCEPT: MAPS-FOIL

ALICE 3 tracker

example: “MAPS foils” — chips within printed circuit boards

- “Novel” concept (revised and updated from 2012)
- Will be studied further as *an* option





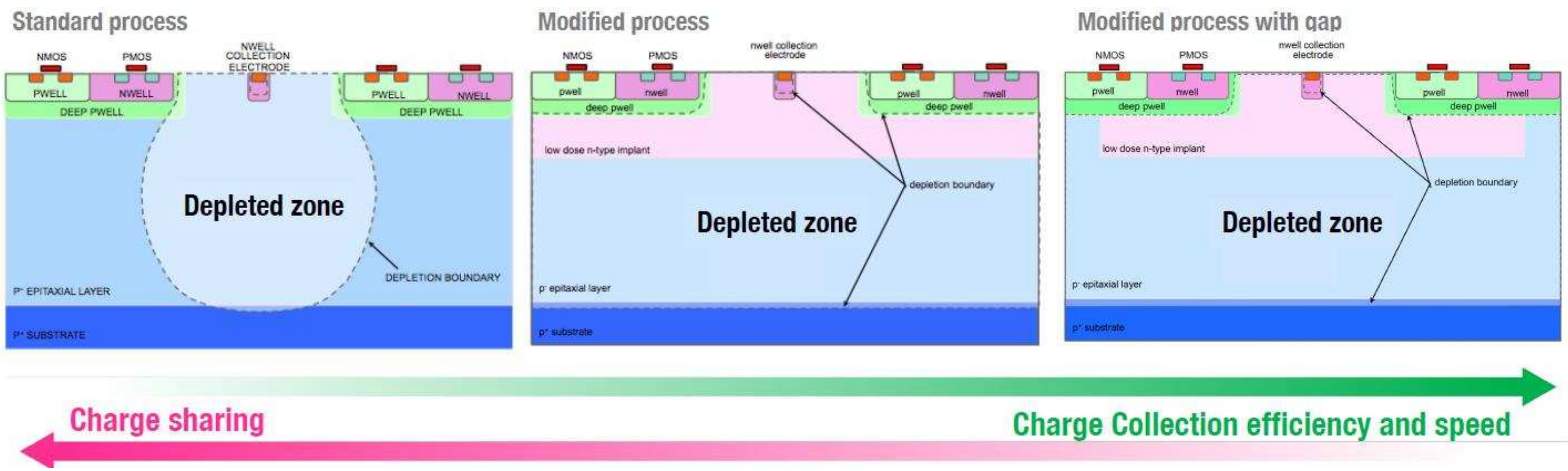
part	thickness
Cu plating	13 µm
Cu gladding	5 µm
Polyimide	45 µm
glue	25 µm
metal stack	10 µm
silicon	45 µm
glue	25 µm
Polyimide	45 µm
total:	**213 µm**

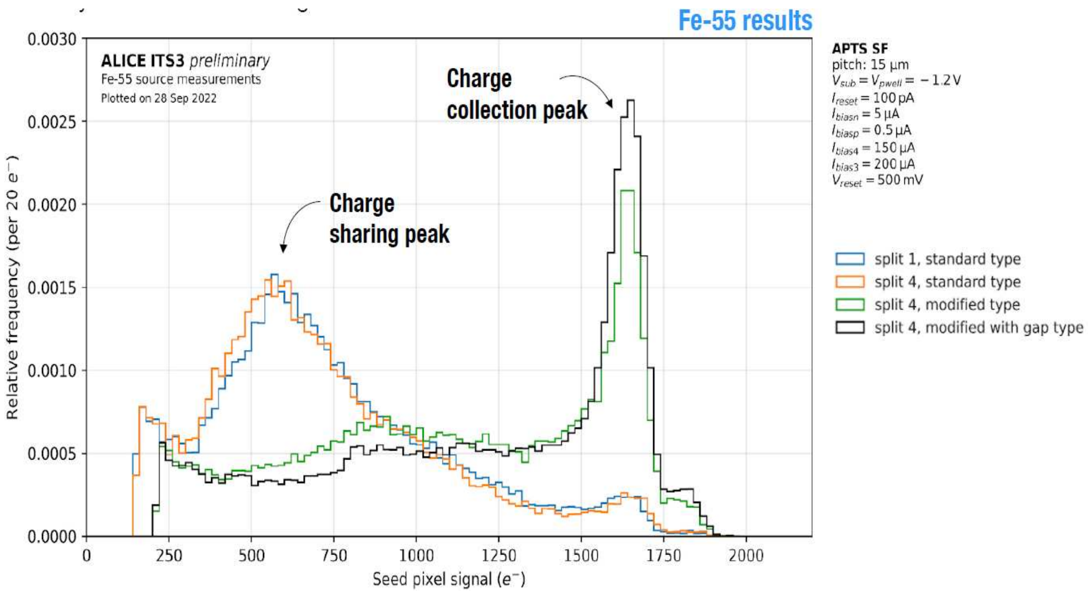
[arXiv:2205.12669]

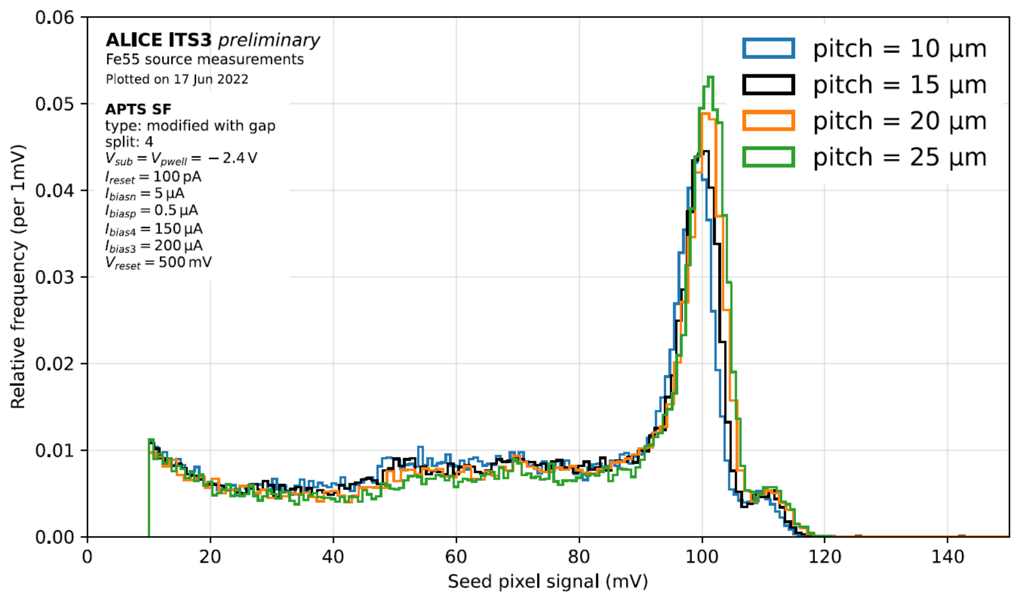
Magnus Mager (CERN) | ALICE ITS3 / ALICE 3 tracker | CBM-MVD retreat | 16.09.2022 | 34

Next steps: stitched sensors, multi-layer module ?

65 nm CMOS TECHNOLOGY: CLUSTER CHARACTERISTICS

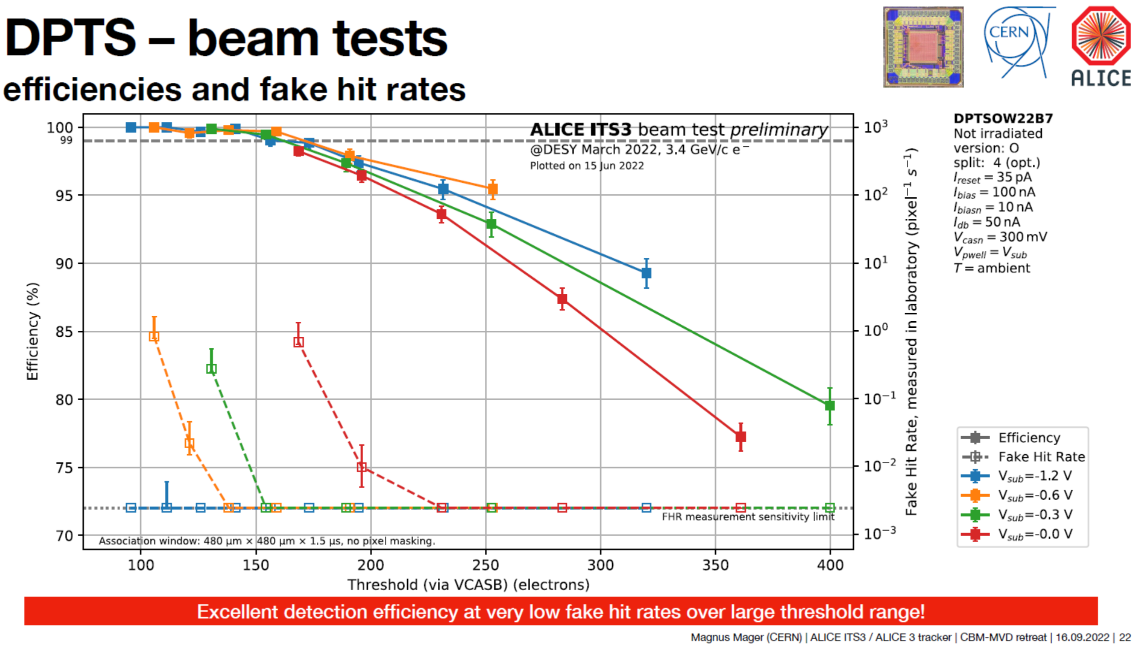


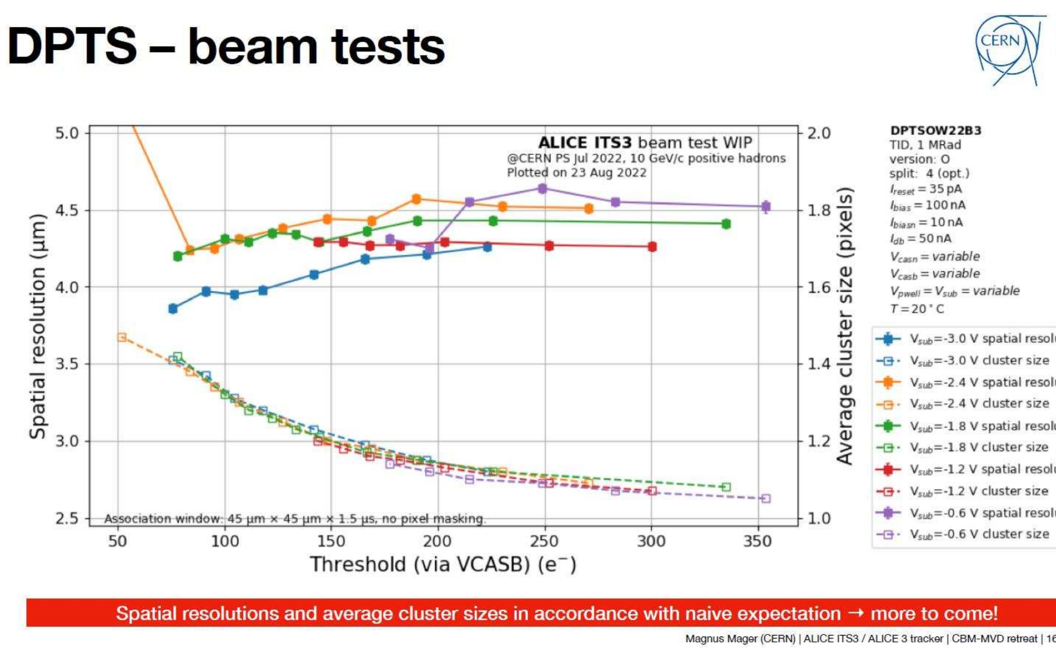




65 nm CMOS TECHNOLOGY: DETECTION PERFORMANCES

- Exploration of 65 nm CMOS process: small prototypes fabricated in 2021 (MLR1)
  - Analog (10, 15, 20, 25 μm pitch) and Digital (25 μm pitch) output mini-prototypes
  - Detection efficiency & Spatial resolution vs discrimination threshold

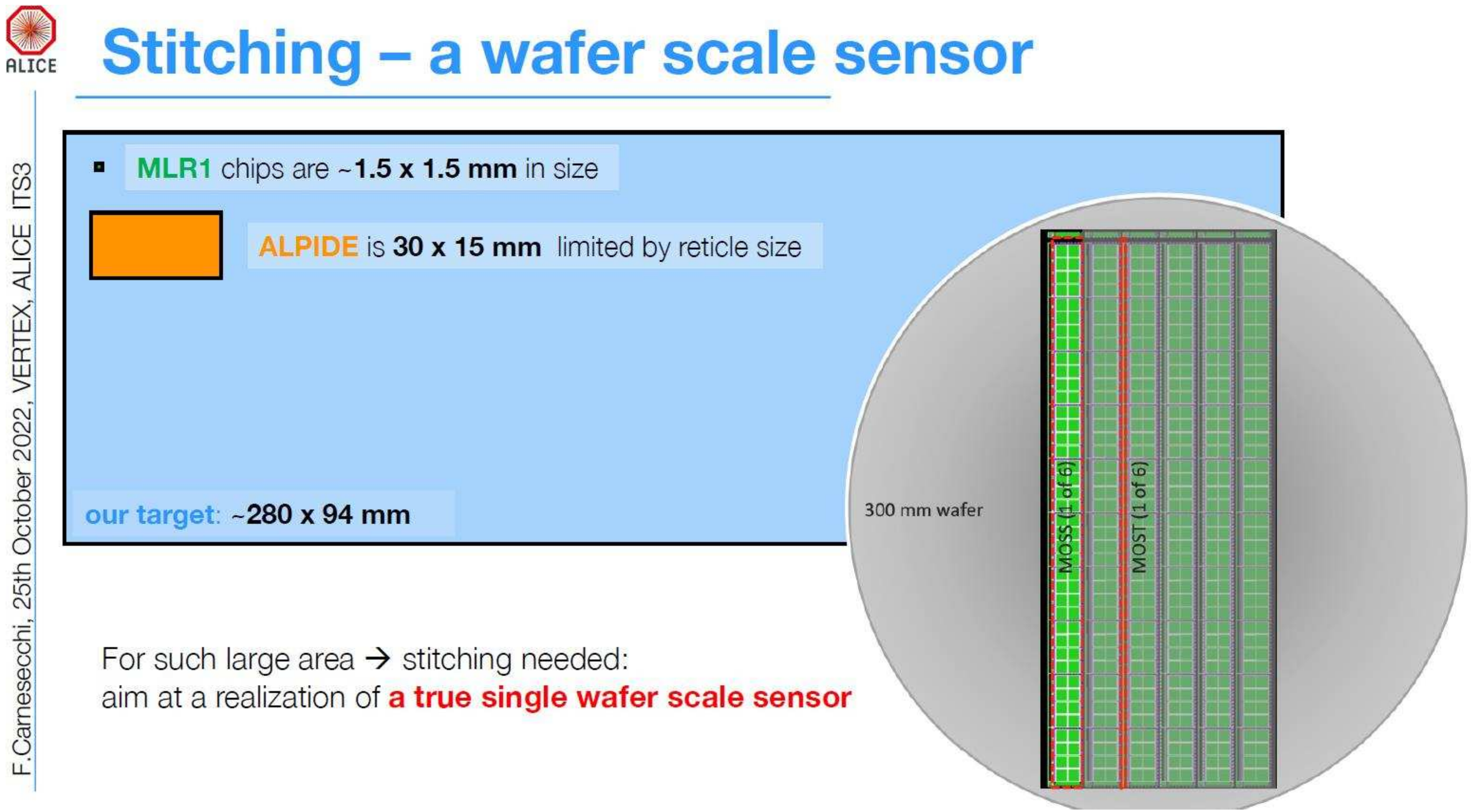




  - Fake rate low
  - Plateau in detection efficiency > 99 % up to $\simeq 150$ e^{-} (despite thin EPI)

65 nm CMOS TECHNOLOGY: STITCHING

- Exploration of 65 nm CMOS process: large prototypes
  - Next step: Engineering run (ER1) with long prototypes trying stitching ⟶ back in Spring'23
  - Ultimate goal: Achieve wafer scale sensor for the ALICE-ITS3 (ER2 in 2024 ⟶ ER3 for LS3)

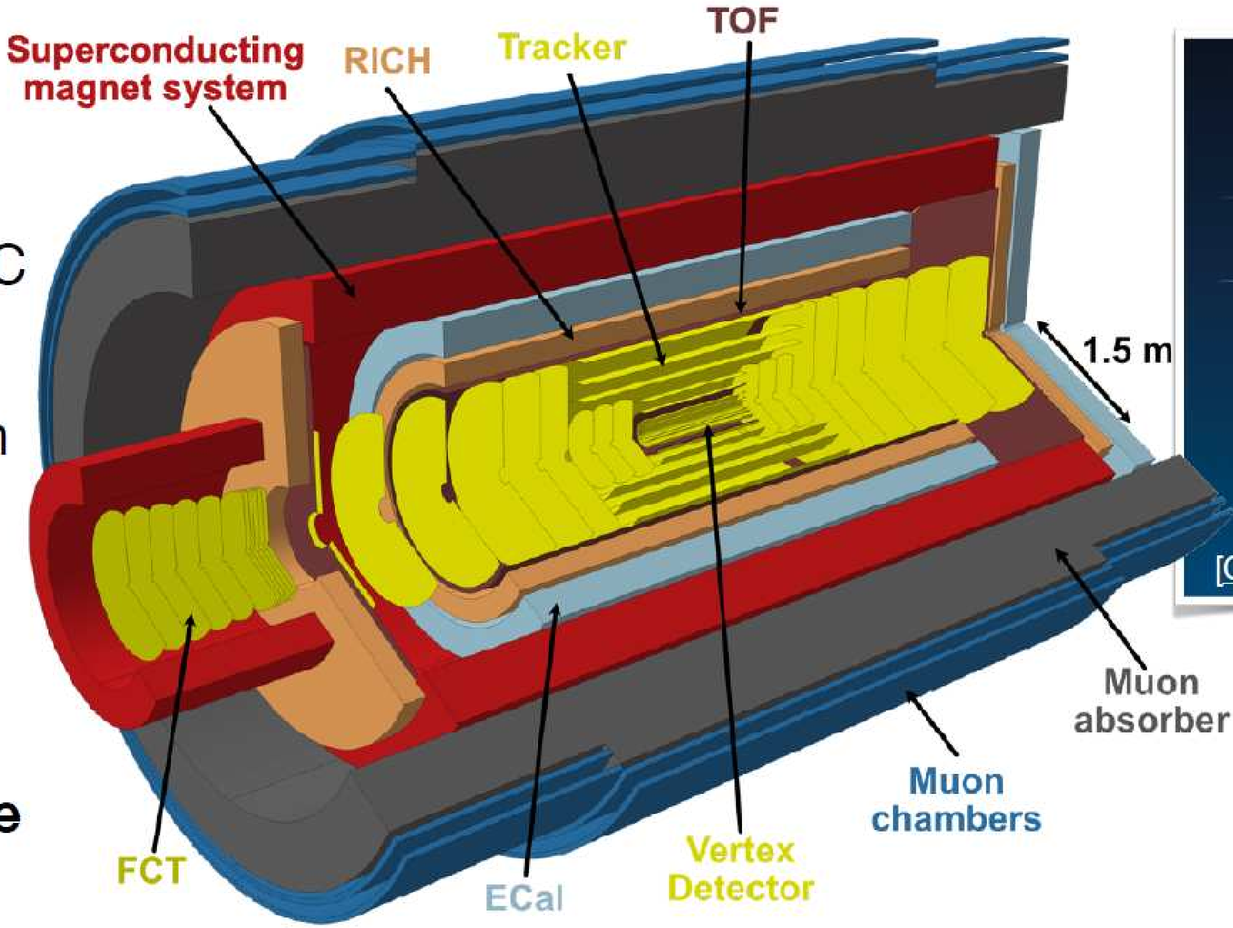


TOWARDS LARGE AREA HIGH RESOLUTION TRACKERS

ALICE 3

Overview

- ALICE proposes to build a completely new detector in LHC LS4 (2033-34)
- It will heavily rely on silicon detectors
- Central part: **a 60 m² MAPS tracker**
  - with **in-beampipe** vertex layers



[CERN-LHCC-2022-009]

Letter of Intent very positively evaluated by LHCC → R&D programme ramping up!

GROUPS INVOLVED – PROJECTS CONCERNED

- DESY: 65 nm generic R&D, Belle-II, EURIZON
  - Charge collection system simulation software (Allpix^2)
  - 65 nm technology design and characterisation
  - CMOS sensor tests (e.g. EUDET beam telescope, PLUME module)
- GSI: experiments at FAIR (e.g. CBM-MVD/STS), ALICE-ITS3, EURIZON
  - CMOS sensor characterisation (MIMOSIS)
  - System integration (MIMOSIS in CBM-MVD)
  - CMOS sensor bending and related integration issues (ITS3)
- IPHC-Strasbourg: 65 nm generic R&D, ALICE-ITS3, BelleII upgrade, Higgs-Factory, EURIZON
  - CMOS sensor design & characterisation for CBM-MVD (MIMOSIS), extension to Higgs-Factory
  - 65 nm generic prototyping (design and testing)
  - ITS3: chip bending, stitching
- IJClab-Orsay: Belle-II (extension to Higgs-Factory)
  - System integration (vertex detector ultra-light cooling)

SUMMARY

- DMlab: hub fostering partnership between groups involved in the development of upcoming & future high precision and ultra-light vertexing and tracking devices for experiments addressing DM search

- Generic concept developed follows ALICE-ITS3 design, complemented with the R&D on CMOS pixel sensors in 65 nm technology

- Rich spectrum of groups' expertise, activities, projects, interests, ... (my own understanding):
  - DESY: sensor response simulation & track reconstruction SW; 65 nm sensor design & tests
  - GSI: curved sensor integration (ITS3 & beyond); sensor tests & integration for expts at FAIR (e.g. CBM)
  - IPHC: sensor design, simul. & tests (ITS3, Belle-II, Higgs-Fact, 65 nm), curved sensor integration (ITS3)
  - IJClab: integration (cooling) of future vertex detector based on CMOS sensors in case of Belle-II upgarde

- Next steps:
  - Identify specific topics of partnership
  - Define type of partnership and modus operandi

- Not addressed yet (resources !):
  - multi-layer detection modules $\Rrightarrow$ multiple impacts per layer traversed
  - sensor stacking $\Rrightarrow$ squeezed pixel dimensions