

Last 5 years of R&D J. Nanni

Conseil scientifique du



V. Boudry, J. Nanni

Silicon Detector

- Sampling Calorimeter
- Based on silicon PIN diode (pixelated wafer)
- Inverse polarisation voltage
- Leakage ~0.5nA
- Depletion zone: trade-off
- 1 MIP = 25000 e- (for 320µm)
- Target : 750µm
- 6 inch vs 8 inch





Produced by Hamamatsu Photonics

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Skiroc 2 (a) ASIC



- 64 channels Internal trigger 15 memories
- Packaged in BGA for thickness
- Power-pulsed
- AMS 0.35µm





Designed by S. Callier @ OMEGA

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ASU version 13 (2018-2019)

- Electronic card handling the reading ASICs and the wafer
- Nominal integration level
- 16 skirocs 1024 channels in 180x180 mm²
- Mechanical precision 20µm
- Interconnections for daisy chaining

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Designed by R. Guillaumat, F. Magniette and J. Nanni

2**B**



Full DAQ

- Slab = ASU + SMB + DIF + Hood
- Low speed DAQ : adapted to ILC timing
 - $\circ~$ 5 or 10 Hz trains
 - $\,\circ\,$ 1 ms for 2700 bunch crossings
 - Bad timing for testbeams
- Cables
 - $\circ\,$ HDMI from DIF to GDCC
 - Ethernet from GDCC to PC

Published in TWEPP'13 & TIPP'14



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Calicoes software

- Based on Pyrame framework
- Allows to configure and run the detector
- Collect and store data
- online stats & monitoring
- Web interface
- Used by Wagasci, HGRoc benches, Pepites

Designed by F. Magniette & M. Rubio-Roy



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Online monitoring

• Decode and plot data in real-time



Short slabs stack prototype

- Up to 10 short slabs (1 ASU)
- Mechanical structure with tungsten plate slots (24 X₀)
- Patch-panel for Power-supplies

Designed by M. Frotin, R. Cornat & J. Nanni





Long slab

- Electrical prototype of the future ILD slab : 8 ASUs long (1440x180 mm² of detecting surface)
- No mechanical constraint



Designed By J. Nanni & F. Magniette



Mechanical structure

- Porting structure with rotation system
- Shielding from EM perturbation



Designed by M. Anduze & E. EdyV. Boudry, J. NanniCALICE/ILD – CS LLR, 20/10/2022





Hints for next version

- Inflexion is a sum of two effects
 - power supply weakening along line
 - Bandgap dispersion (uniform random)
- Need for octopus power-supply (same line length for all ASU)
- Need for better bandgap or software compensation





y=a*ASU+b+c*BG(ASU)

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Control PC

New DAQ system (2020)



- New interface board: SL-Board •
- New concentrator board: Core-mother ٠

CORE-MO

THER

- Add backplane board for stack •
- Software based on LabWindows ٠

Gbit UDP/USB/Optical Fibre

Other utility I/Os

External clock





Interface board SL-Board

Delivers the regulated power supplies (LV, HV)

- Control the SK2A
- Perform full data readout for LONG slab
- Connected by USB or kapton (through backplane)
- MAX 10 + ADC for monitoring
- Consumption: <1W
- Flash EEPROM for serial number





Front end side

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Backplane: Core-kapton



Core Module connector (100 pins):

7 common differential pairs for sensitive signals,30 individual pairs for control and readout,14 common lines, GND

Core-kapton length: 40cm

- Interface between Core-Mother and SL-Board
- Permit to drive up to 15 SLABs + synchronisation
- Transmit clock and fast signals

Slow control speed: 40MHz

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SL_board connectors (40 pins):

7 common differential pairs for sensitive signals,*1 individual pair* for control and readout,14 common lines, GND



Core Module

COntrol and REadout Mother board

- 2 connectors for individual acquisition system (Core daughter)
- External I/O for synchronisation with other detector
- Core mother send common clocks and fast signals for sync
- Control and readout possible with: USB, Ethernet or optical link
- Consumption: 5W





The CORE mother CALICE/ILD – CS LLR, 20/10/2022



The CORE daughter

Core Daughter

- Based on CYCLONE IV FPGA
- Interface between CORE kapton and mother board
- Buffer clock and fast signals
- Readout: 60Mbyte/s if USB and 125Mbyte/s if UDP

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Acquisition software

- Written in C under Labwindows CVI
- Handle whole detector
 - Two sides with 15 SLABs
 - 5 ASU per SLAB
- Make advanced measurement
- Hardware automatically detected
 - Number of SLAB
 - FEV type + number of ASU
- Slowcontrol:
 - All parameters programmable



Calibration pulses

- 2 ranges of amplitudes for HG & LG DAC on SL board: few mV to 150mV
- FPGA can generate equidistant pulses:
 - Testing synchronisation
 - Study re-triggers, ...

Help to adjust common/individual threshold up to 0.25MIP

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New front end board FEV2.0 (2021)

Observation from previous test beam @ DESY 2018 with electrical long SLAB:

- Voltage drop
- Clock configuration integrity
- Power pulsing

New feature of FEV 2.0:

- 1 LDO (low drop out) per SK2A on analog power supply
- 1 LDO per 4 SK2A on digital power supply
- Add buffer on configuration clock (every 8 SK2A)
- Driving HV (up to 350V) + add filter for each wafer
- Improve shielding for analog signal and power supply

6 months delayed due to cabling problem & components supply

Designed by T. Dos Santos & R. Guillaumat & S. Callier & J. Nanni



Power distribution dedicated for LONG SLAB



Expected results

In the electrical long SLAB, 8 boards are chained and due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.



 \rightarrow We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop and reduce common noise.



Preliminary results

Pedestal measurements: mean values



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FEV 11

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FEV 2.0

Preliminary results

Pedestal width measurements: RMS values (adc count)

FEV 2.0: Mean RMS 2.2 adc count, max 5.8 Pedestal/Charge Measurements Enable Pedestal/Charge Measurements: V On/Off Select for Plot or Histo Measurement: Left V SLAB 0 @0 V ASU0 V Measurements Type Select for Plot: ALL ASICs V All Channels V All SCAs V High Gain V Max Nb Of Entries (per SCA) = 1000 Pedestal (No Hit Flag) Charge (Hit Flag) Histogram and RMS Plots available for Plot Type RMS Core Left SLAB 0 T ASU 0 T 0.000 0.000 After gaussian fit; 0.000 0.00 Histos Mean Values RMS Nb Of Entries Update Histo % 100 acquired frames No Of Entries Pedestal RMS Values [adc] vs Channel and SCA Nb Of Bins for Histo 327 I On/Off Histogram Exclude 0n/Off 56 Pedestal/Charge Values below 54 \$ 0.00 [adc count] 5.2 and above 5.0 10.00 [adc count] 48 Pedestal Measurement: 4.6 4.4 Save Pedestal Values to Calib Structure 42 (for selected Core/Slab/Asu:) If Nb of entries >= 100 Save Pedestals from Calib Structure to Calib Files Charge Measurements Save Charge Measurement to Files Skiroc/Ch8 [1 Skiroc/Ch9 [16] Skiroc/Ch11 [16] Skiroc/Ch13 [16] 200 300 400 500 800 900 1000 1100 1200 1300 1400 146 100 600 700 Skiroc/Ch7 I16 Skiroc/Ch15 [16] channel + SCA_Index x 100 Y Axis Scale Manual Auto Y min 🗍 0.00 Y max 🗍 100.00 X Axis Scale Manual Auto X min 🗐 0.00 X max 🖏 1465.00

FEV 11: min RMS 2.2 adc count, max 138! Pedestal/Charge Measurements Enable Pedestal/Charge Measurements: 🔽 On/Off Select for Plot or Histo Measurement: Left V SLAB 0 @0 V ASU0 V Measurements Type Select for Plot: ALL ASICs V All Channels All SCAs V High Gain V Max Nb Of Entries (per SCA) Pedestal (No Hit Flag) Charge (Hit Flag) Histogram and RMS Plots available for : Plot Type: RMS Mean Mean Sigma Core Left SLAB 0 T ASU 0 T 0.000 0.000 After gaussian fit: 0.000 0.00 Mean Values RMS Nh Of Entries Update Histo % 100 acquired frames Pedestal RMS Values [adc] vs Channel and SCA Nb Of Bins for Histo 2 952 I On/Off 138.3 135.00 Histogram Exclude 0n/Off 130.00-Pedestal/Charge Values below: 125.00-10.00 [adc count] 120.00and above 115.00-10.00 [ade count] 110.00-105.00 Pedestal Measurements 100.00-Save Pedestal Values to Calib Structure 95.00 for selected Core/Slab/Asu) 90.00 If Nb of entries >= 2 100 85.00 80.00 Save Pedestals from Calib Structure to Calib Files 75.00 70.00 65.00 Charge Measurements 60.00 55.00 Save Charge Measurement to Eles 50.00 45.00-40.00 35.00 30.00-Skiroc/Ch9 [16] 25.00-20.00-Skiroc/Ch11 [16] 15.00-10.00 Skiroc/Ch13 [16] Skiroc/Ch5 [16] 2 29 Skiroc/Ch15 [16] Skiroc/Ch7 (16) channel + SCA Index x 100 Y Axis Scale Manual Auto Y min 🗐 0.00 Y max 🗐 100.00 X Axis Scale Manual Auto X min 🗐 0.00 X max 🗐 1465.00

Preliminary results

Hit vs threshold



FEV 11: All Skirocs/All Channels/All SCAs

Noise on every channel

FEV 2.0: All Skirocs/All Channels/All SCAs



Good results except on channel 9 of SK6

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Threshold scans and effect of shielding

Threshold scan between 200 and 250 with 20 steps (3 adc count/step)



Without shielding

With shielding

New HV kapton

Higher reliability

- □ Easy to handle ASU
- Only 1 board glued per kapton
- Protection of wafer for U insertion
- Easy to chain board for LONG slab





Designed by R. Guillaumat & T. Dos Santos & J. Nanni 24

Delamination of ASU

Since 2018, we observed problem of delamination PCB bending ?

- o Deformation of PCB
- o Carry out fake cabling with existing material
- o Metrology at each step

Surface issues ?

- o Handling, intensive tests, degradation of pad surface
- o Will inquire with glue producers
- Try to produce fake sensor with AI or Au coating

Quality of glue ?

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- o Glue is 2 components material, mixture is correct ?
- o Always use small quantity ...
- o Did the glue perish over the year







Debugging with SK2A

Analog probe: slow control parameter

- o Allow for reading DC preamplifier output voltage
- o System already implemented in DAQ
- o Measure voltage change if Si connected or not polarised







Need 1024 configuration to test all pads Clearly spotted non connected Si pad Very useful tool to debug gluing

LONG Slab assembly

Launch production before end of 2022:

- o FEV2.1 + supply components
- o HV kapton
- Make metrology after each step (production, cabling, gluing)
- Understand problem of gluing with partners
- Assembly ASU one by one
- Dead line: TB in November 2023

- Designed by E. Edy
- Mechanic structure recycled from previous one







Technical conclusions

- New FEV2.0 give very promising results
 - Good news for LONG slab
- Single ASUs (with FEV13) fully functional with very good S/N ratio
 - High energy response to be validated
- Unique expertise on design and integration
- Reflexion for Higgs factory with our expertise on frontend
 - Need a new version of ASIC
 - with new technology (TSMC)
 - Zero-suppression ?
 - Specification to Higgs factory (need physics simulations)