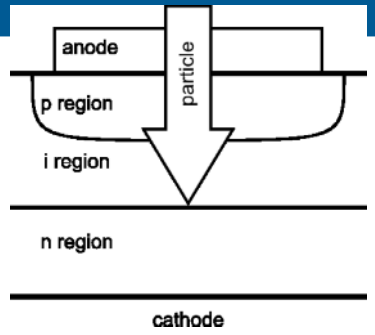
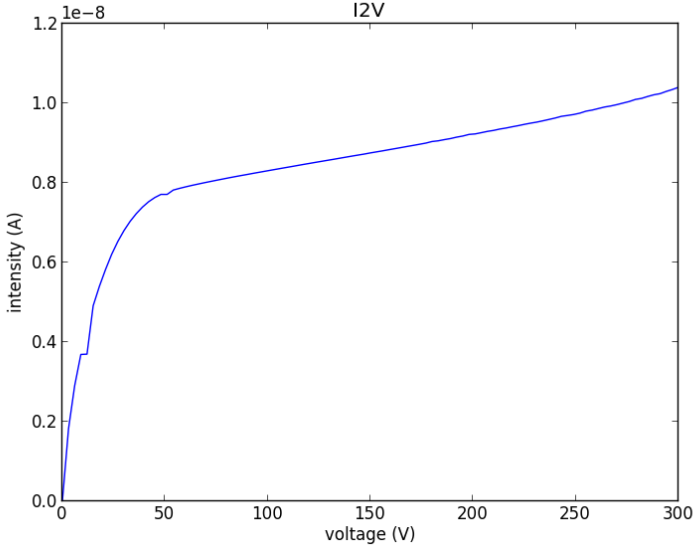
Last 5 years of R&D
J. Nanni

Conseil scientifique du LLR

Silicon Detector

- Sampling Calorimeter
- Based on silicon PIN diode (pixelated wafer)
- Inverse polarisation voltage
- Leakage ~0.5nA
- Depletion zone: trade-off
- 1 MIP = 25000 e- (for 320µm)
- Target : 750µm
- 6 inch vs 8 inch

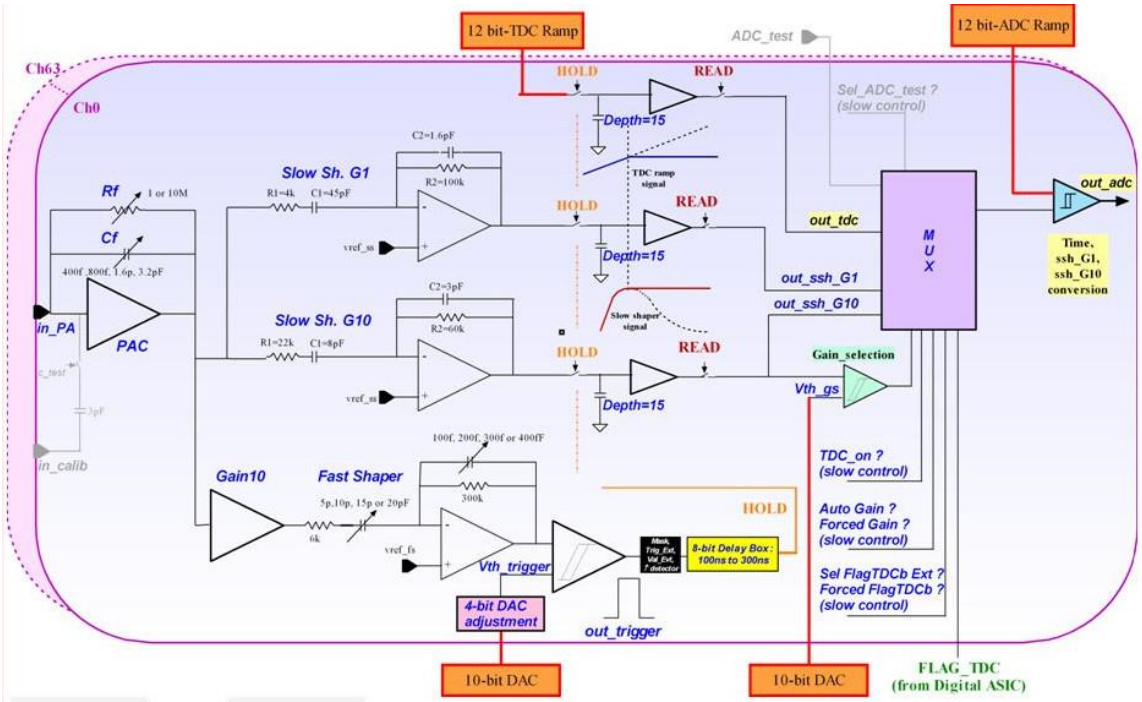




Produced by Hamamatsu Photonics

Skiroc 2 (a) ASIC

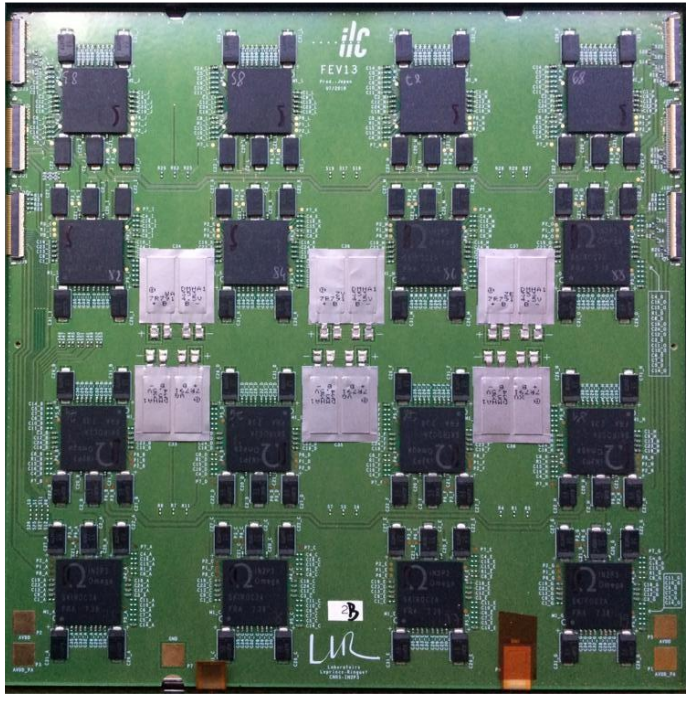
- 64 channels - Internal trigger – 15 memories
- Packaged in BGA for thickness
- Power-pulsed
- AMS 0.35µm

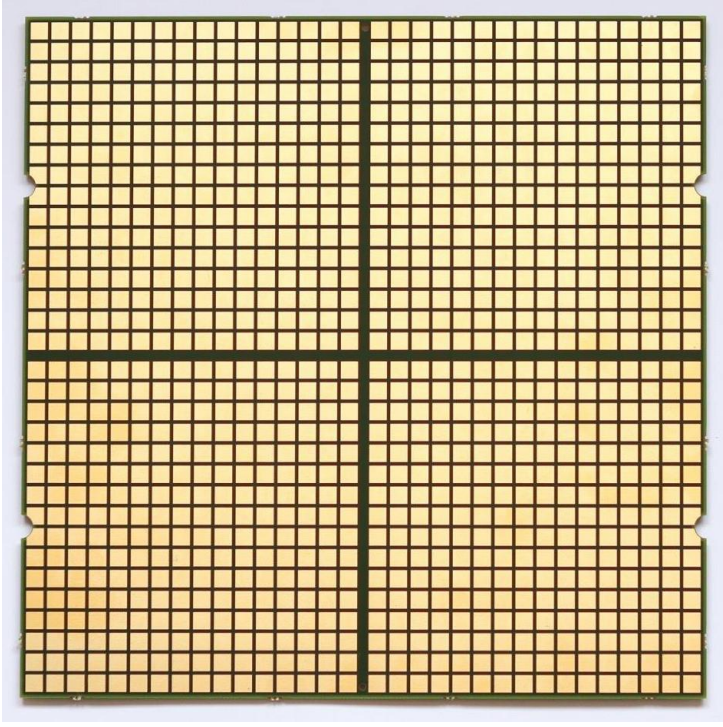


Designed by S. Callier @ OMEGA

ASU version 13 (2018-2019)

- Electronic card handling the reading ASICs and the wafer
- Nominal integration level
- 16 skirocs 1024 channels in 180x180 mm²
- Mechanical precision 20µm
- Interconnections for daisy chaining



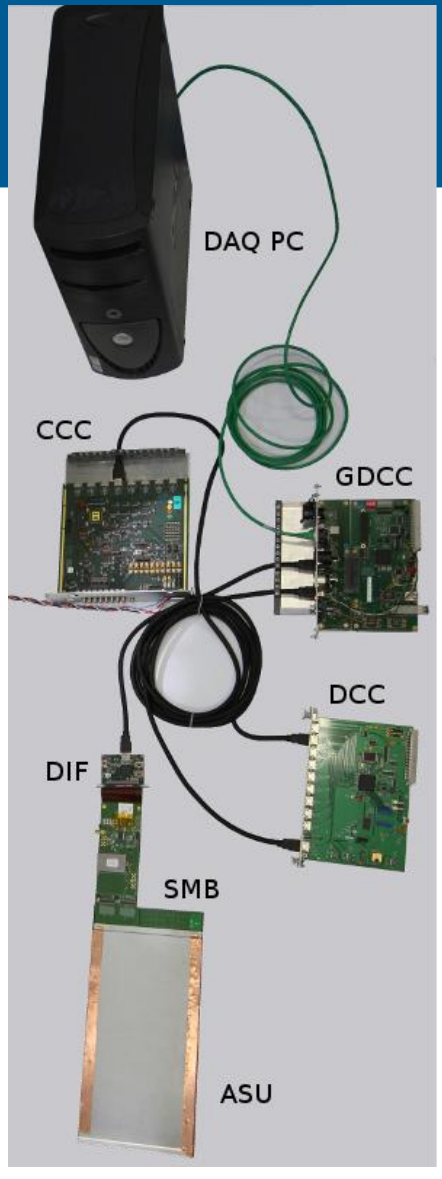


Designed by R. Guillaumat, F. Magniette and J. Nanni

Full DAQ

- **Slab = ASU + SMB + DIF + Hood**
- **Low speed DAQ : adapted to ILC timing**
  - 5 or 10 Hz trains
  - 1 ms for 2700 bunch crossings
  - Bad timing for testbeams
- **Cables**
  - HDMI from DIF to GDCC
  - Ethernet from GDCC to PC

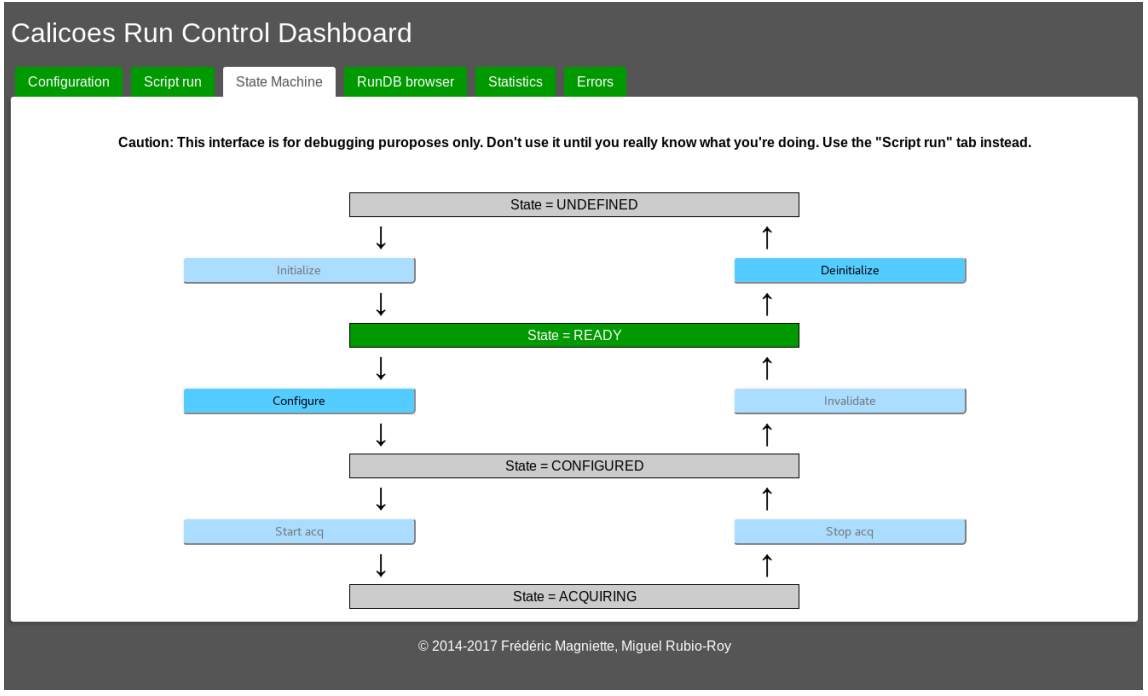
Published in TWEPP'13 & TIPP'14



Calicoes software

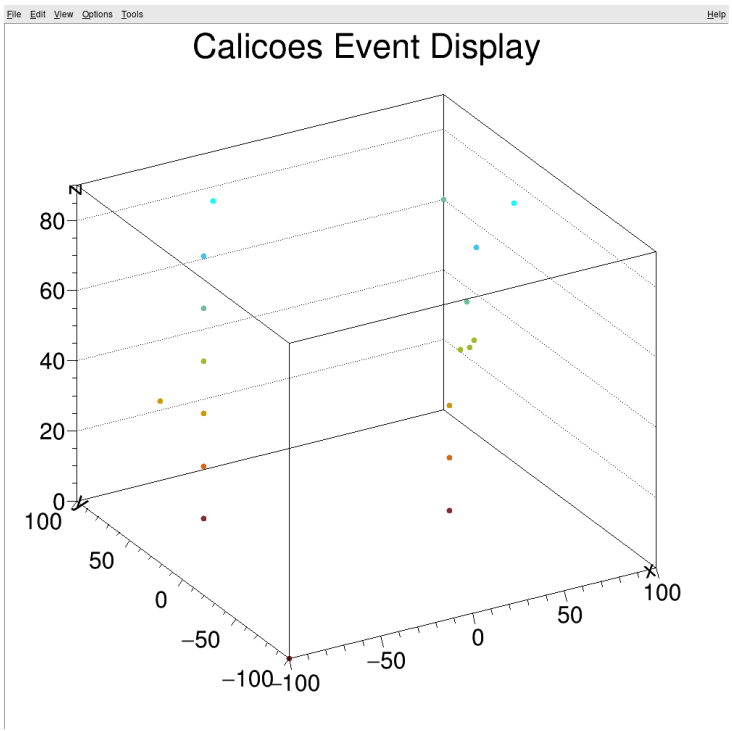
- Based on Pyrame framework
- Allows to configure and run the detector
- Collect and store data
- online stats & monitoring
- Web interface
- Used by Wagasci, HGRoc benches, Pepites

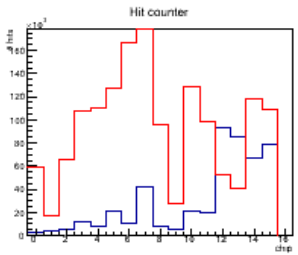
Designed by
F. Magniette & M. Rubio-Roy

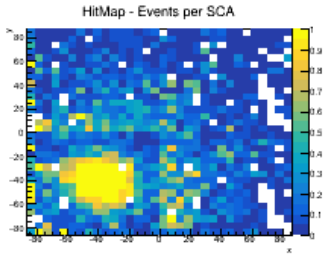


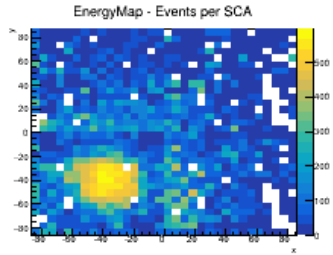
Online monitoring

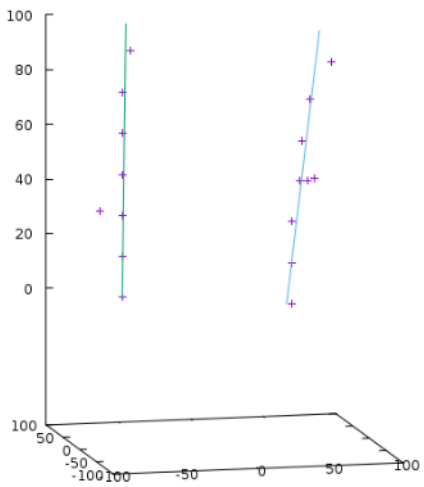
- **Decode and plot data in real-time**
- **Automatic and self-adjusting sub-sampling**









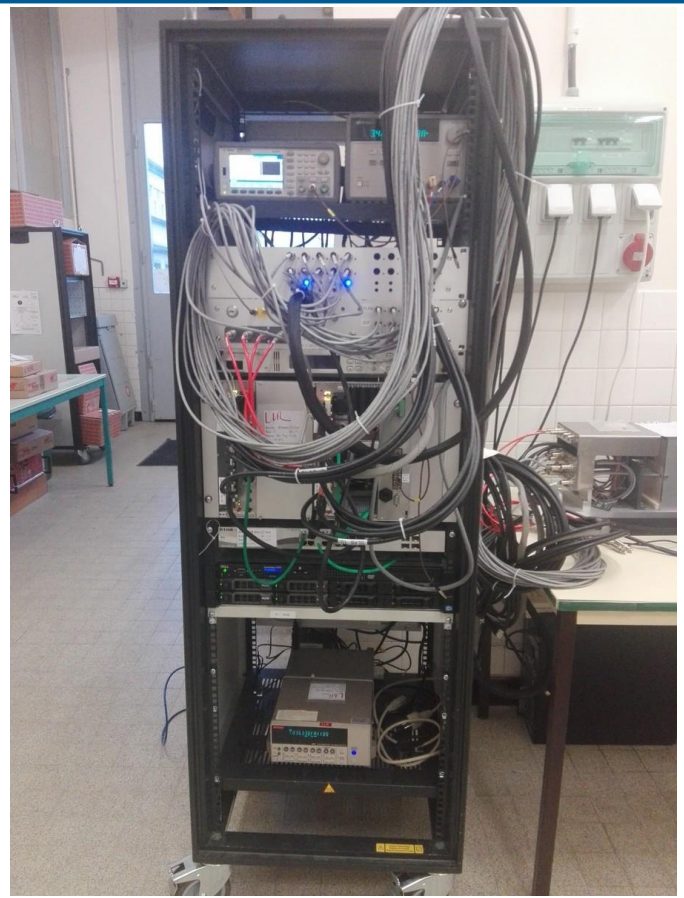


Designed by A. Irles & F. Magniette
Published in CHEF'17

Short slabs stack prototype

- Up to 10 short slabs (1 ASU)
- Mechanical structure with tungsten plate slots (24 X_0)
- Patch-panel for Power-supplies

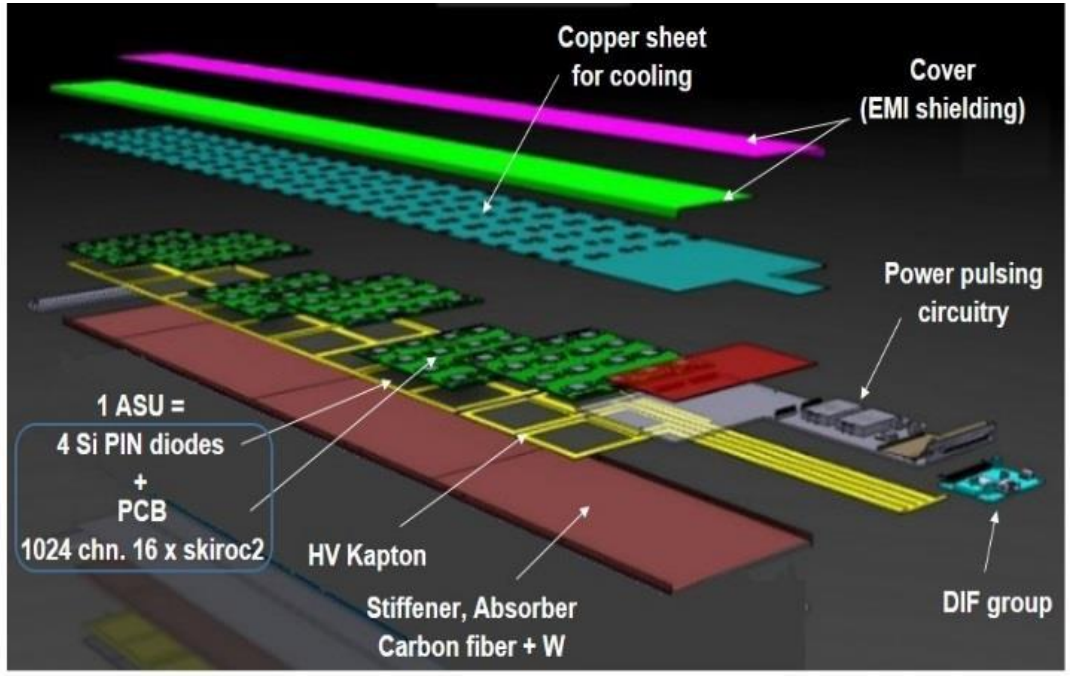
Designed by M. Frotin, R. Cornat & J. Nanni



Long slab

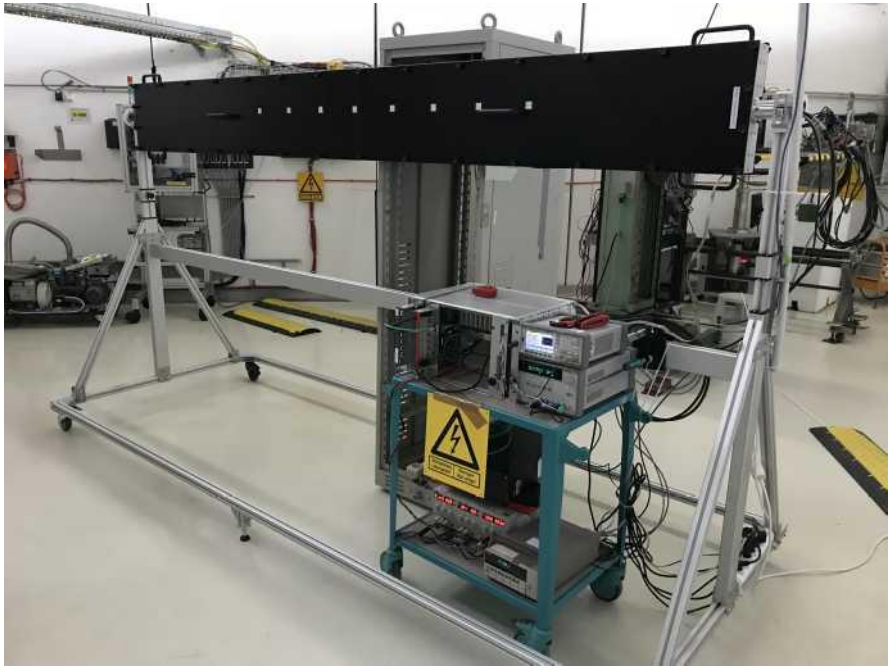
- **Electrical prototype of the future ILD slab : 8 ASUs long (1440x180 mm² of detecting surface)**
- **No mechanical constraint**

Designed
By
J. Nanni &
F. Magniette

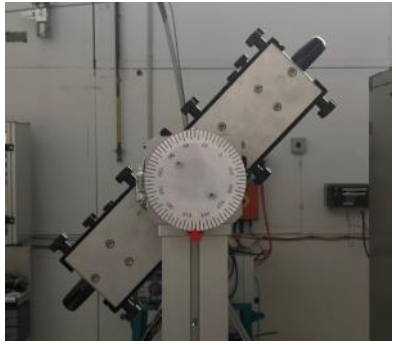


Mechanical structure

- Porting structure with rotation system
- Shielding from EM perturbation

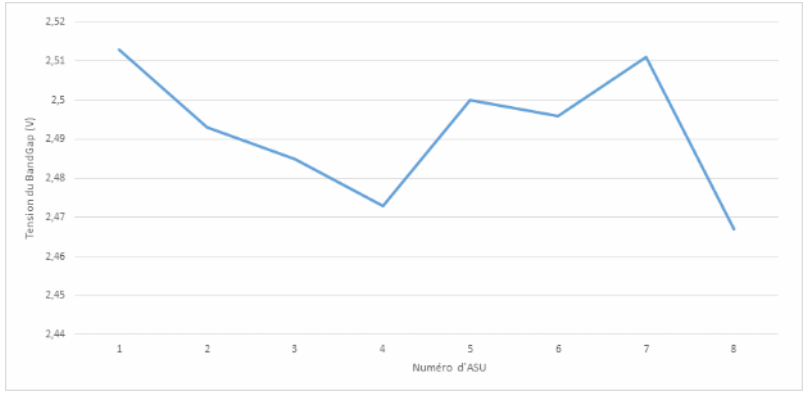


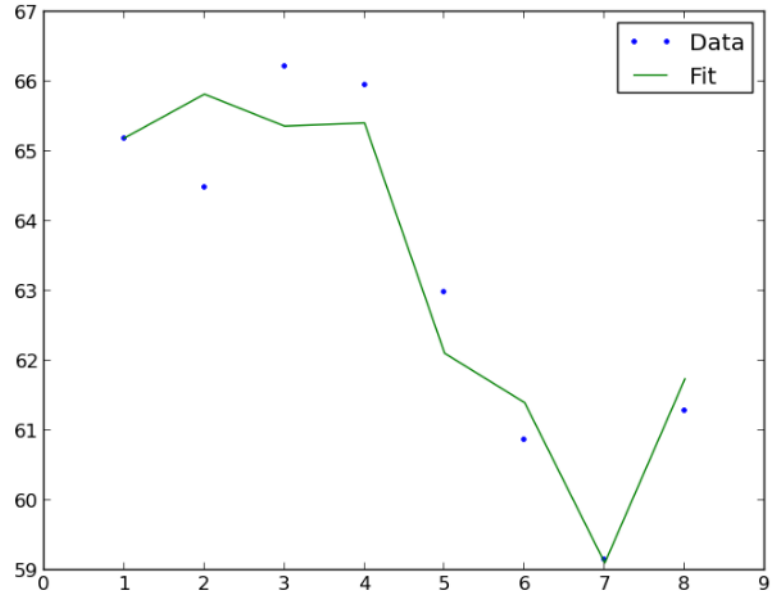
Designed by M. Anduze & E. Edy



Hints for next version

- **Inflexion is a sum of two effects**
  - power supply weakening along line
  - Bandgap dispersion (uniform random)
- **Need for octopus power-supply (same line length for all ASU)**
- **Need for better bandgap or software compensation**



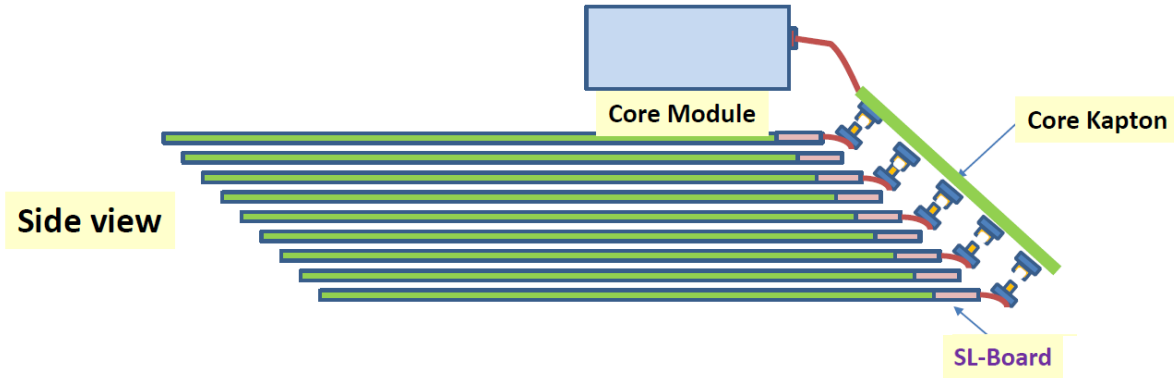


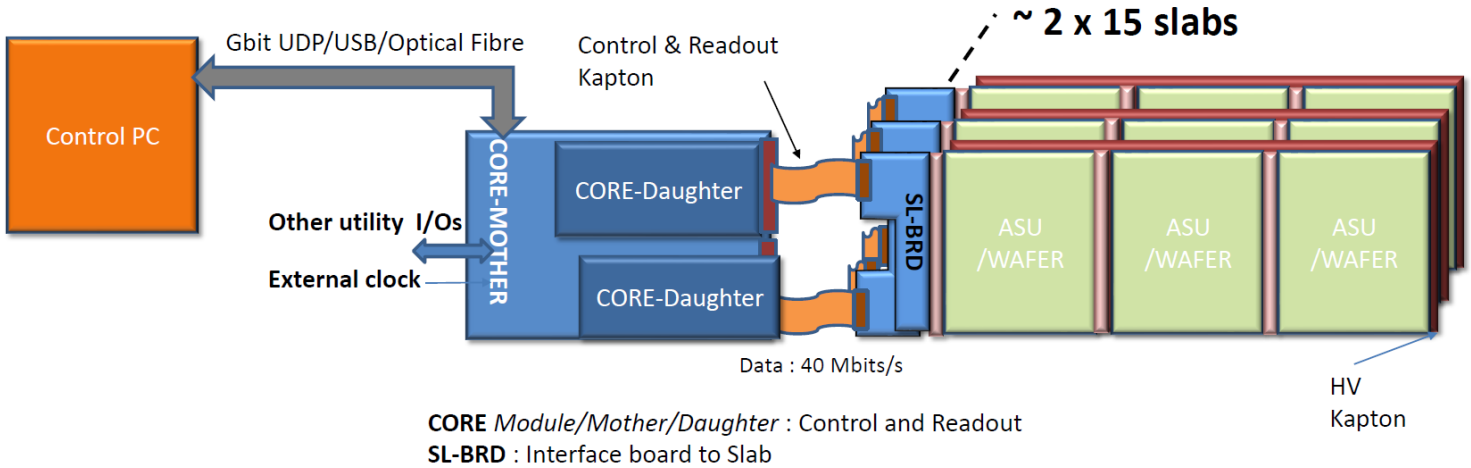
y=a*ASU+b+c*BG(ASU)

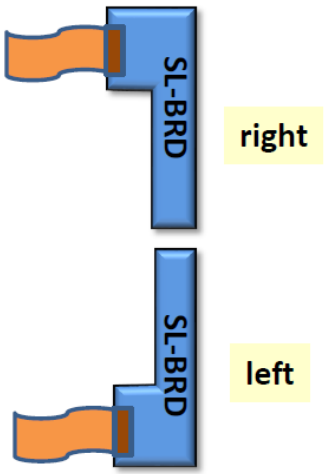
New DAQ system (2020)

Since 2018, IJClab develop new DAQ

- New interface board: SL-Board
- New concentrator board: Core-mother
- Add backplane board for stack
- Software based on LabWindows



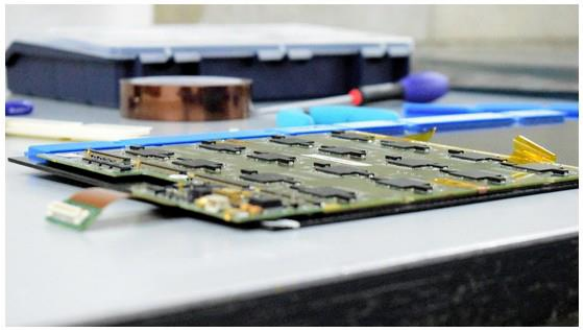


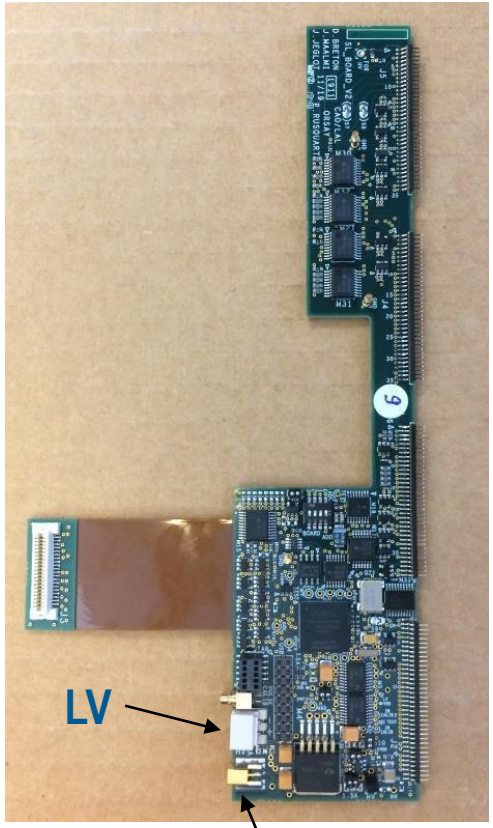


Interface board SL-Board

Delivers the regulated power supplies (LV, HV)

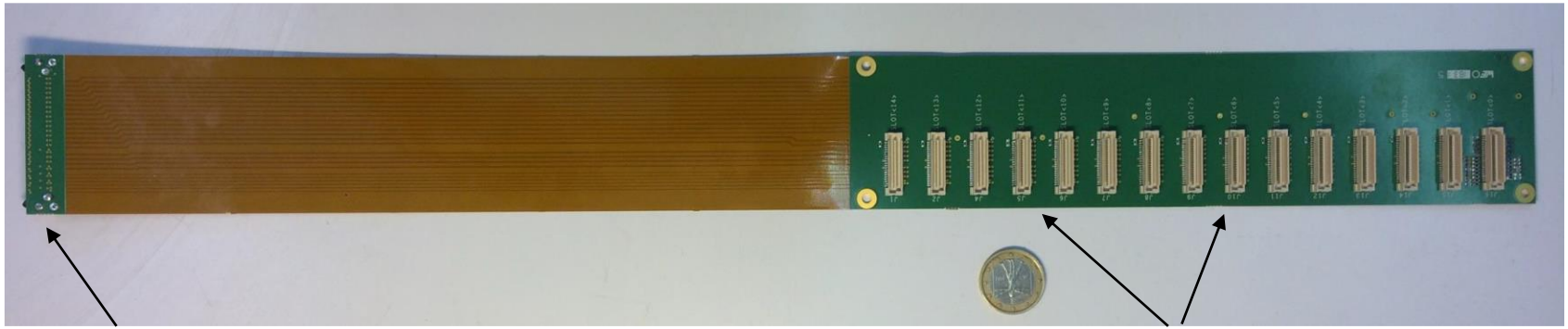
- Control the SK2A
- Perform full data readout for LONG slab
- Connected by USB or kapton (through backplane)
- MAX 10 + ADC for monitoring
- Consumption: <1W
- Flash EEPROM for serial number





Front end side

Backplane: Core-kapton



Core Module connector (100 pins):

7 common differential pairs for sensitive signals,
30 individual pairs for control and readout,
14 common lines, GND

SL_board connectors (40 pins):

7 common differential pairs for sensitive signals,
1 individual pair for control and readout,
14 common lines, GND

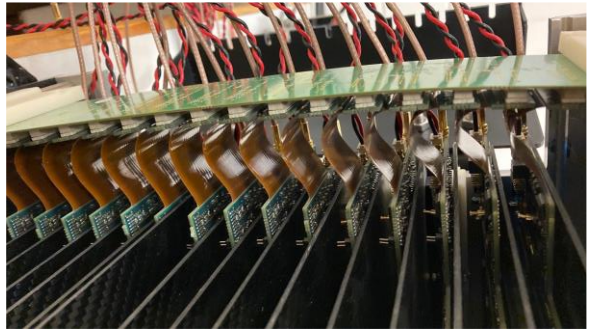
Core-kapton length: 40cm

Interface between Core-Mother and SL-Board

Permit to drive up to 15 SLABs + synchronisation

Transmit clock and fast signals

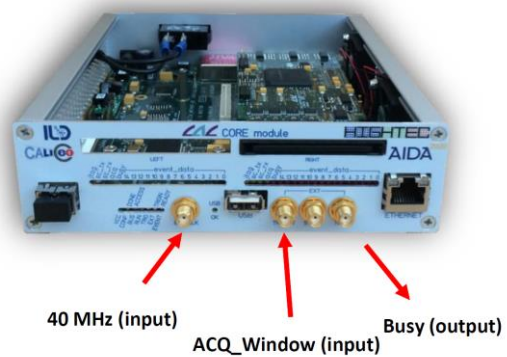
Slow control speed: 40MHz



Core Module

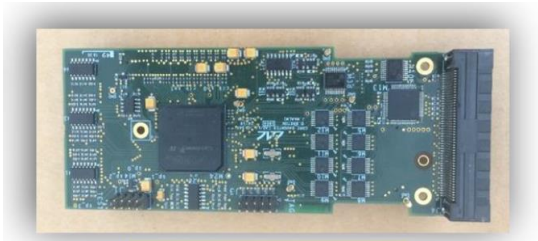
COntrol and REadout Mother board

- 2 connectors for individual acquisition system (Core daughter)
- External I/O for synchronisation with other detector
- Core mother send common clocks and fast signals for sync
- Control and readout possible with: USB, Ethernet or optical link
- Consumption: 5W



The CORE module

The CORE mother



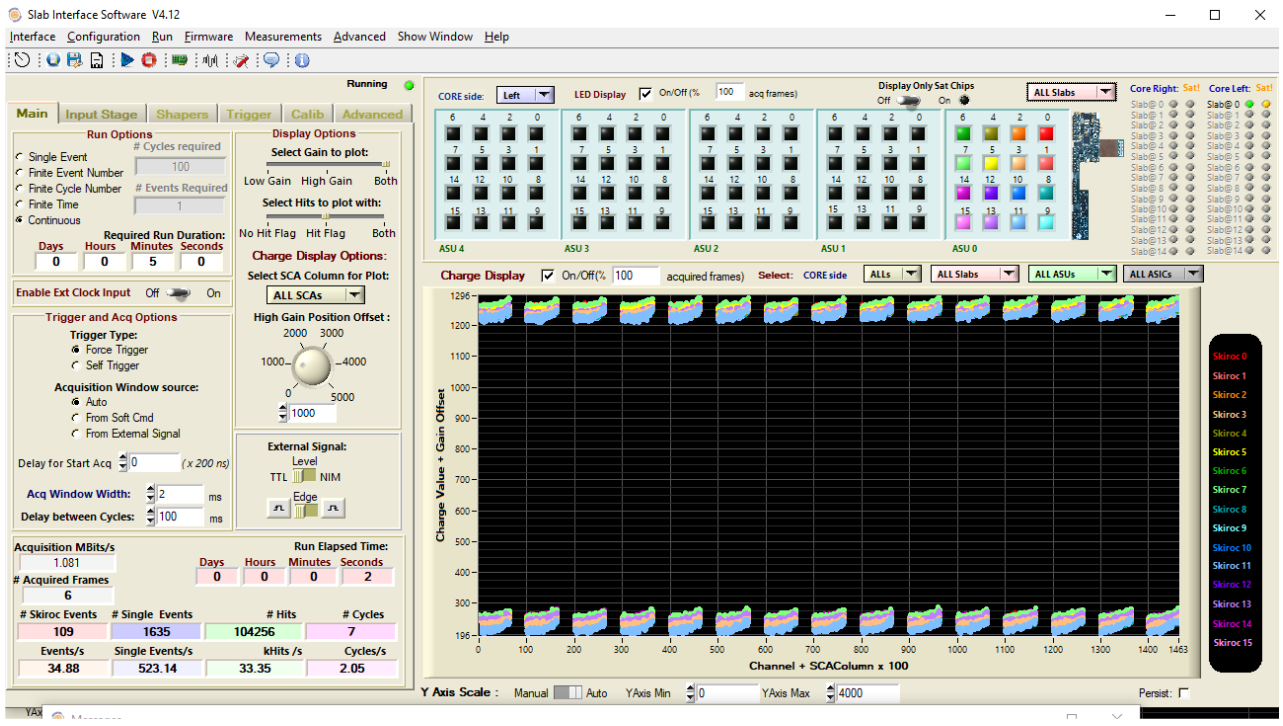
The CORE daughter

Core Daughter

- ❑ Based on CYCLONE IV FPGA
- ❑ Interface between CORE kapton and mother board
- ❑ Buffer clock and fast signals
- ❑ Readout: 60Mbyte/s if USB and 125Mbyte/s if UDP

Acquisition software

- **Written in C under Labwindows CVI**
- **Handle whole detector**
  - Two sides with 15 SLABs
  - 5 ASU per SLAB
- **Make advanced measurement**
- **Hardware automatically detected**
  - Number of SLAB
  - FEV type + number of ASU
- **Slowcontrol:**
  - All parameters programmable



Calibration pulses

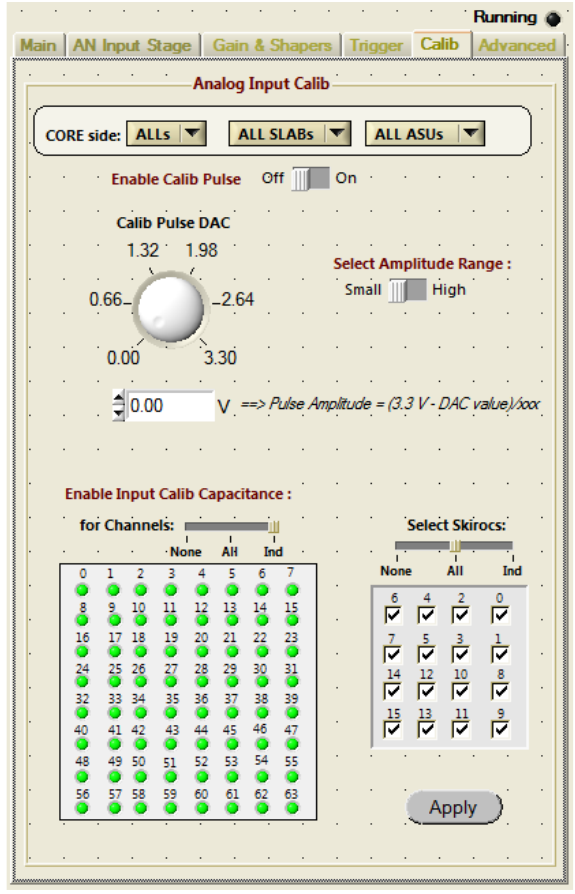
2 ranges of amplitudes for HG & LG

DAC on SL board: few mV to 150mV

FPGA can generate equidistant pulses:

- Testing synchronisation
- Study re-triggers, …

Help to adjust common/individual threshold up to 0.25MIP

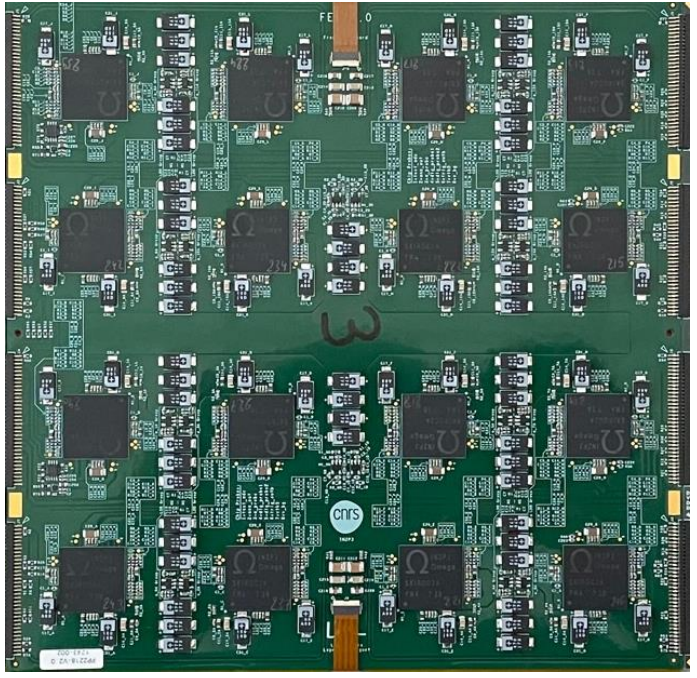


New front end board FEV2.0 (2021)

Observation from previous test beam @ DESY 2018 with electrical long SLAB:

- Voltage drop
- Clock configuration integrity
- Power pulsing

Designed by T. Dos Santos & R. Guillaumat & S. Callier & J. Nanni

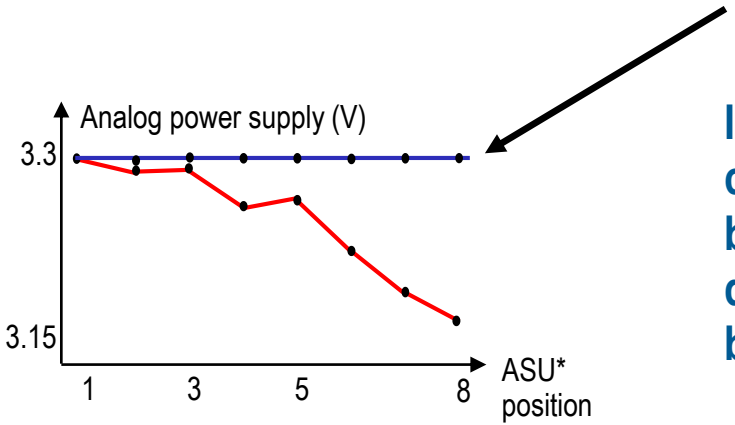


New feature of FEV 2.0:

- 1 LDO (low drop out) per SK2A on analog power supply
- 1 LDO per 4 SK2A on digital power supply
- Add buffer on configuration clock (every 8 SK2A)
- Driving HV (up to 350V) + add filter for each wafer
- Improve shielding for analog signal and power supply

6 months delayed due to cabling problem & components supply

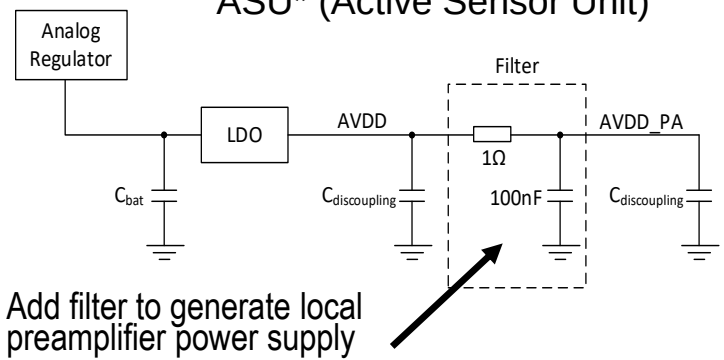
Power distribution dedicated for LONG SLAB



Expected results

In the electrical long SLAB, 8 boards are chained and due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.

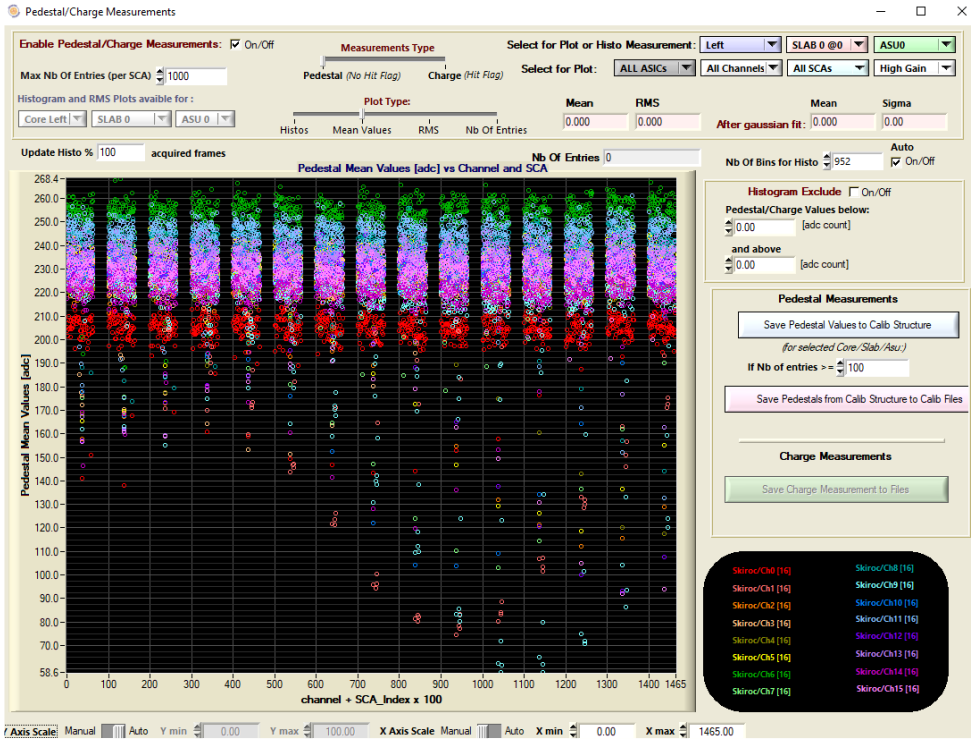
ASU* (Active Sensor Unit)



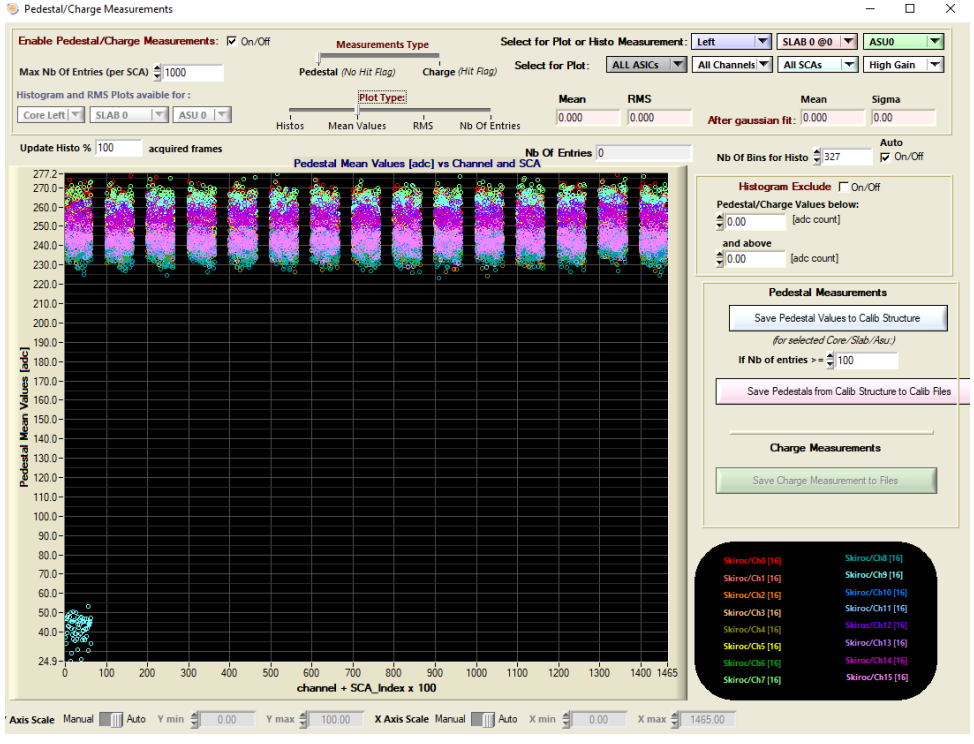
→ We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop and reduce common noise.

Preliminary results

Pedestal measurements: mean values



FEV 11

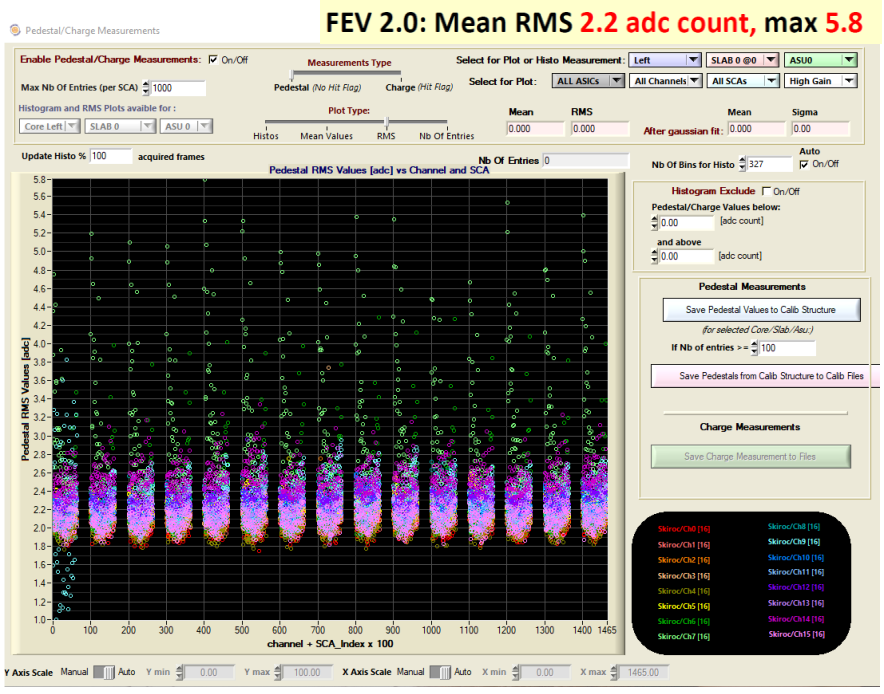


FEV 2.0

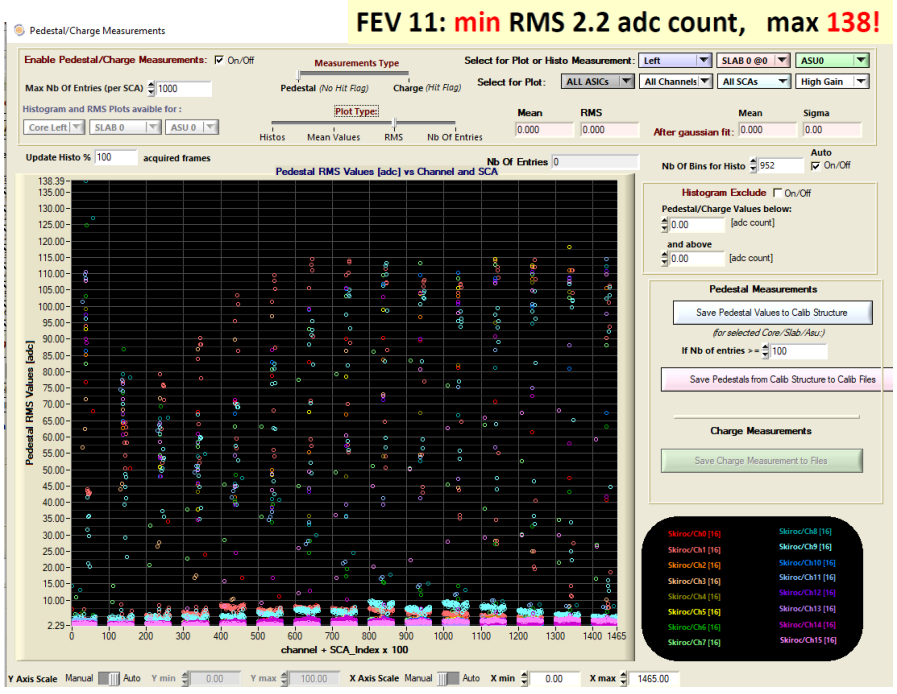
Preliminary results

Pedestal width measurements: RMS values (adc count)

FEV 2.0: Mean RMS 2.2 adc count, max 5.8



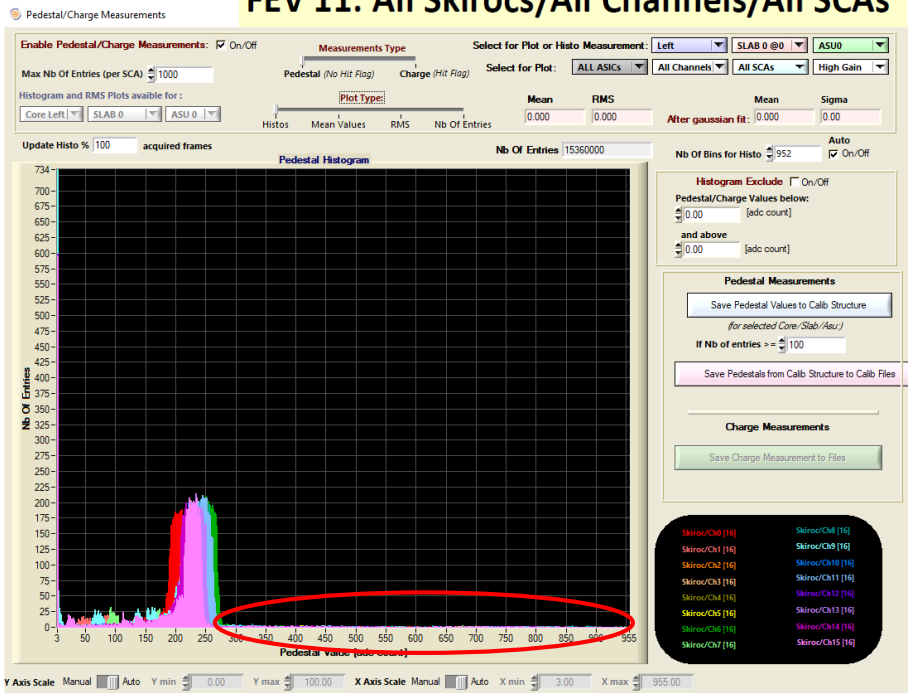
FEV 11: min RMS 2.2 adc count, max 138!



Preliminary results

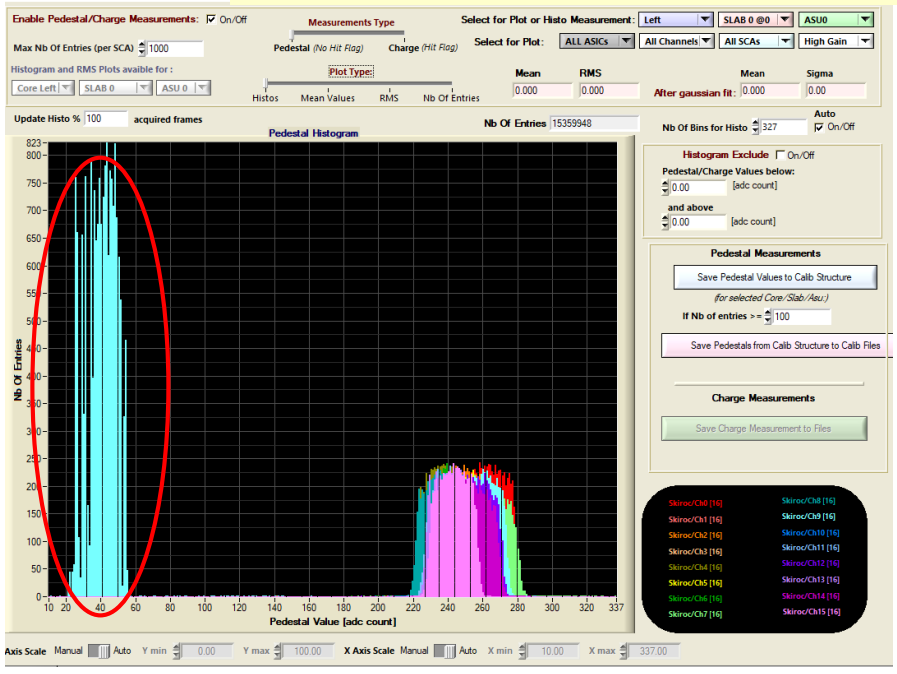
Hit vs threshold

FEV 11: All Skirocs/All Channels/All SCAs



Noise on every channel

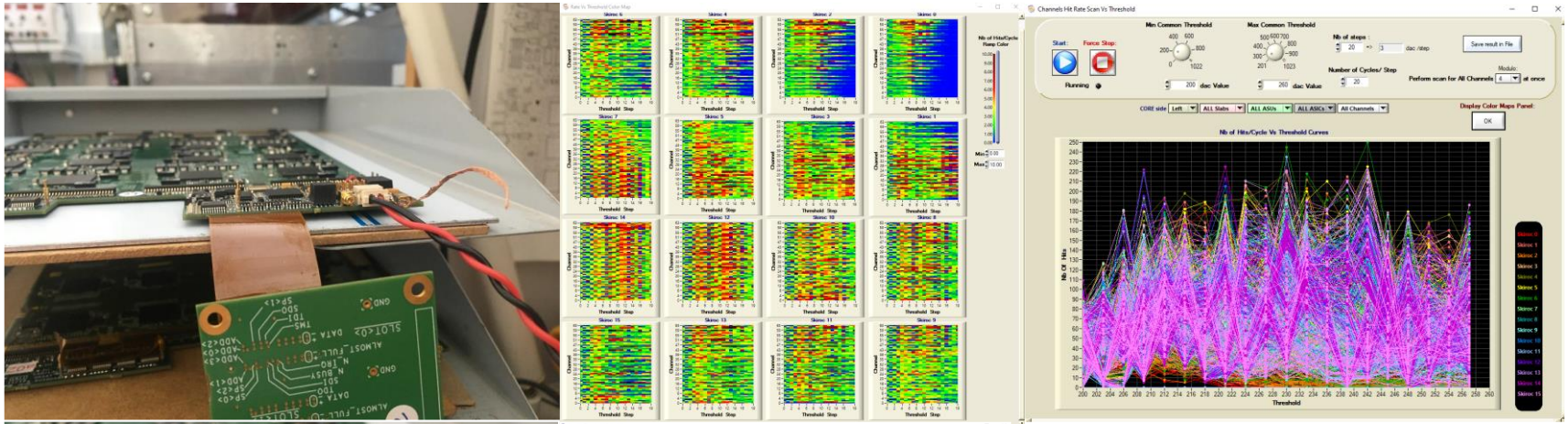
FEV 2.0: All Skirocs/All Channels/All SCAs



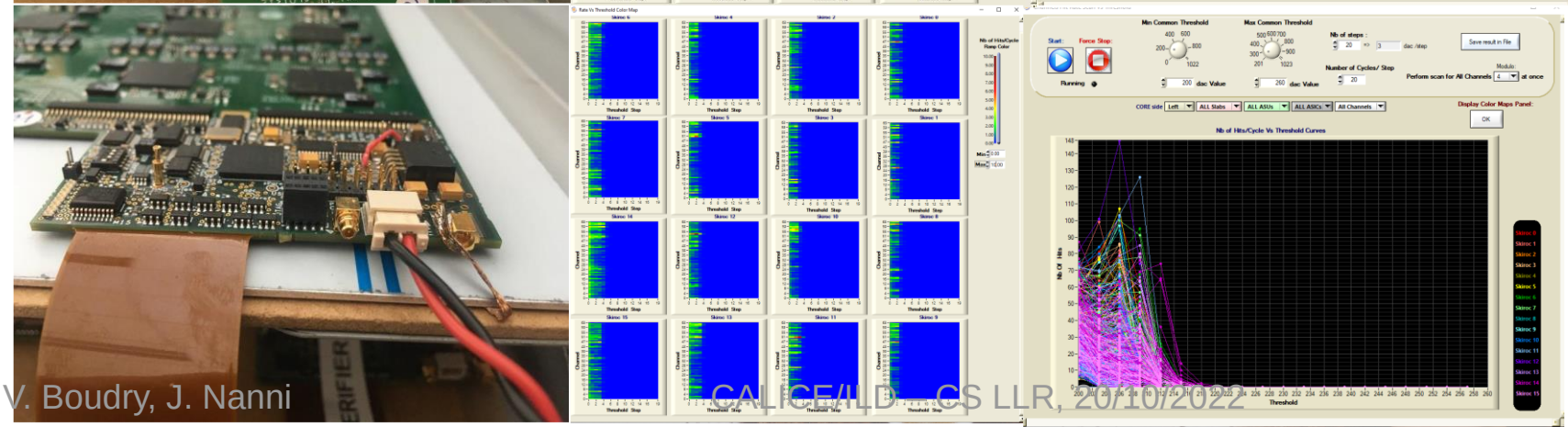
Good results except on channel 9 of SK6

Threshold scans and effect of shielding

Threshold scan between **200** and **250** with 20 steps (**3 adc count/step**)



Without shielding



With shielding

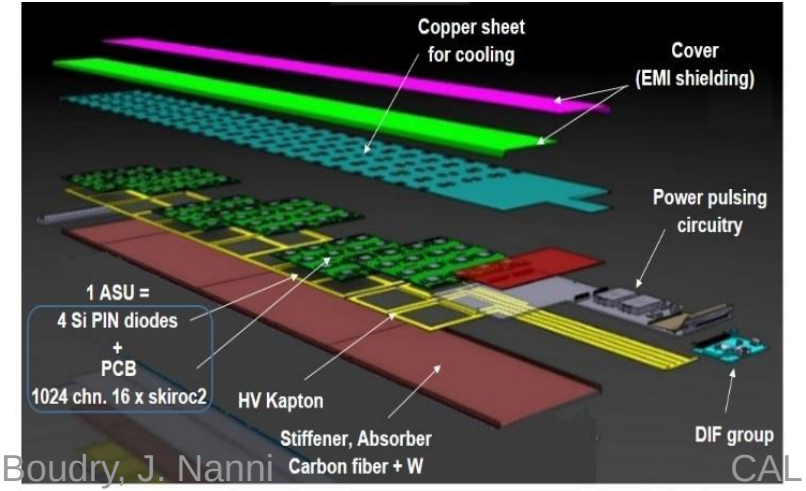
New HV kapton

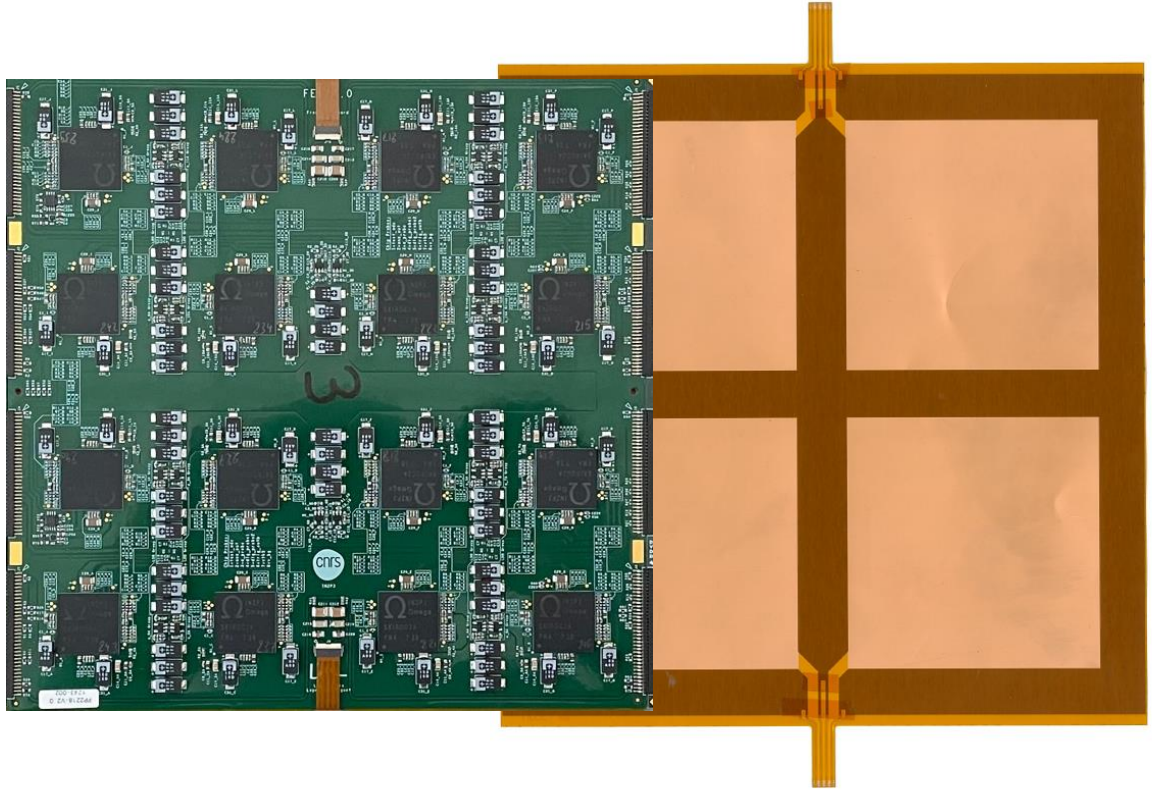
Higher reliability

- Easy to handle ASU
- Only 1 board glued per kapton

Protection of wafer for U insertion

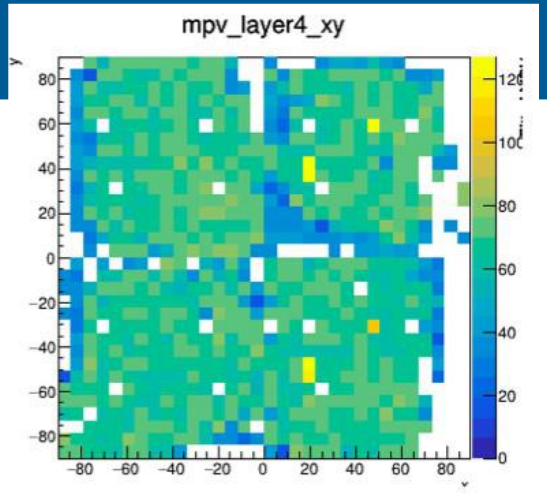
Easy to chain board for LONG slab

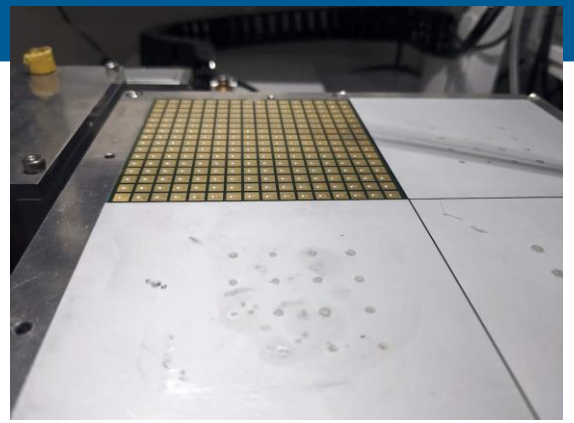




Designed by R. Guillaumat & T. Dos Santos & J. Nanni

Delamination of ASU





Since 2018, we observed problem of delamination

PCB bending ?

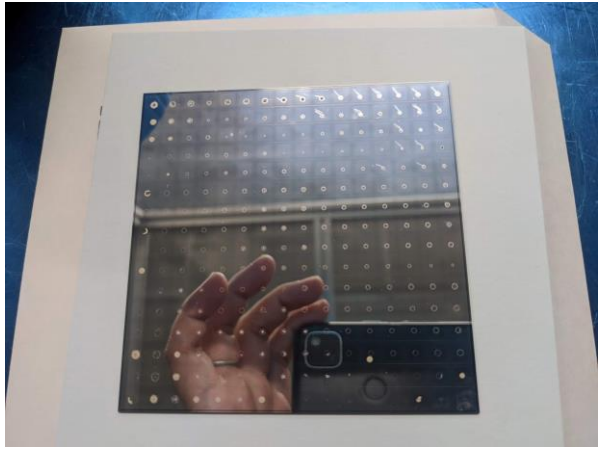
- Deformation of PCB
- Carry out fake cabling with existing material
- Metrology at each step

Surface issues ?

- Handling, intensive tests, degradation of pad surface
- Will inquire with glue producers
- Try to produce fake sensor with Al or Au coating

Quality of glue ?

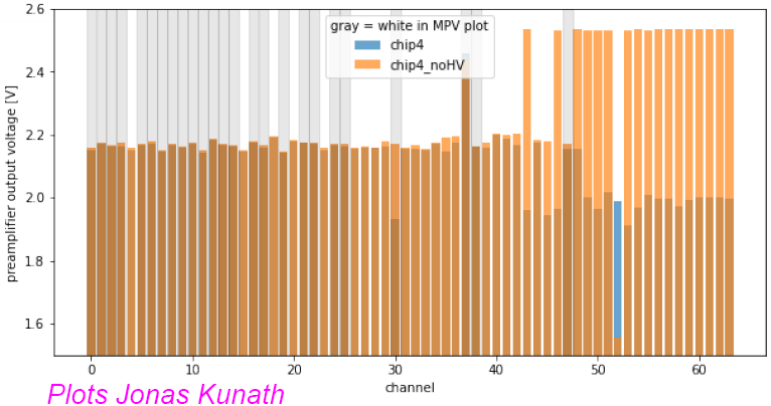
- Glue is 2 components material, mixture is correct ?
- Always use small quantity …
- Did the glue perish over the year



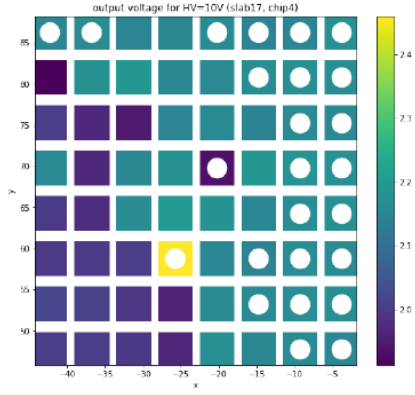
Debugging with SK2A

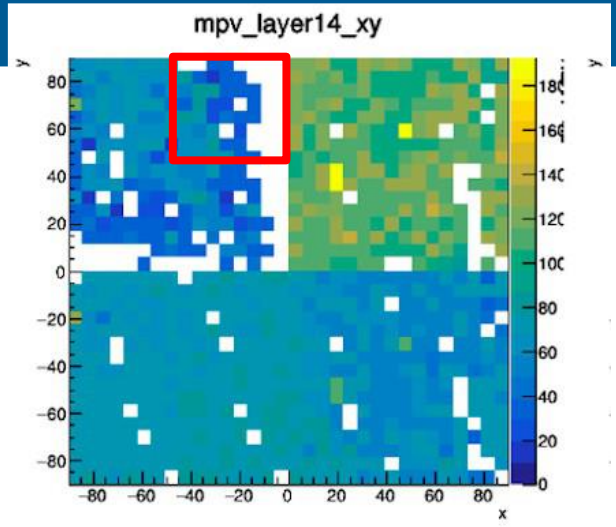
Analog probe: slow control parameter

- Allow for reading DC preamplifier output voltage
- System already implemented in DAQ
- Measure voltage change if Si connected or not polarised



Plots Jonas Kunath





Need 1024 configuration to test all pads

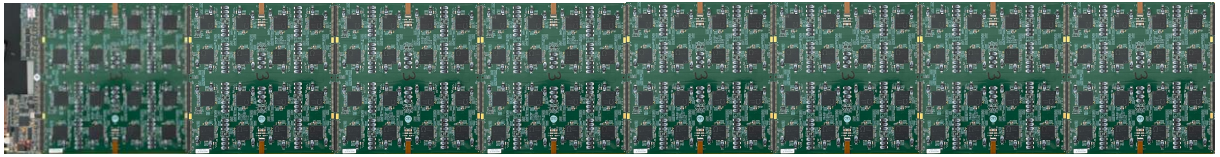
Clearly spotted non connected Si pad

Very useful tool to debug gluing

LONG Slab assembly

Launch production before end of 2022:

- FEV2.1 + supply components
- HV kapton



Make metrology after each step (production, cabling, gluing)

Understand problem of gluing with partners

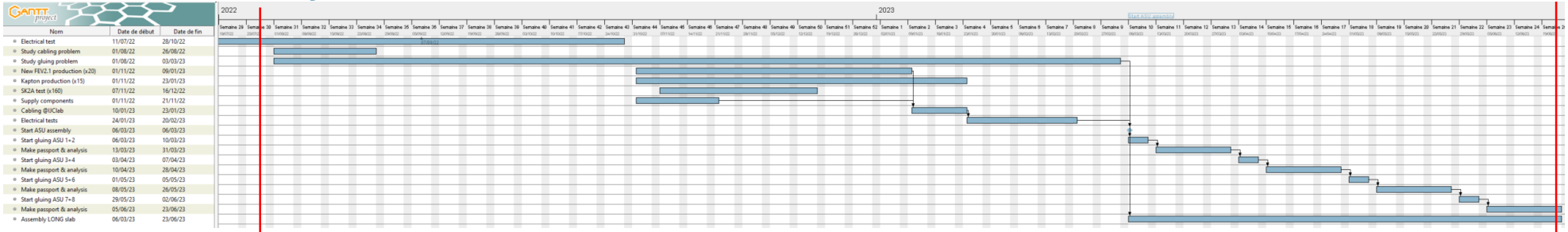
Assembly ASU one by one

Dead line: TB in November 2023

Mechanic structure recycled from previous one

Designed by E. Edy

30/06/2023



Technical conclusions

- **New FEV2.0 give very promising results**
  - Good news for LONG slab
- **Single ASUs (with FEV13) fully functional with very good S/N ratio**
  - High energy response to be validated
- **Unique expertise on design and integration**
- **Reflexion for Higgs factory with our expertise on frontend**
  - Need a new version of ASIC
    - with new technology (TSMC)
    - Zero-suppression ?
    - Specification to Higgs factory (need physics simulations)