CALICE Si ECAL

Description du Demonstrateur
Campagnes de tests et résultats/performances démontrées

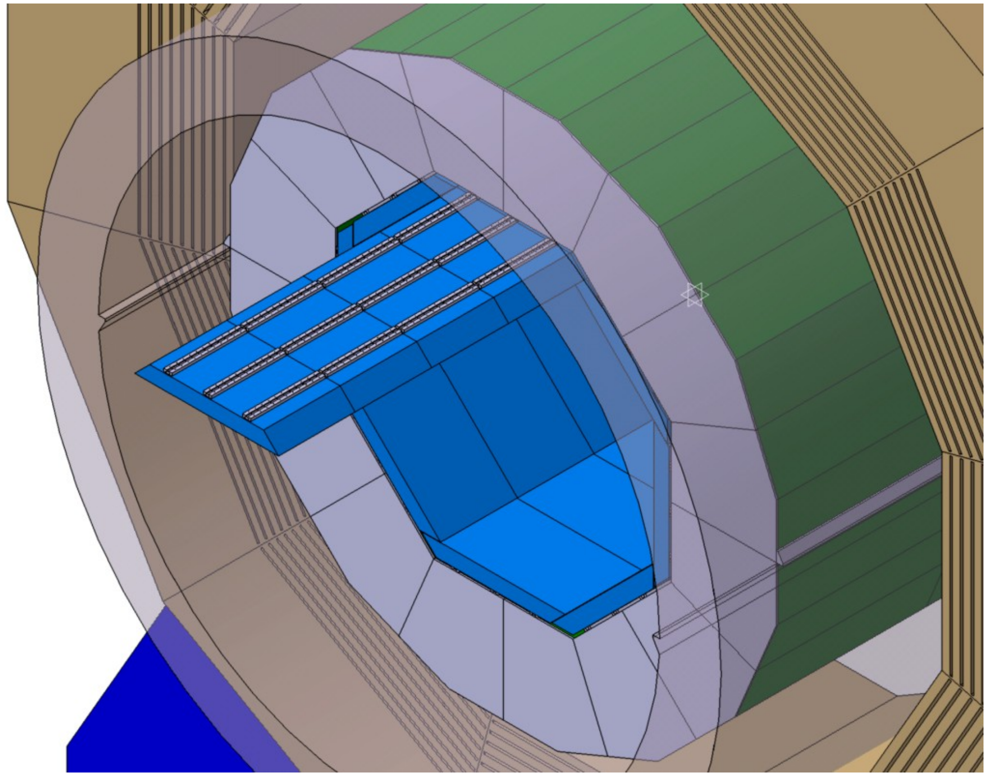
Roman Pöschl

The work presented here has received funding from:

Revue IN2P3 – September 2022

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- O(108) cells
- “No space”
=> Large integration effort

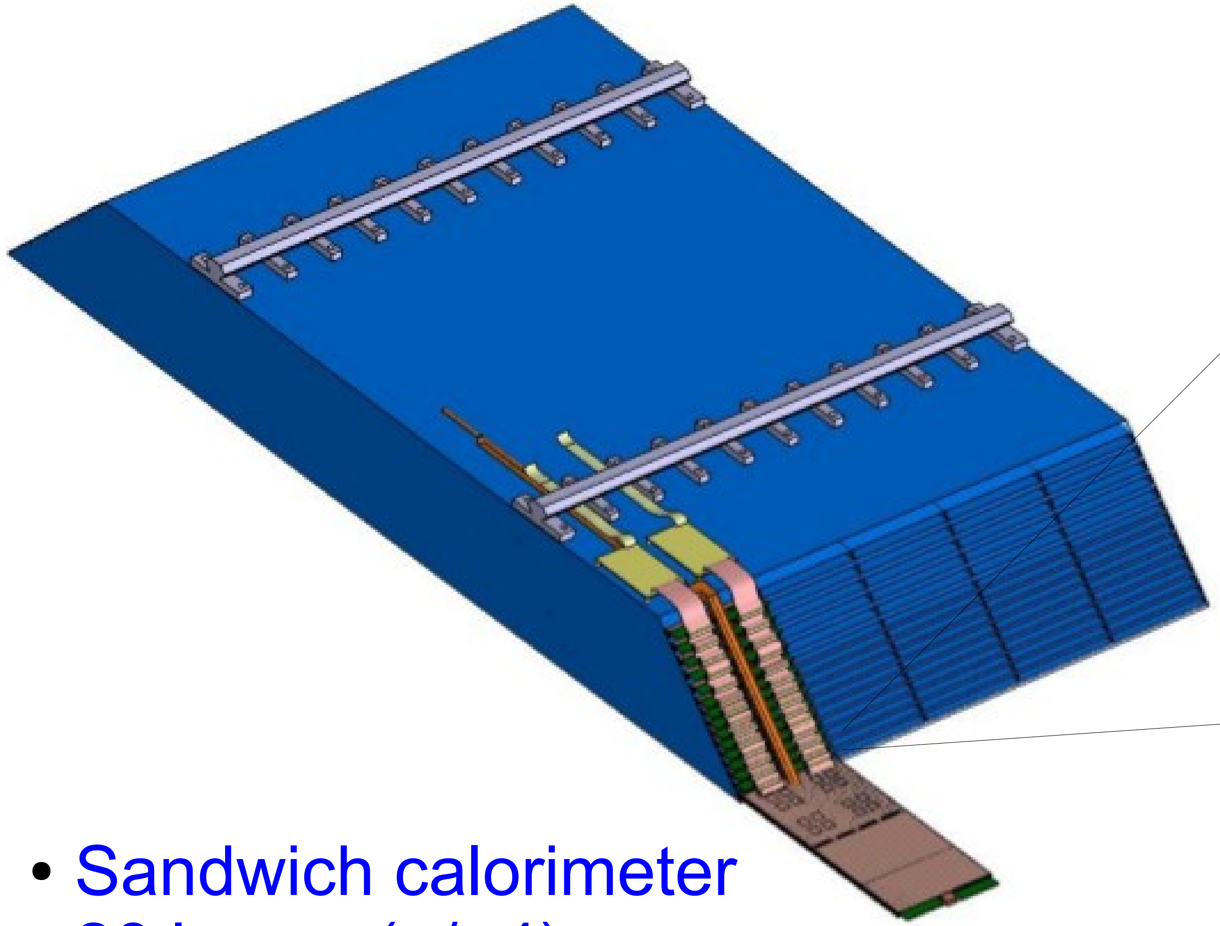
Basic Requirements:
- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

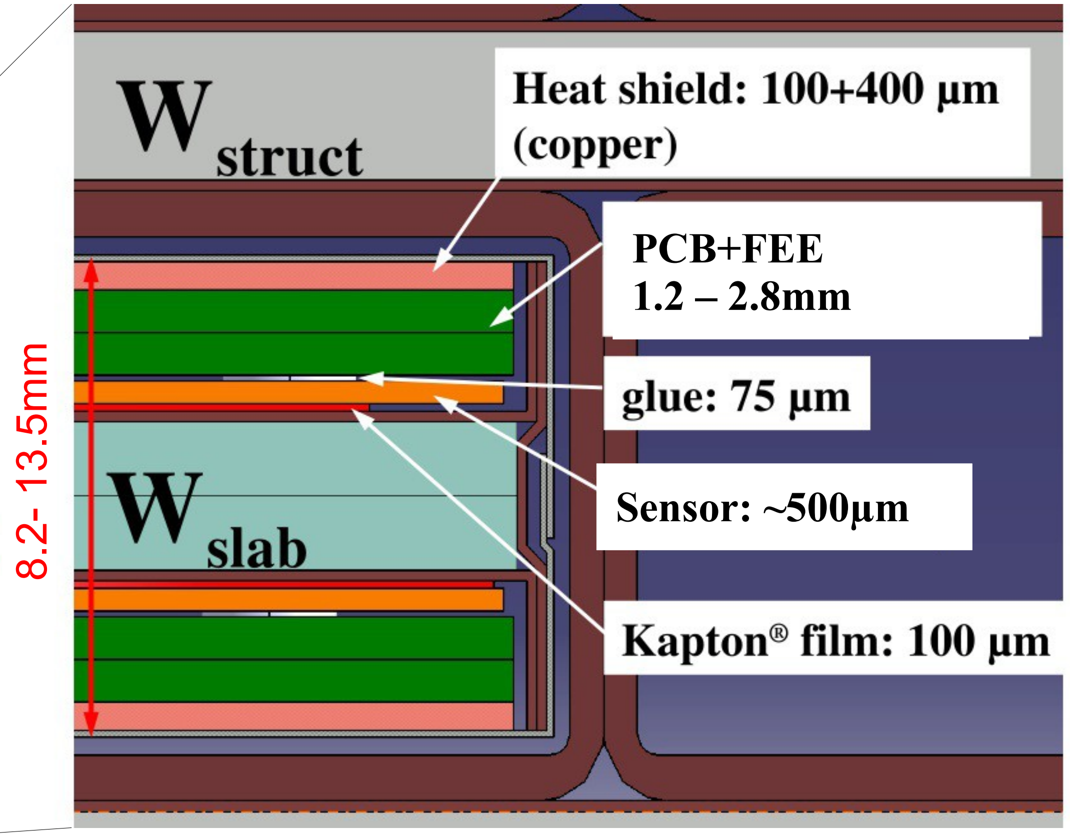
Basic Choices:
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 as design value

- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

Silicon Tungsten electromagnetic calorimeter – Example ILD

Ecal alveolar structure



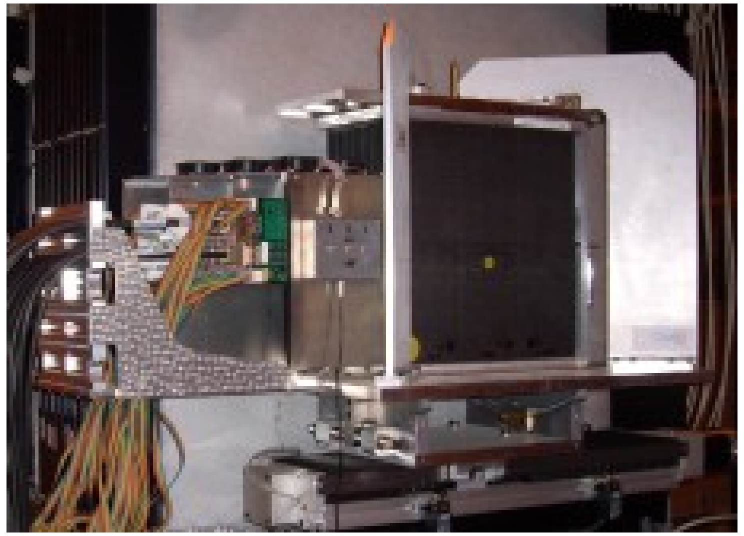


- Sandwich calorimeter
- 26 layers (+/- 4)
- Thickness: ~20cm, 24 $X_0/1\lambda_I$
- Pixel size ~5x5 mm^2
- Expected elm. energy resolution 15-20%/√E

Steps of R&D

Physics Prototype

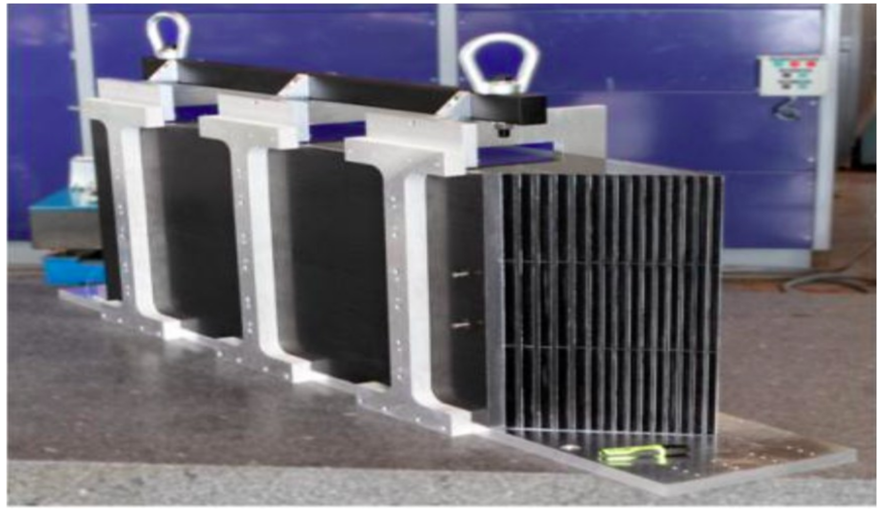
2005 - 2011



- Proof of principle of granular calorimeters
- Large scale combined beam tests

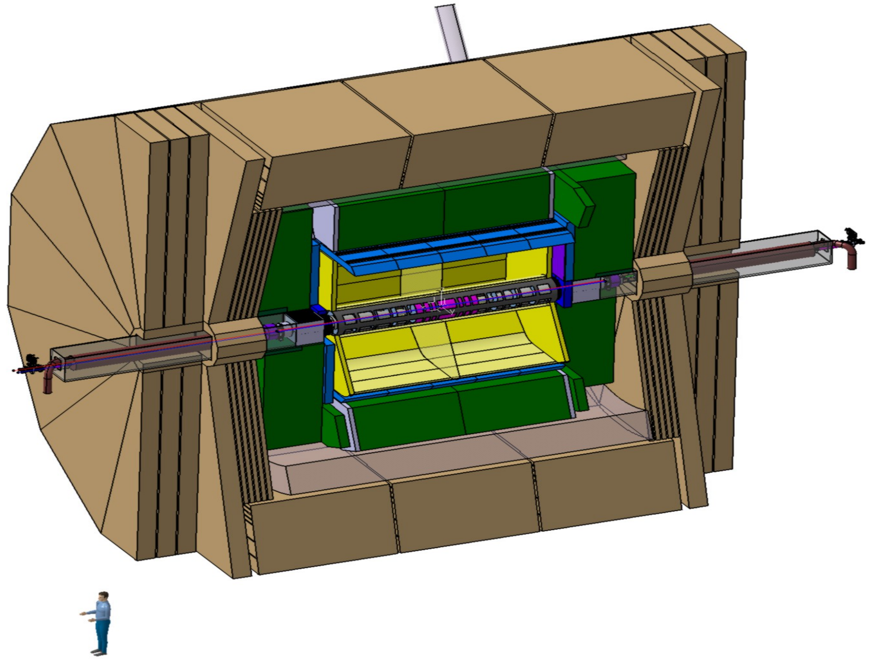
Technological Prototype

2010 - ...



- Engineering challenges
- Higher granularity
- Lower noise

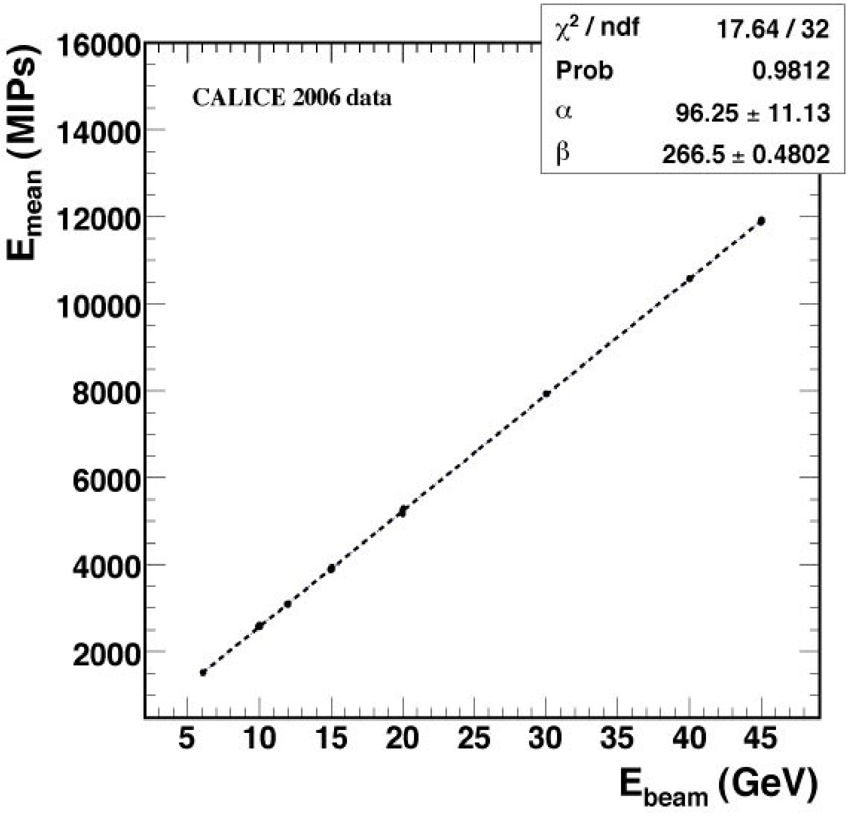
LC detector



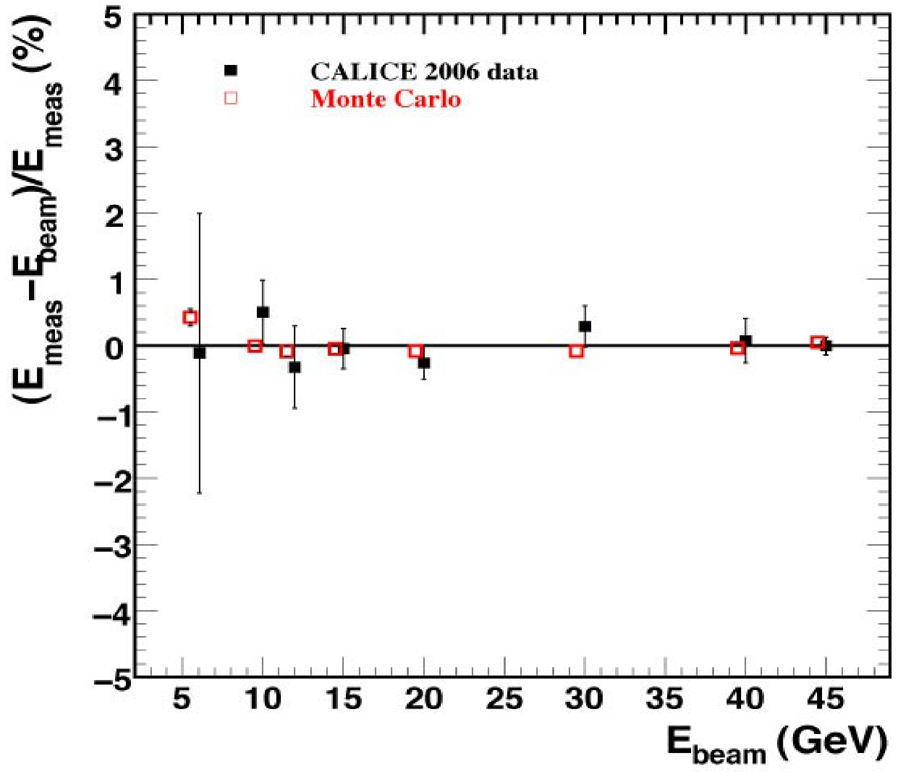
- The goal
  - Typically 10^8 calorimeter cells
- Compare:
  - ATLAS LAr ~10^5 cells
  - CMS HGCAL ~10^7 cells

Physics Prototype – Response to Electrons

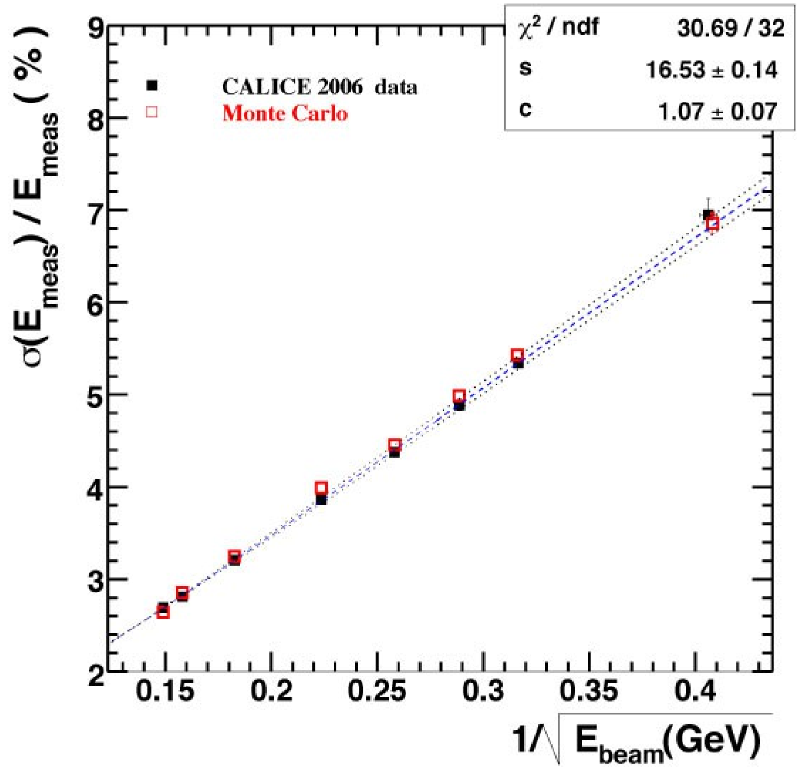
Linearity - Overview



Linearity - Residuals



Energy resolution



- Highly linear response over large energy range

- Linearity well reproduced by MC
  MIP/GeV ~ 266.5 [1/GeV]

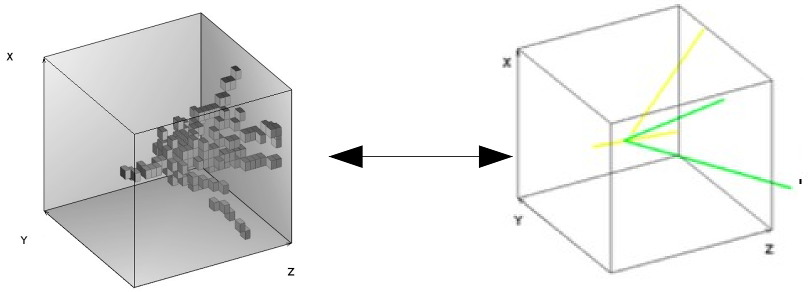
- Non-Linearity O(1%)

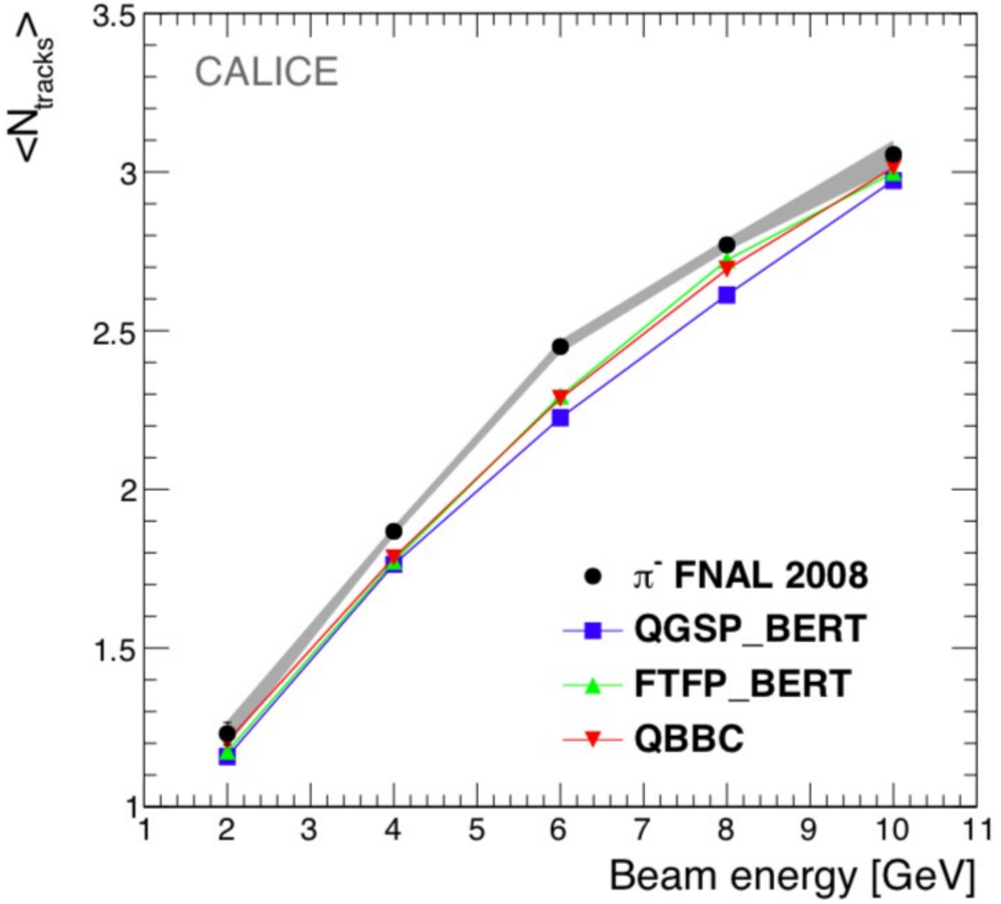
Resolution curve shows typical √E dependency

$$\frac{\Delta E_{meas.}}{E_{meas.}} = \left[\frac{16.6 \pm 0.1 (stat.)}{\sqrt{E\,[\mathrm{GeV}]}} \oplus (1.1 \pm 0.1) \right] \%$$

C. Carloganu et al.
NIM A608 (2009) 372; e-print: arXiv:0811.2354

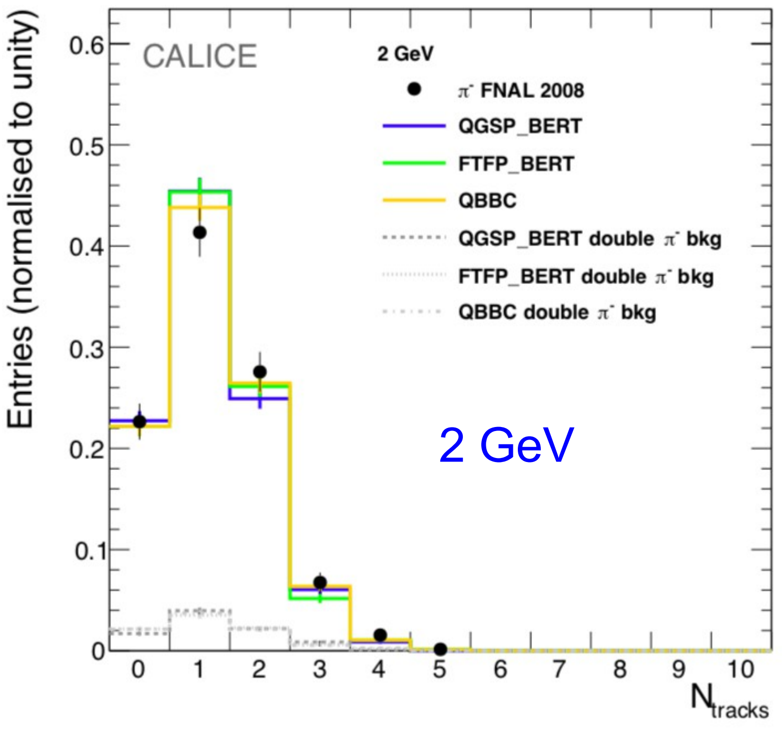
Physics Prototype – Secondary Tracks in Si ECAL

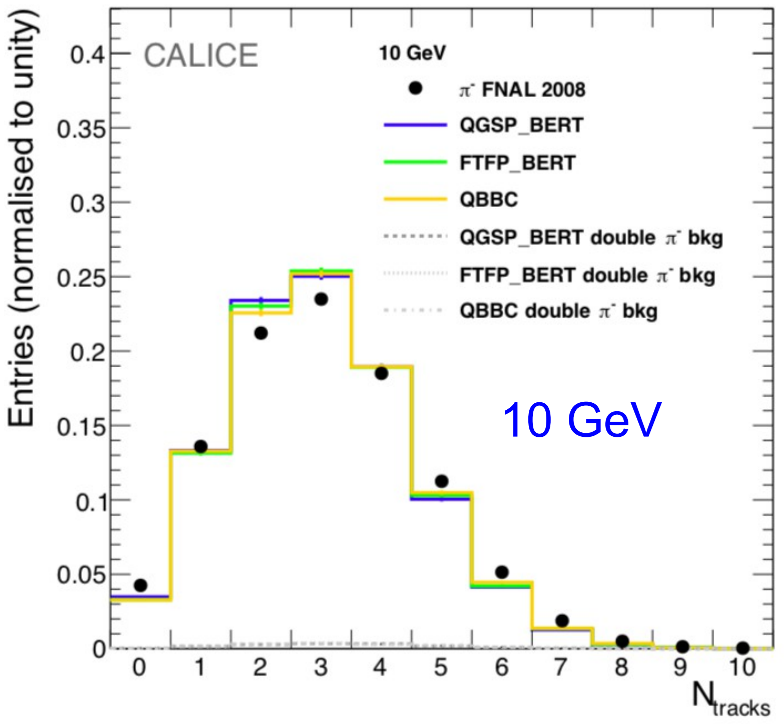




PhD Thesis, S. Bilokin (LAL)
TYL-FJPPL Young Investigator Award
NIM A937 (2019) 41-52; e-print: arXiv:1902.06161

PhD Theses P. Doublet, (LAL,) H. Li (LAL)
P2IO PD N. v.d. Kolk (LLR/LAL)
NIM A794 (2015) 240-254; e-print: arXiv:1411.7215

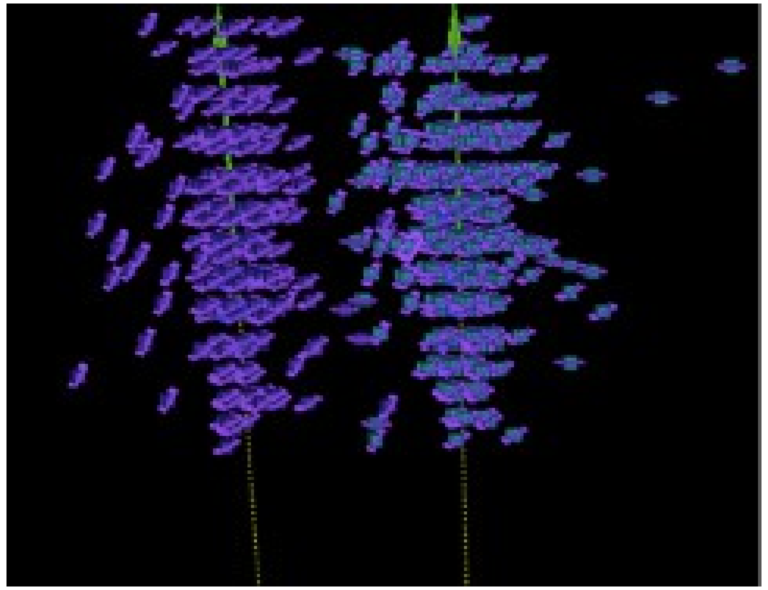




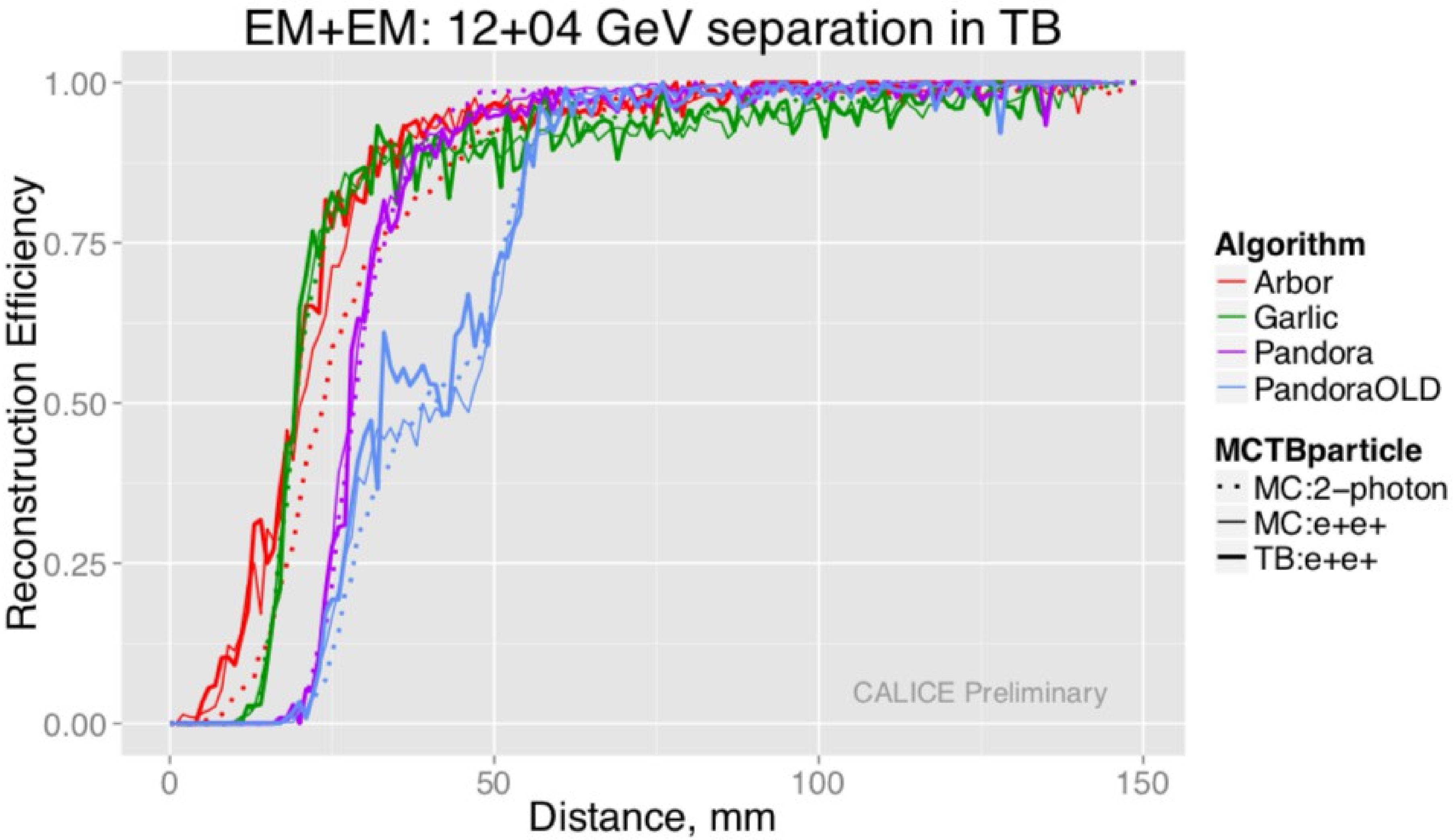
- Mean number of secondary tracks increases with beam energy as expected from fixed target kinematics for π--tungsten scattering
- Good reproduction of data by simulation with GEANT4
- Study motivated inclusion of CALICE Si ECAL into G4 Validation Chain

Physics Prototype – Particle Separation

Photon-pion: Separation using beam test data



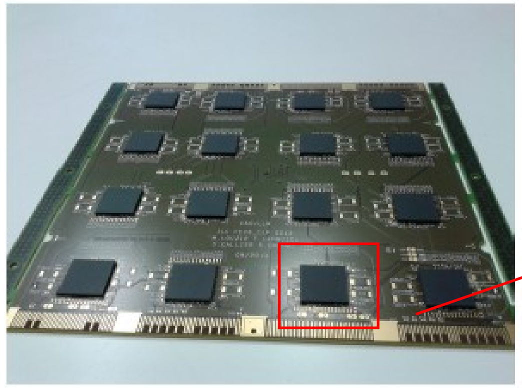
PhD Thesis K. Shpak (LLR)
CALICE-CAN-2017-001



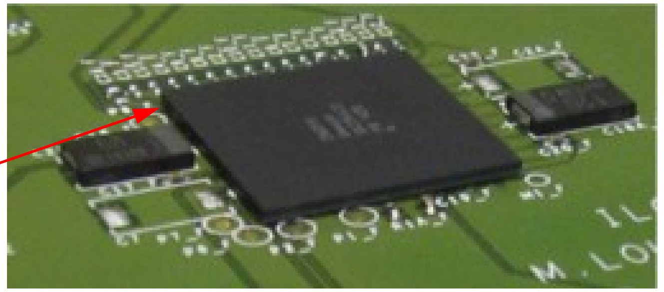
- Test of particle separation using different particle flow algorithms
  - ARBOR, GARLIC developed by in2p3 (LLR, IPNL)
- Full separation power at around 30mm

SiW Ecal Technological prototype – Elements of (long) layer

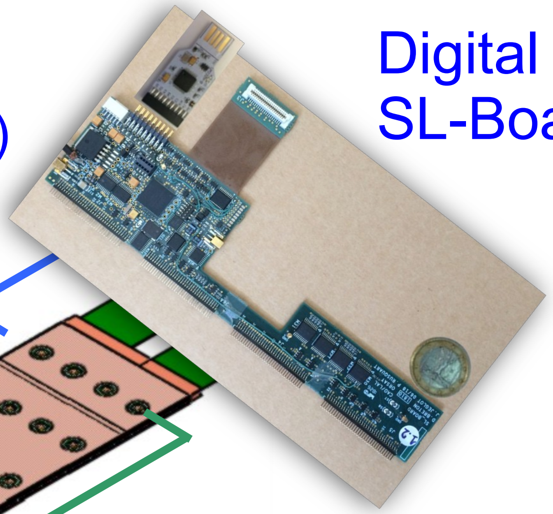
ASIC+PCB+SiWafer
=ASU
Size 18x18 cm^2
(IJCLab, Kyushu, OMEGA, LLR, SKKU)



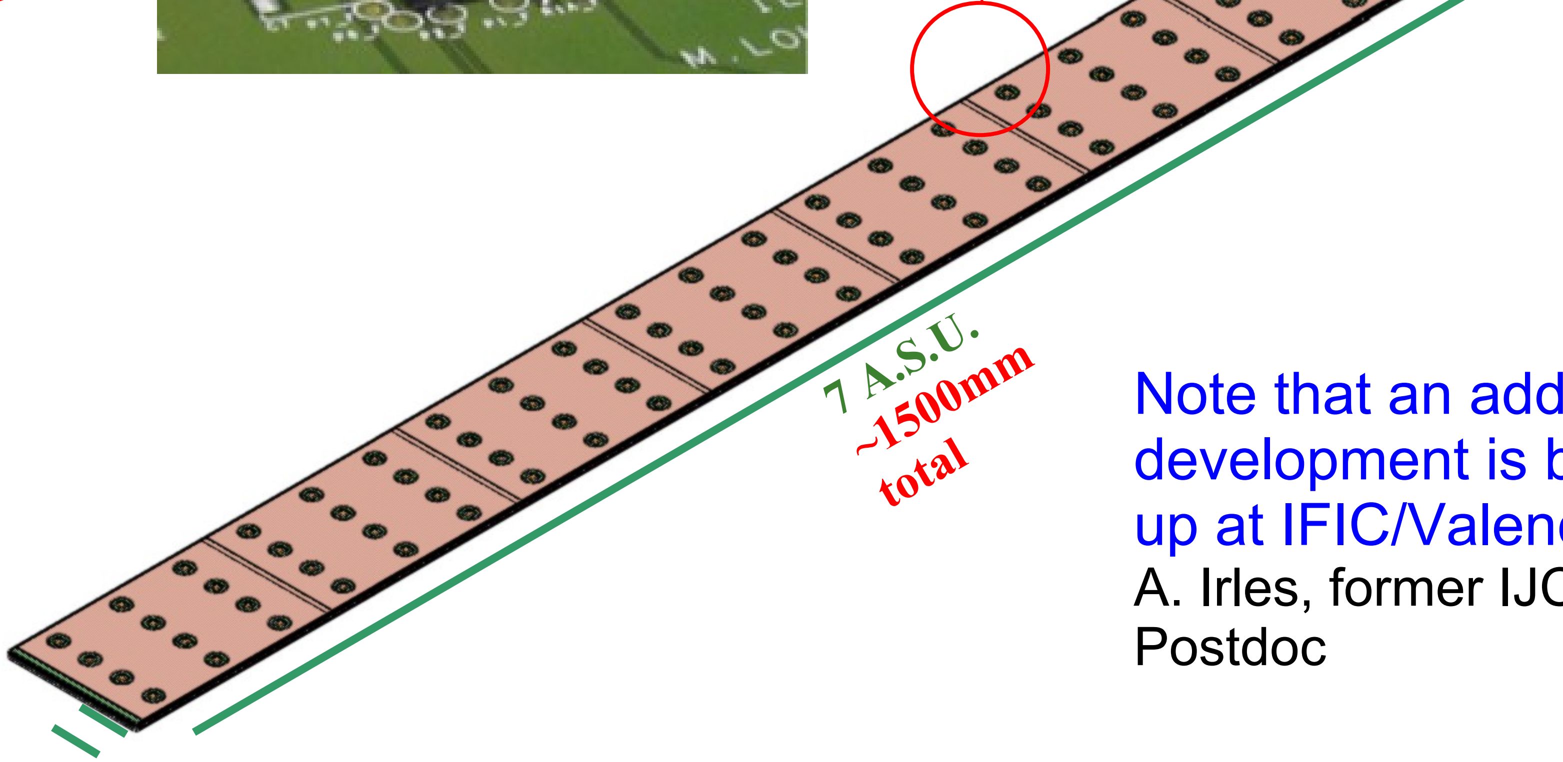
ASIC SKIROC2(a)
(OMEGA)
Wire Bonded or
In BGA package
(IJCLab, Kyushu, LLR)



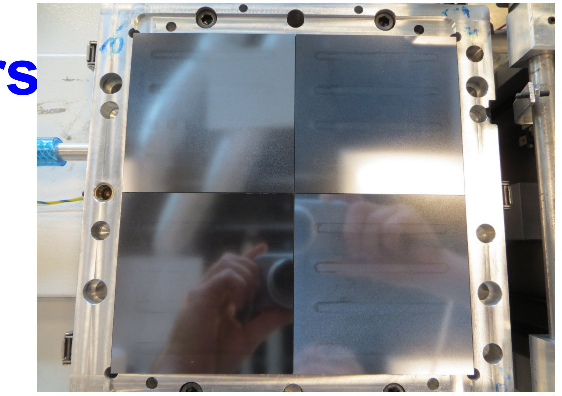
Interconnection
(IJCLab)
HV Supply
(IJCLab, LLR)



Digital readout
SL-Board (IJCLab)



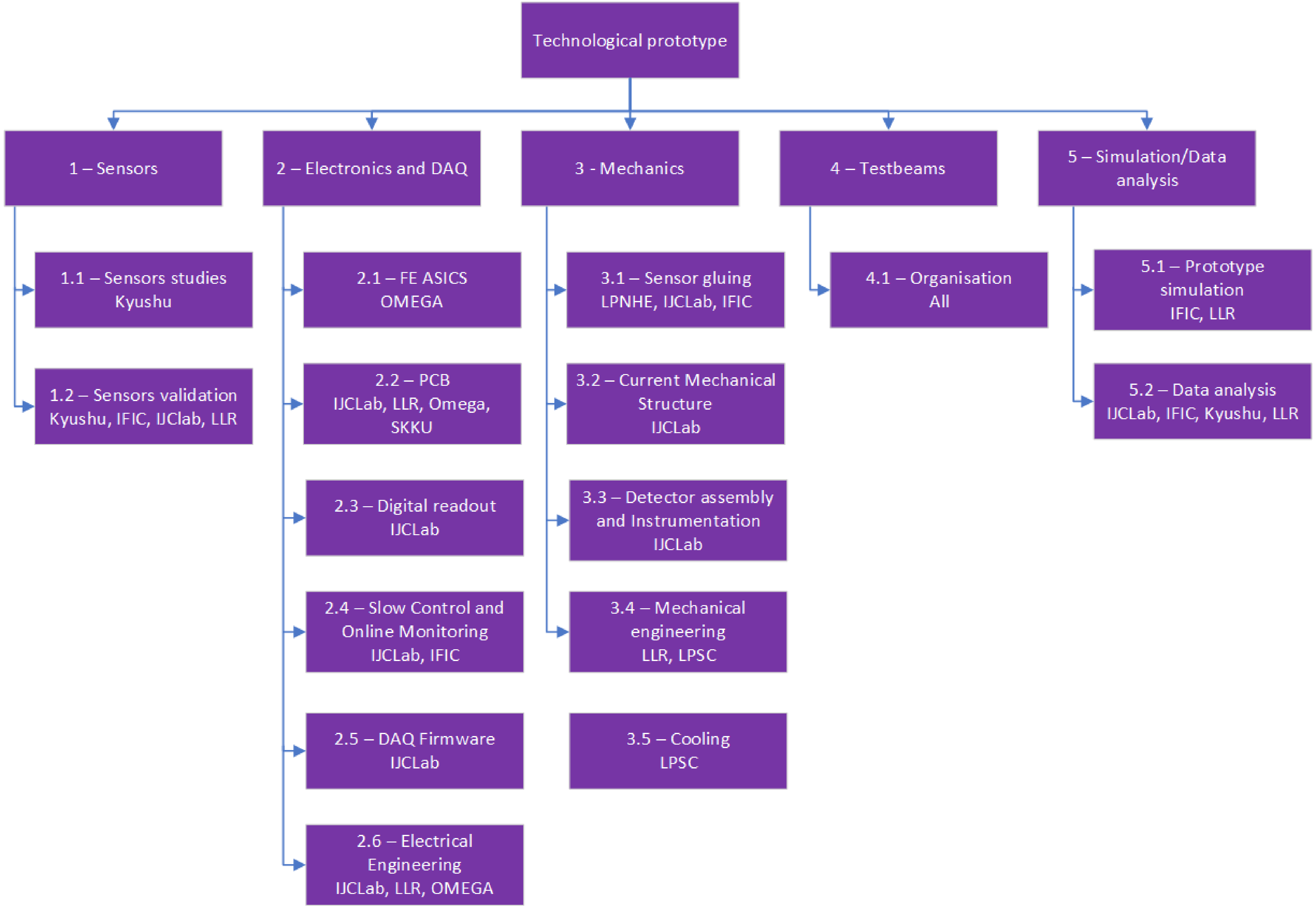
Si Sensors
glued
onto PCB
Pixel size
5.5x5.5 mm^2
(LPNHE)



Note that an additional hub for hardware development is being set up at IFIC/Valencia
A. Irles, former IJCLAb/LAL (P2IO HIGHTEC) Postdoc

- The beam test set ups comprised mainly **short layers** consisting of one ASU and a readout card each

SiW Ecal Technological Prototype – Organisation



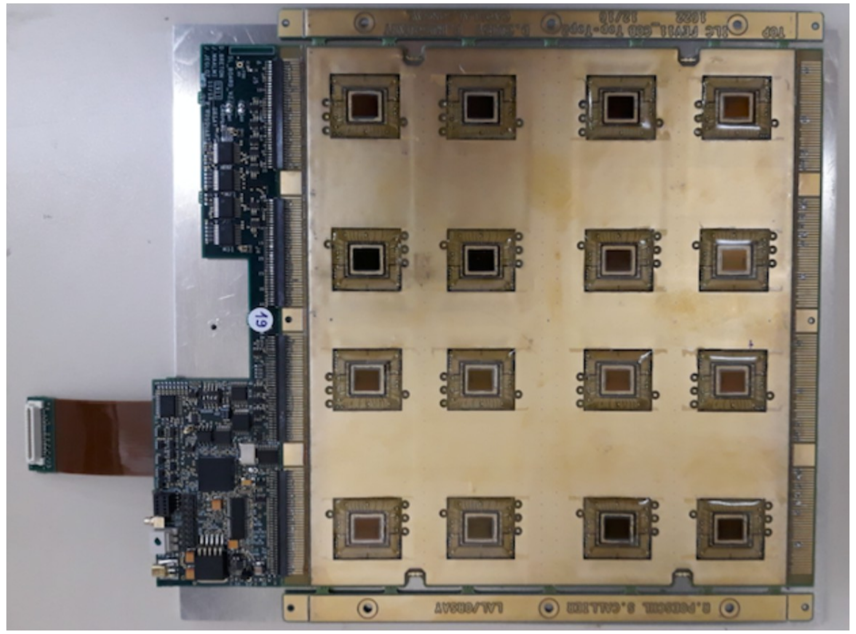
PCB Development

- Crucial (and often underestimated) detector component
  - Overview on developed variants

FEV10-12

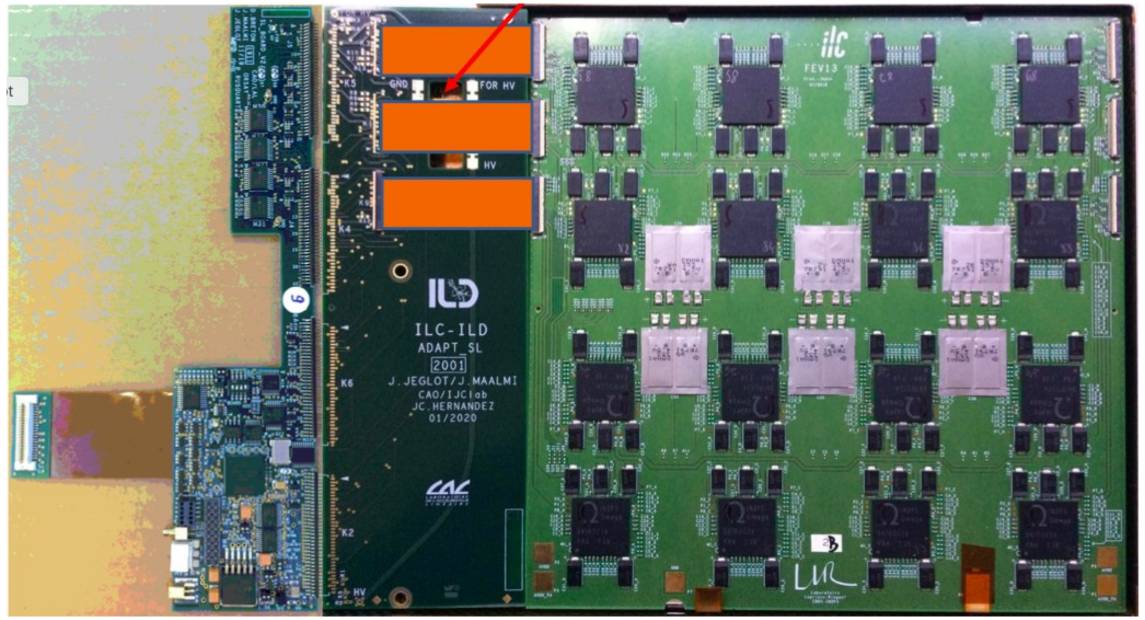
- ASICs in BGA Package
- Incremental modifications From v10 -> v12
- Main "Working horses" since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13

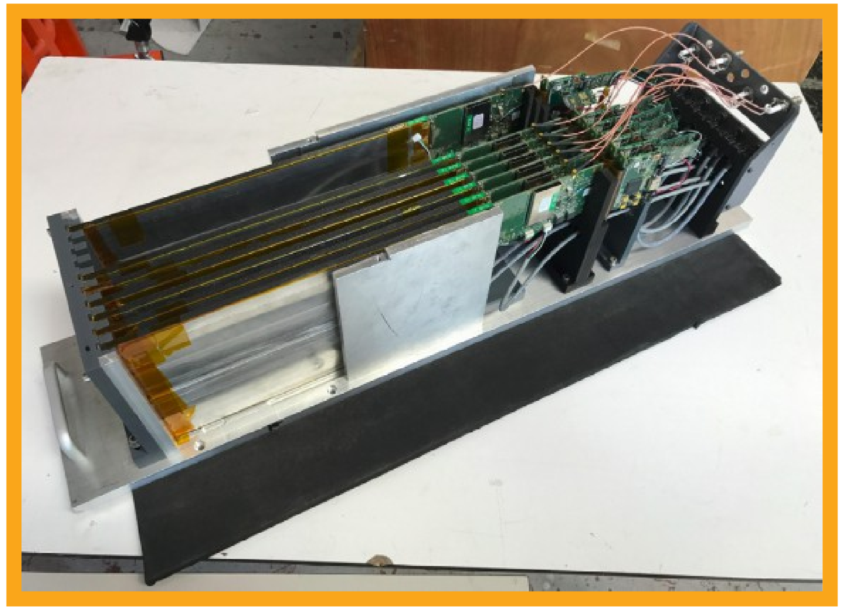


- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

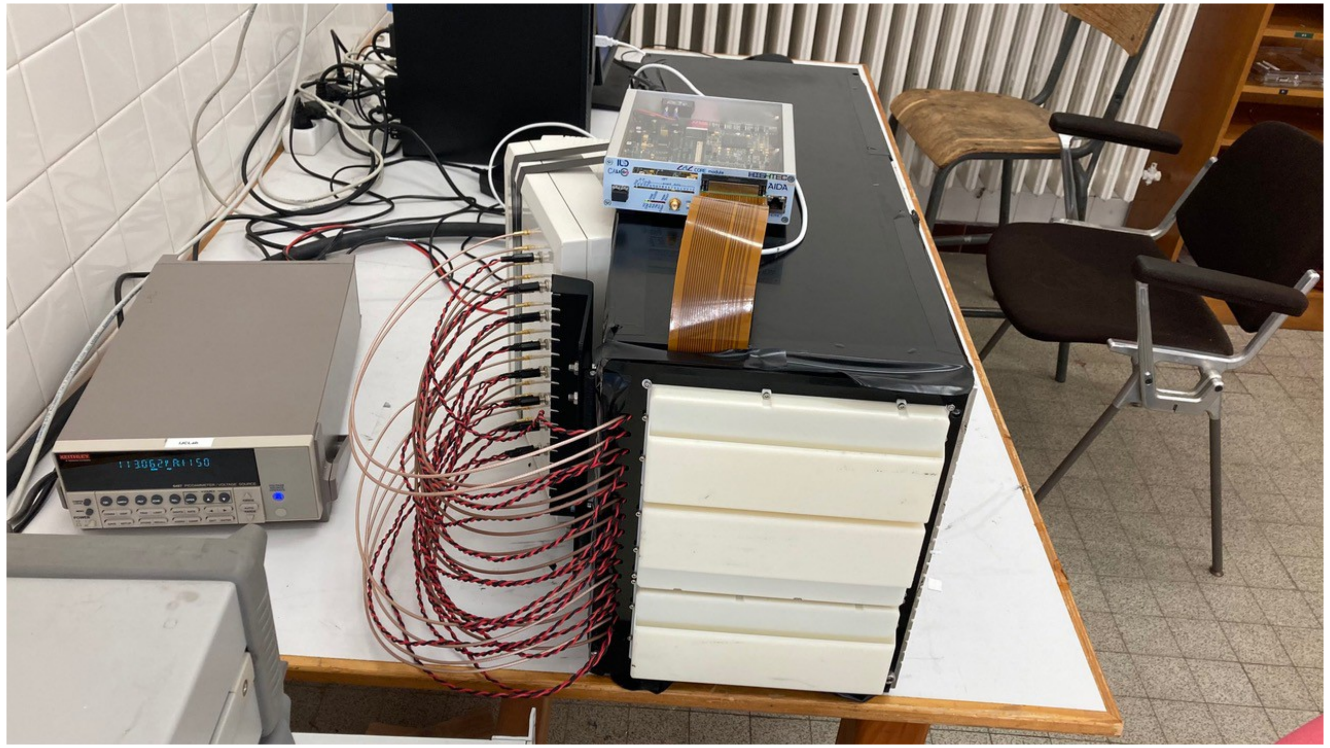
Tested prototypes were/are equipped with all of these PCBs

SiW ECAL Technological Prototype – Development phases

≤ 2018



> 2018

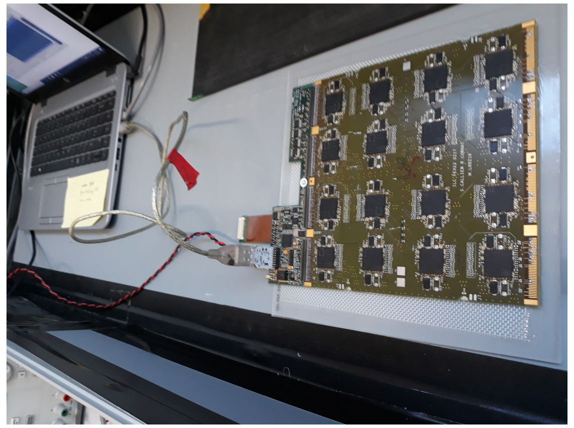


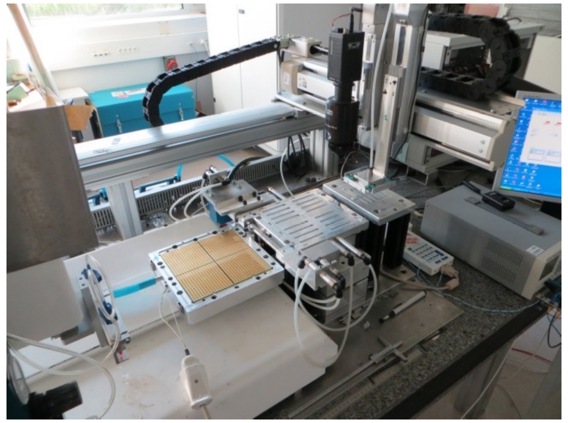
- Up to 7 short layers (18x18x0.5cm^3)
  - Up ~10 X_0
- 1024 channels per layer => 7186 cells
- Technical tests at "MIP level"

- 15 short layers equivalent to 15360 readout cells
  - Up to 21 X_0
- Overall size 640x304x246mm^3
  - Commissioned 2020-2022
  - Partially by ***recycling*** of ASUs from earliear stacks
  - Testbeams (finally) in November 2021 and during 2022

Assembly and QA Chain

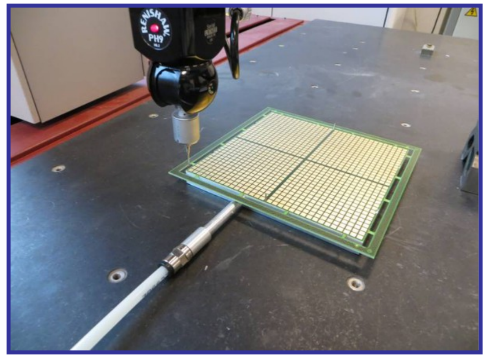
(In house) cabling and electronics tests with highly mobile DAQ system



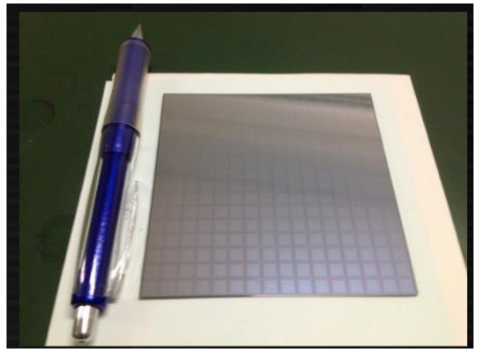


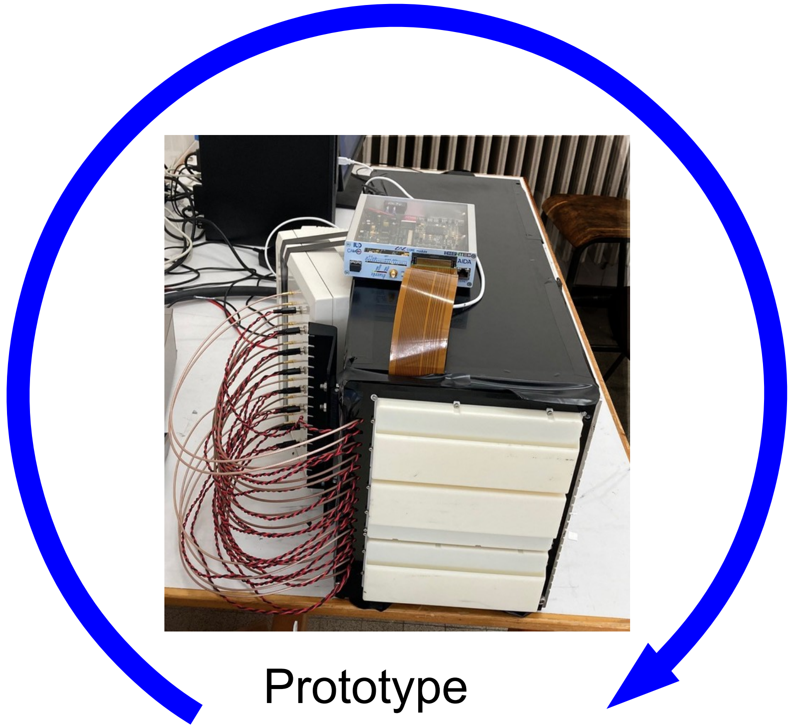
Wafer Gluing with robot

Metrology of PCBs

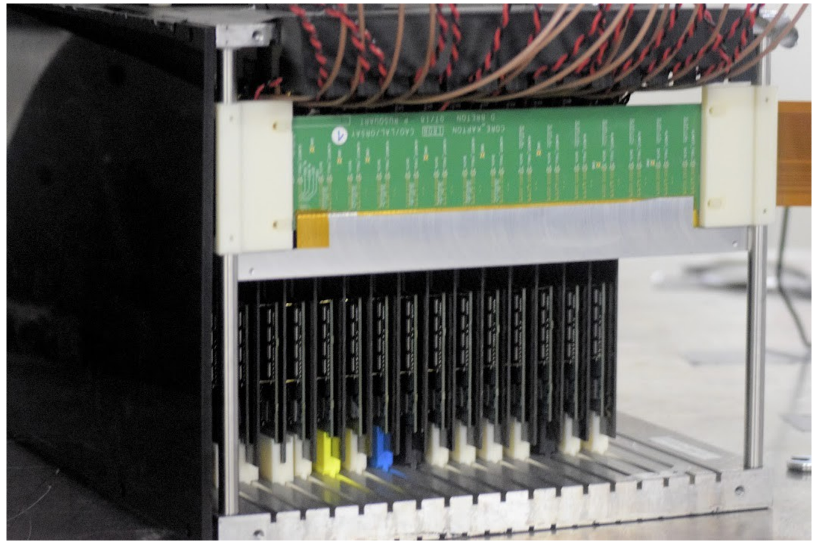


Si sensor tests





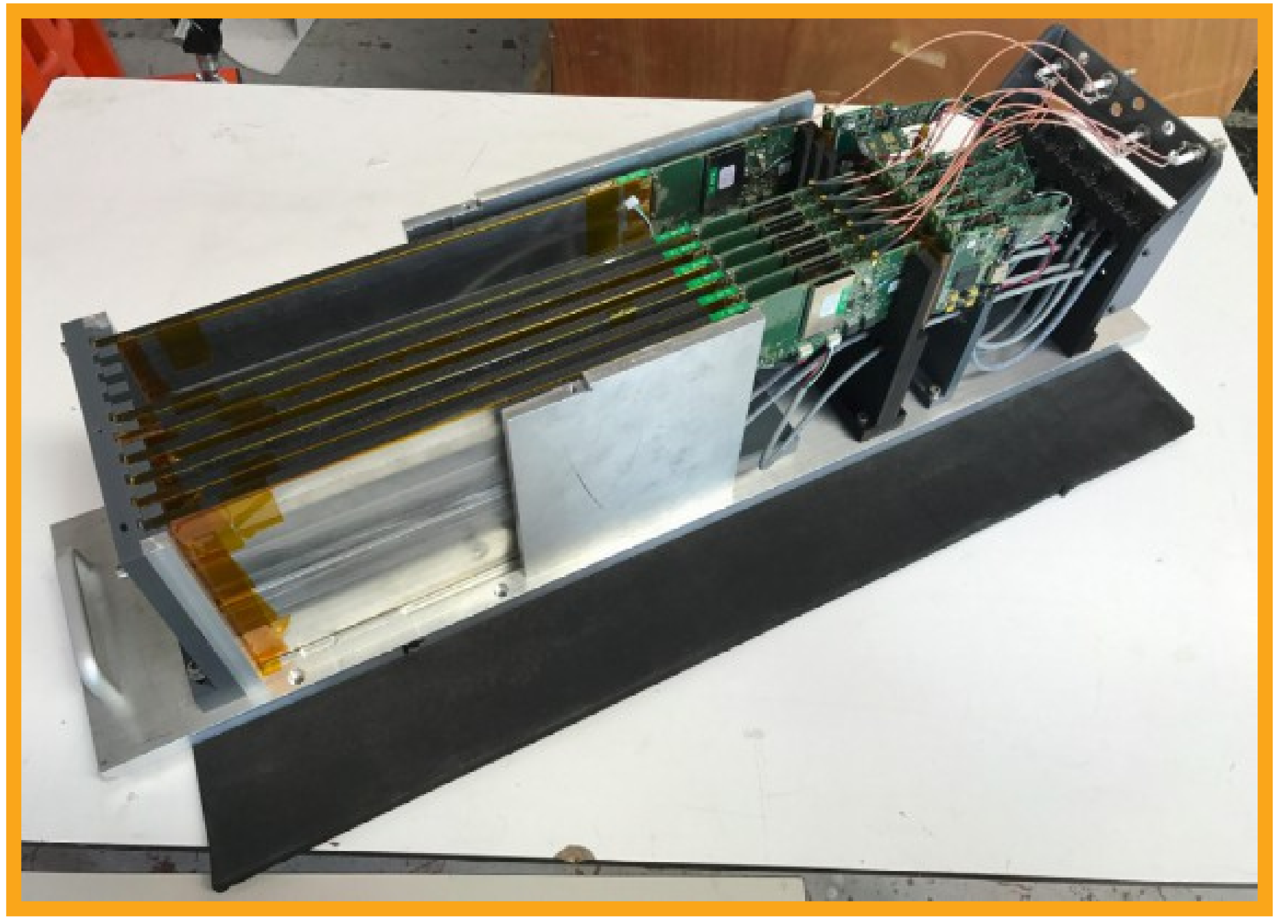
Prototype



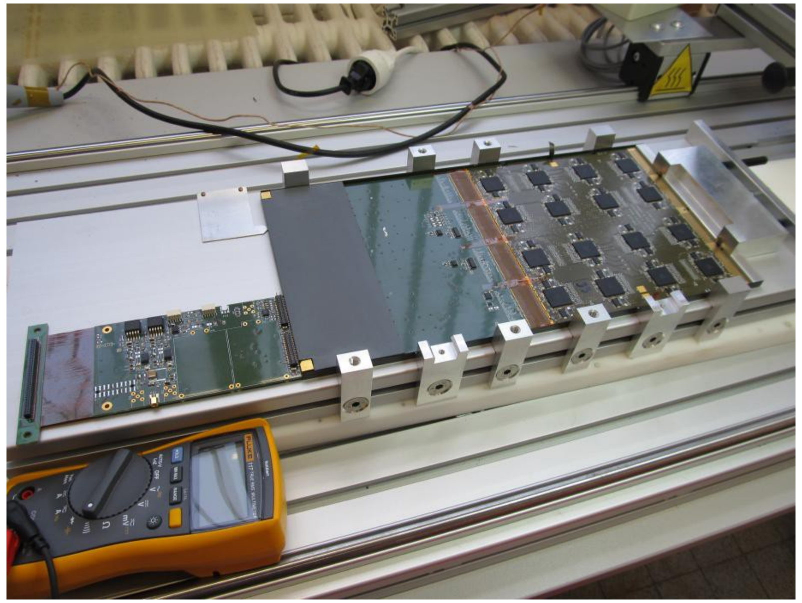
Detector assembly and commissioning

Deliverable of AIDA-2020

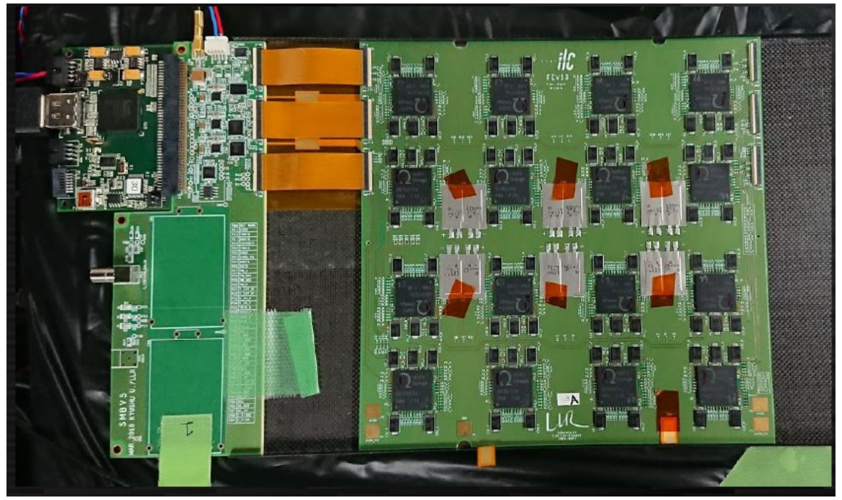
Prototypes until ~2018



- Total ~15 short layers constructed
- Main campaign 2017 with 7 layers



PCB FEV10-12
with long adapter card
Sensor thickness
325 µm



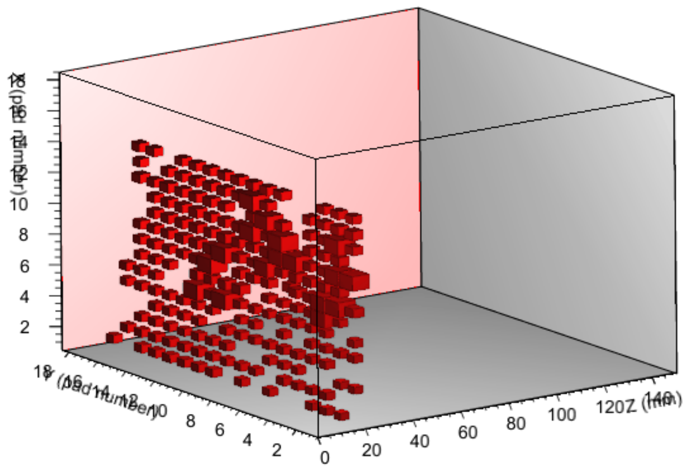
PCB FEV13
with shorter adapter card
Sensor thickness
650 µm

Test beams 2012/13

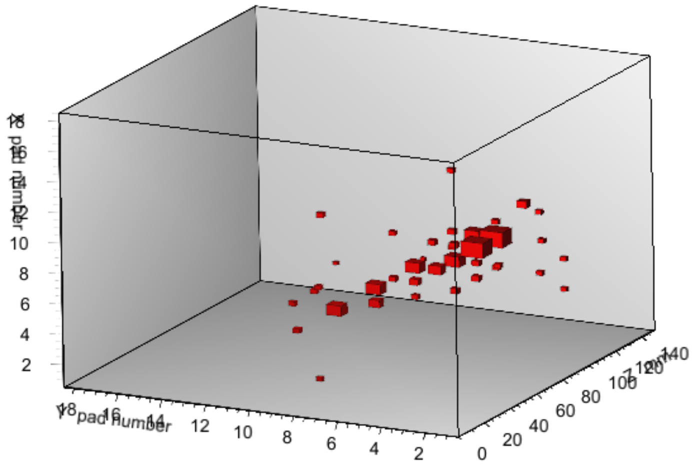
- DESY 2012 and 2013
  - Simplified ASUs (four ASICS, one sensor)
  - First thorough examination of SKIROC2 ASICs

    IN2P3 PD T. Frisson (LAL), PhD Thesis J. Rouene (LAL), Nucl.Instrum.Meth. A778 (2015) 78-84

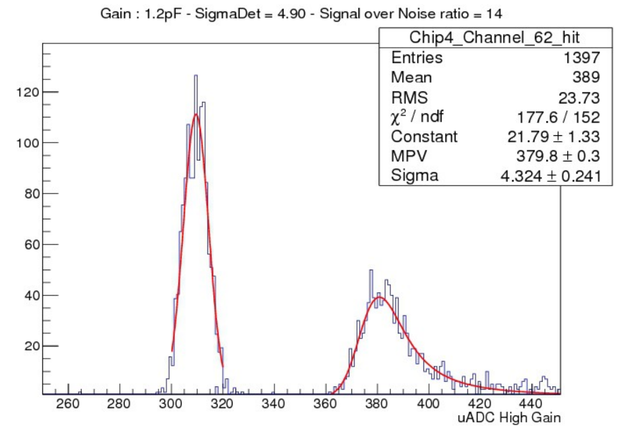
Event filtering 'Plane events???'



1 e- (5 GeV)
5 W plates between layers



Excellent Signal/Noise separation



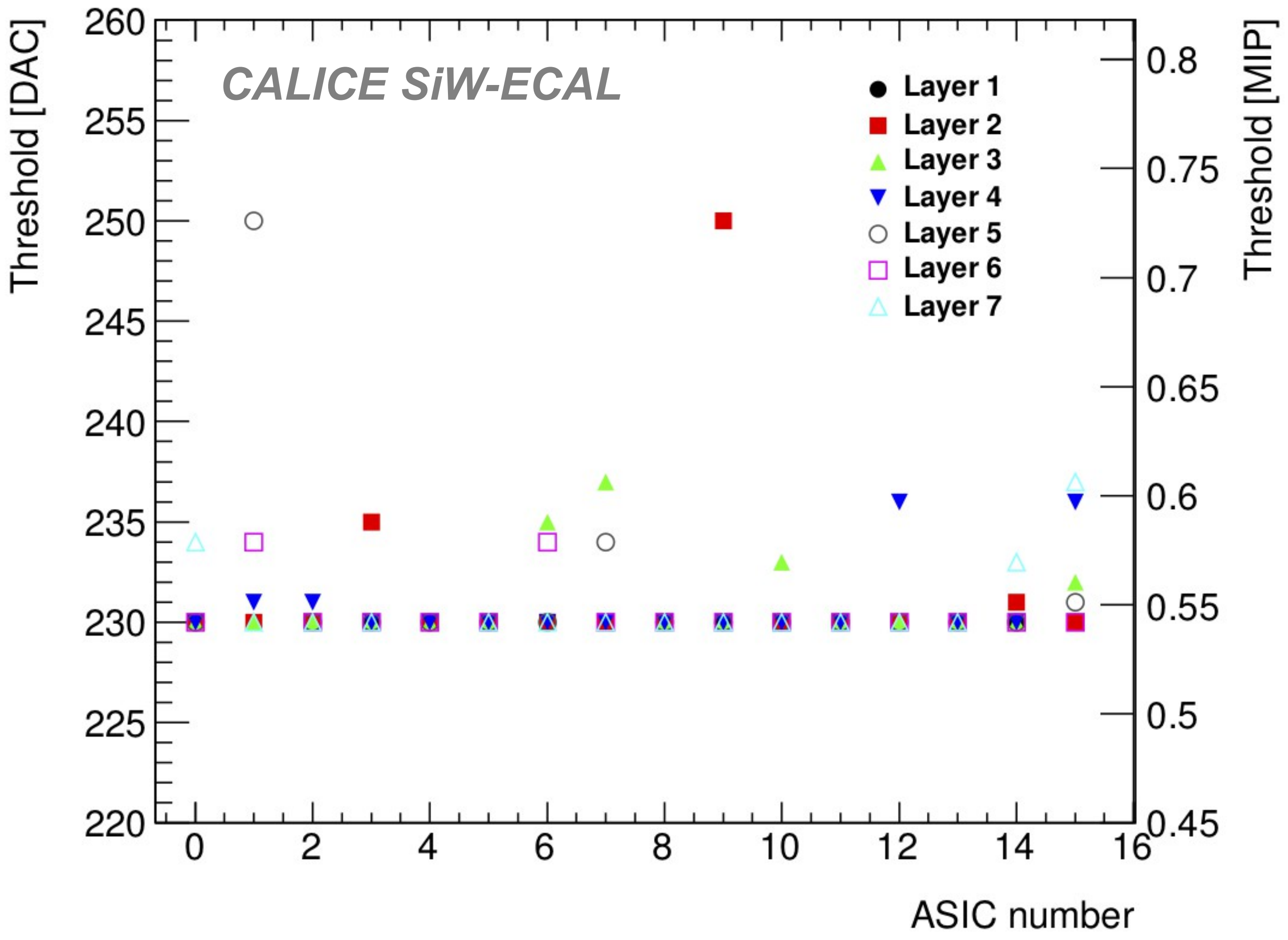
=> SKIROC2 -SKIROC2a

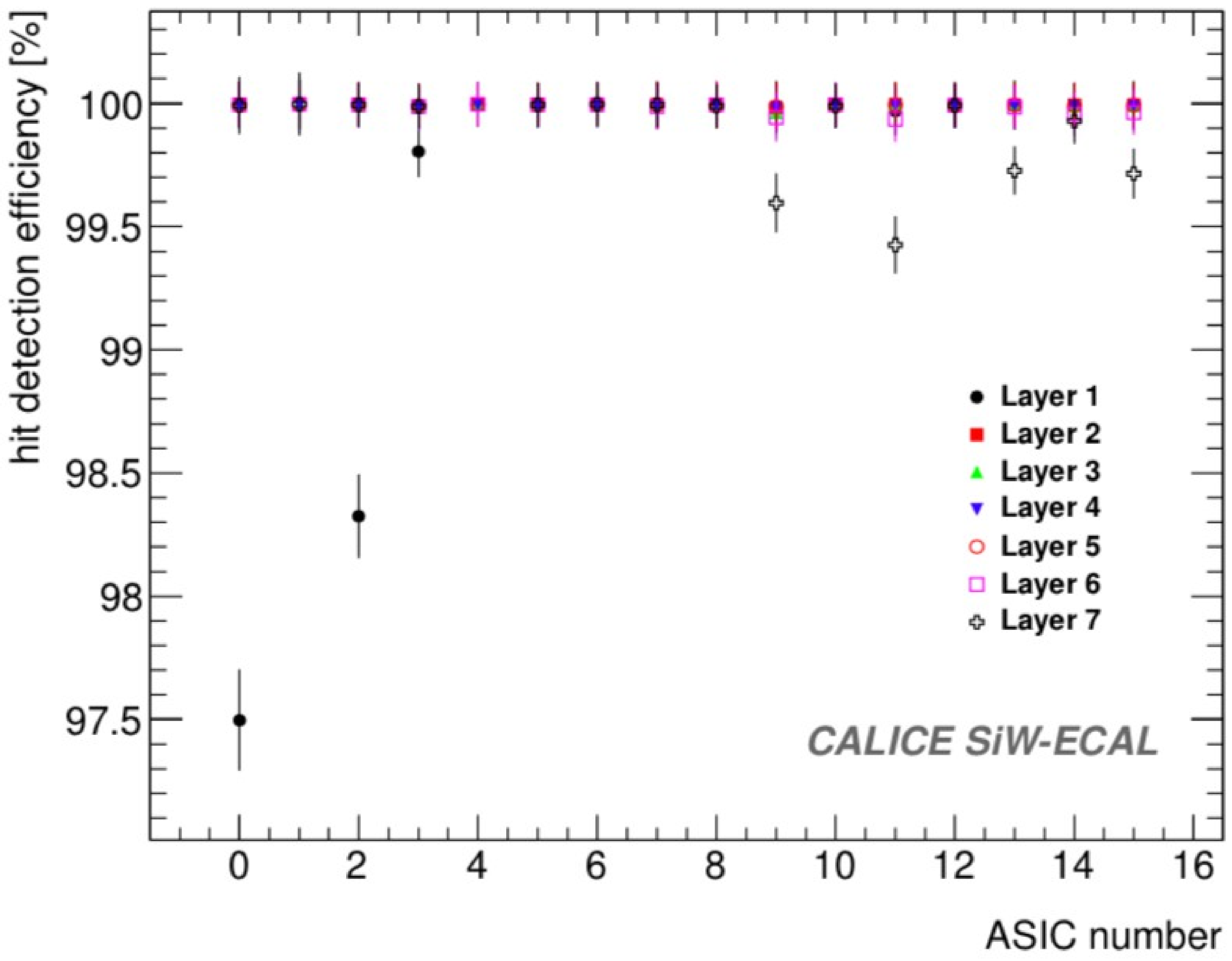
- CERN 2015
  - First ASUs with 1024 pads, temporary connection sensor <-> PCB

    PhD Thesis K. Shpak (LLR)

Testbeam 2017 - Results

Arxiv:1810.05133





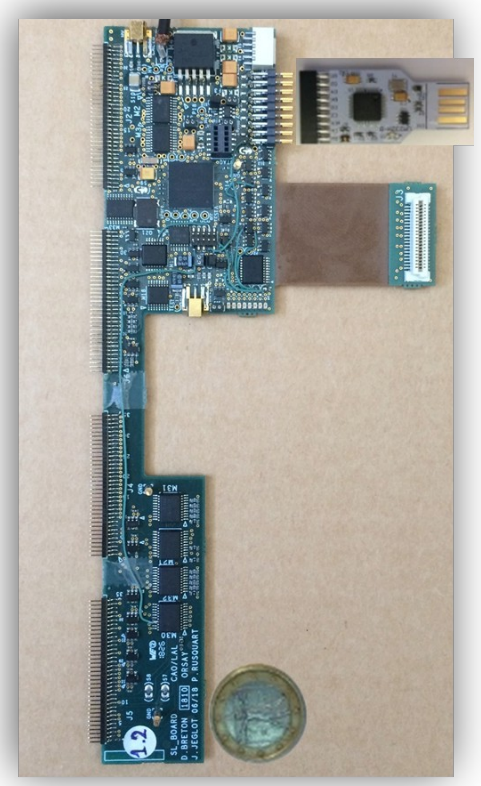
Trigger thresholds uniform at around 1/2 MIP
S/N ratio ~12 (in auto trigger chain)

MIP Detection efficiency ~100%

PFA requires:
a) Access to small signals -> Low trigger thresholds ✔
b) Tracking in calorimeters -> High MIP detection efficiency ✔

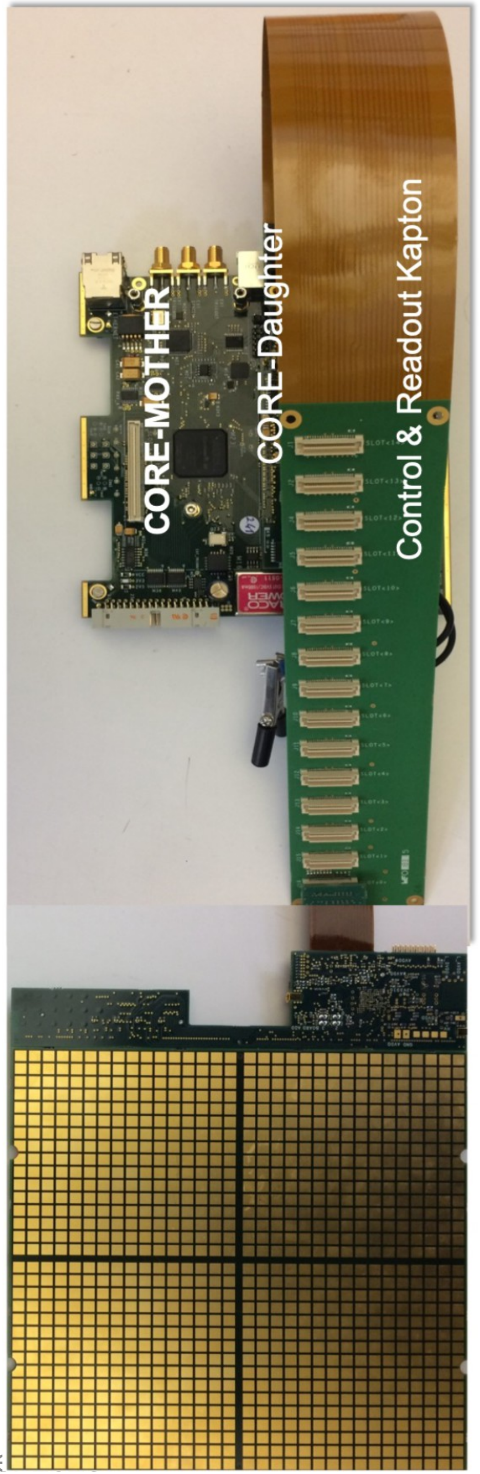
Compact readout

Current detector interface card (SL Board) and zoom into interface region

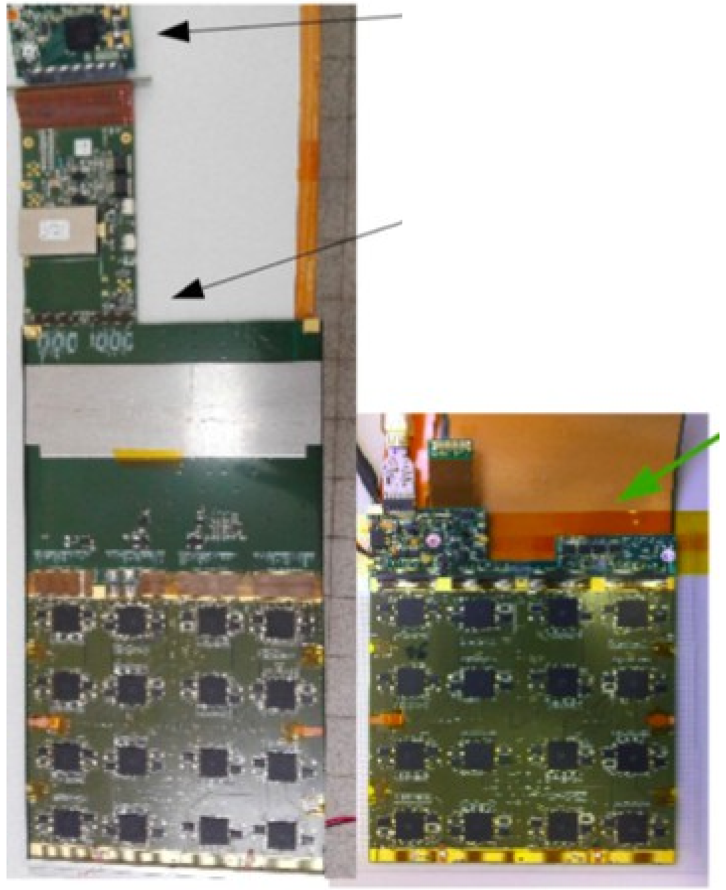


SL Board

Complete readout system



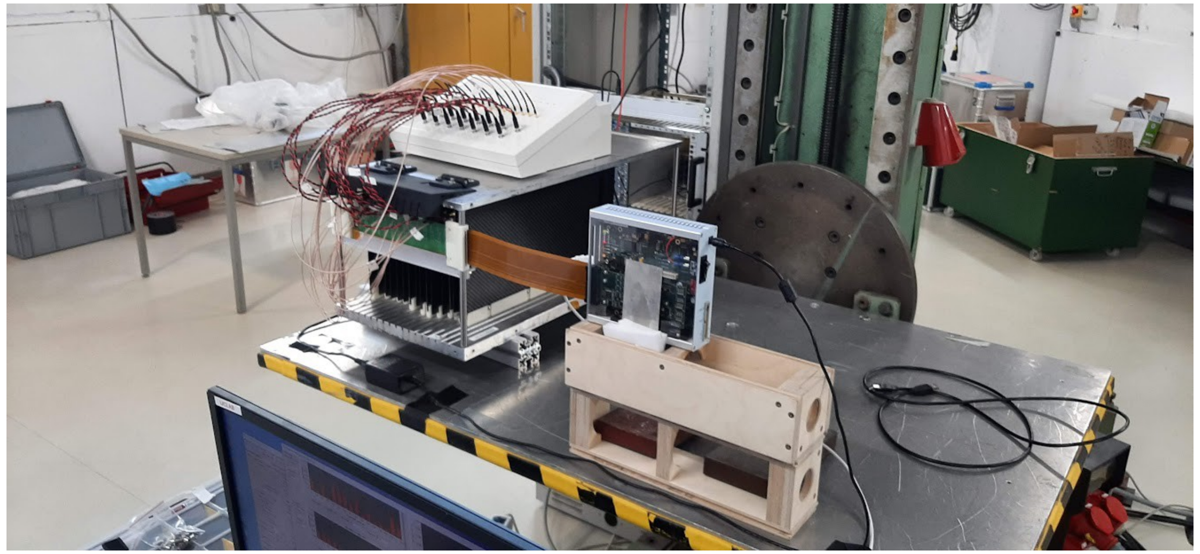
For reference
Comparison old/new r/o system



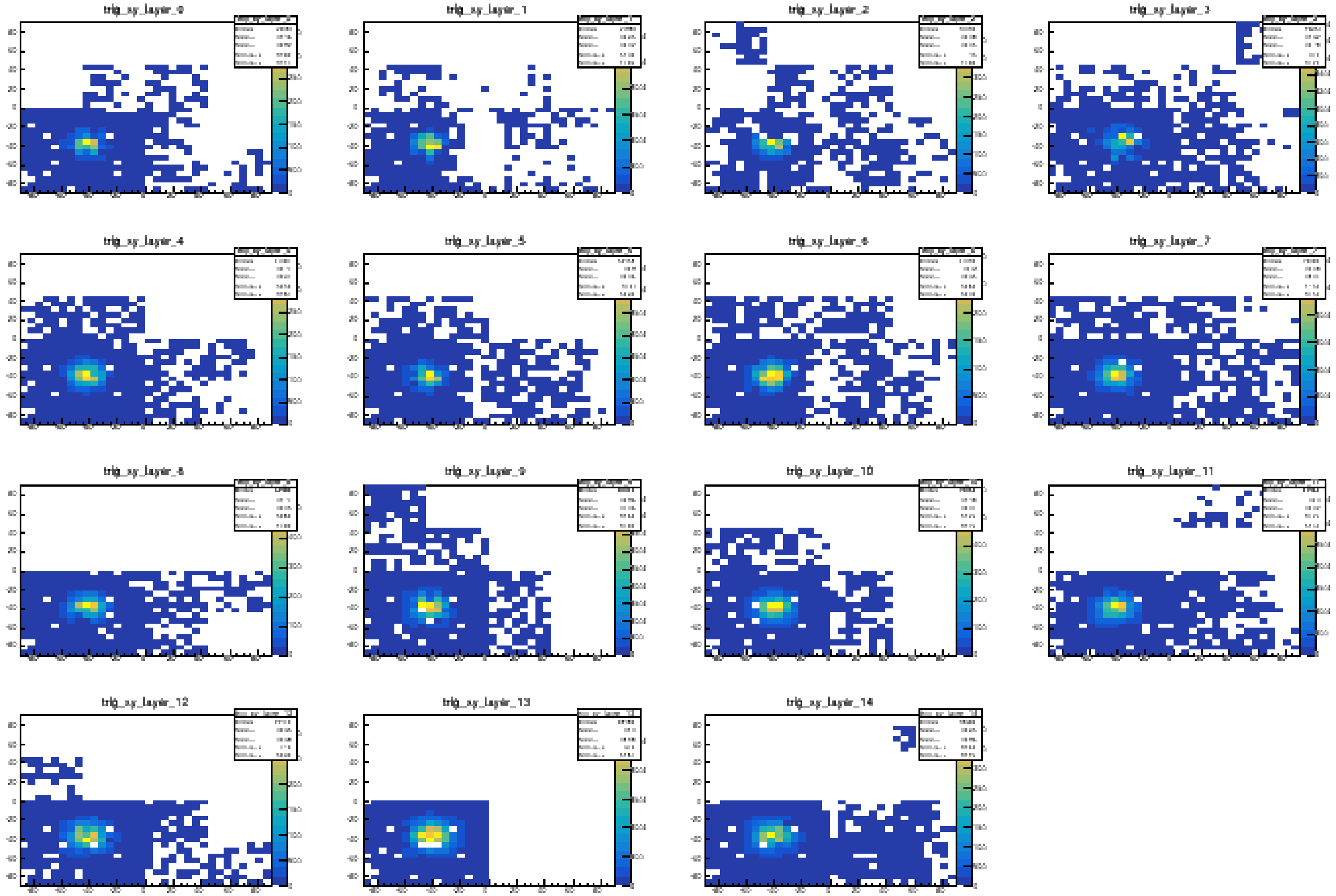
- “Dead space free” granular calorimeters put tight demands on compactness
  - Current developments in for SiW ECAL meet these requirements
- System allows to read column of 15 layers <-> to be expected in ILD
  - Important that full readout system goes through scrutiny in beam tests
- Readout piloted by performant firmware

Deliverable of AIDA-2020 and HIGHTEC

Detector Setup



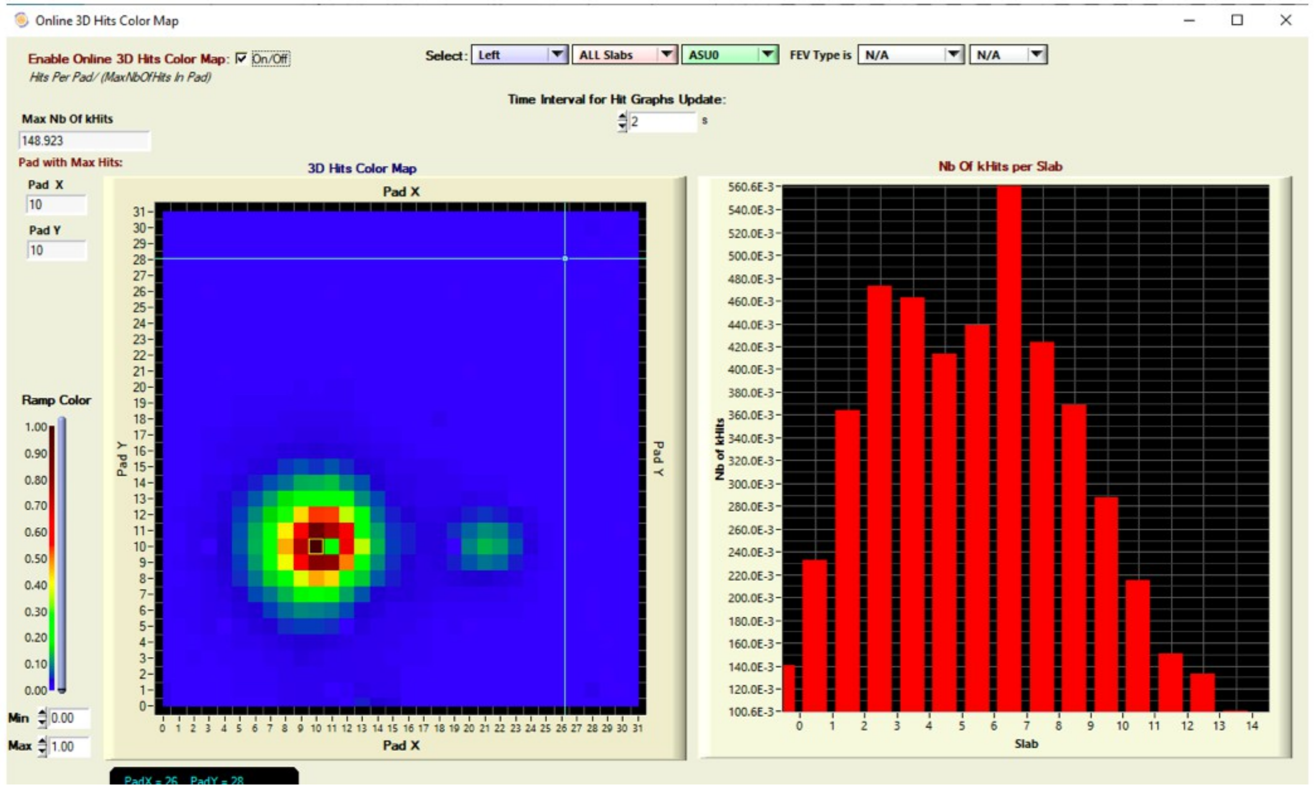
Detector in beam position



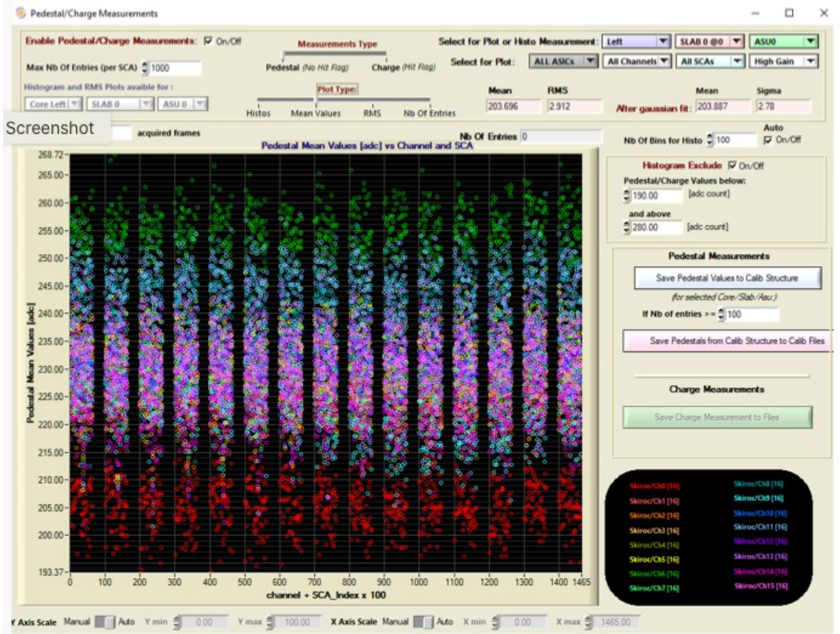
- Beam spot in 15 layers

SiW-ECAL Beam test – Online Monitoring

Jihane Maalmi, CALICE Meeting Valencia



- Online Hit Maps and shower profiles
- Allow for real time beam and detector tuning
  e.g. Adaptation of beam rates or thresholds

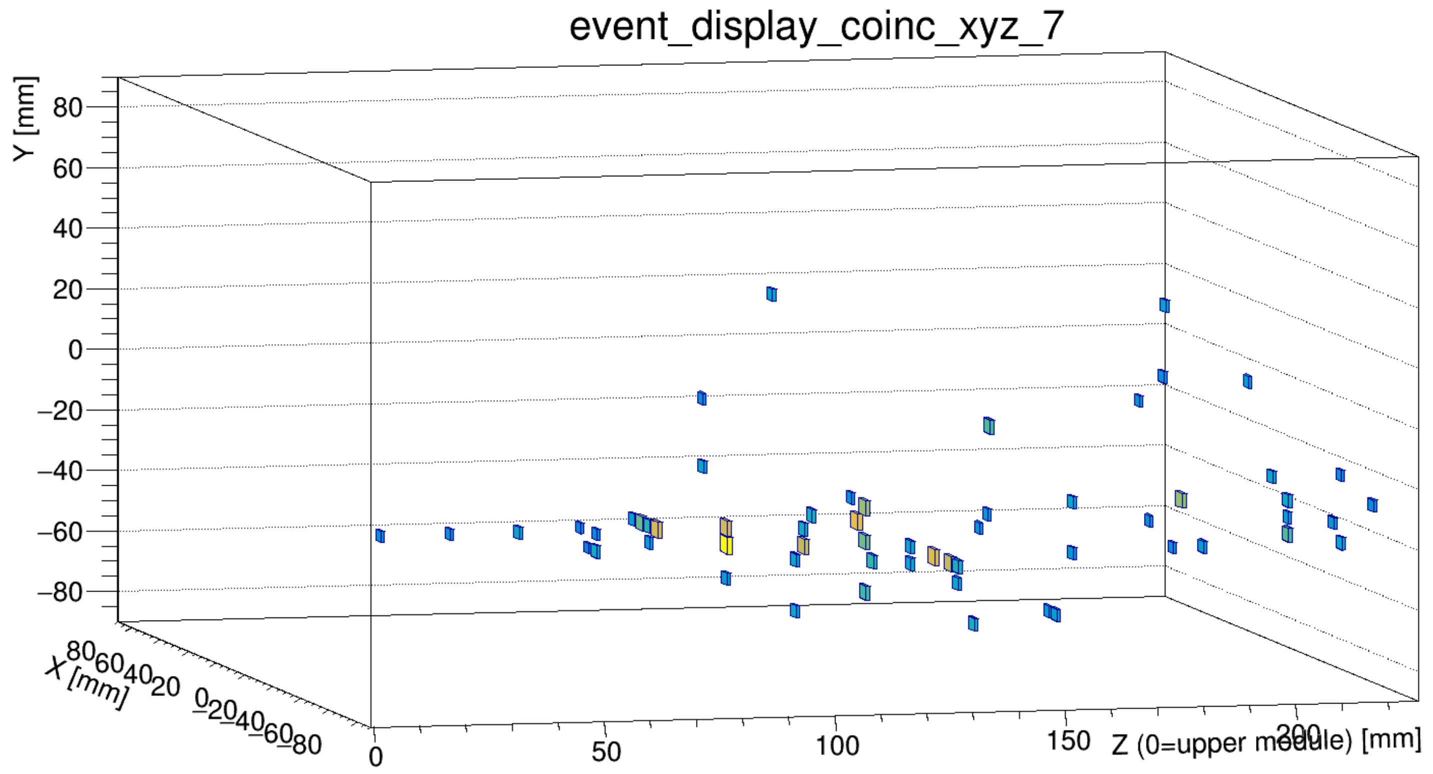


- Further online tools
- Pedestal measurement and subtraction
- Charge measurement and histogramming
- MIP gain correction

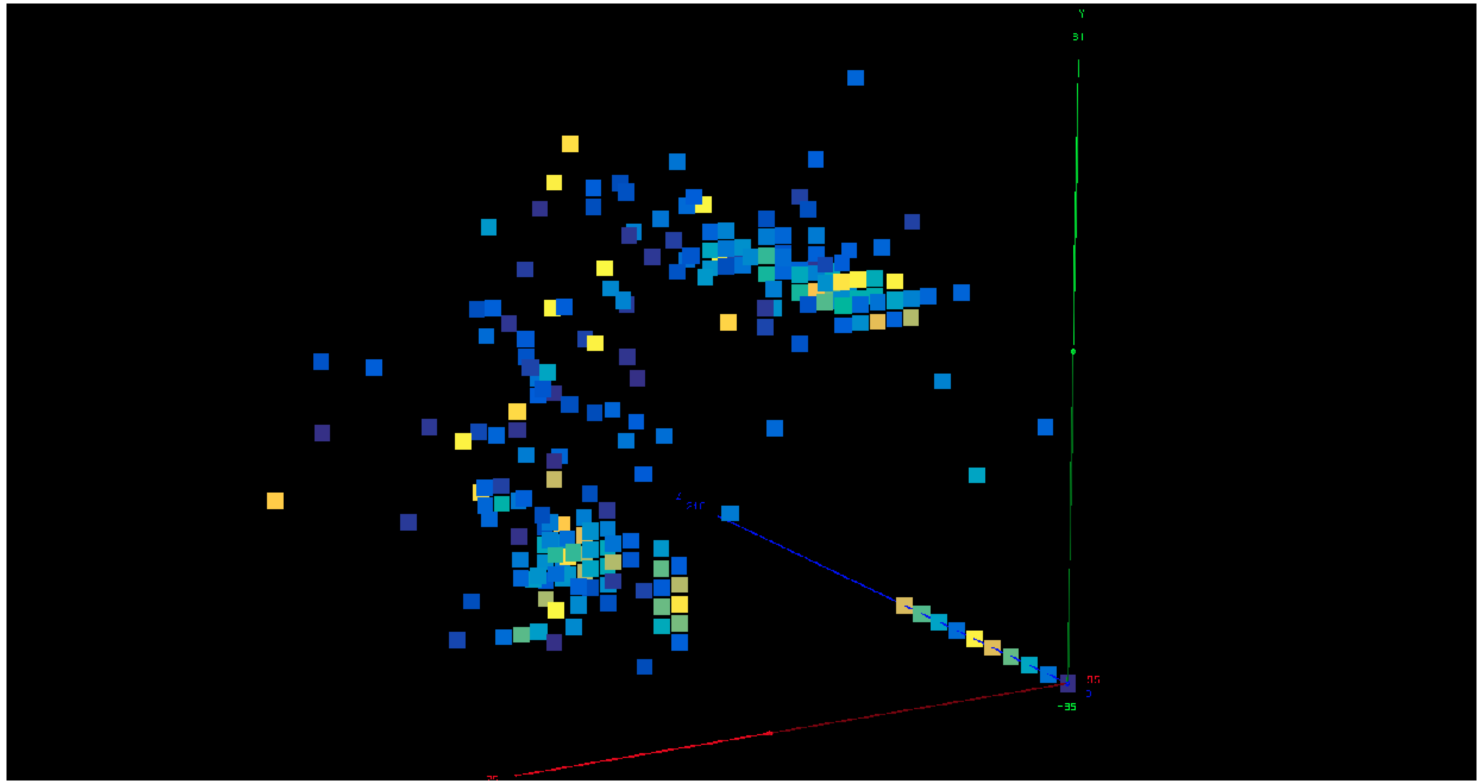
These are just a few examples from the powerful online suite

SiW-ECAL Beam tests 2022 – Onlline/Offline Event Displays

First contained electron showers since physics prototype (2011)



J. Kunath (LLR)



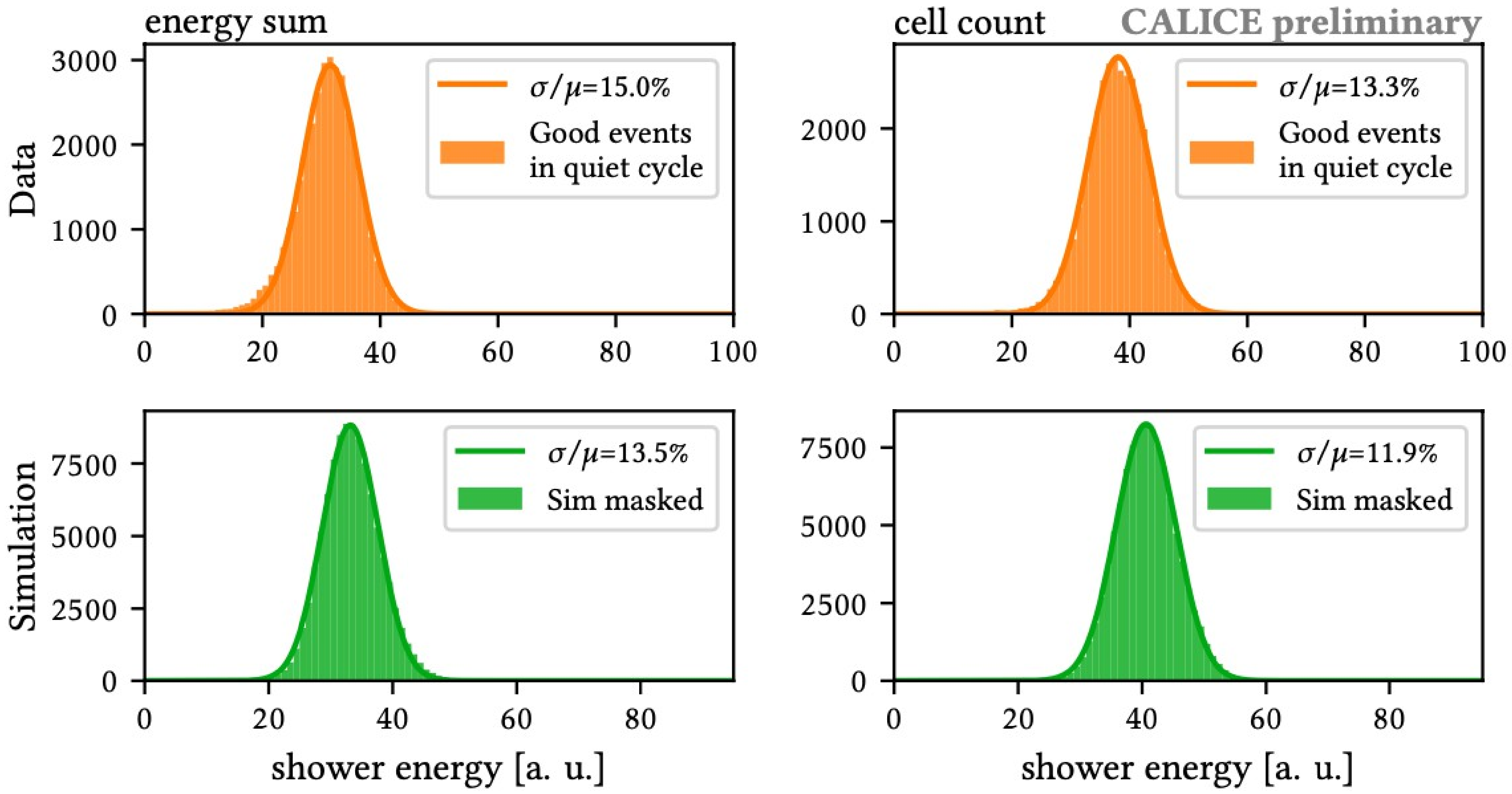
Y. Okugawa (IJCLab)

- Clear showers measured during beam test campaigns
  - Requires full event reconstruction
  - These (and more) “high level” views are available already while a run is going on

- “Particle separation continued”
  - Two electrons “seen” in 20 GeV e- run at CERN

Hot news - First results from DESY beam test 03/22

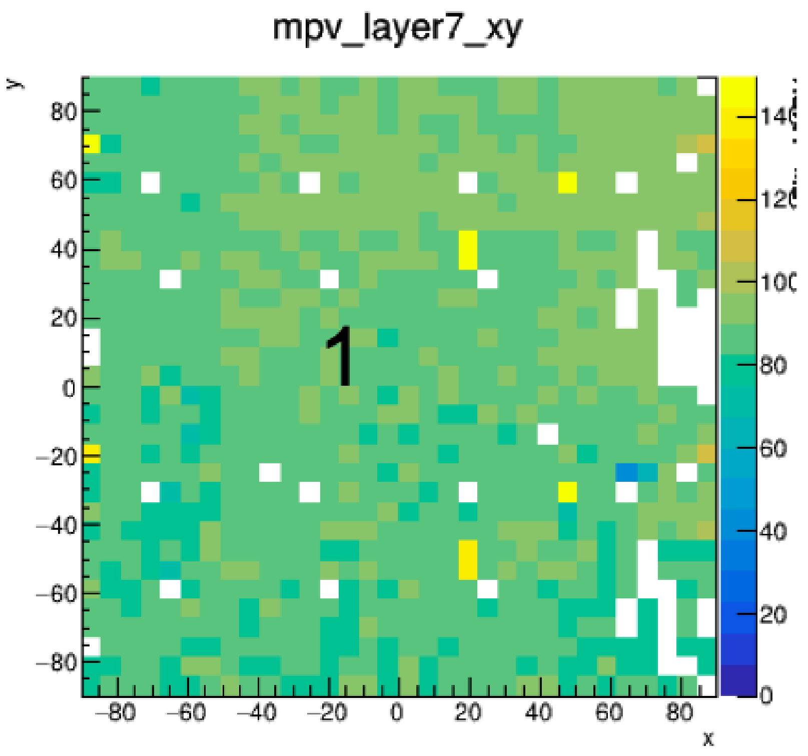
J. Kunath, F. Jimenez-Morales, SiW Ecal Analysis Meeting, 22/09/22

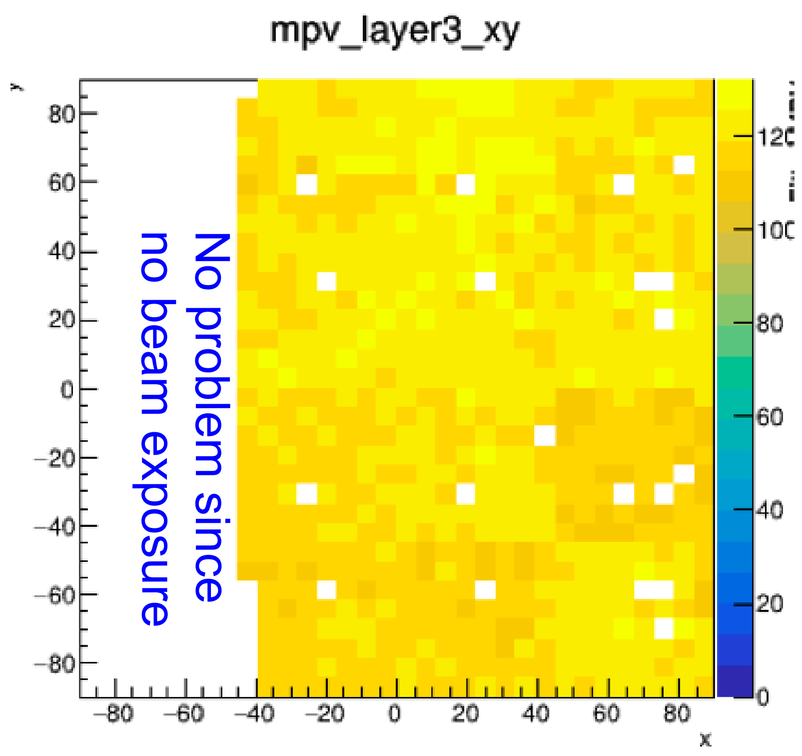


- After proper filtering energy resolution in right ballpark for current prototype
- Convergence in agreement data/MC

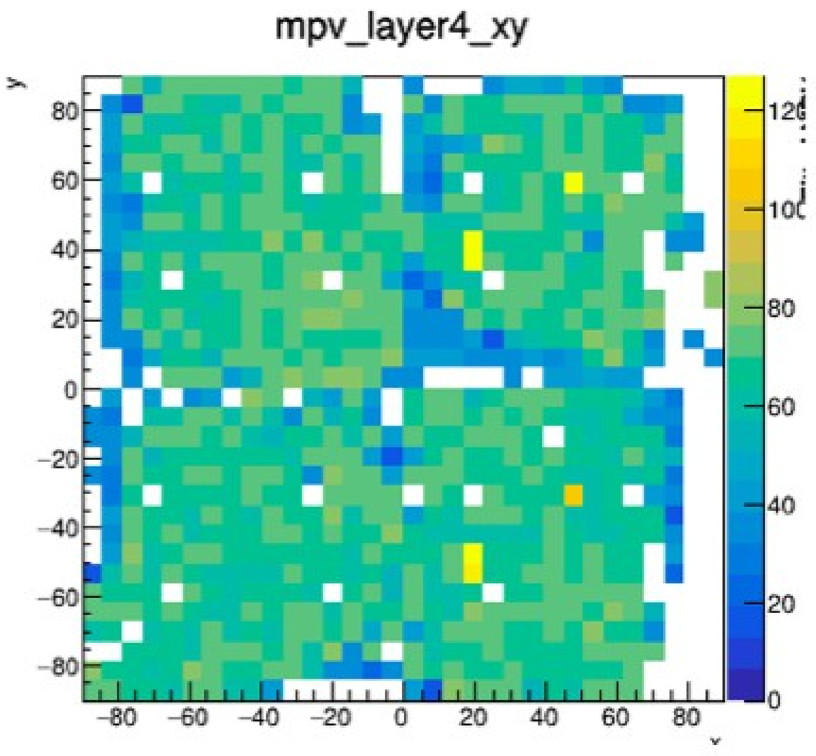
SiW-ECAL Beam test 2022 – Further observations

Adrian Irles





- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - > 90% efficiency for MIPs
  - Here white cells are masked cells due to PCB routing
    - understood and will be corrected

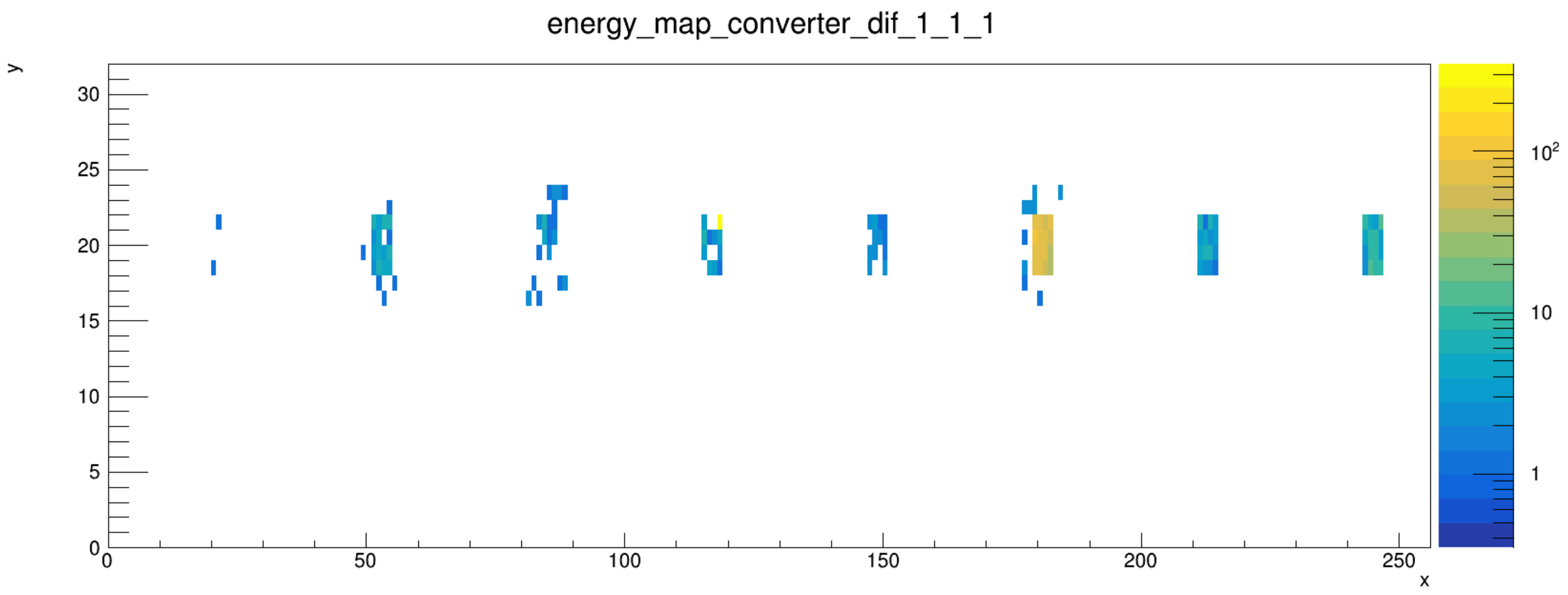


... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - Not seen in 2017, degradation observed during 2018/19
  - To be understood, ***will require dedicated aging studies***
- Since Summer 2022 access to the different stages of the ASICs
  - => analogue probes, <u>major</u> debugging tool

Electrical long slab

Chain of
8 detection elements
~2m

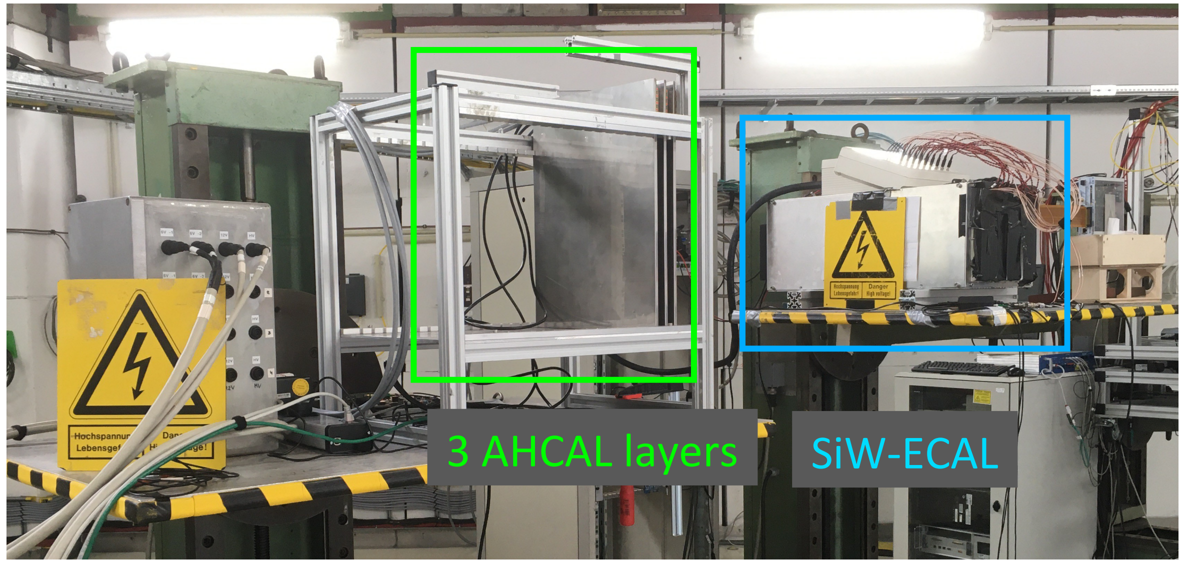


- Very encouraging results in first beam test in 2018
  - Credibility for concept as foreseen for e.g. ILD
  - Issues with signal drop towards extremities
- Long slab studies will be resumed with new FEV
  - Adapted for power pulsing, will avoid voltage drop, etc ...

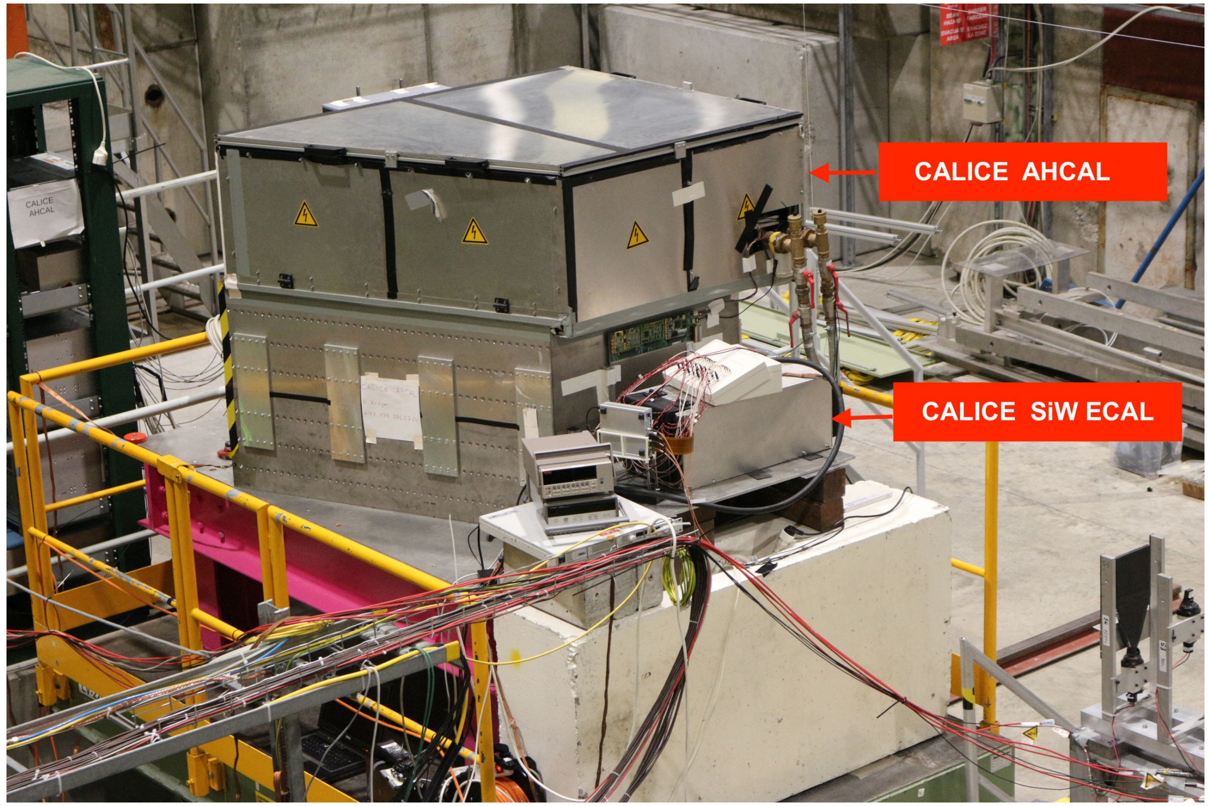
Common developments

CALICE meets DARK MATTER LAB

SiW-ECAL + AHCAL DAQ test @ DESY in March 2022



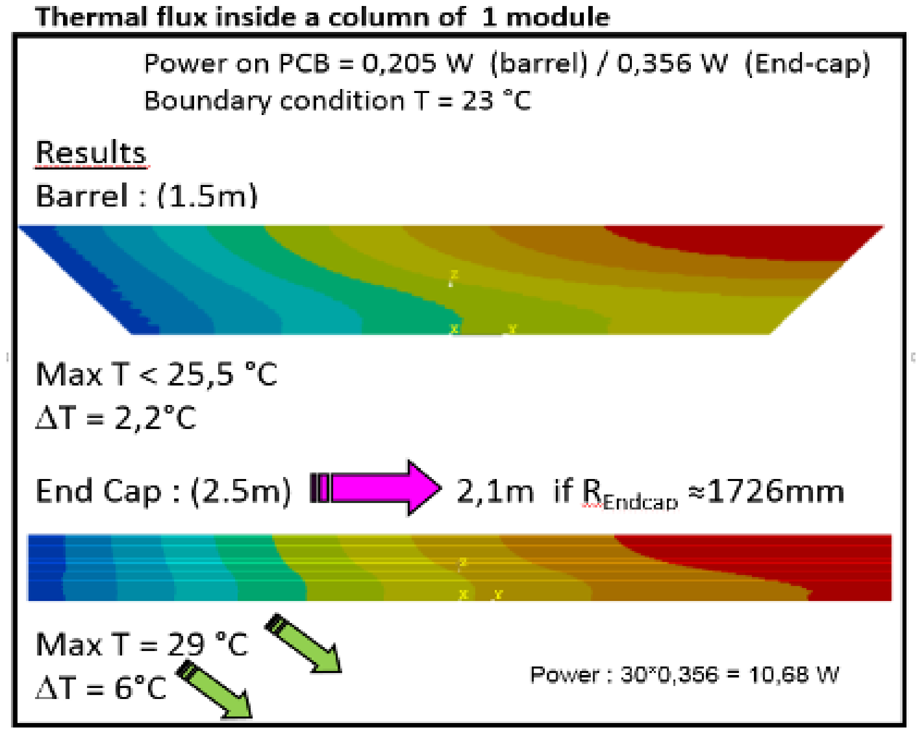
Common setup at CERN June 2022



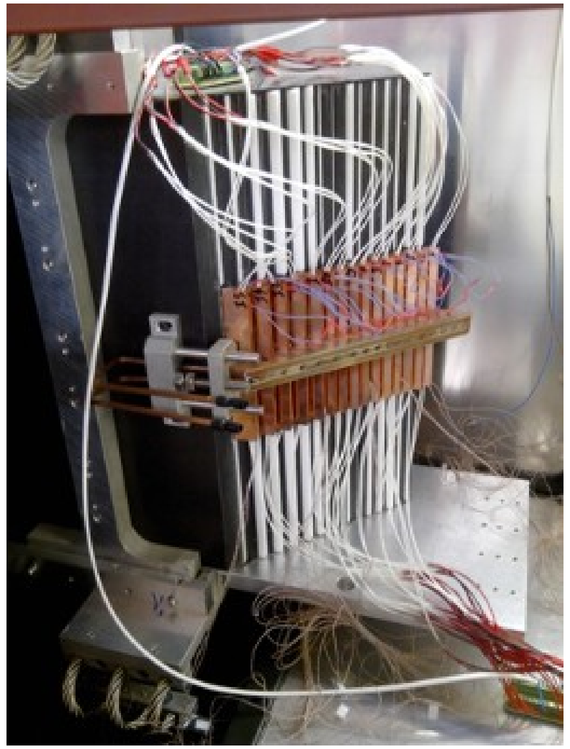
- 15360 + 22000 (full analogue) readout cells
- Successful synchronisation of data recorded with SIW-ECAL and AHCAL
  - First step of ***knowledge transfer*** on compact readout system to AHCAL → AIDA innova
- Common running makes full use of EUDAQ tools (developed within European projects)
- Common data anlalysis ongoing

Deliverable of AIDA-2020

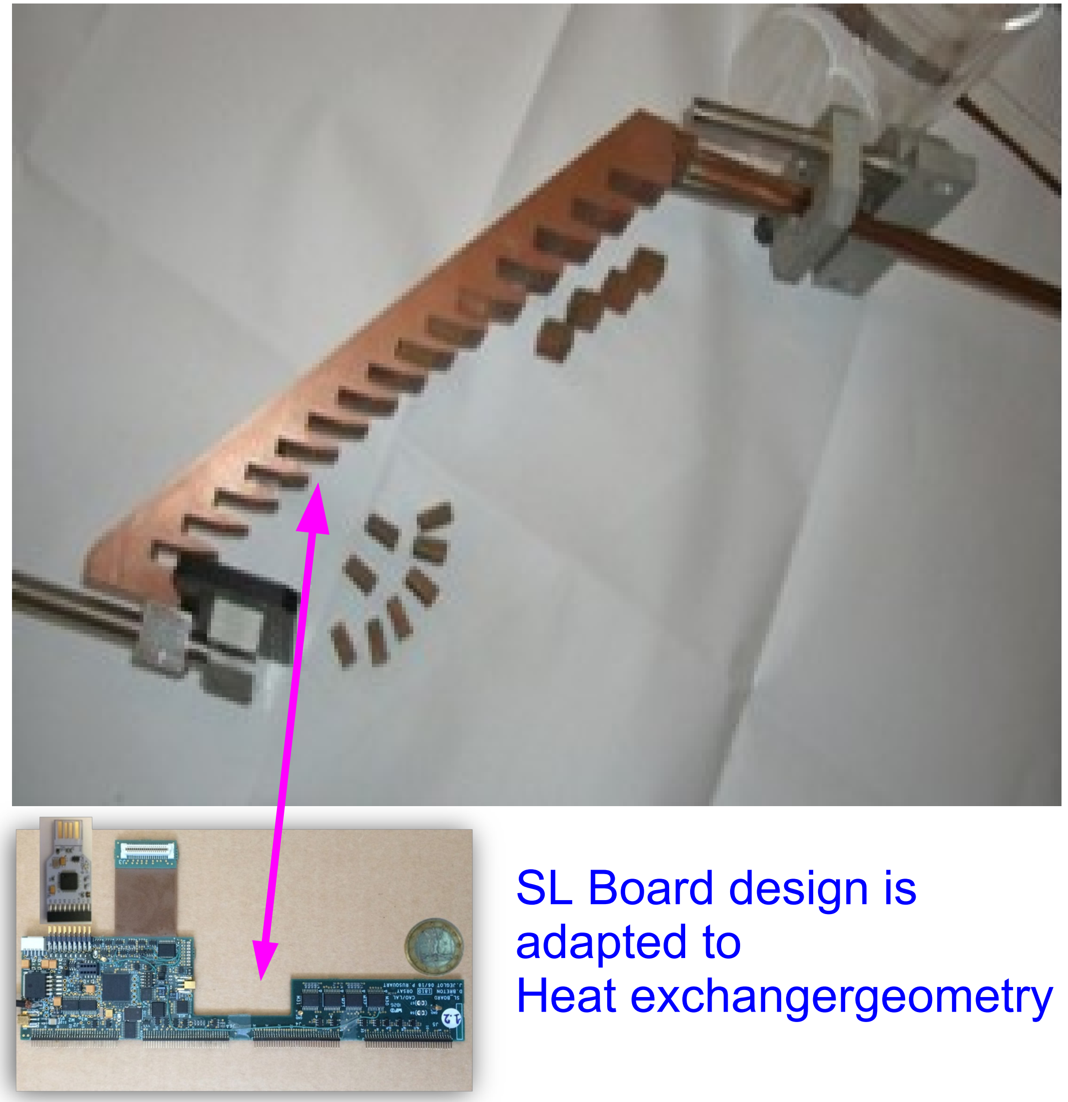
Thermal simulation within barrel module



Thermal tests with alveolar structure



Heat exchanger



SL Board design is adapted to Heat exchangergeometry

- Full design study for ILD like detector and ILC like beam structure
  - Passive cooling is sufficient
- Common development of interface cooling system <-> detector layers
  - Hardware exist, requires test with instrumented prototype

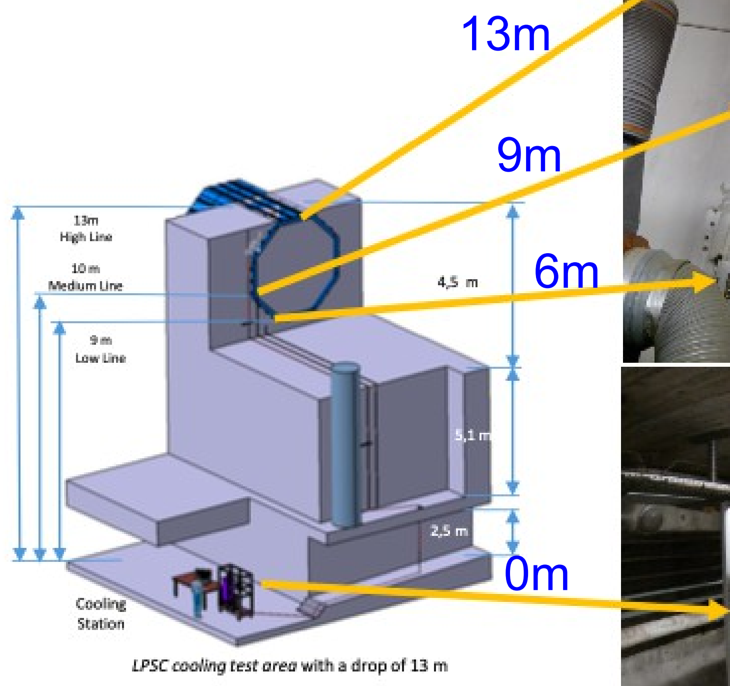
Full Cooling System – ILD SiECAL

Demonstrator of large leakless loop for CALICE/ILD ECAL

Deliverable of AIDA-2020

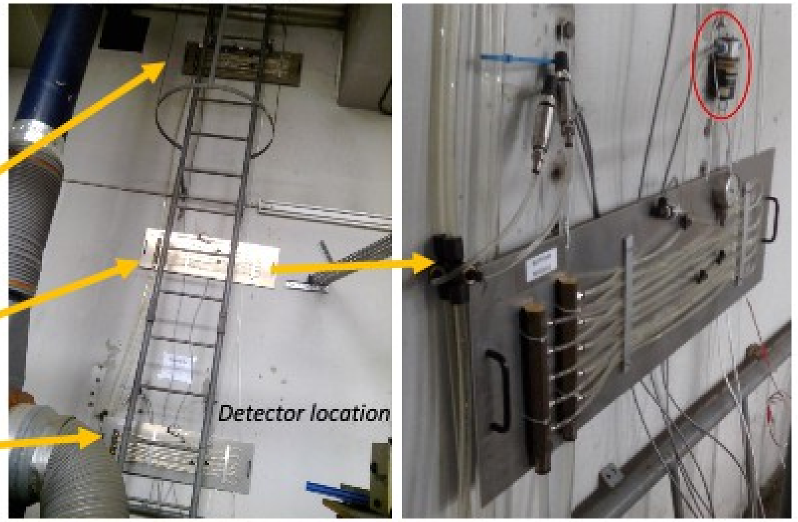
- Thermal model as milestone
- Probes at different heights to establsih full model of Cooling system for large detectors

a large leak-less cooling-loop



LPSC cooling test area with a drop of 13 m

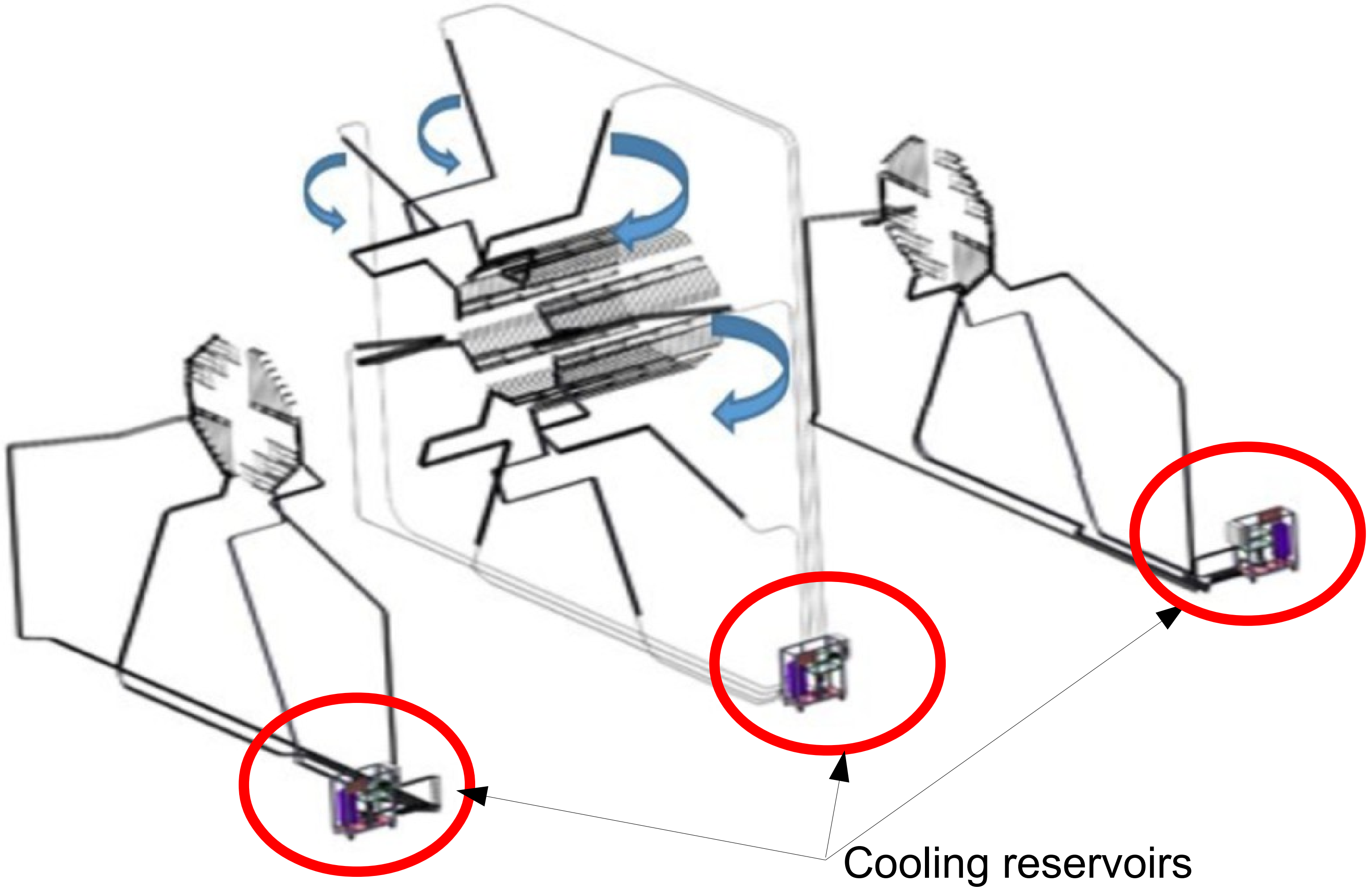
Upper part of the experiment



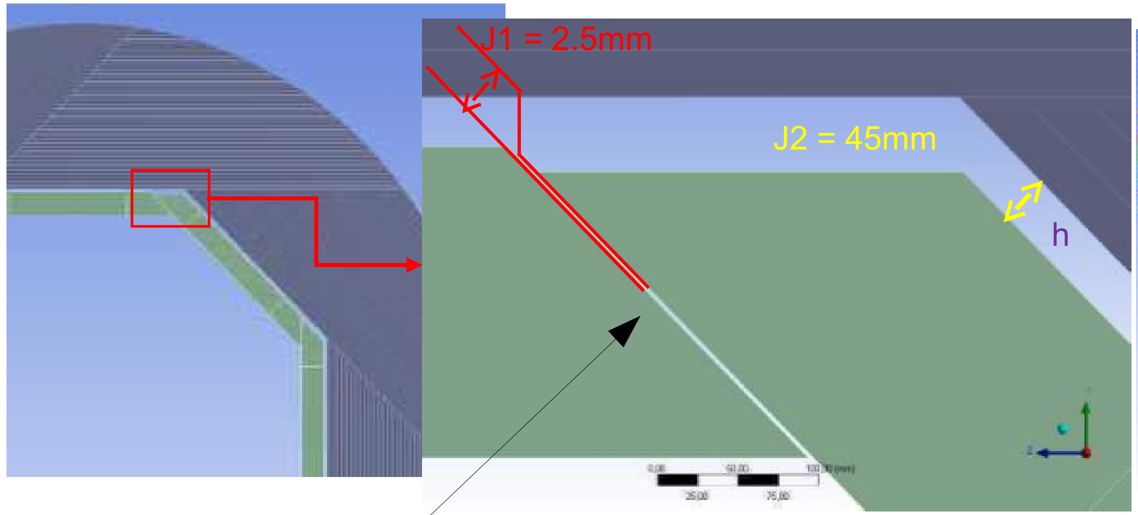
Julien Giraud

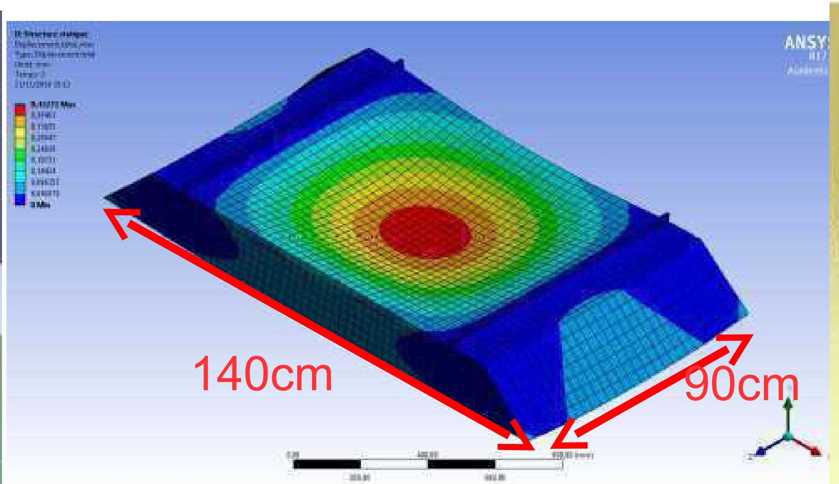
Studies for efficient leak detection Ongoing (Polarographic probe)

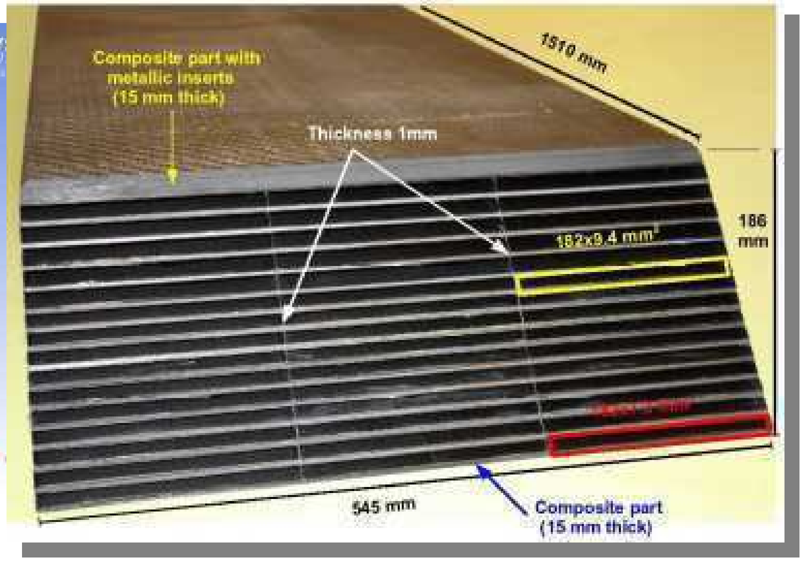
LPSC



ILD SiECAL – Mechanical structures and studies



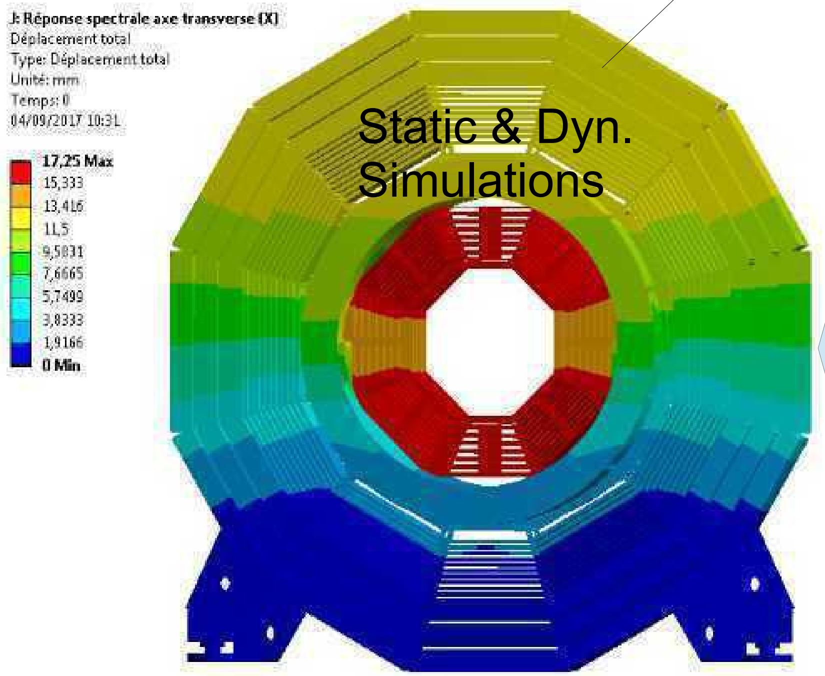


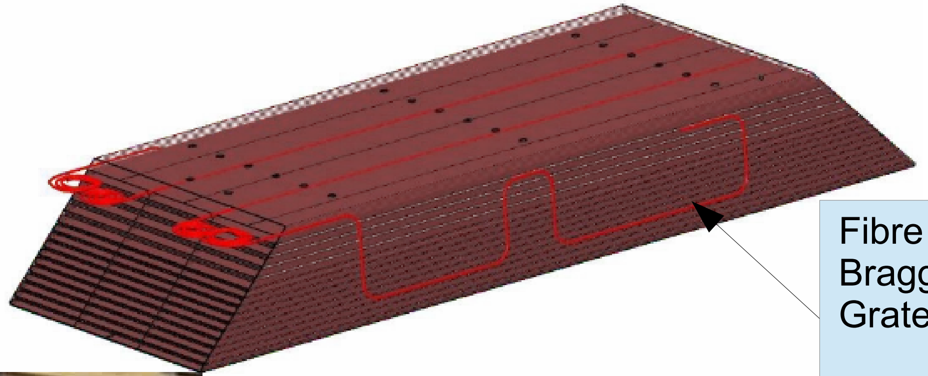


J1 = clearance between modules for the ECAL

J2 = Clearance at ECAL edges between ECAL and HCAL

h = height of the rails 30mm



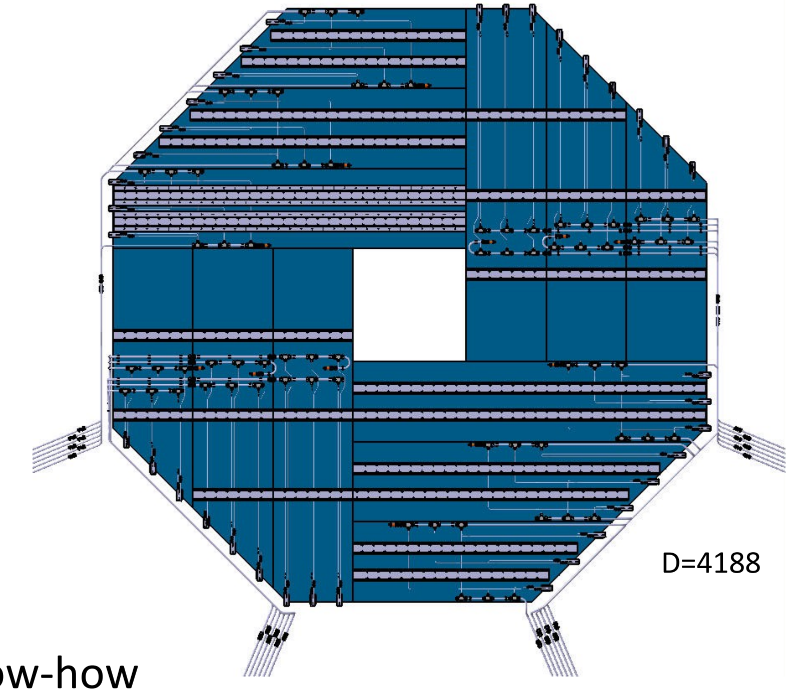


Fibre Bragg-Grated

measurements still to be done...

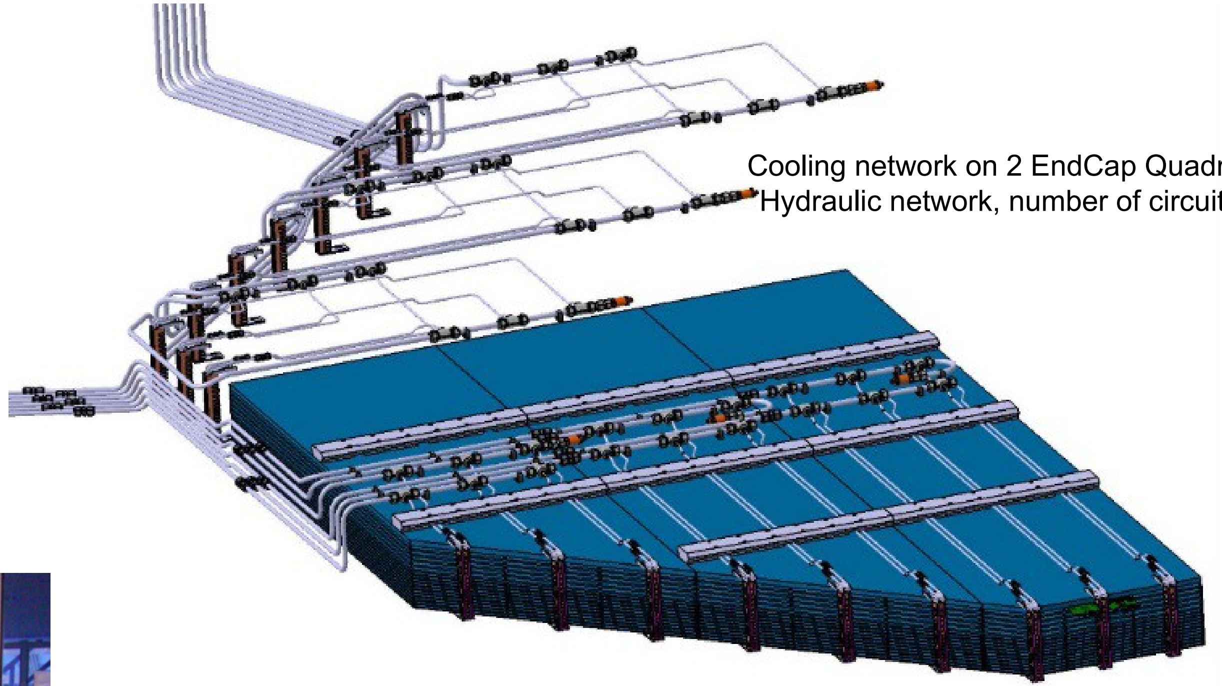
ILD SiECAL – Endcaps

End-Caps: modular alveolar structure - composite W / Carbone HR - 25,5 t
2 x 12 independent modules - 2 x 540 alveoli



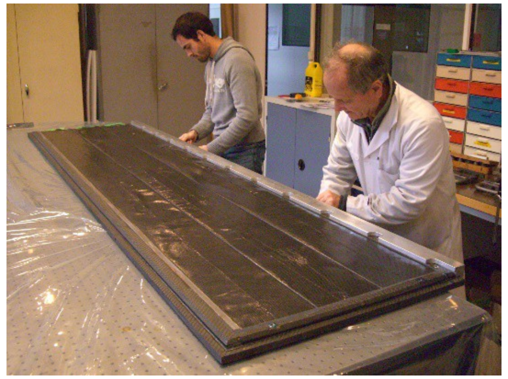
D=4188

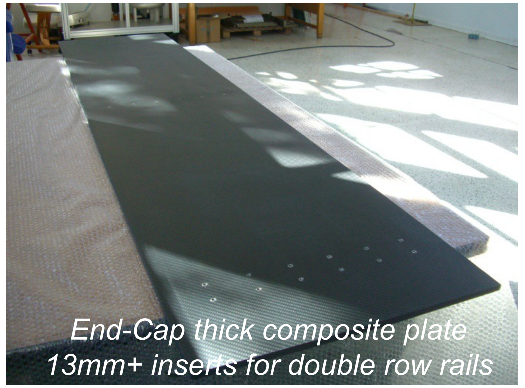
25,5 t / EC
4 quadrants of 3 modules
2 x 12 modules
2 x 540 alveoli



Cooling network on 2 EndCap Quadrants
Hydraulic network, number of circuits…

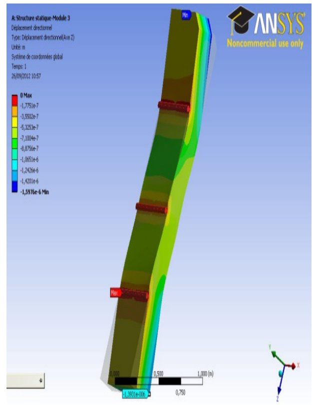
Know-how

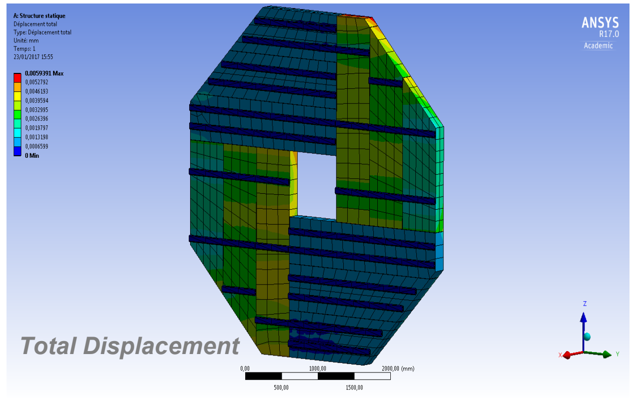




End-Cap thick composite plate
13mm+ inserts for double row rails

Composite simulation
/ rails positioning





Total Displacement

CFRP structures / End-Cap module : thick plates with inserts & longest layer : 3 alveoli L = 2.5 m wall thick. = 0.5mm

Summary

- R&D and testbeam campaigns 2012 – 2018 allowed for studying individual aspects of technological prototype
  - SKIROC ASIC
  - ASUs with 1024 readout cells
  - Different types of PCB
  - Maximum of seven layers in stack
  - Detector response at MIP Level
  - Elements of assembly chain
  - First experience with long layers

- Successful operation of a fifteen layer stack in beam tests at DESY and CERN in 2021 and 2022
  - Major milestone for technological prototype
  - Demonstration of performance of compact DAQ
  - Rich set of data to study detector performance
  - First “calorimeter” since physics prototype
    - However, physics prototype had 30 layers
    - 15 layers include recycled older ASUs
  - Have already precious feedback on future programme

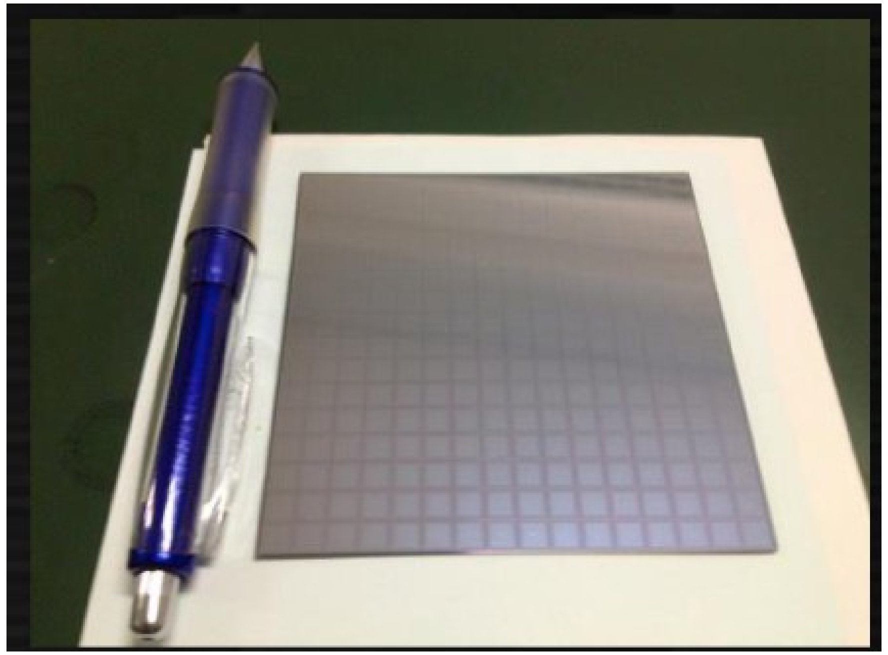
- Performant infrastructure to conduct conclusive system tests in coming years

- Advanced engineering studies accompany ongoing R&D activities
  - Interplay detector concepts and R&D Collaborations is vital for success

Backup

SiW Ecal – Wafer R&D I

Si Sensor (9x9cm² from 6" wafer)



N-type silicon
Crystal Orientation: <100> or <111>

Wafer specs

Tab 1 : Summary of the substrate characteristics

	Min.	Typ.	Max.
N type silicon	-	-	-
Resistivity (kOhms.cm)	4	5	-
Thickness (µm), option T1	310	320	**330**
Thickness (µm), option T2	490	500	**510**
Width (mm), option S1	89.7	89.8	89.9
Width (mm), option S2	44.7	44.8	44.9

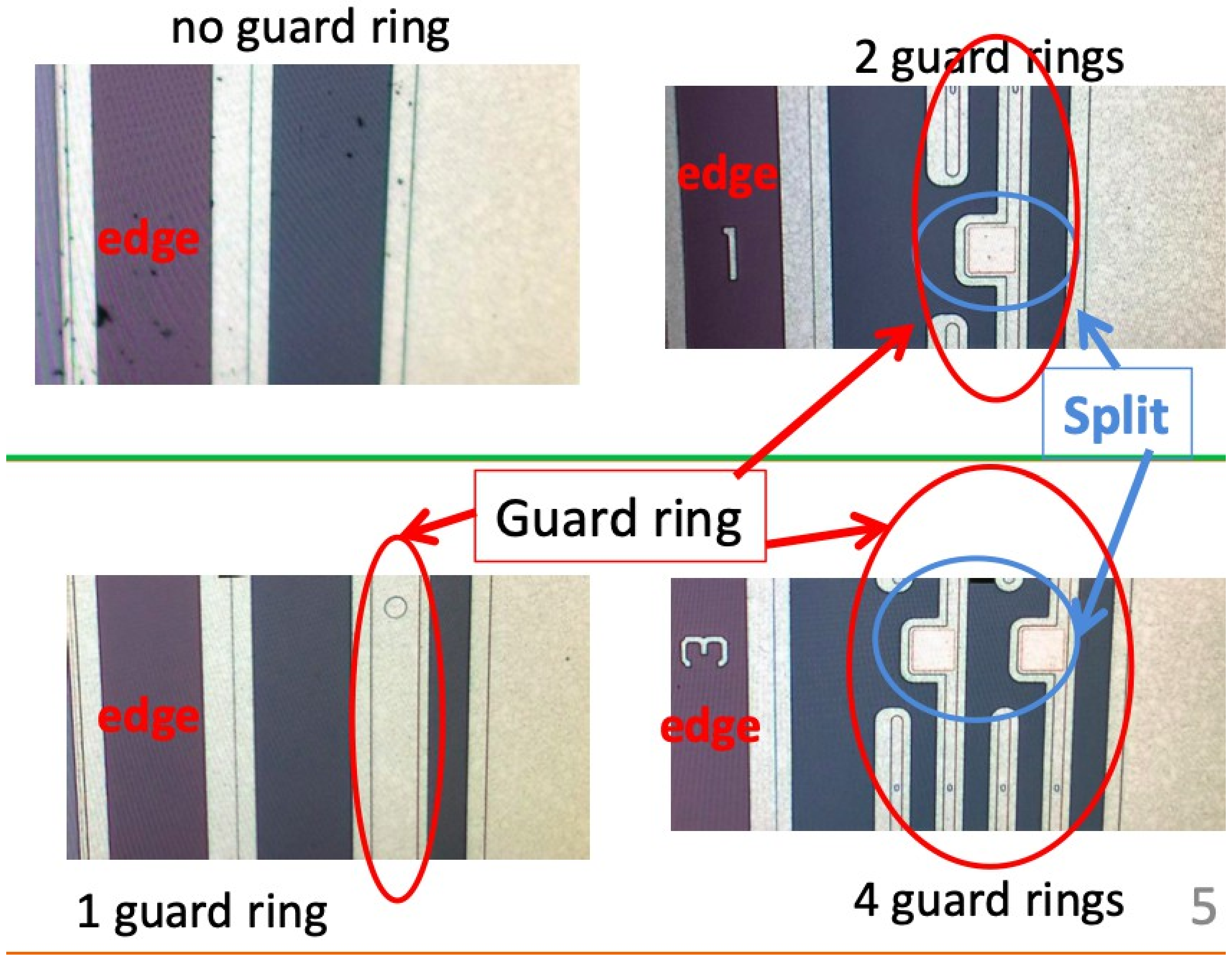
Definition of specifications for different wafer types:
Resisitvity: > 5 kΩxcm
Price: Typically 1000-1500 EUR/wafer (when ordering small quantities)

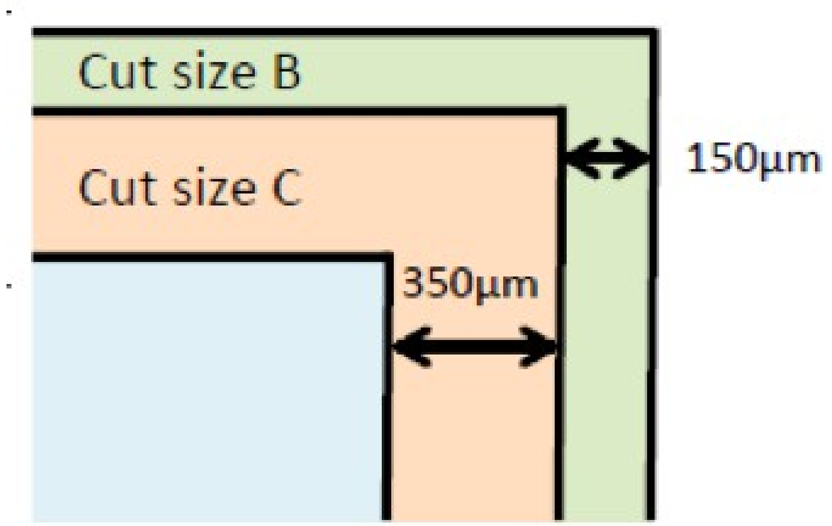
- In addition we require small leakage current:s under full depletion a few nA/pixel but for cost reasons we tolerate a certain fraction of pixels with higher leakage currents

- Vendors: OnSemi (CZ) and Russian company for physics prototype (~2003)
  Hamamatsu for technological prototype (since ~2010)
  Contacts with other vendors (e.g. LFoundry) hibernating mainly for funding reasons
  The drop-out of Infineon for the CMS HGCAL was/is bad news

SiW Ecal – Wafer R&D II

We (i.e. Mainly Kyushu) have tested several wafer types in previous years





- Cut size determine the actual sensitive area of a wafer
- Different designs mainly on test samples of "baby wafers"
- The "Hamamatsu" standard is still 0 or 1 full guard ring
  - 0 is "fake 0" guard ring, in fact there is still a small guard ring

Observations in recent years (see also backup for more details)

- Split or no guard ring lead to suppression of square events
- In prototype we still use full wafers with 0 or 1 guard ring
- General trend of reduction of bias voltage
- Can operate 500mum wafers at 60-80 V in full depletion

- Towards 8" wafers?
  - General trend (e.g. CMS) is to use 8" wafers
  - Larger surface/wafer =>smaller cost
  - Standard thickness 725mum
  - Impossible to get access to HPK production
  - Lines (CMS HGCAL Production)

SiW Ecal – Front end electronics

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
- High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
- Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)
- Auto-trigger at ½ MIP, on chip zero suppression
- Low Power: (25µW/ch) power pulsing