# Objectifs d'un démonstrateur ultragranulaire ECAL

Revue CALICE

*QUOI , QUAND, COMMENT, QUI ?*

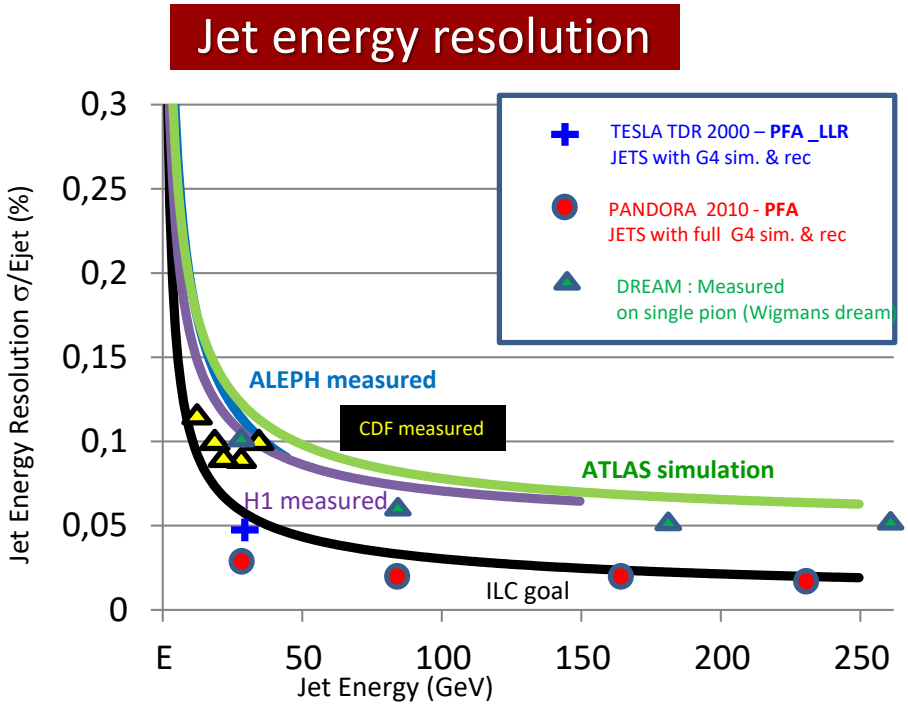
**Jean-Claude Brient**

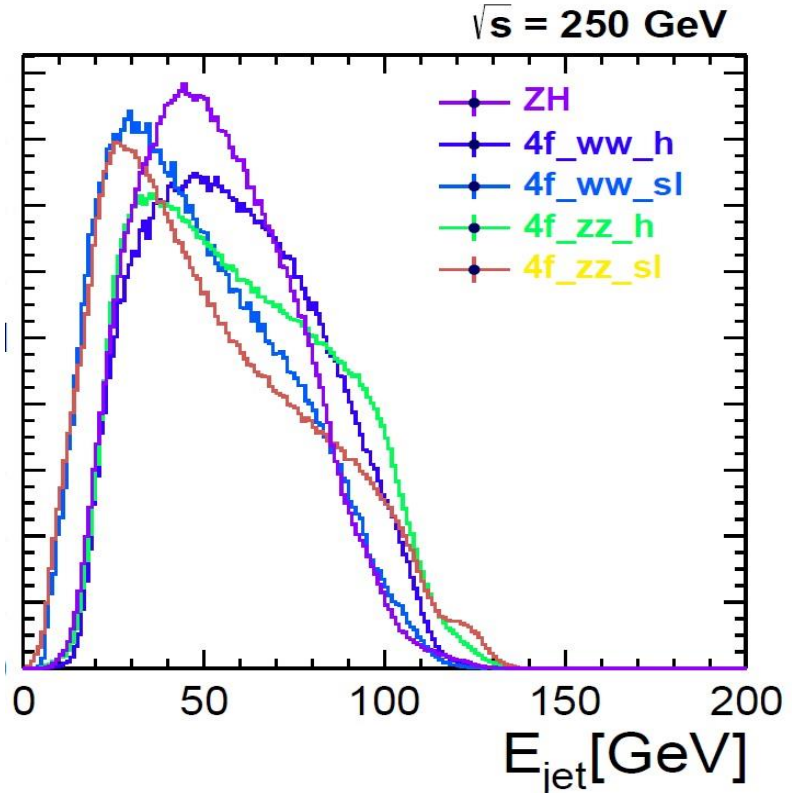
Laboratoire Leprince-Ringuet
Ecole Polytechnique – CNRS
Palaiseau

# QUOI

## Higgs Factory

- Study of $e^+e^-$ physics from Z to 350 GeV
- ZH, ZZ, WW , ttbar , etc…
- BEST use of luminosity : Tag the boson through 2 jets decays
- tau polarization (H CP violation, AFB(pol) …)

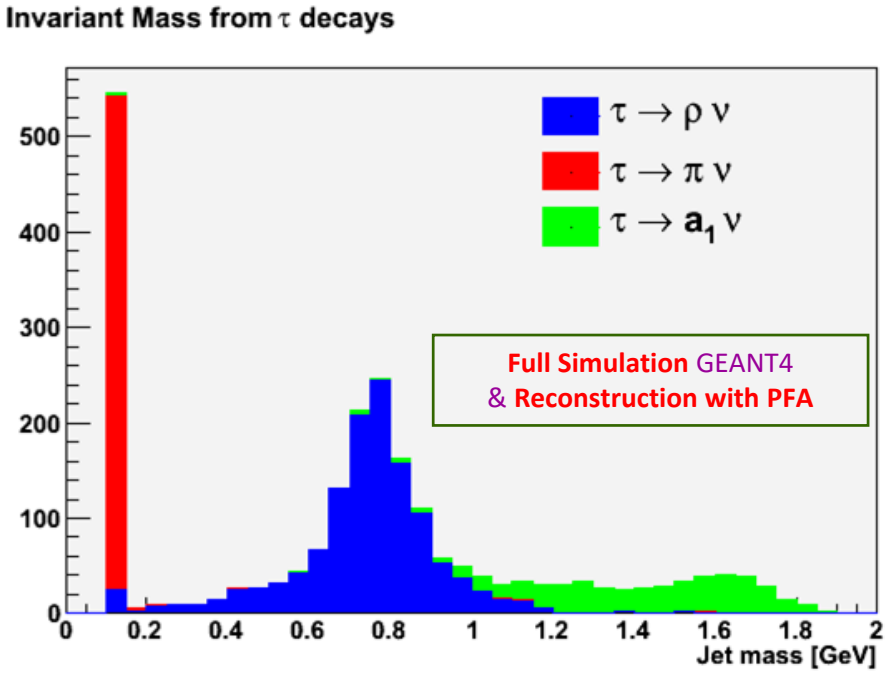


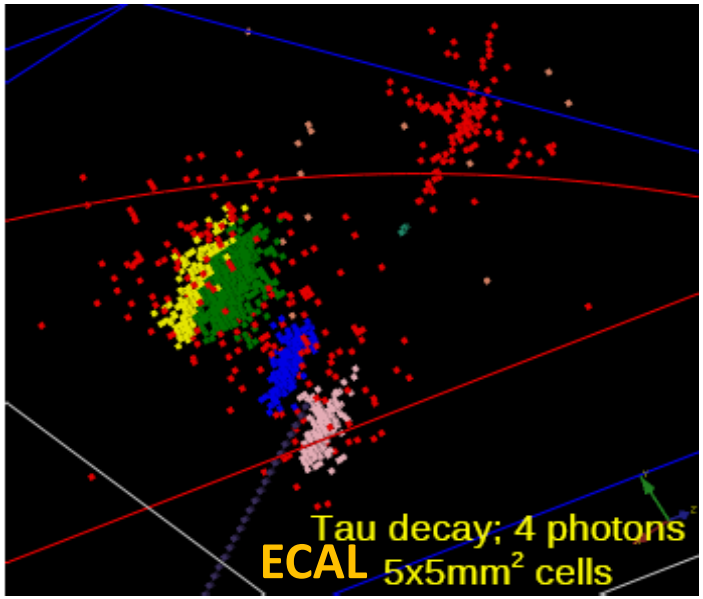




Ultragranular calorimeter with all detector inside coil ("a la CMS")

# QUOI

## on e+e- interaction : $\tau^{\pm}$ as a polarisation analyser




| | Jet mass < 0.2 | Jet mass in 0.2-1.1 | Jet mass >1.1 |
|---|---|---|---|
| $\tau \rightarrow \pi\nu$ | 90.2 % | 1.7 % | 8.1 % |
| $\tau \rightarrow \rho\nu$ | 1.7 % | 87.3 % | 7.4% |
| $\tau \rightarrow a_1\nu$ | 0.6 % | 7.4 % | 92.0 % |

# QUAND

Avoir une réponse en 2025 pour

- CEPC en 2025
- ILC ???
- FCC CERN-report et new ESPP en 2025

Petit reverse-agenda

Pour rappel, un tel calo, c'est 10 ans de construction.
Donc meme pour un FCC en 2040, 1-2 ans d'installation,
début de construction en 2030,

Soit
Design, Enginering fait et test beam analysés en ≤ 2027-2028 !!!

# COMMENT

Donc, partons de l'hypothèse
que c'est bien un calo optimisant les performances PFA
C'est à dire un calo ultragranulaire : **CONSEQUENCES**

a) Calibration of O(100) millions channels and signal stability (we want same response for same collision)

b) Capability to make zero suppress "on site" (we don't want to read empty pixel)

c) Keep S/N ≥ 10 at MIP level and coherent noise under control (noise , radio/TV , telephone, ground loop, etc… )

d) Multiplexing for the quantity of signal line out (we don't want to have 100M cables)

e) Power management due to large number of channels (we don't want to burn our electronics readout)

f) KEEP the COST UNDER CONTROL (we want an affordable cost)

g) Do we know how to build a self-supporting structure tungsten-CFi with active cooling ? (R&D at IN2P3)

h) …..

Les prototypes doivent nous permettre de répondre a ces questions

Et à la question essentielle

Ce type de ECAL est-il adapter et faisable pour une Higgs Factory ,

quelque soit l'accélérateur !!!

# COMMENT

Exemple de R&D d'engineering sur le cooling pour un accélérateur circulaiure

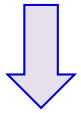
## This ECAL for CIRCULAR ACCELERATOR

But which level of granularity can be afforded without powerpulsing ?

- For physics, the smaller is the best (it continue to improve largely even for $S_{Pixel}$<<Rm)
  BUT for the electronics cost and cooling , … there is some limits

- Readout every 25 ns; no power pulsing
  readout frequency versus ILC x **14** (350 ns to 25 ns)
  conso/cell = 2.8 mW ( Analogic part SKIROC2 without PP) +
  2,1 mW (=0,15 x**14** for digital part with readout every 25ns)
  ---
  = 5mW …. Propose to use 10 mW/channel (including a safety factor of 2)

- From CMS upgrade project-**HGCAL** , active cooling system can be stabilized in temperature
  for about 100W/layer, with fluid running in tube inside cooper plate (Rm not so good than ILC… but)



Taking into account the choosen layer size (= 150x20 cm²) and the 100W
The cooling can afford pixel size of about 0.6x0.6 cm² !!! We have it

# QUI

Si un groupe de labo de l'IN2P3 propose ce type de détecteur,
Il faut que cette proposition soit sérieuse et crédible !!

Il y a **nécessité d'un démonstrateur et d'un soutien fort de l'institut**

Pour rappel, l'IN2P3 est vu dans le monde comme le lieu
de l'expertise dans ce type de calorimètre !!!!

**MAIS**

La nature a horreur du vide !!!

IL y a des labos travaillant sur les ECAL scintillateur (Japon, Chine, USA)
ou sur IDEA (Italie, USA) ou sur des cristaux (CERN,USA)

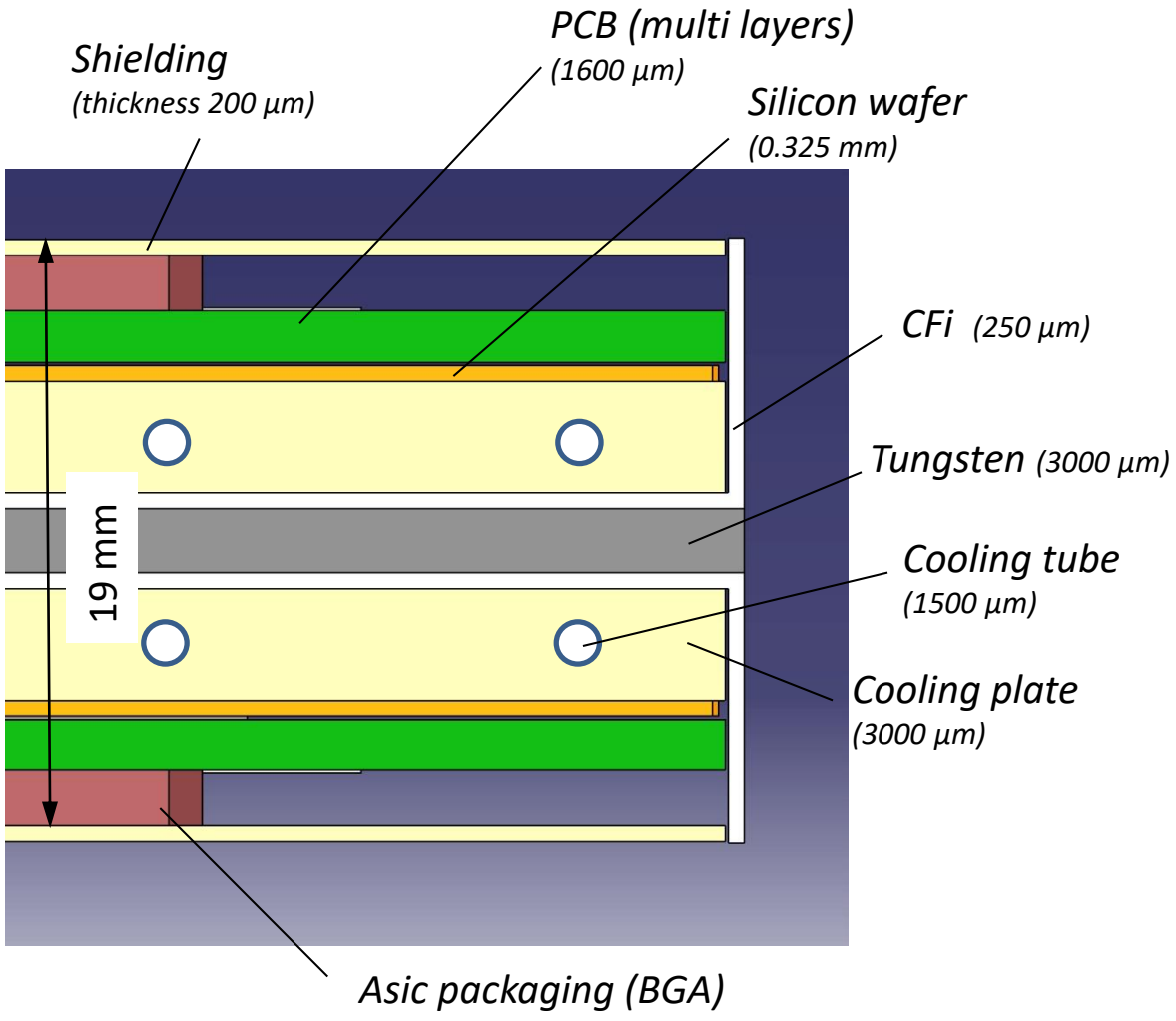
Maintenir notre position , ce n'est pas facile ,
vu le soutien technique et jeune physicien

Voir présentation de Roman Poeschl

# Possible cross section of the ECAL with active cooling (based on CMS study for HGCAL)

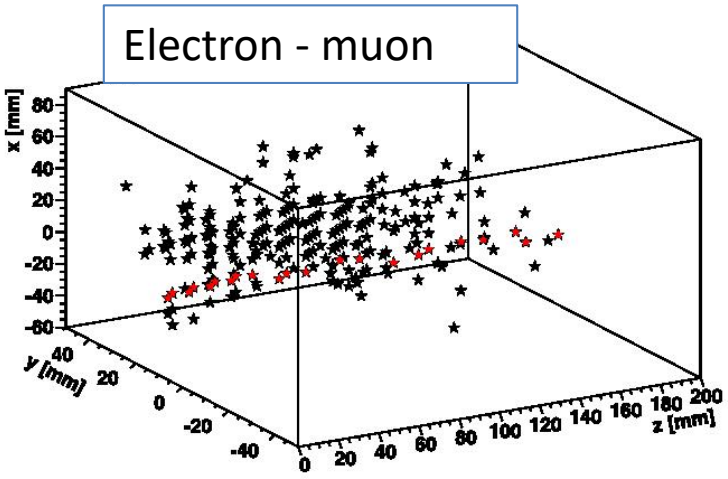
**About 8.7 mm/layer**

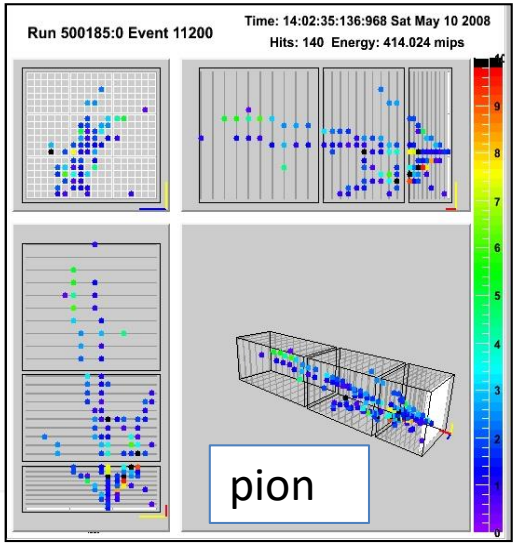
$R_M^{eff}$= 2.4 cm(2cm in CALICE-ILD)
Total thickness for 23 X0, 30 layers is 26 cm.

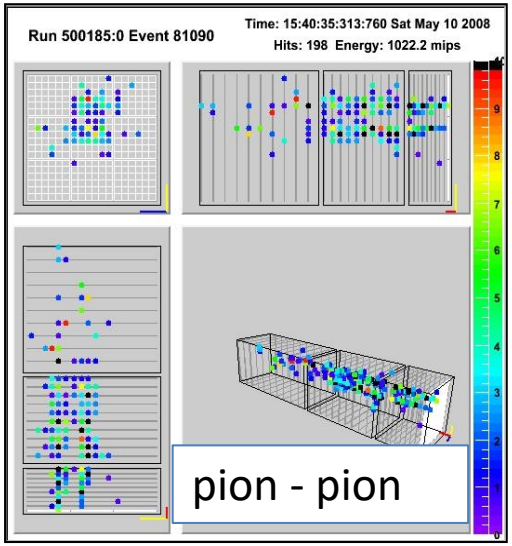


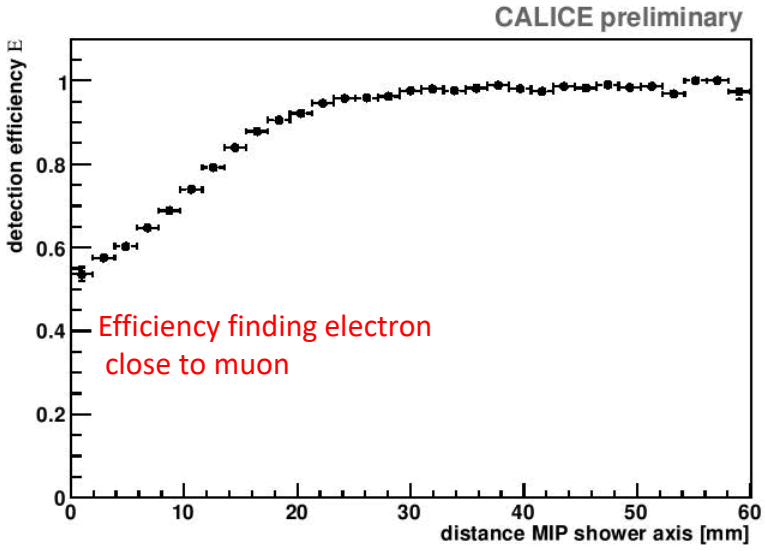
# BACKUP

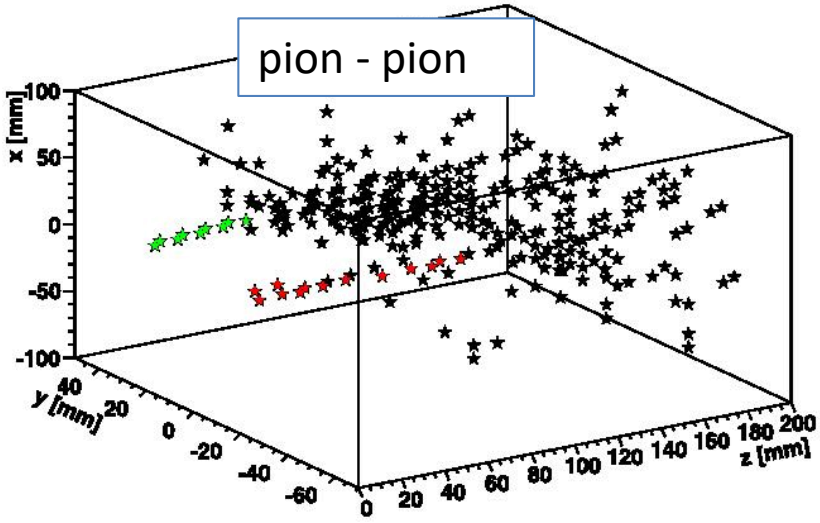
# The tests of the camera




Quantitative test has been published by CALICE (test of PANDORA PFA with TB data)

## Scintillator or silicon ?

- Stability
- Capability to go down to 0.5x0.5 cm²
- Good S/N at MIP level
- VERY good uniformity (guarding vs uniformity in strip or tile)
- Cost …

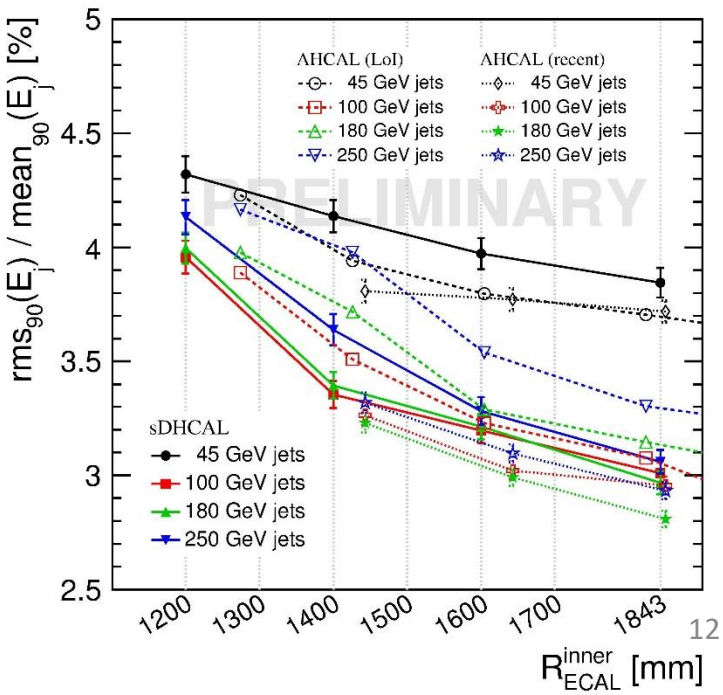
Today price is about **2.0-3.0 €/cm²** for silicon PIN diodes
If you include the scintillator, fibers, monitoring system and SiPM the price is marginally different from silicon PIN

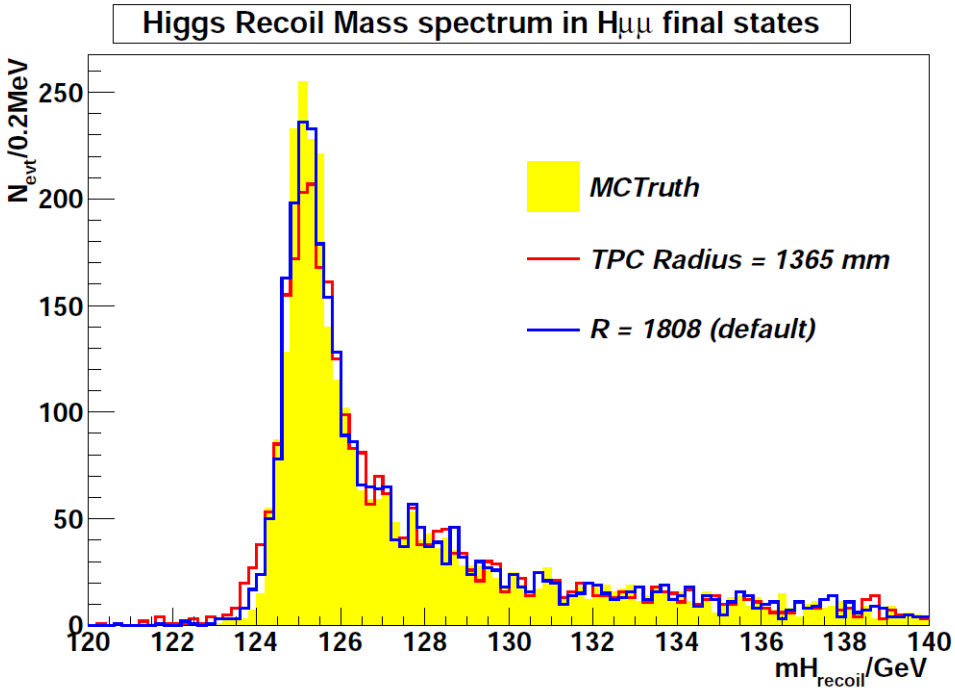
**HOWEVER, about the overall detector cost**
It depends of the ECAL barrel radius and length.
For the same physics(jet, tau, etc..) performances, a smaller detector with smaller pixel could do the job

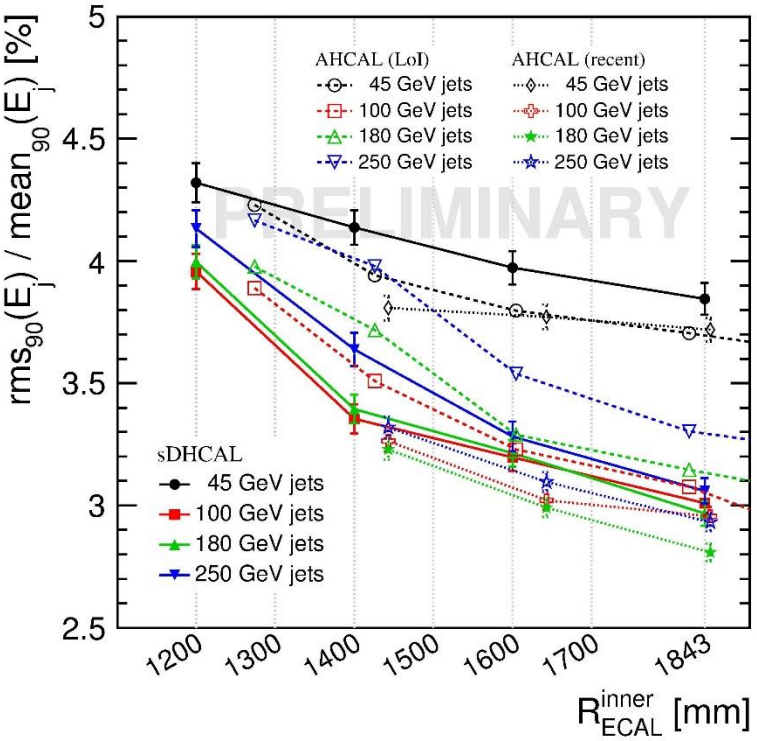
Smaller detector ⇒
smaller cavern, smaller Yoke, smaller return yoke, etc… **COST !!**

**CONCLUSION**

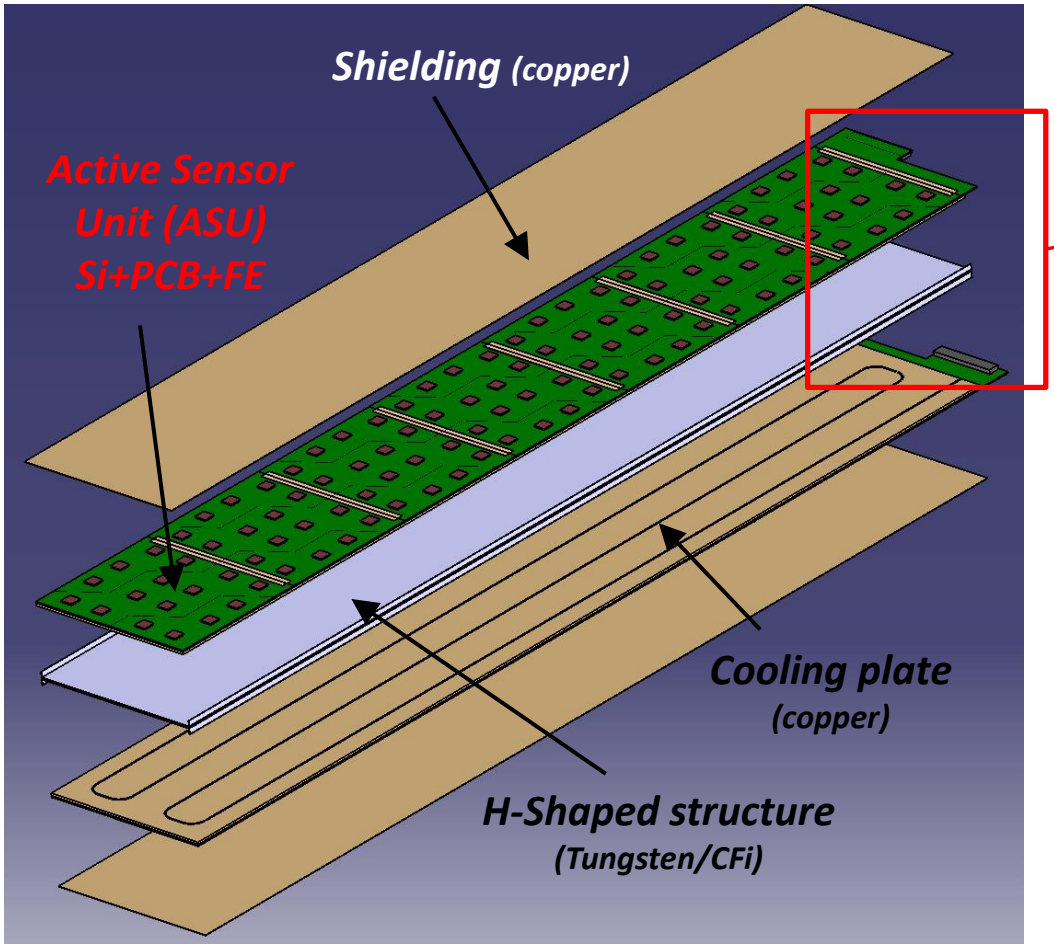
**Small pixels, small radius**
**OR**
**Larger pixels (scintillator), larger radius**
**…**
**SID , ILD ===== same detector cost**

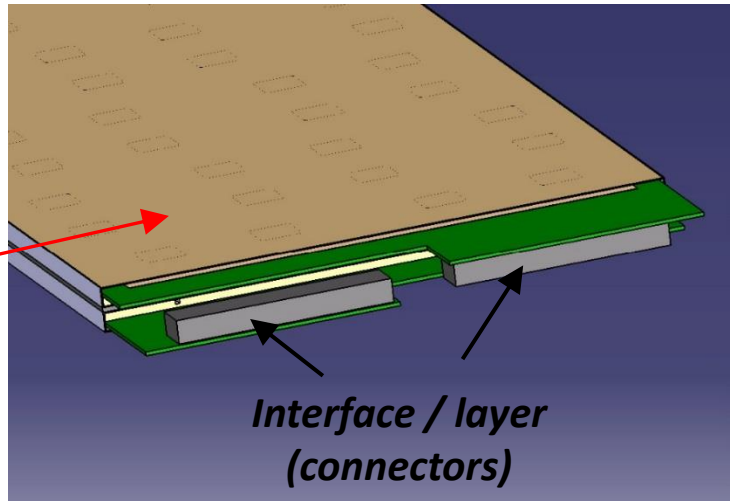



Higgs Recoil Mass spectrum in Hμμ final states
N_evt/0.2MeV
MCTruth
TPC Radius = 1365 mm
R = 1808 (default)
mH_recoil/GeV

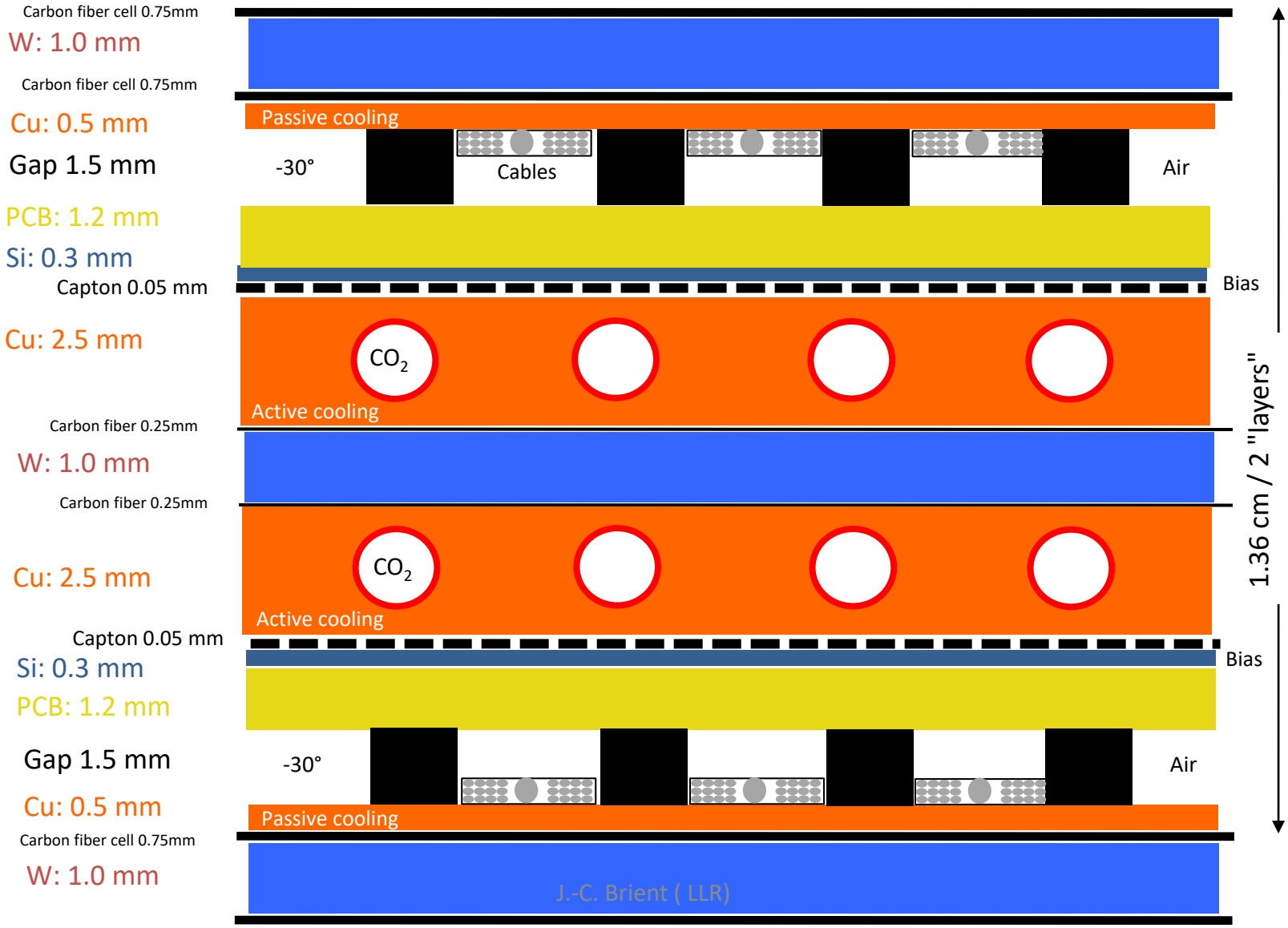

AHCAL (LoI)
AHCAL (recent)
45 GeV jets
100 GeV jets
180 GeV jets
250 GeV jets
PRELIMINARY
sDHCAL
rms90(Ej) / mean90(Ej) [%]
R^inner_ECAL [mm]

# Detector SLAB (exploded view)



# Front of ECAL – Shower start



# COMMENT

Donc, partons de l'hypothèse
que c'est bien un calo optimisant les performances PFA
C'est à dire un calo ultragranulaire : **CONSEQUENCES**

a) Calibration of O(100) millions channels and signal stability (we want same response for same collision)

b) Capability to make zero suppress "on site" (we don't want to read empty pixel)

c) Keep S/N ≥ 10 at MIP level and coherent noise under control (noise , radio/TV , telephone, ground loop, etc… )

d) Multiplexing for the quantity of signal line out (we don't want to have 100M cables)

e) Power management due to large number of channels (we don't want to burn our electronics readout)

f) KEEP the COST UNDER CONTROL (we want an affordable cost)

A set of answers to be verified by demonstrator

a) Choose stable device (silicon) or control & monitor the signal stability (Scintillator)

b) ADC& digital memory in readout chip, close to active layer. Read memories at each end of bunch train

c) i.e. Silicon PIN diodes …. AC/DC coupling , ground loop …

d) Large number of Channels/VFE ASIC… (KPIX, SKIROC), but only few readout line

e) Power pulsing (thanks to machine structure) → reduced the power to dissipate… no cooling inside

f) Reduce the overall surface or use lower cost active device (scintillator)

BUT warning versus point a) and c) . 10 years contacts with producers, defining wafers design which reduce the cost