Silicon Detector R&D for IDEA

Manuel Rolo (INFN),

on behalf of the **IDEA Community**

and on behalf of the **ARCADIA Collaboration.**

The First Joint FCC - France & Italy Workshop on Higgs, Top, EW, HF and SM physics

21 – 23 Nov 2022

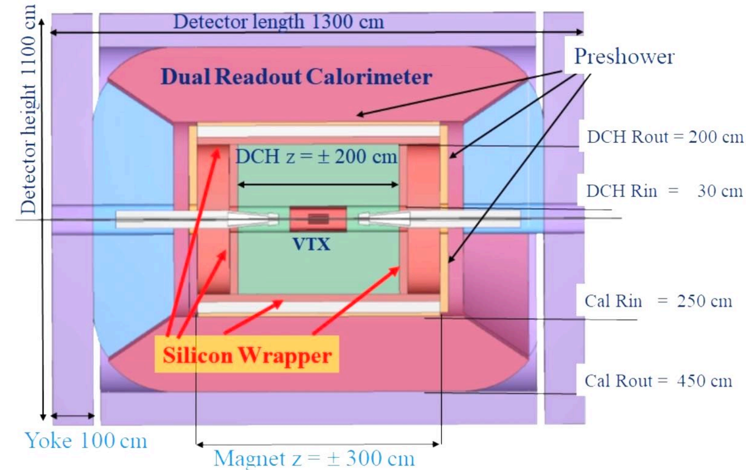
IP2I Lyon (FR)

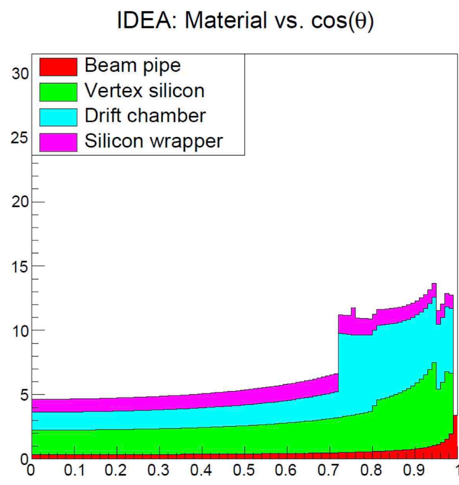
IDEA Detector: proposal for FCC - ee

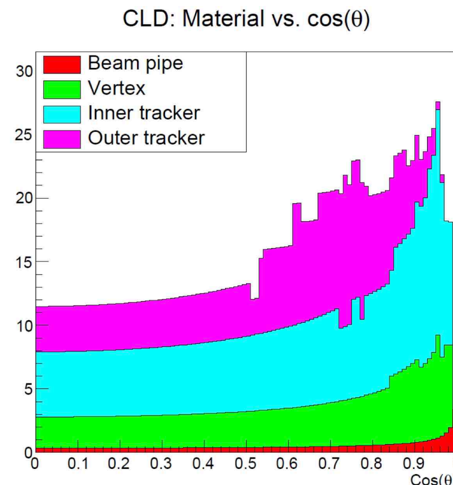
- an "**I**nnovative **D**etector for **E**lectron-Positron **A**ccelerators",

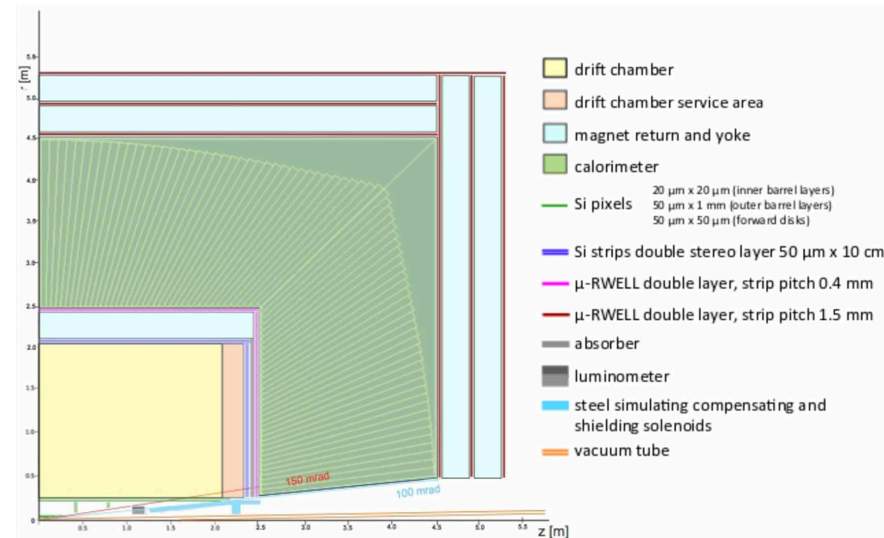
inspired on R&D "4th detector concept" for ILC (DREAM/RD52)

- ultra-light drift chamber wrapped by silicon microstrip layer
- dual-readout calorimeter and thin, low-mass superconducting solenoid coil
- **MAPS-based silicon pixel vertex detector and silicon tracker**









Silicon Detector R&D for IDEA: Outline

- an "**I**nnovative **D**etector for **E**lectron-Positron **A**ccelerators", inspired on R&D "4th detector concept" for ILC (DREAM/RD52)
- ultra-light drift chamber wrapped by silicon microstrip layer
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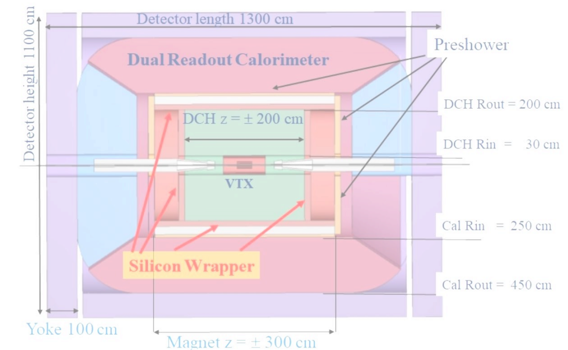
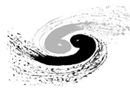


MAPS-based silicon pixel vertex detector and silicon tracker

- **ATLASPix3** HV-CMOS: multi-chip module assembly and system integration
- **ARCADIA** CMOS FD-MAPS: design, production and characterisation platform
- Vertex detector mechanical and integration: **Fabrizio Palla**

17:00 — **Vertex detector study for its integration in the IR**
Room 3

ATLASPix3 KIT + China + UK + INFN Collaboration


Institute of High Energy Physics
Chinese Academy of Sciences

Karlsruhe Institute of Technology

Istituto Nazionale di Fisica Nucleare
MILANO
PISA
TORINO

The University Of Sheffield.

山东大学
SHANDONG UNIVERSITY

李政道研究所
Tsung-Dao Lee Institute

上海交通大学
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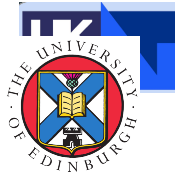

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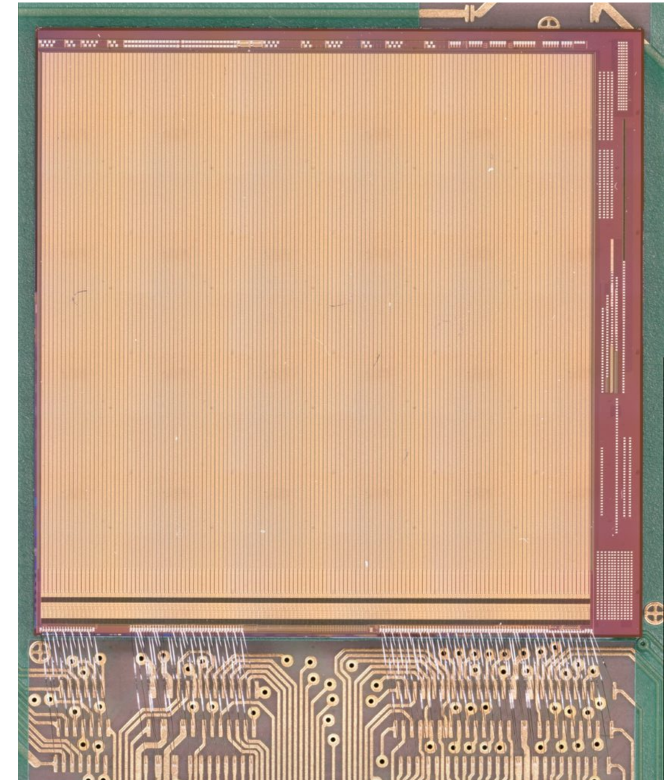
中国科学技术大学
University of Science and Technology of China

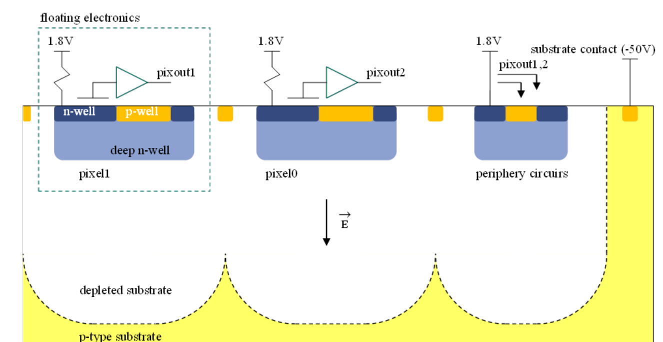
Physics | Lancaster University

Contact: Attilio Andreazza

ATLASPix3 features in a nutshell

- pixel size **50×150 μm²**
  (25×165 μm² small size prototypes delivered)
- up to 1.28 Gbps downlink
- **reticle size 20×21 mm²**
- TSI 180 nm process on 200 Ωcm substrate
- 132 columns of 372 pixels
- digital part of the matrix located on periphery
- 25 ns timestamping
- 8 bits Time-over-Threshold
- both **triggerless** and **triggered** readout possible:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout





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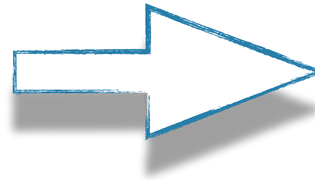
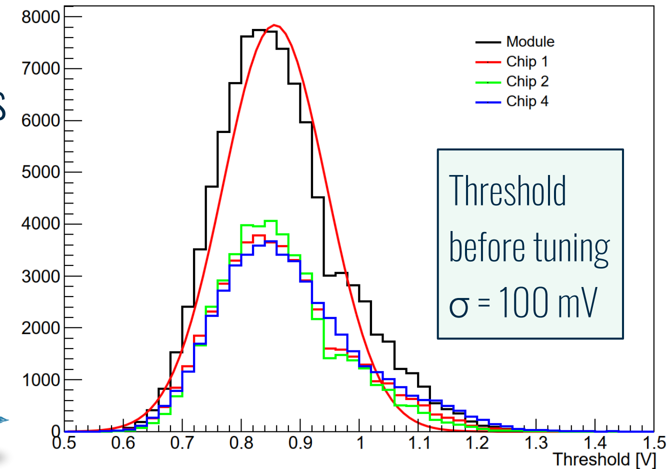
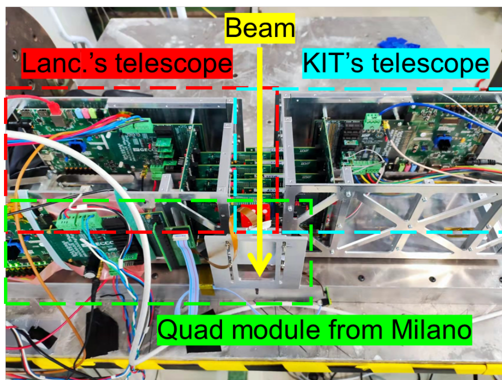
ATLASPix3 quad-chip modules

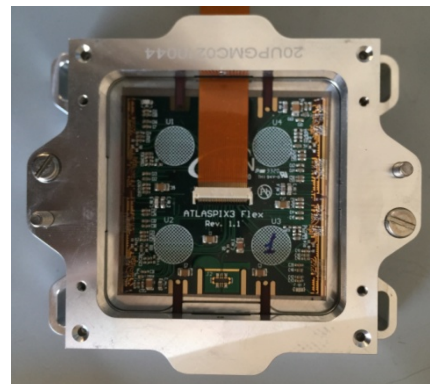
Multi-chip module assembly

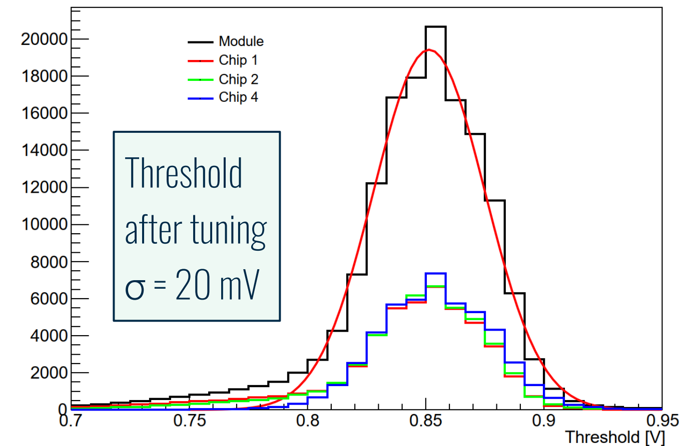
- aggregates electrical services and connection for multiple sensors
  - **critical step for deployment of large size system**
- quad module, inspired by ITk pixels
- implemented interface to readout system
- developed software for module calibration:
  no loss of performance vs. single chip sensors











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ATLASPix3.1 modules

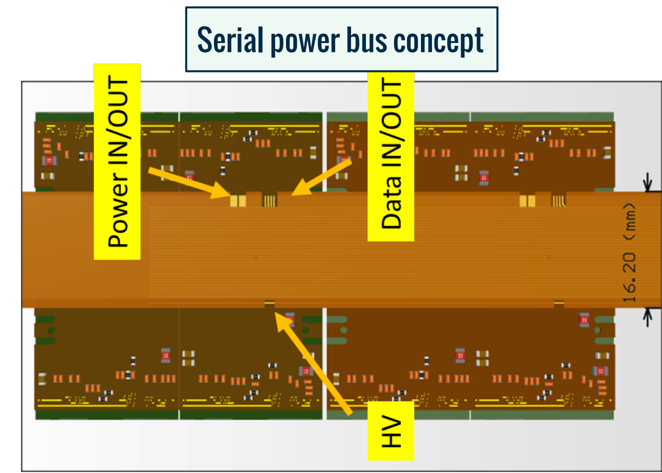
ATLASPix3.1 implement a fix in the constant current power regulators:

- regulator output stable above turn-on
- output power sufficient for digital and analog operation of the chip
- suitable for serial powering chains of chips/modules

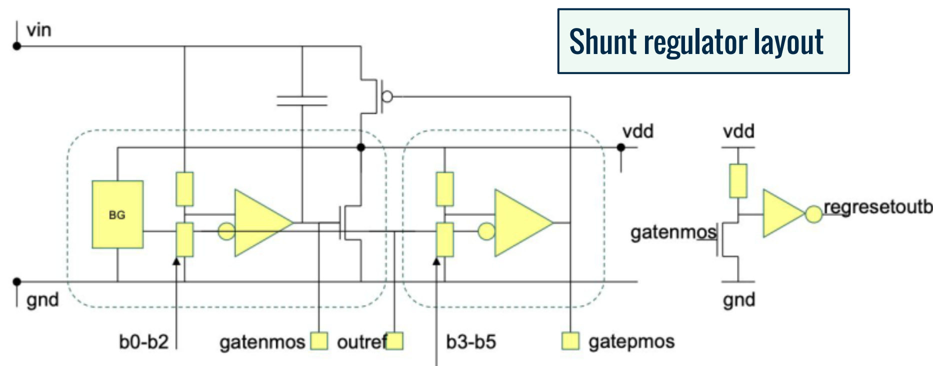
Designing a hybrid exploiting the shunt regulators:

- Single external power source can provide the 6 different voltages required by the chip
- Allows for serial powering, reducing the connections at the system level
- More realistic module for large scale application

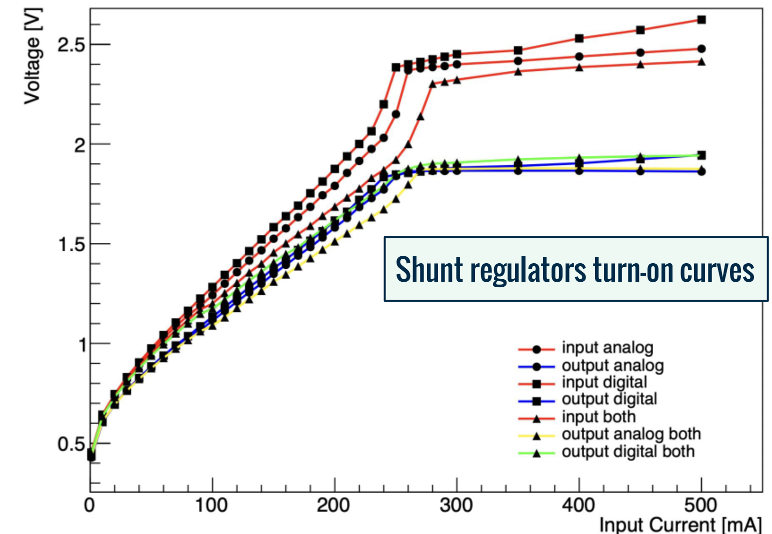
Serial power bus concept



Shunt regulator layout



Shunt regulators turn-on curves



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ATLASPix3: Collaboration Opportunities

INFN

- **DAQ Development**
  - The current laboratory DAQ system does not simply scale for multi-module readout and synchronisation
- **System design for multi-module operation**
  - Conceptual design of a serial power chain biasing and readout
  - Data aggregation to reduce data connections
  - Service routing along mechanical supports (see Fabrizio Palla's talk)
- **Characterization of new sensor developments**
- **Explore other multi-chip aggregation strategies**
  - INFN approach based on ATLAS quads
  - It would be interesting to explore ALICE ITS-like configurations

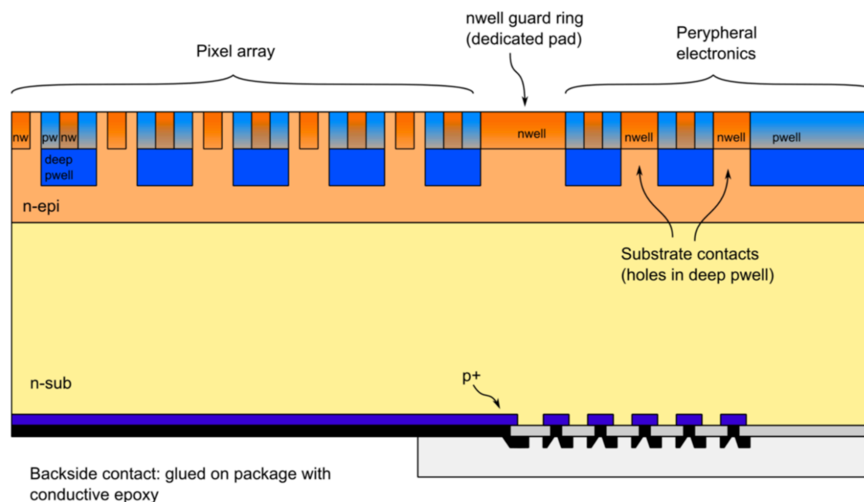
Contact: Attilio Andreazza

ARCADIA DMAPS R&D at INFN

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

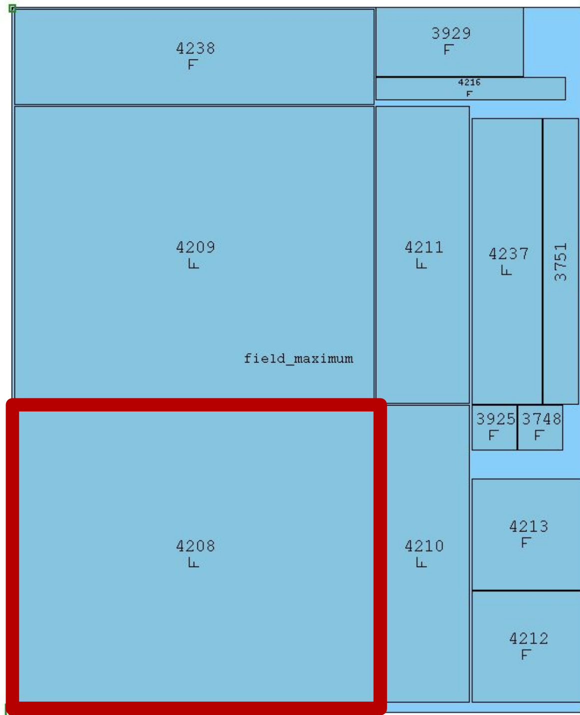
- Active sensor thickness in the range 50 µm to 500 µm or more;
- Operation in full depletion with fast charge collection by drift, small collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry

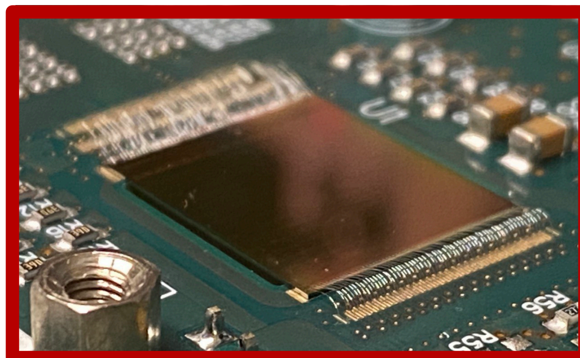


ARCADIA

"Fully Depleted MAPS in 110-nm CMOS Process With 100–300-µm Active Substrate," in IEEE Transactions on Electron Devices, June 2020, doi: 10.1109/TED.2020.2985639.

ARCADIA Technology demonstrators





- ARCADIA-MD1a/b Main Demonstrator
- ARCADIA-miniD (debug)
- ARCADIA-miniD with on-chip LDOs for large-scale yield management
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10µm pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and embedded readout electronics
- (LC2) MATISSE_TIMING: VFE for fast timing (R&D for ALICE3 timing layers)
- (LC3) Small-scale demonstrator of a X-ray multi-photon counter
- (LC3) Wafer splits with timing layer, new R&D towards <<100 ps timing performance: test structures and multi-pixel active demonstrator chip

ARCADIA-MD1: Chip Floorplan

Matrix: 1,28 x 1,28 cm²

Top Padframe
Auxiliary supply, IR Drop Measure

Matrix
512x512 pixels, Double Column arrangement

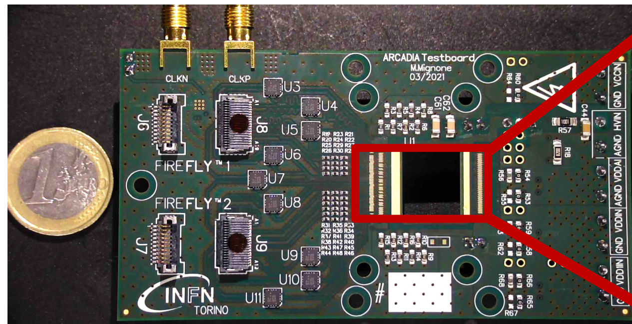
End of Sector (x16)
Reads and Configures 512x32 pixels

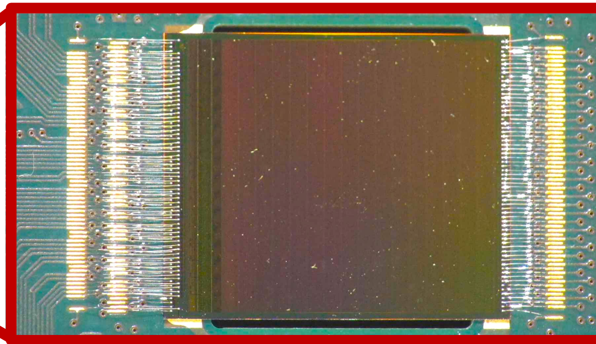
Sector Biasing (x16)
Generates I/V biases for 512x32 pixels

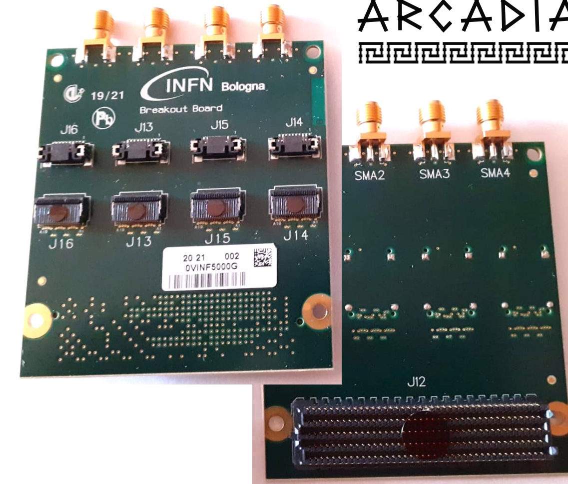
Periphery
SPI, Configuration, 8b10b enc, Serializers

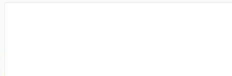
Bottom Padframe
Stacked Power and Signal pads

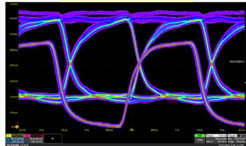
Front-end FEB-MD1 and DAQ

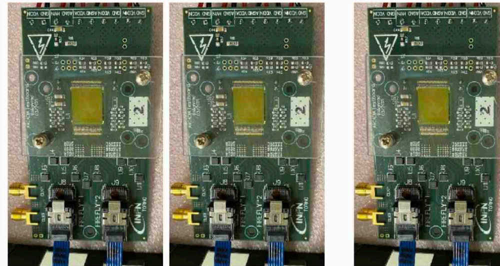


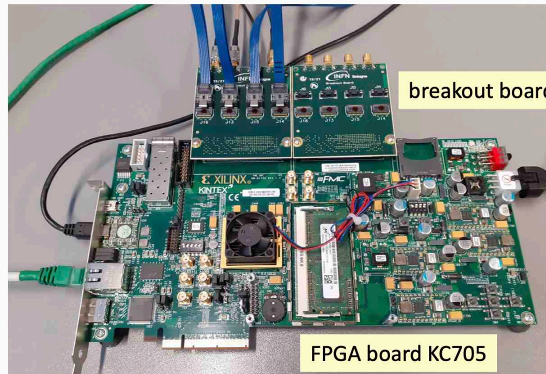








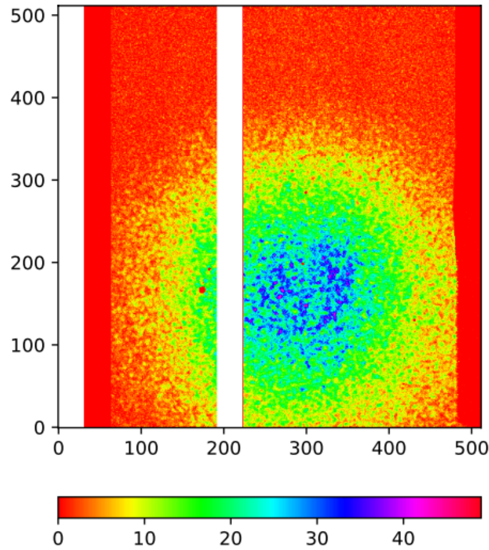




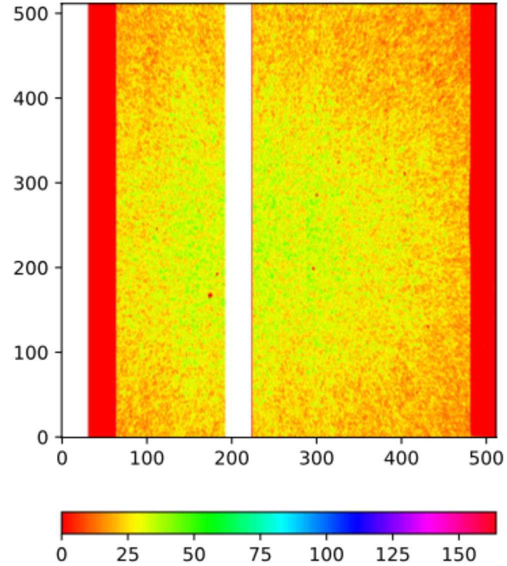
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Connection to external low jitter Clock (via SMA connectors)
- Bias to the DMAPS backside or (wirebonded) to top pads
- Independent LDOs for IO Buffers, Analog Core, Digital Core
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board

MD1 characterisation data: particles

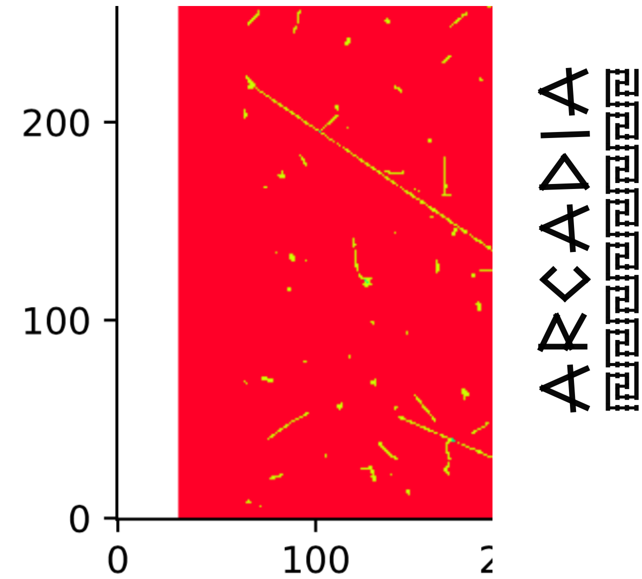
^{241}Am



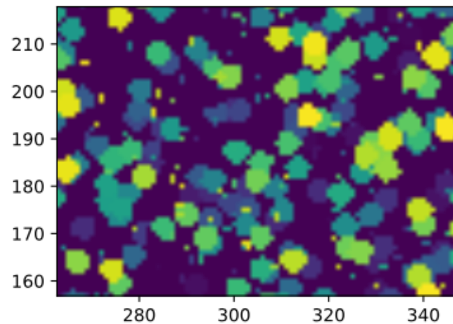
^{90}Sr



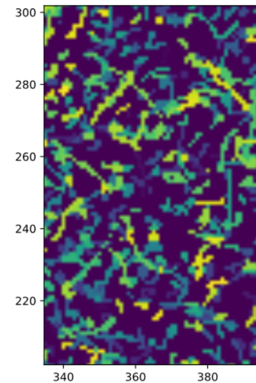
Few cosmic tracks (Tilted sensor)

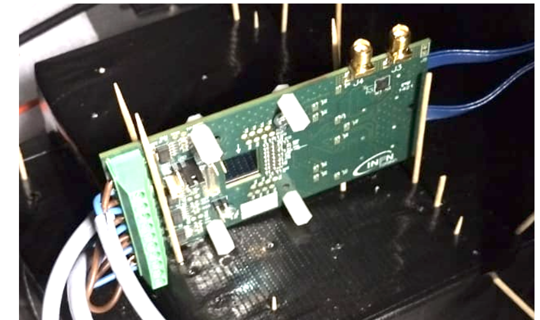


Few events (zoom)

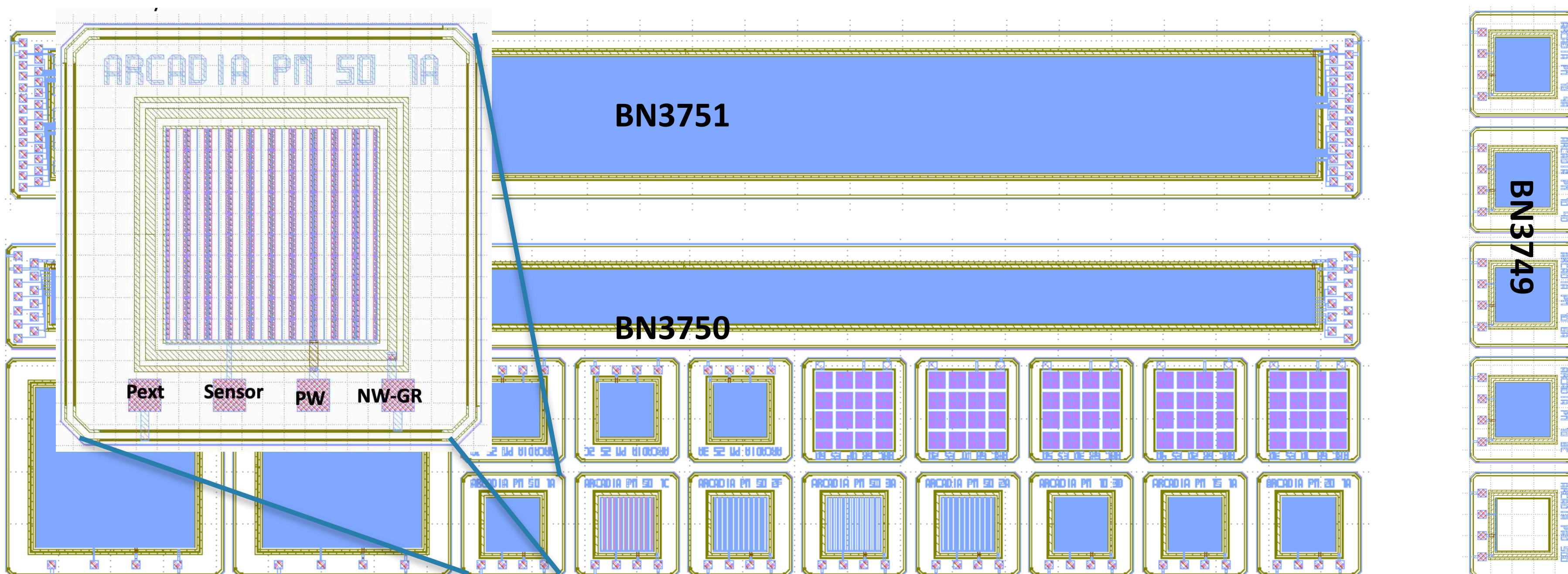


Few events (zoom)





Pixel/Strip Test Structures



pixels come in different flavours:

- Pseudo-Matrices of 1x1 and 2x2 mm^2
- 50 µm (5 variants)
- 25 µm (3 variants)
- 10 µm (6 variants)

and strips as well:

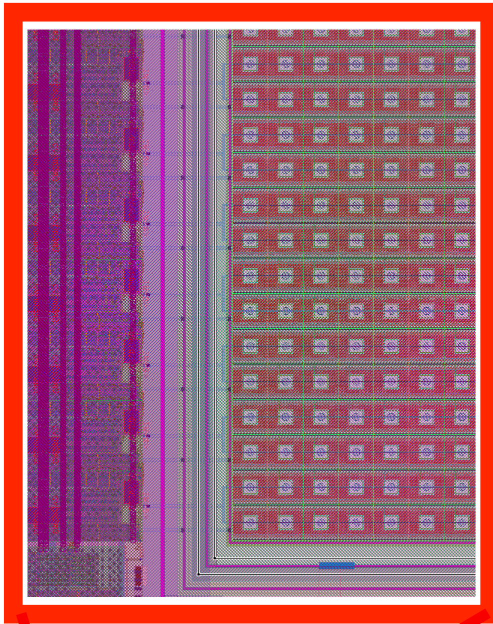
- 25 µm pitch pixelated + 25 µm continuous (10+10) [2 variants]
- 10 µm pixelated (4 groups of 12 strips connected to pads) [4 variants]

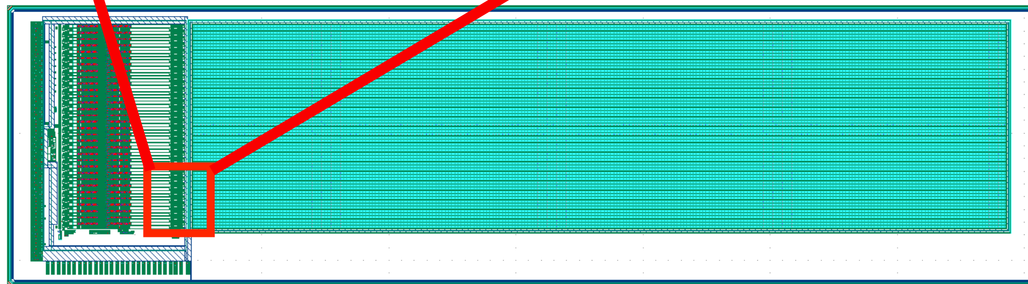
ARCADIA

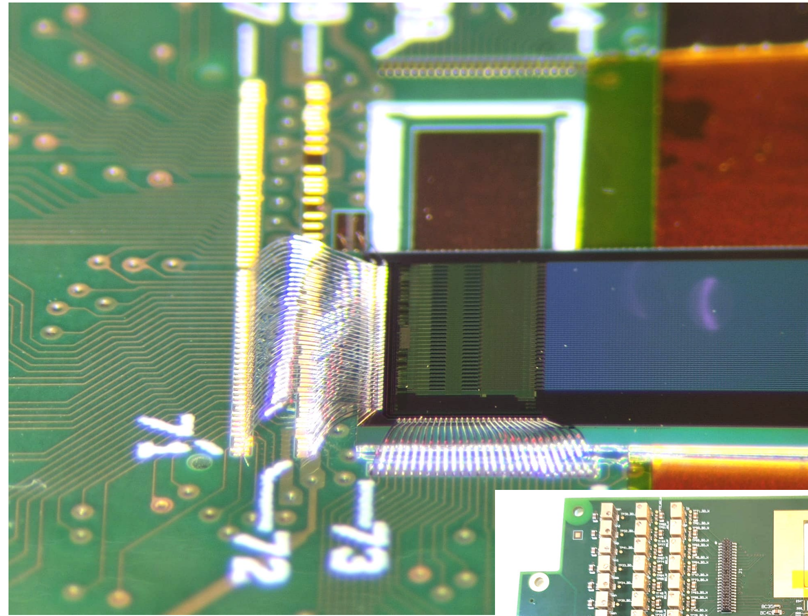
CMOS Embedded Si-strip and readout

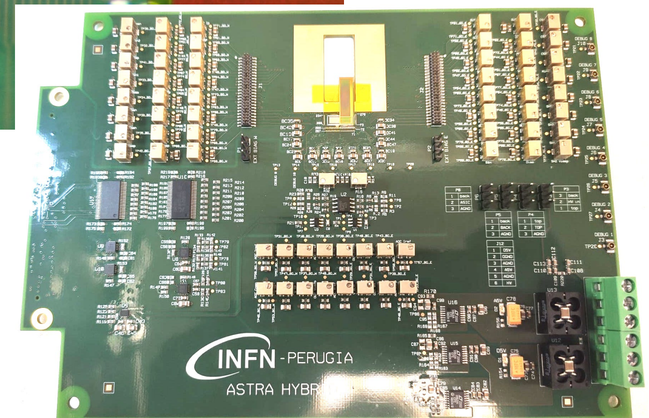
- Design and Production of continuous and "pixelised" strips, range 10 - 100µm pitch
- Proof-of-concept: CMOS monolithic strip block and readout electronics (active sensor area is 12800 × 3200 μm^2)
- Smoke tests OK (analogue power, bias and output baseline) , problems with test board (mfg & components) being solved

Figure: CAD Layout of 32-block of 2x2566 50µm pixelised strips









Fully Depleted Monolithic Active Microstrip Sensors: TCAD Simulation Study of an Innovative Design Concept. Sensors 2021, 21, 1990. https://doi.org/10.3390/s21061990

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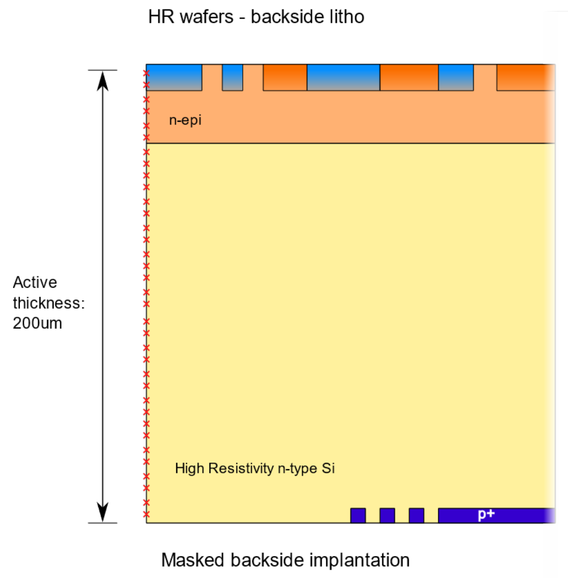
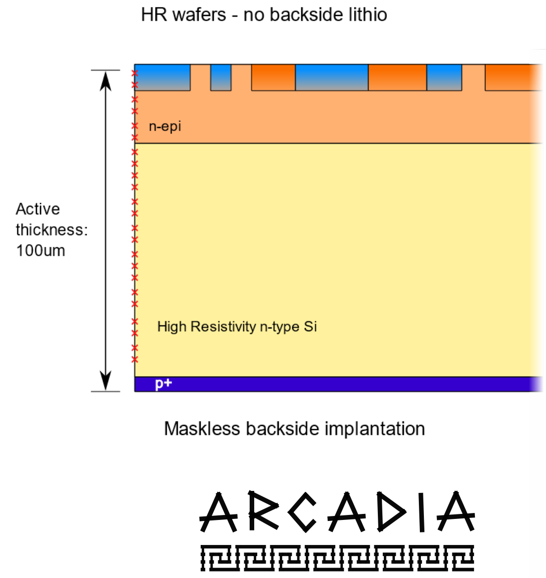
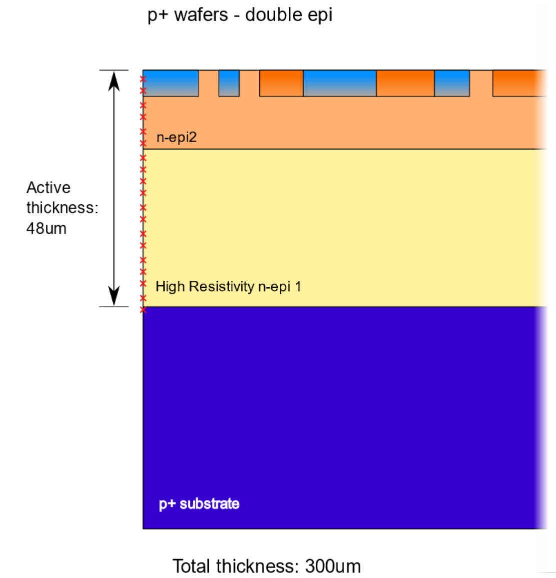
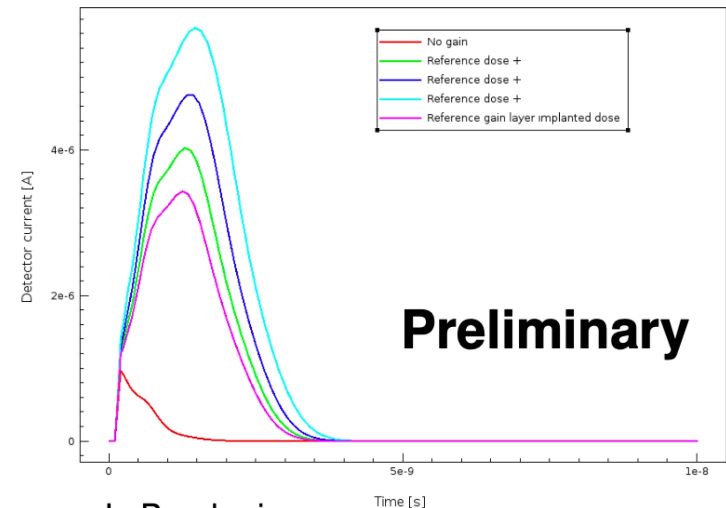
ARCADIA Sensor: wafer splits and new silicon





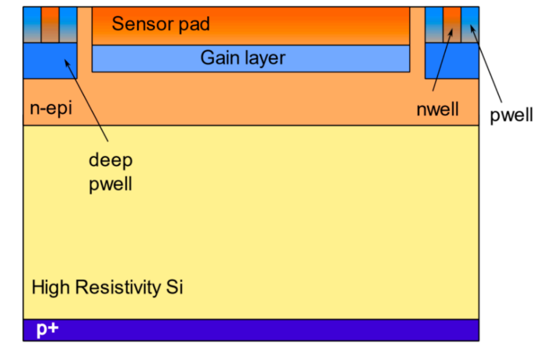


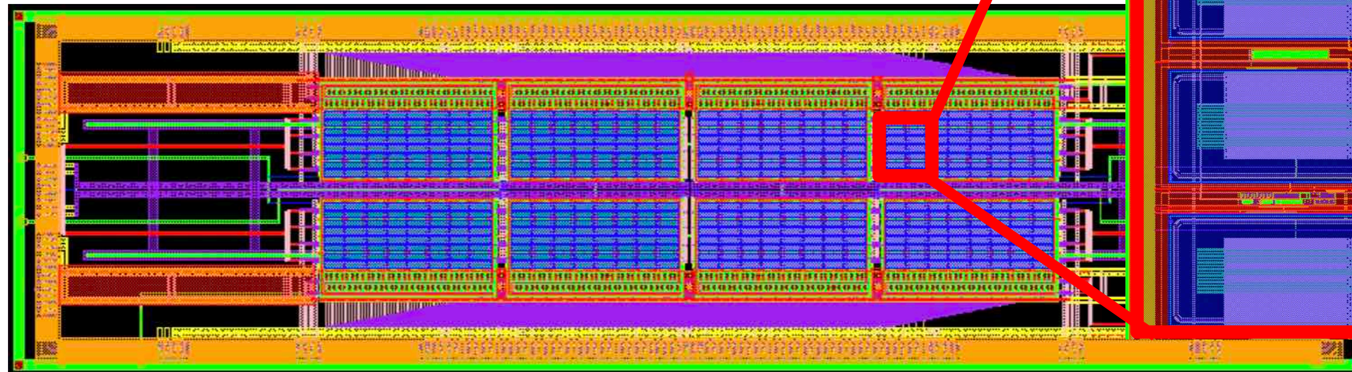
- 23 wafers delivered with process splits on n-epi, substrate type and thickness, lithography on backside;
- low resistivity epi-layer for delayed on-set of punch-through currents;
- preliminary studies show the possibility to add a gain layer (10-20) wit minor modifications to the process;
- fab out of new silicon scheduled end January (2 lots with 42 wafers).

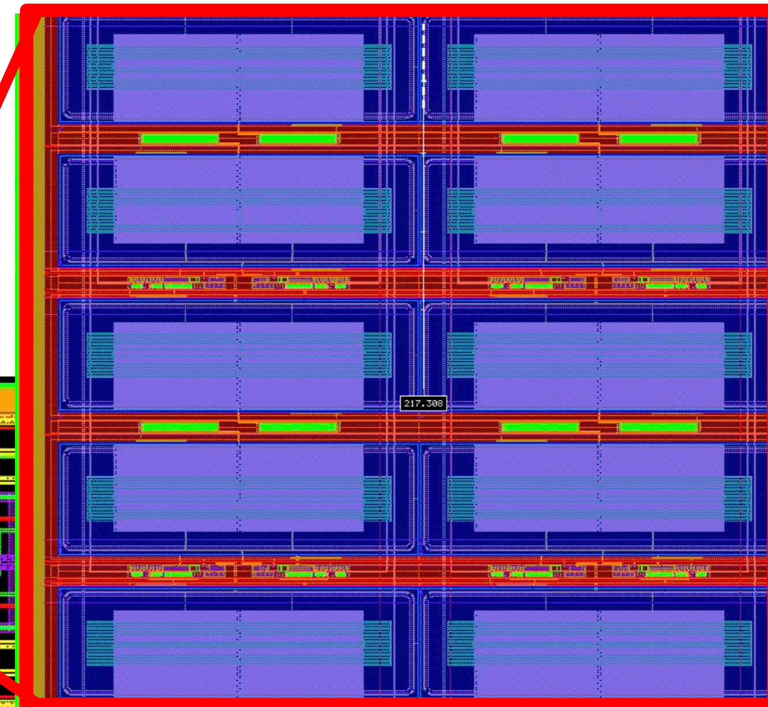


ARCADIA Sensor: R&D for fast timing

- partial lot of HR and p+ wafer splits implement an extra gain layer added to the sensor;
- first small-scale demonstrator 4 x 16 mm^2;
- 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- 250 x 100 μm^2 pixel pads;
- 64 analogue outputs on each side, rolling shutter of single matrix readout;

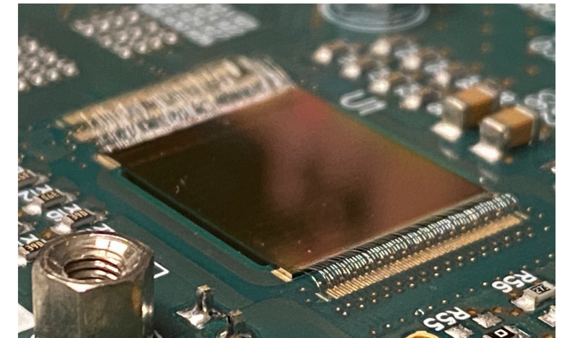






ARCADIA FD-MAPS: Collaboration Opportunities

- **ARCADIA:** CMOS sensor design and fabrication platform with several INFN groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments
- **Collaboration Opportunities**
  - **Joint engineering runs**: third-party involvement for design and technology sharing agreed with foundry, integration flow demonstrated on 3 full single-project wafer productions;
  - **Characterisation** of full-scale prototypes (e-kit available) and sensor test structures, joint beam tests and DAQ future developments.



Merci de votre attention!

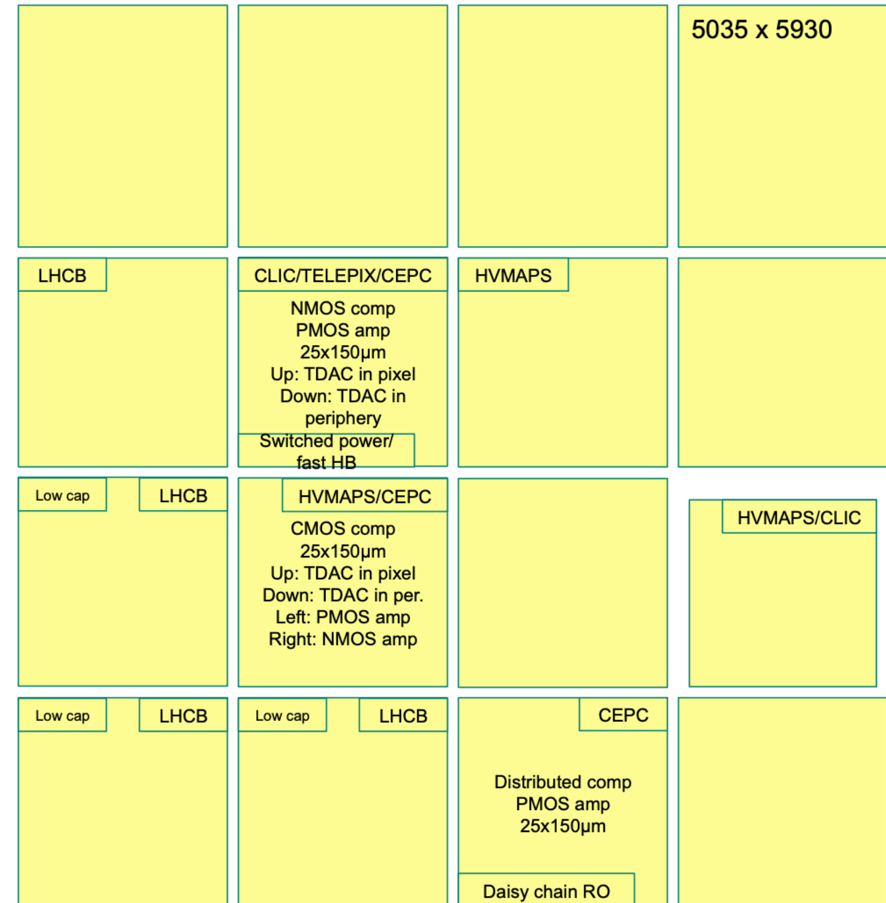
Manuel Rolo (INFN),

on behalf of the **IDEA Community**

and on behalf of the **ARCADIA Collaboration.**

ATLASPix3 ongoing and future developments

- Engineering run developing the ATLASPix3 family
- Design driven by KIT
- Contribution from LHCb Mighty Tracker (scintillating fibre and CMPS MAPS technologies combined), CEPC and other projects
- To test evolutions of ATLASPix3:
  - 25 μm pitch in the bending plane
  - Lower capacitance
  - Amplifier and comparator re-design
  - Electronics in pixel or in periphery
  - Daisy chain readout



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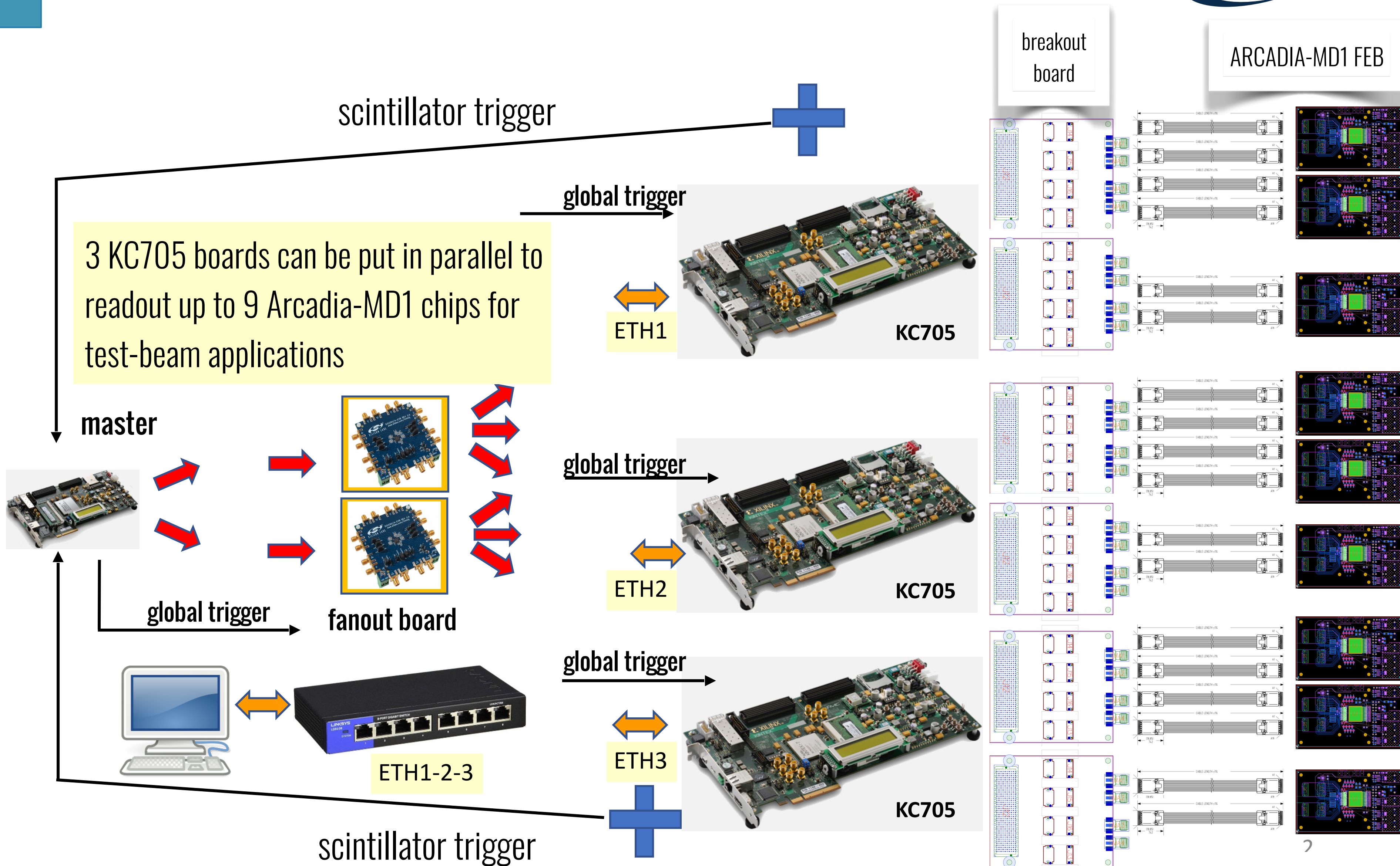
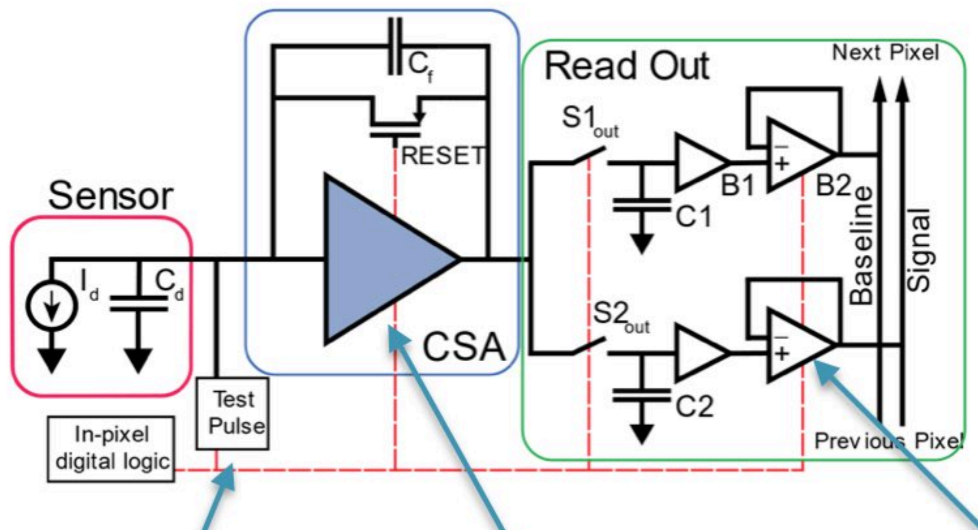
Multi-plane MD1 Telescope Configuration

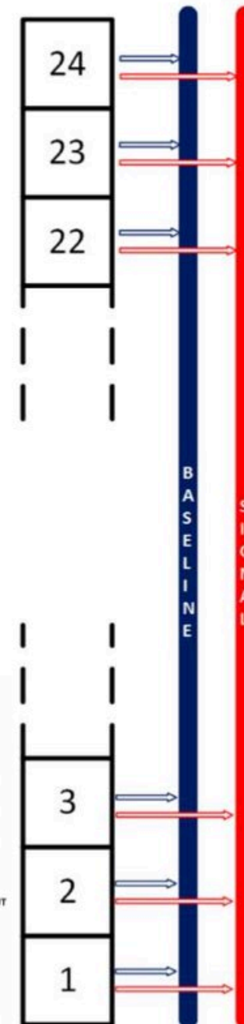


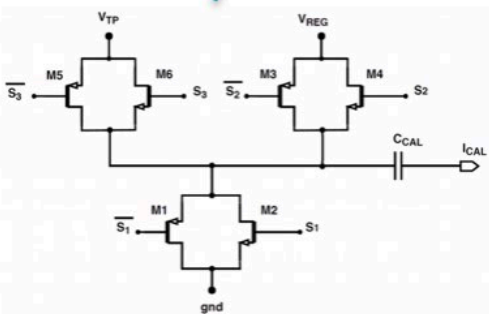
Small-scale demo: MATISSE

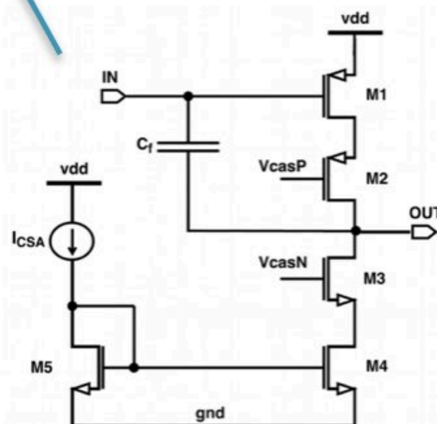
Charge Sensitive Amplifier
With a RESET transistor

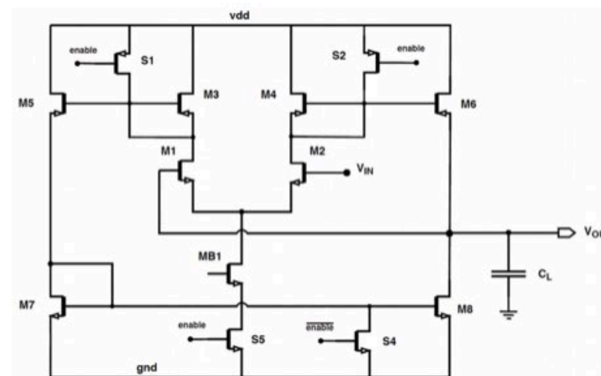
Correlated Double Sampling



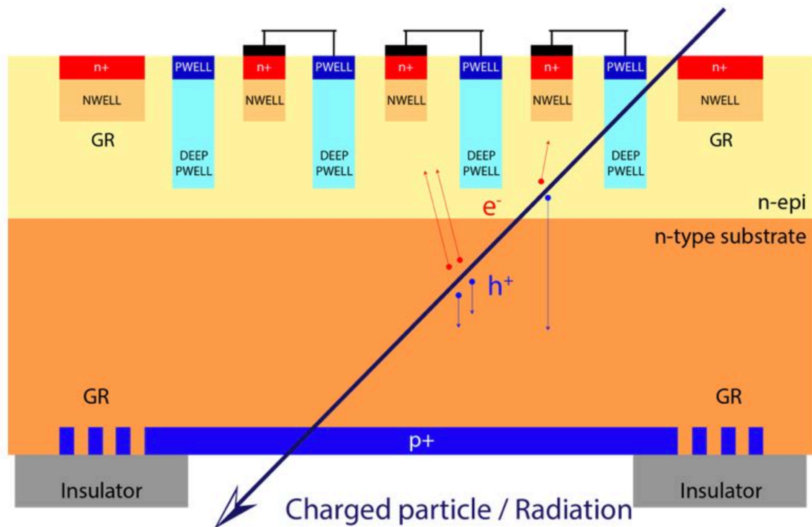


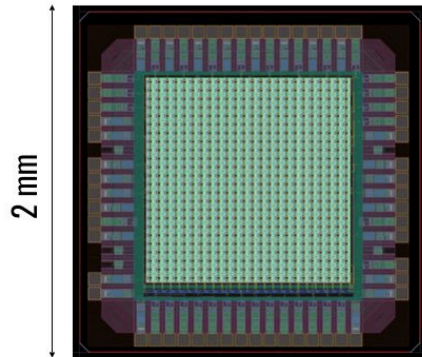




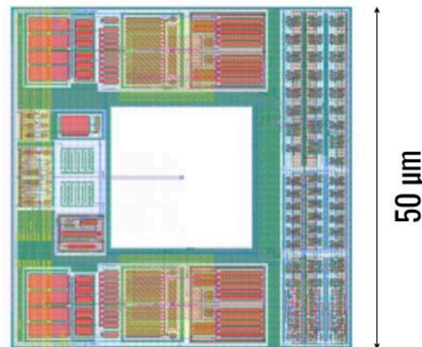


Small-scale demo: SEED MATISSE





MATISSE

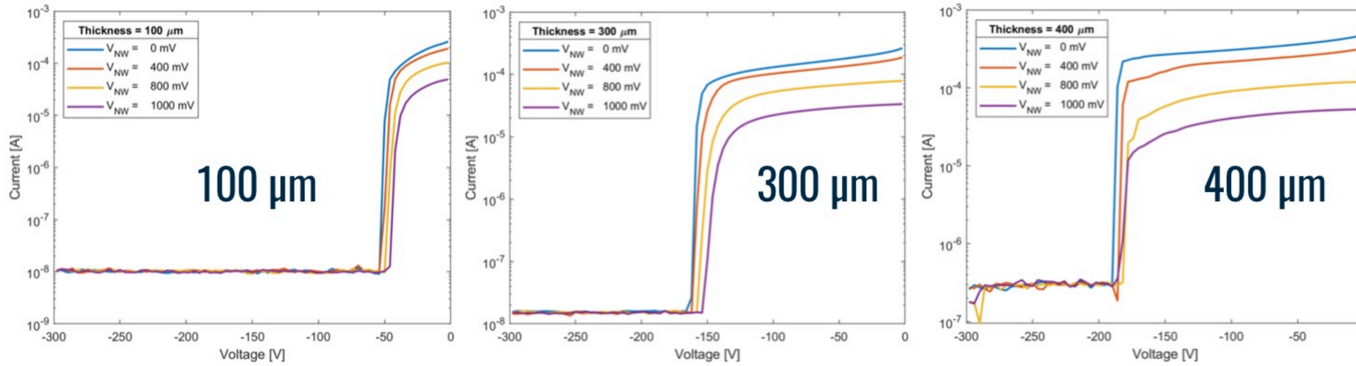


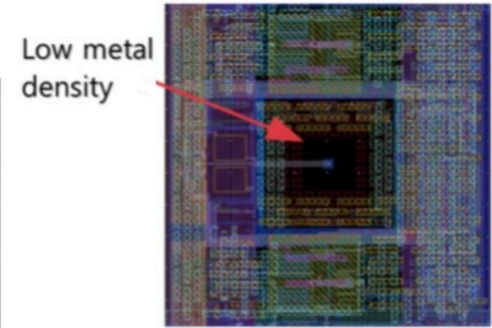
Pixel CAD Layout

PIXEL ELECTRONICS		
	DESIGN SPECs	RESULTS
Technology	CMOS 110 nm	
Voltage Supply	1.2 V	
Measurements	Hit Position Energy Loss	
Number of Channels	24 × 24	
Input Dynamic Range	Up to 24 ke^-	
Sensor Capacitance	~20 fF	
Analog Gain	131 mV/fC	116 mV/fC
CSA Input Common Mode Voltage	> 600 mV	
Local Memories	2 (~70 fF each)	
Noise	$< 100\ e^-$	$\sim 40\ e^-$
Shutter Type	Snapshot	
Readout Type	Correlated Double Sampling Double Sampling	
Readout Speed	Up to 5 MHz	
Other Features	Internal test pulse	

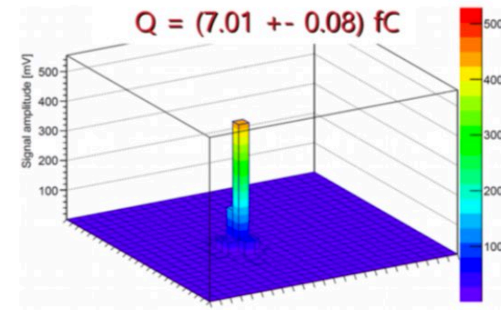
Characterisation with SEED MATISSE

Full depletion studies in 100-300-400 μm prototypes

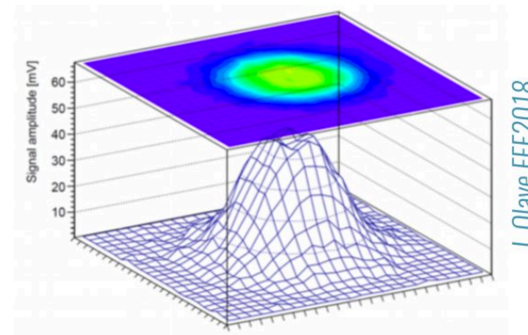




Focused pulse

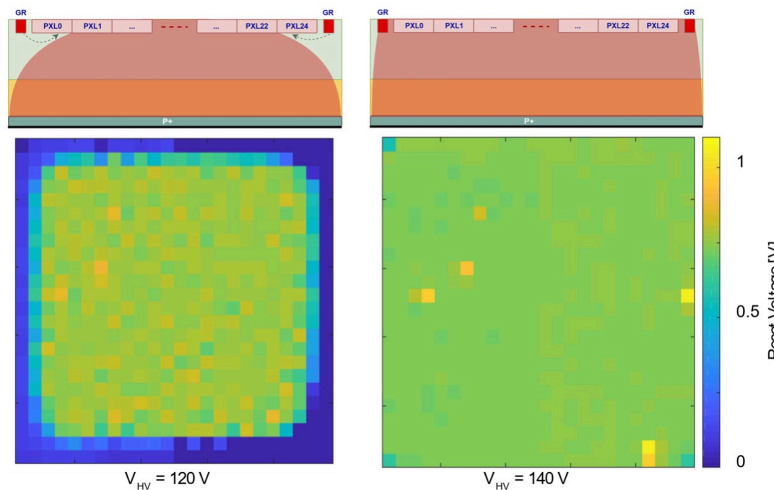


Non focused pulse



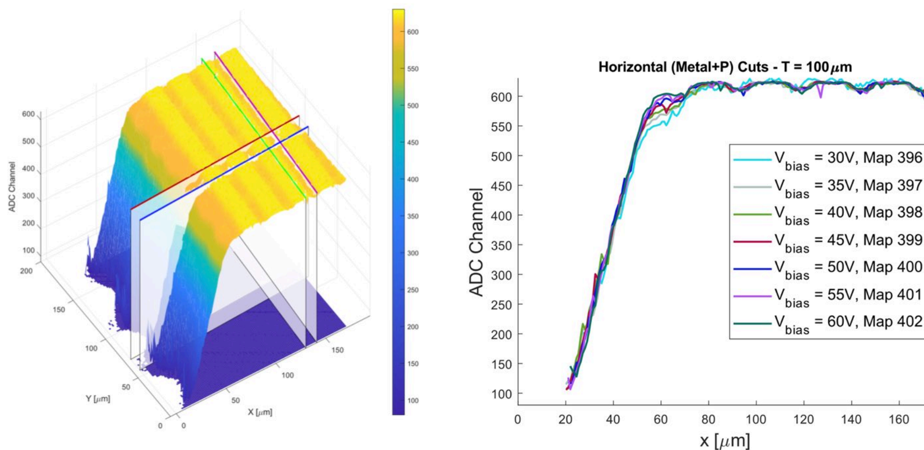
J. Olave FEE2018

Map of pixel reset voltage (MATISSE 24x24 pixel matrix) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.

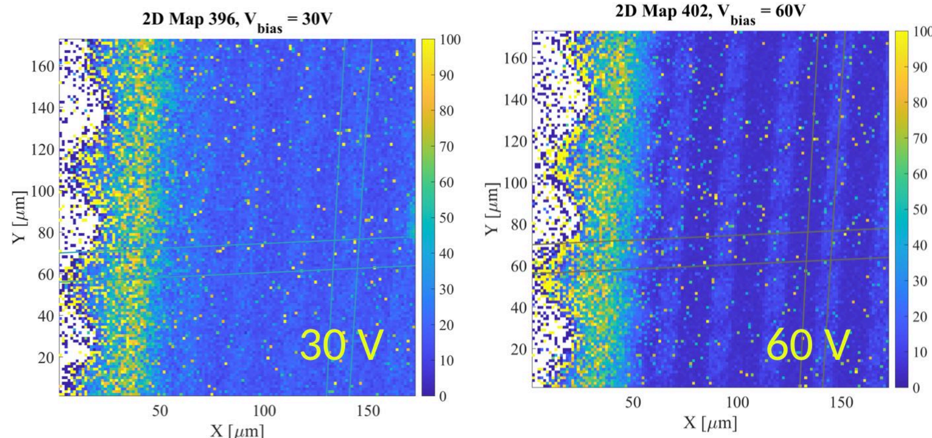


Characterisation with pseudo-matrices

Cuts along the Metal + P and Metal + N lines on the energy map with varying bias voltages show uniform CCE above FD with ~1.7 % loss over metals (100 µm thick)

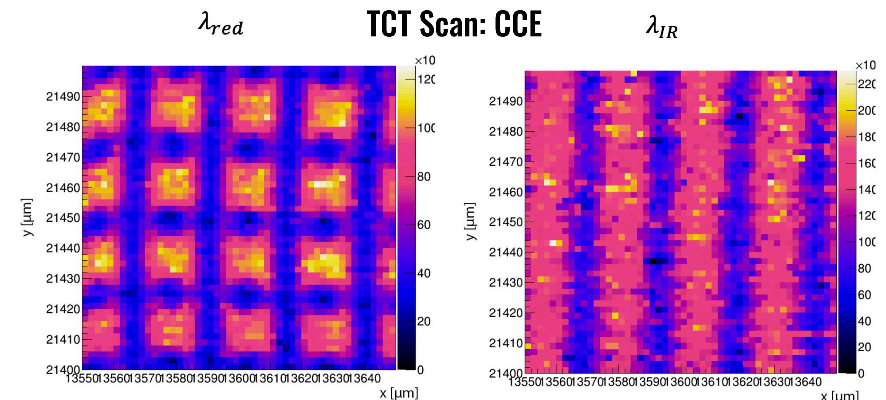


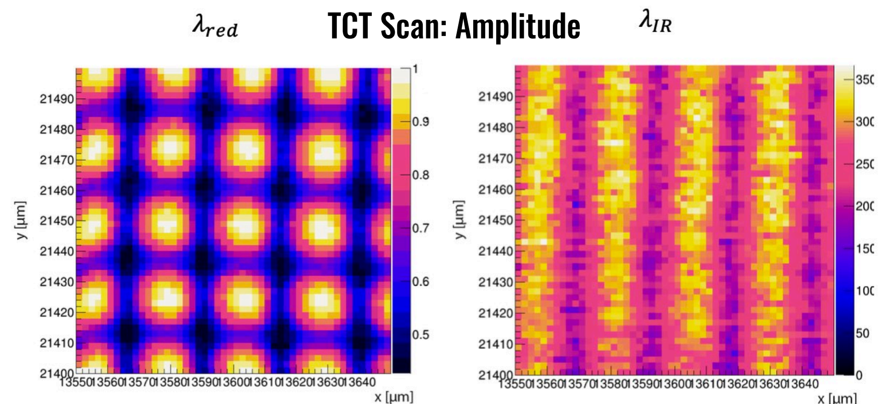
Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.



(RUĐER BOŠKOVIĆ INSTITUTE)* Zagreb, Croatia

- 600 keV to 2 MeV Tandetron
- TANDEM 1-6 MeV proton source
- LASER TCT laboratory

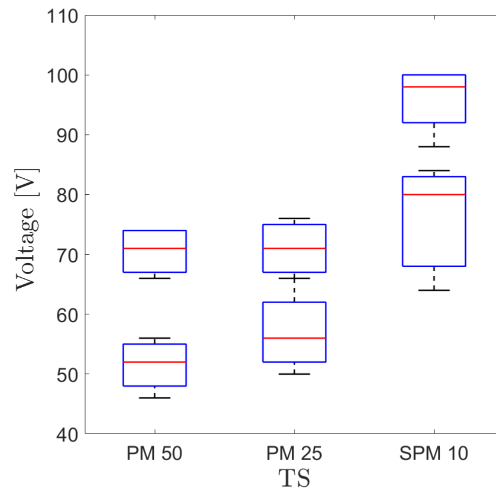


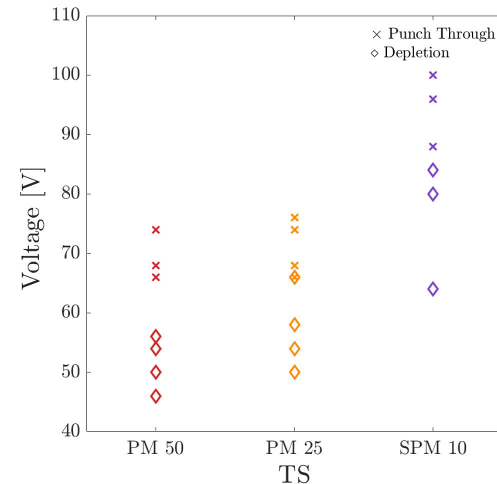


ARCADIA Depletion studies

Group	thickness	Vdepl	Vpt
GROUP 1: wafer #06 and #07 (BSI 8µm n- epi / N-)	200µm	87 – 102	105 – 111
GROUP 2: wafer #02 and #03 (FSI 8µm n- epi / N-)	100µm	20 – 30	36 – 39
GROUP 3: wafer #15 and #16 (BSI 7µm n- epi /N-)	**200µm**	**50 - 66**	**66 - 76**
GROUP 4: wafer #10 and #12 (FSI 7µm n- epi /N-)	100µm	9 – 18	20 – 25
GROUP 5: wafer #20 and #24 (FSI 8µm n-epi 1 40 µm / P+)	300µm	21 – 23	24 – 26
GROUP 6: wafer #22 and #23 (FSI 8µm n-epi 1 40 µm / P+)	100µm	20 – 30	24 – 33

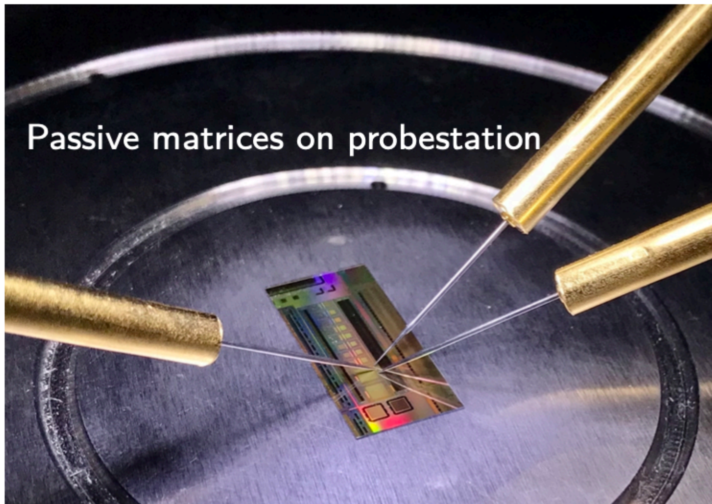
note: V_{depl} and V_{PT} ranges are reported in absolute value. Below: distribution of V_{depl} and V_{PT} for different pixel pitches

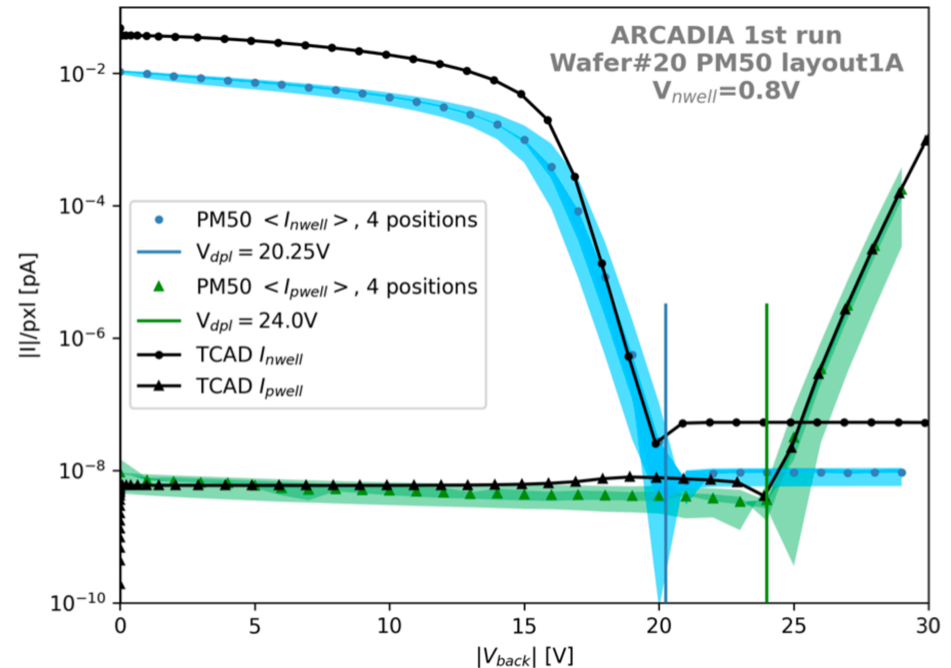


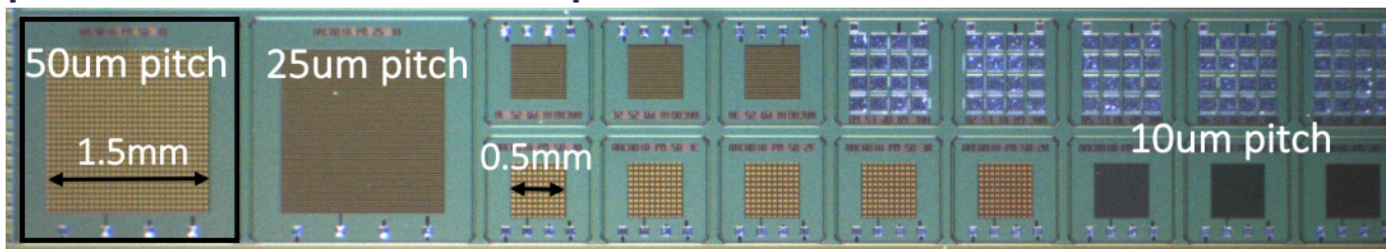


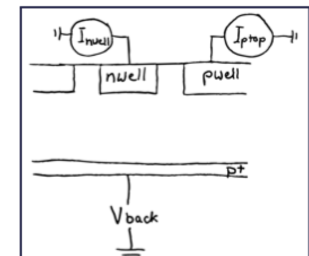
ARCADIA sensor characterisation

IV and CV measurements of test-structures: proven functionality, stable operation at full depletion, and good agreement with TCAD simulations









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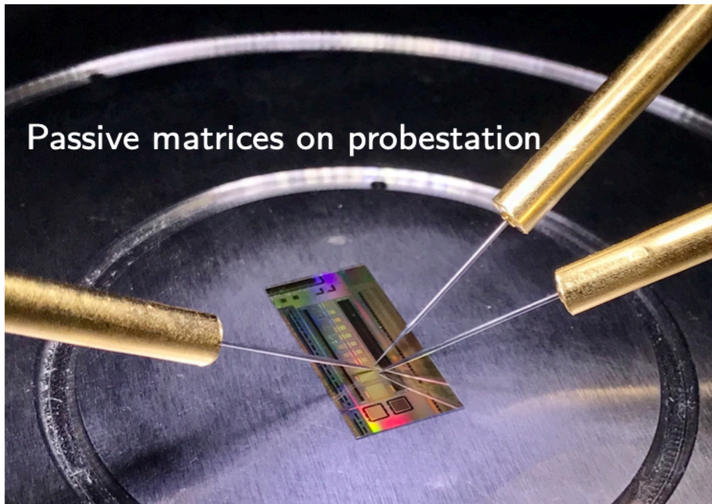
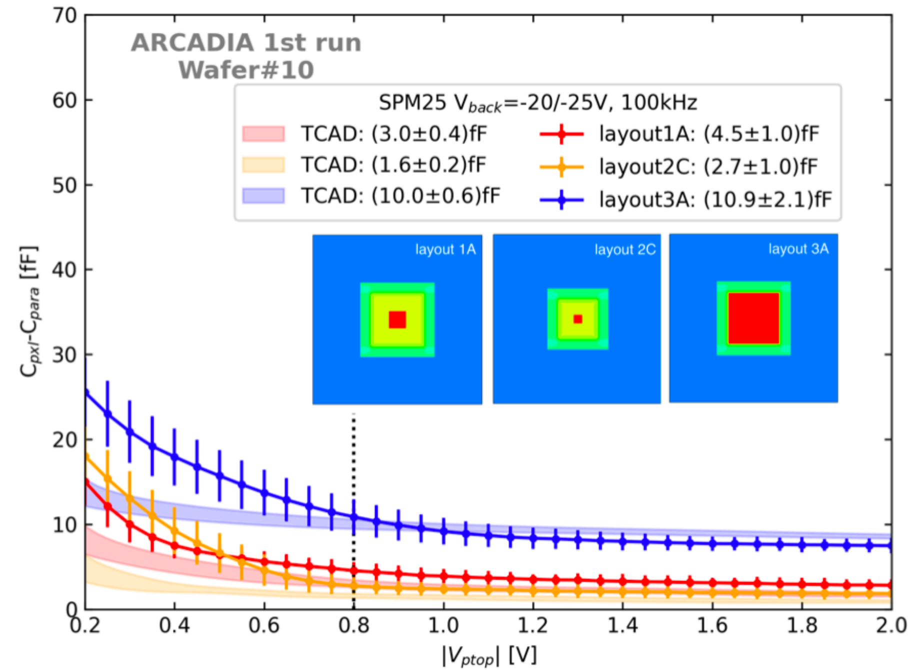
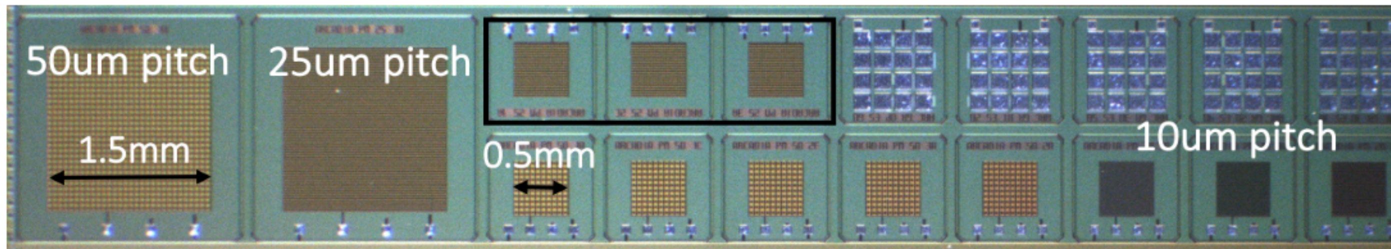
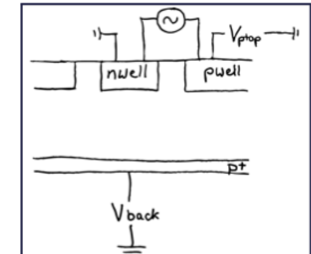
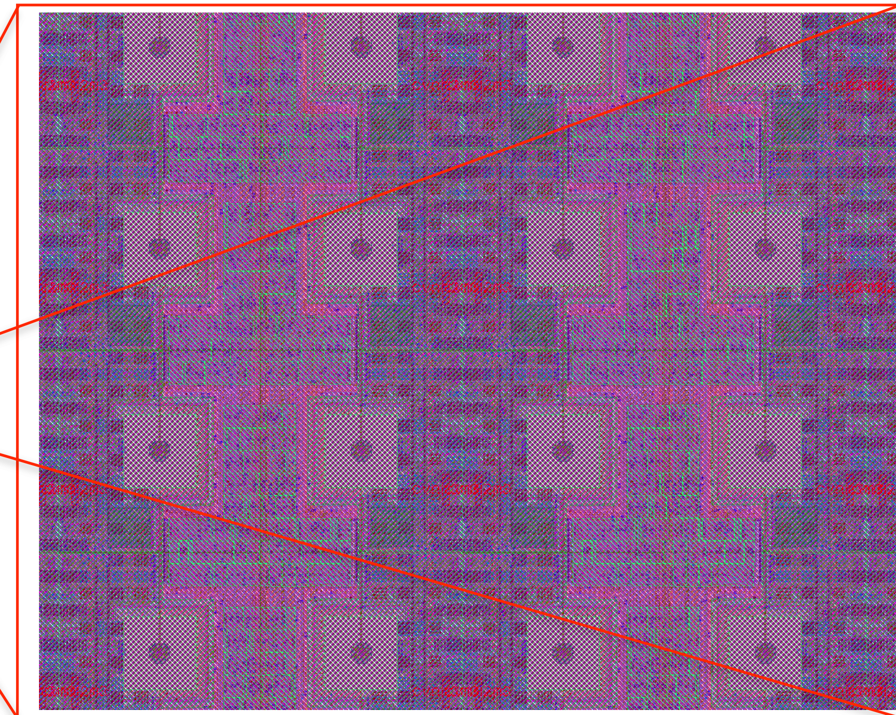








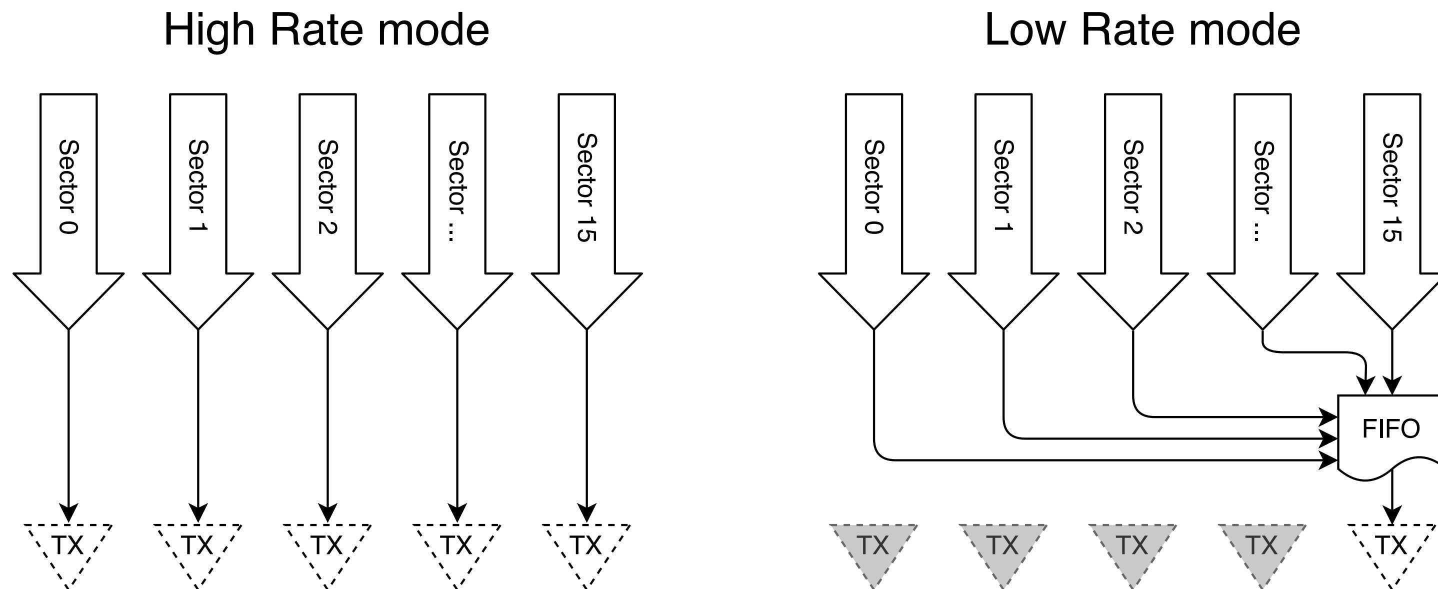
ARCADIA-MD1: Integration



* The Matrix is composed of 16 identical Sectors (32x512), each of which contains 16 Double Columns
* Each 2x512 Double Column is composed of 16 2x32-pixel Cores: the minimum "synthesisable" entity bundling together 8 Pixel Regions for optimal PNR and Signal Propagation
* Clock-less matrix integrated on a power-oriented flow

ARCADIA-MD1: Peripheral Dataflow

- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.

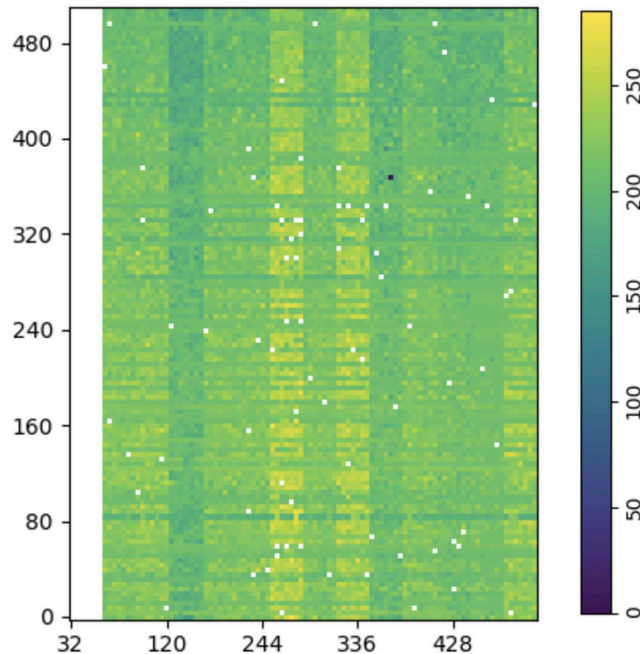


* "A 2 Gbps custom LVDS transceiver for the ARCADIA project", talk at IEEE NSS-MIC 2021

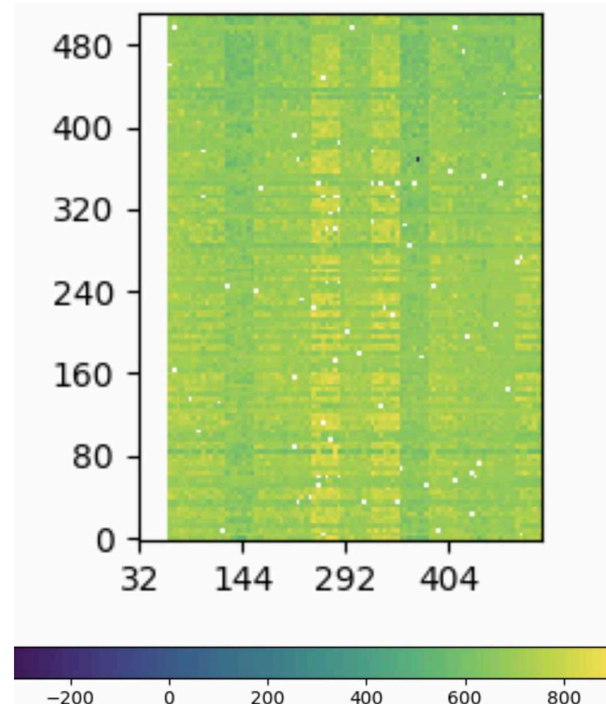
MD1 characterisation data: gain/noise

Results before threshold equalisation, good match with simulation and monte-carlo

FEB3 Baseline (mV)



FEB3 Gain (mV/fC)



FEB3 Noise (mV)