CE65 developments / tests

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Corrections/improvements for final gds (15 chips of CE65V2) on 25/08/2022

reminder:

Modification	Purpose	Pitch, um	Comment	N	status
CE65V2_C_xx	Charge collection ("_C_") measurements, rolling shutter readout (AC pixel from CE65 is implemented)	15, 18, 22.5, 18_{hexsq}, 22.5_{hexsq}	For lab and beam test, charge collection node, techno, optimization	5 chips (x 3 flavors: 1) no n-implant 2) Blanket n-implant 3) n-implant with gaps)	DRC, LVS are OK for all chips 5 chips x 3 pixel flavors ready : sent to CERN final on 25/08/22

1. Removed (reserved, but unused) A2V33, A3V33 pads – two more pads are used for:
   - ✓ Introducing PWELL and PSUB - separate back biasing possible
   - ✓ One optional digital pad which allows for programmable any size "windowed" readout of matrix (for ex. 3x3 block) – shorter frame readout - measure heavily irradiated sensors

2. Custom DRC checks satisfied (see next slide)
3. HVLV violations corrections (nwell spacing)
4. Recommended and ESD is waved
5. Density verifications (to avoid marginal cases) for reticle size

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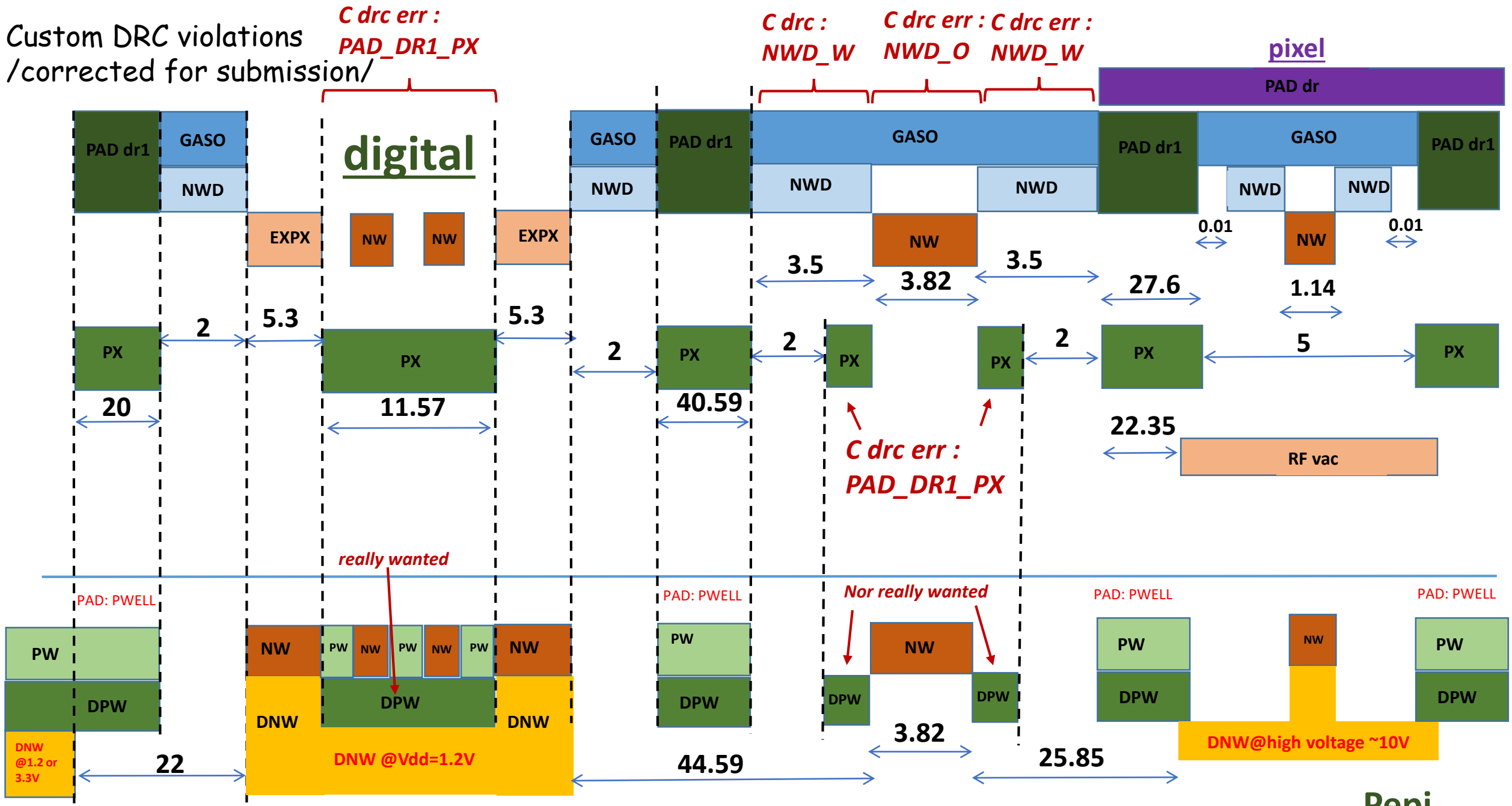
Custom DRC violations
/corrected for submission/



Pepi

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Additional chips for ER1 submission

The CE65V2 chips have completely reworked layout, so no corresponding pixel layout matches MLR1 submission (only pitch size of one chip is same as in previous submission)

1. One chip CE65A is ported to new metal stack:
   - some blocks are redesigned
   - pixel matrix is kept unmodified – to keep same charge collection and overall behavior

2. Effectively we have three flavors (no –n implant, blanket, with gaps), which give 3 additional chips (equivalent to CE65A, CE65B, CE65C) included in ER1 submission

3. All DRC violations not satisfied with new custom rules will be waves, because otherwise not possible to keep same layout

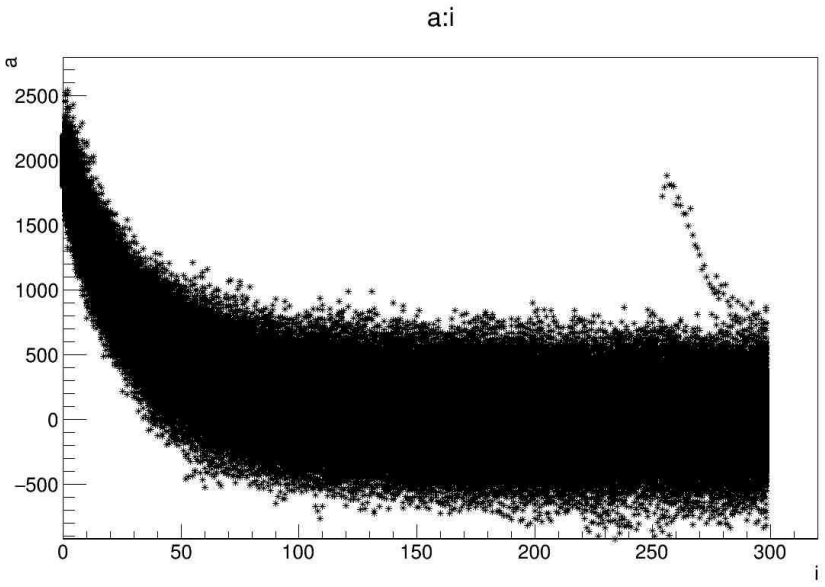
The purpose of this chips is not to conduct extra extensive test program as for other 15 chips, the purposes are:

1. Test if charge collection not modified with new technology nor pixel layout – so simple tests are sufficient
2. To reinforce development in case something wrong in completely new chips
3. To complement with SF pixels structures for detail study (if needed)
4. As obvious advantage – we have already all hardware/firmware/software developed for MLR1 chips – test can start immediately (for new chips we need to do major re-development of hardware, a bit less of firmware and smaller of software)

Measurements of leakage current: precise measurements pixel by pixel: to evaluate dispersion

Signal waveform(AC pixel) after Fe55 particles, ~850 superimposed

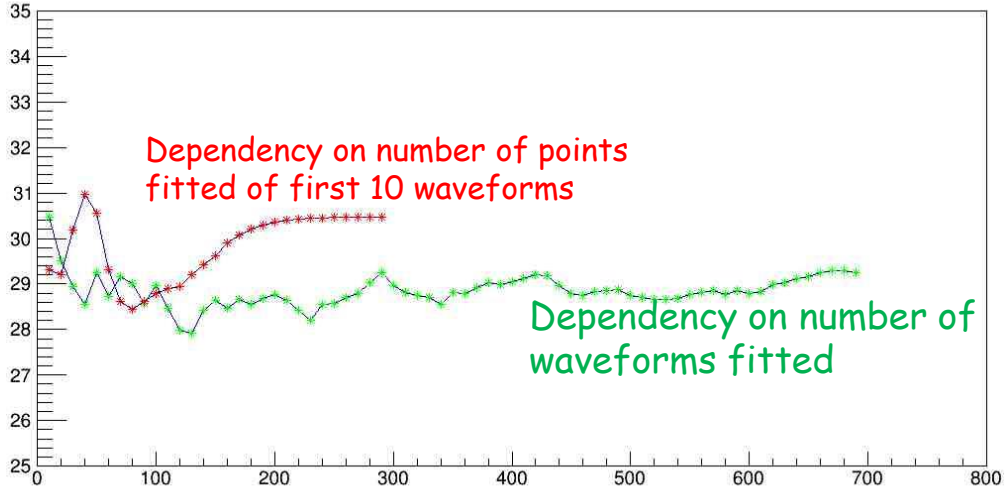
Spectre simulation shows very similar exponential decay with possibility to extract leakage current (knowing input capacitance)
There may be uncertainty due to that, but the aim is to verify if we have large variation of leakage current between pixel

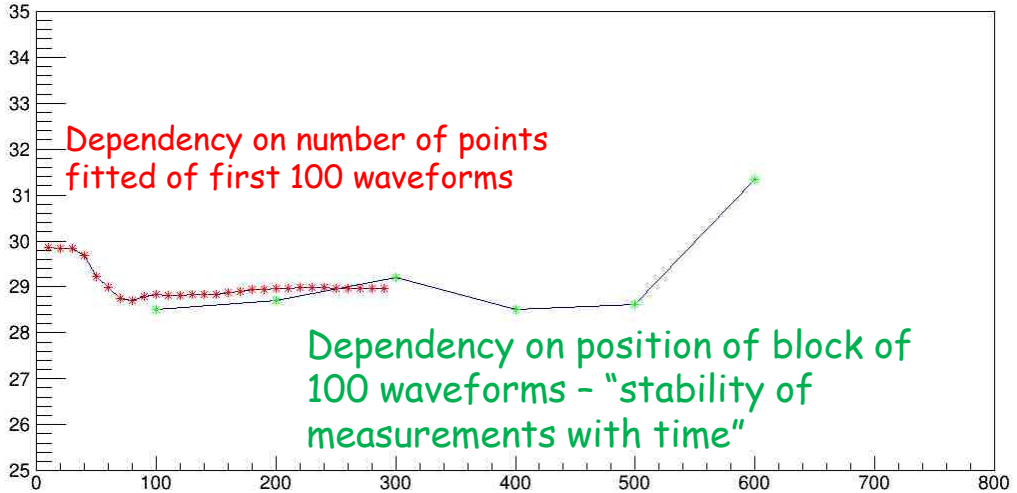


We can do ~10% precision even out of 10 waveforms and 10 points (one point 100ns) fitted:

1. robust enough for study of big variation of leakage current for different irradiation doses
2. Allows to perform tests in reasonable time for all pixels

Extracted leakage current, pA





Time to get all waveforms ~30min

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