IPHC contribution to the stitched sensor for ALICE-ITS3

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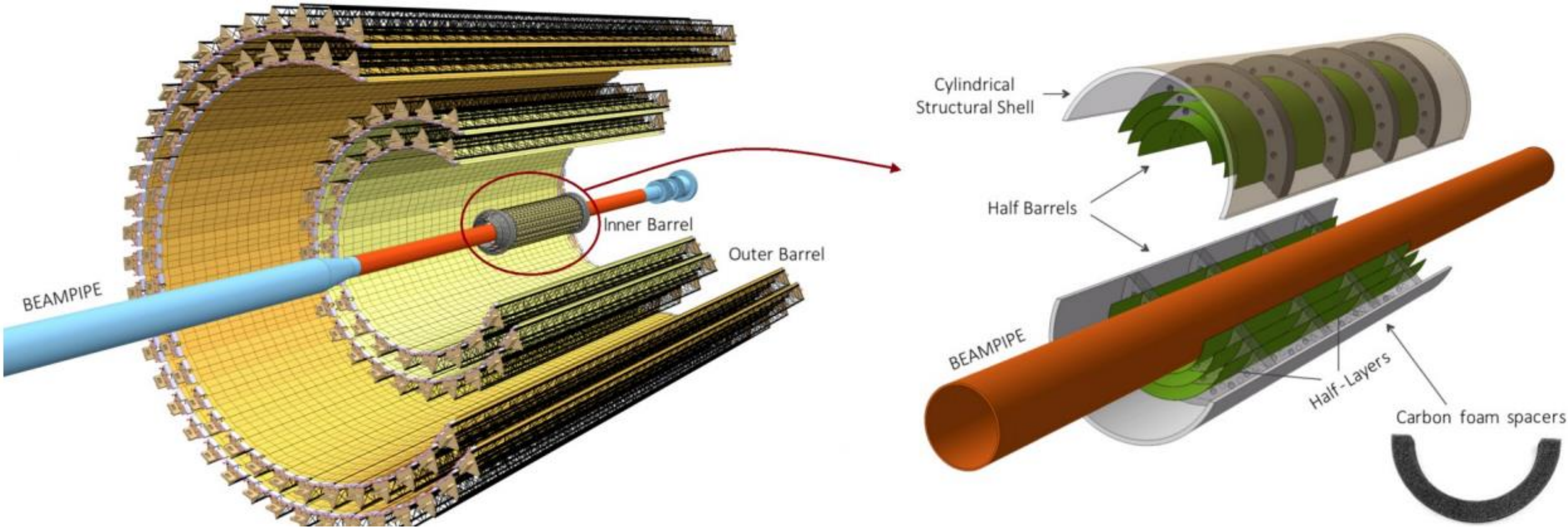
Outline

- Introduction
- Wafer scale stitched sensors
- MOSS (MOnolithic Stitched Sensor) Prototype
- Contributions of IPHC
- MOSS2
- Conclusion

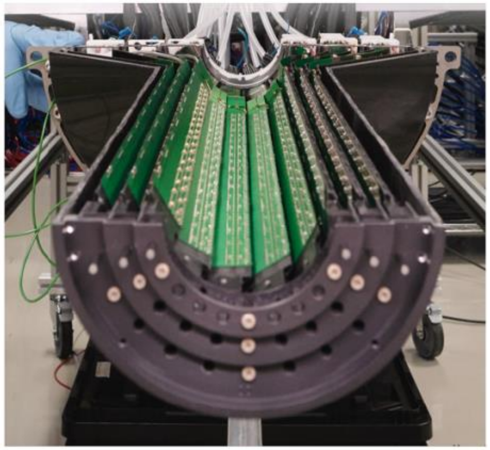
ALICE ITS3 upgrade

- ALICE ITS2 to ITS3 upgrade
  - Replacing the barrels by real half-cylinders of bent, thin silicon
  - Minimized material budget
    - Only 1/7th of the material budget
  - Minimized distance to interaction point
    - Large improvement of vertexing precision and physics yield
  - Less power consumption allows for air cooling
  - Onchip data transmission allows for no flex in the active area



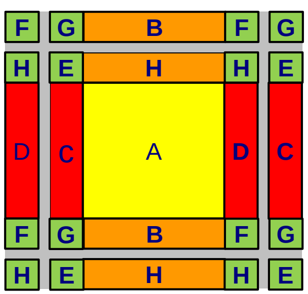
ITS3 layout

- 3 Cylindrical layers
  - Rely on wafer-scale sensors (1 sensor per half-layer) in 65 nm technology
  - Made with 6 curved wafer-scale single-die Monolithic Active Pixel Sensors
  - Radii 18/24/30 mm, length 27 cm
  - Thinned down to <50 µm
  - Position resolution ~5 µm
    - Pixels pitch 20 µm



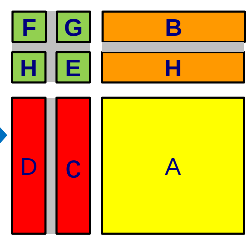
Wafer scale stitched sensors

- 3 design steps
  - Design a baby circuit composed by Endcap, Corner and Repeated sensor unit (RSU)
  - Split the endcap , the Corner and the repeated unit (send to foundry)
  - By repeating the repeated units (and the endcaps), the foundry constructs the stitched objects

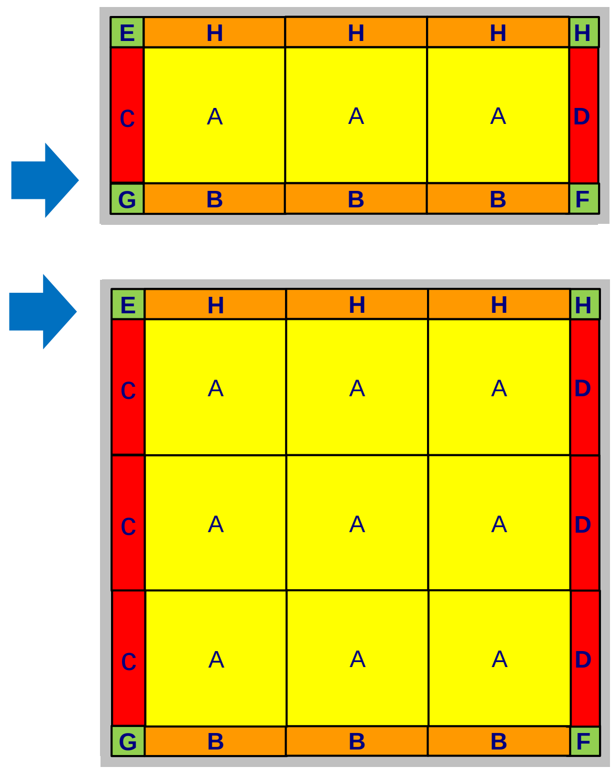


Baby circuit

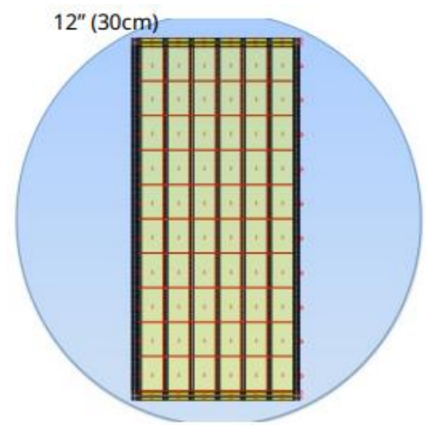
A: Repeated sensor unit
DC, BH: Endcap
FGHE: Corner



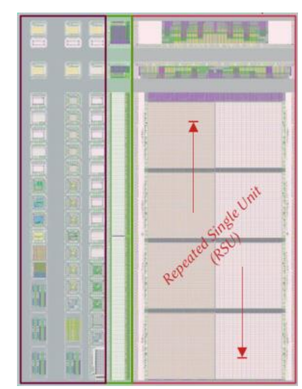
splitted



stitched object

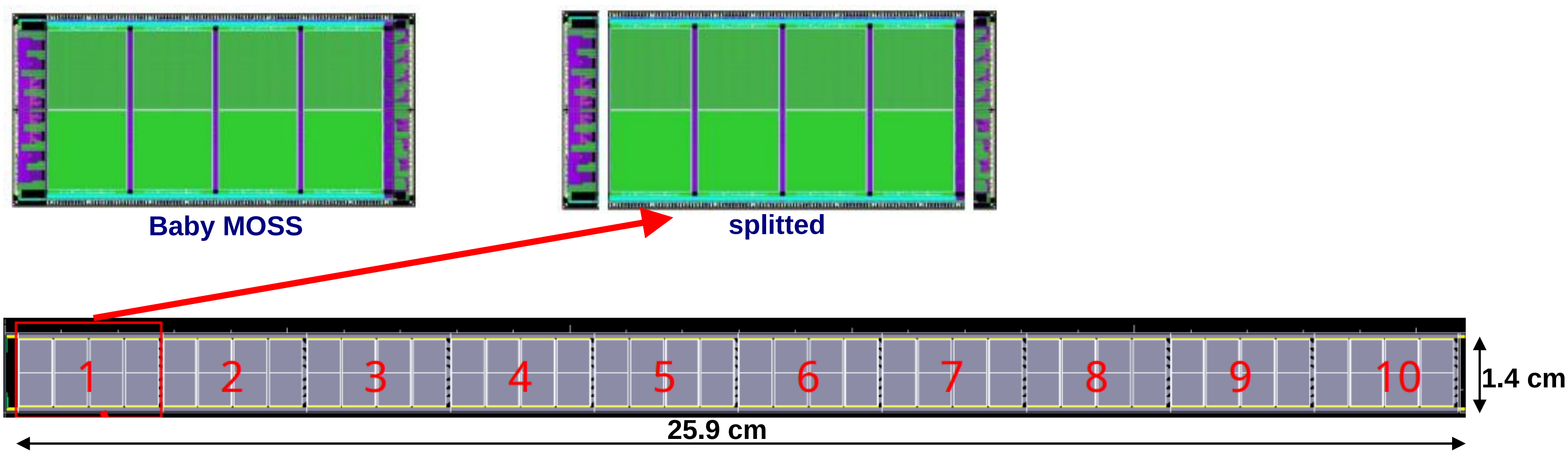


ER1 submission



MOnolithic Stitched Sensor (MOSS)

- MOSS prototype is a proof-of-concept
  - To understand if we can design a stitched monolithic particle detector with satisfactory yield
- Primary goals:
  - Learn stitching techniques
  - Interconnects
  - Learn about yield and design-for-manufacturing (DFM)
  - Study power schemes, leakage, spread, noise and speed
  - Develop inhouse stitching methodology

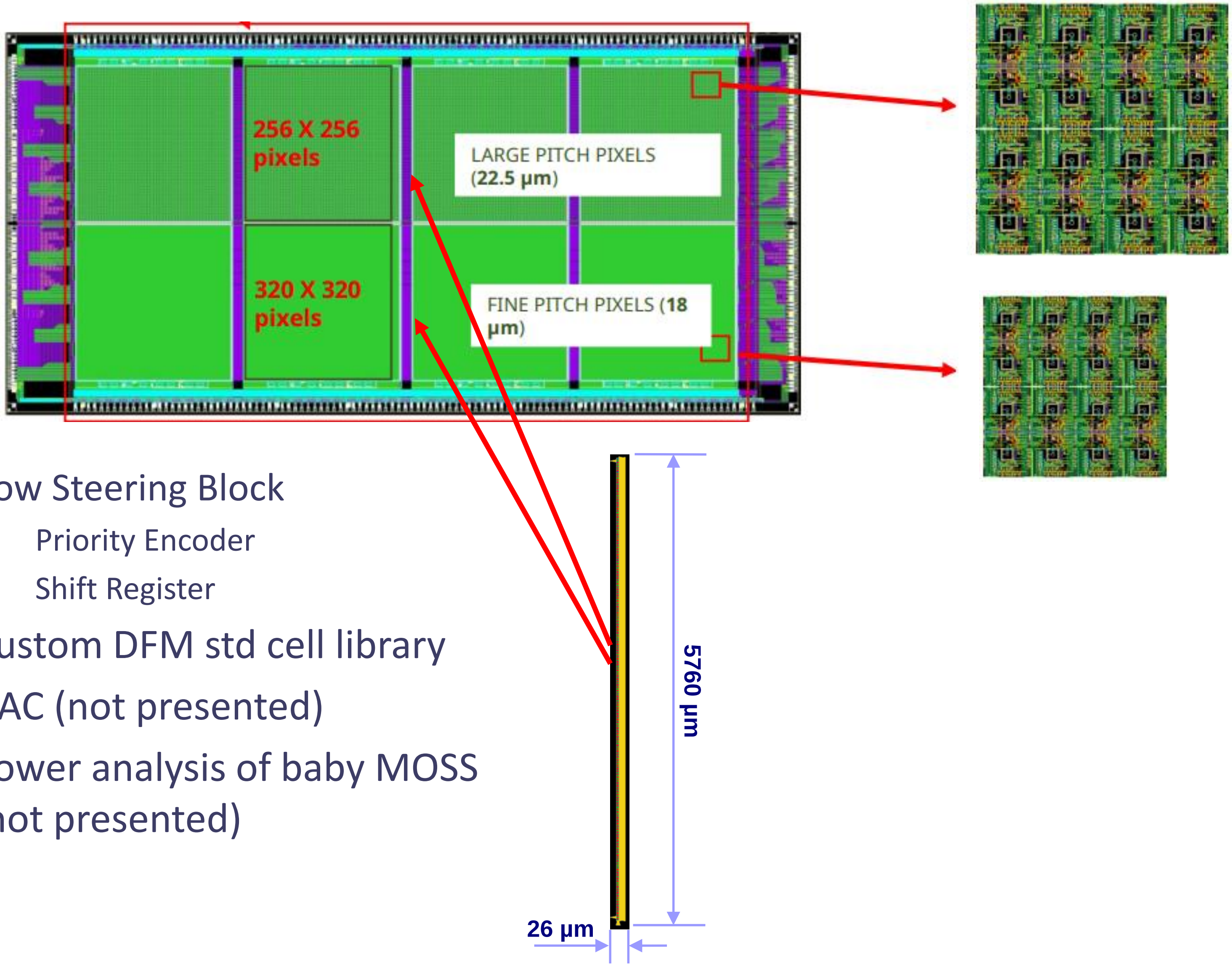


Baby MOSS

splitted

MOSS

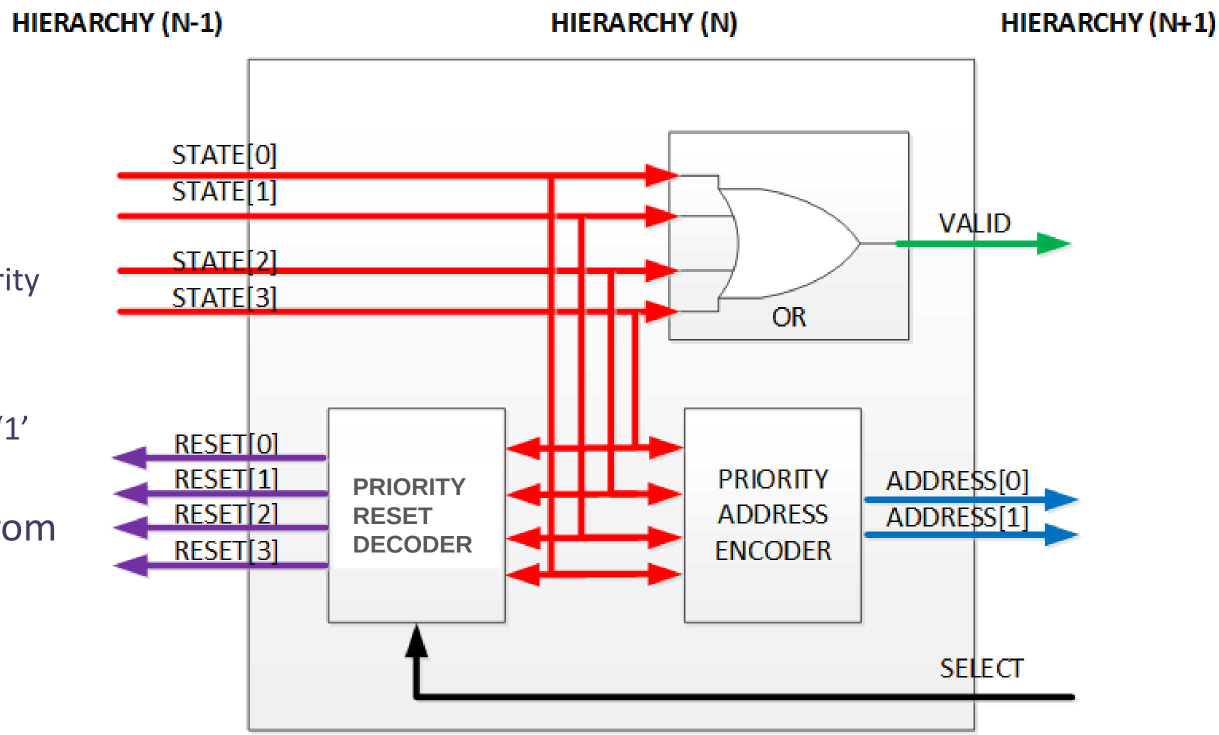
Contribution of IPHC in MOSS



- Row Steering Block
  - Priority Encoder
  - Shift Register
- Custom DFM std cell library
- DAC (not presented)
- Power analysis of baby MOSS (not presented)

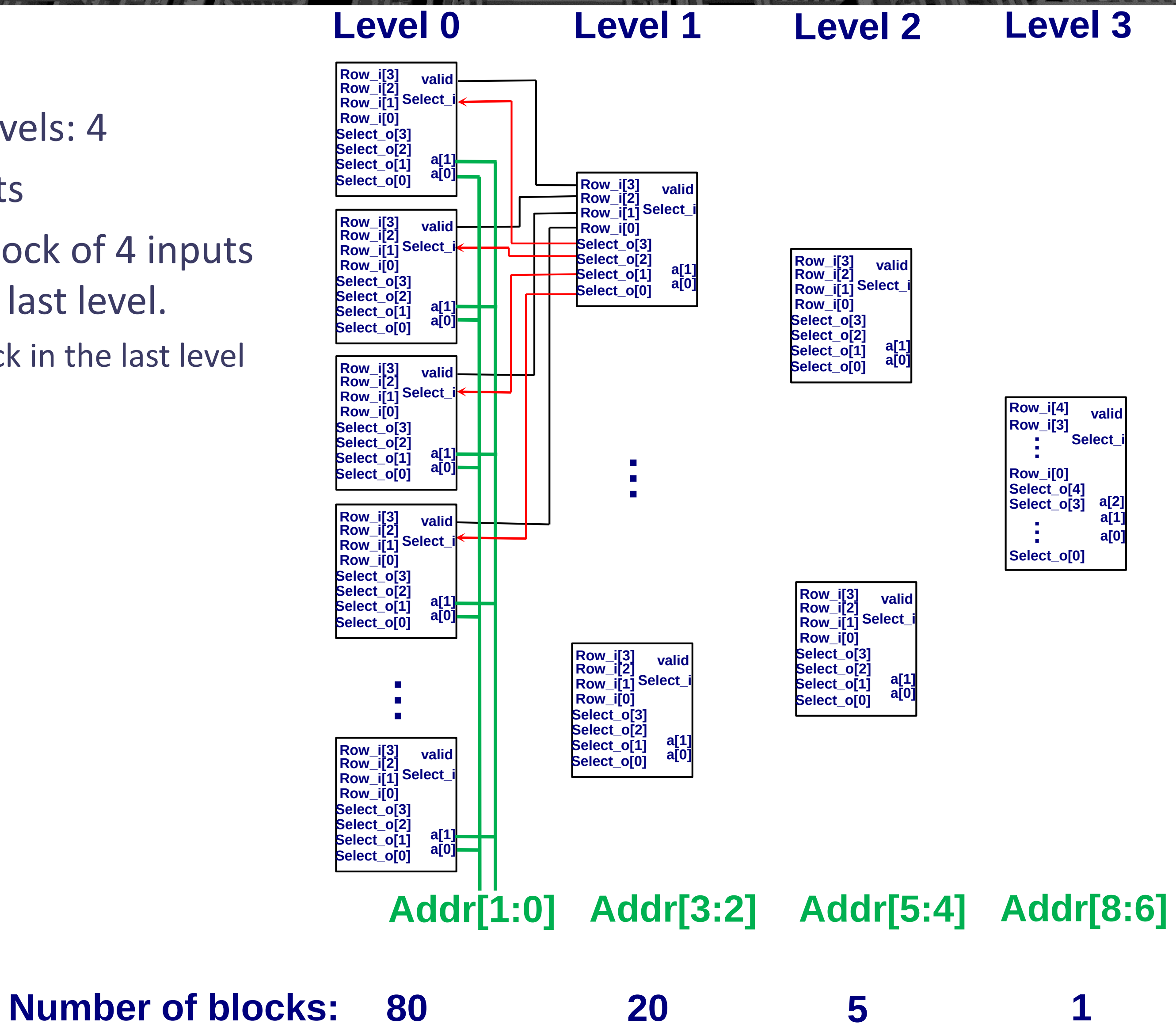
Row Steering Block

- Priority Encoder
  - Matrix readout
  - Based on a 4 input sub-block
  - Combination circuit
  - Priority Address Encoder
    - Encode the address of a priority input
  - Priority Reset Decoder
    - Set only the priority reset to ‘1’ after the address readout
  - Configurable RTL (support from 65 rows to 2048 rows)
- Design with Flowkit environment



PE for Bottom Row Steering

- Rows: 320
- Number of levels: 4
- Address: 9 bits
- Based on a block of 4 inputs except of the last level.
  - 5 inputs block in the last level



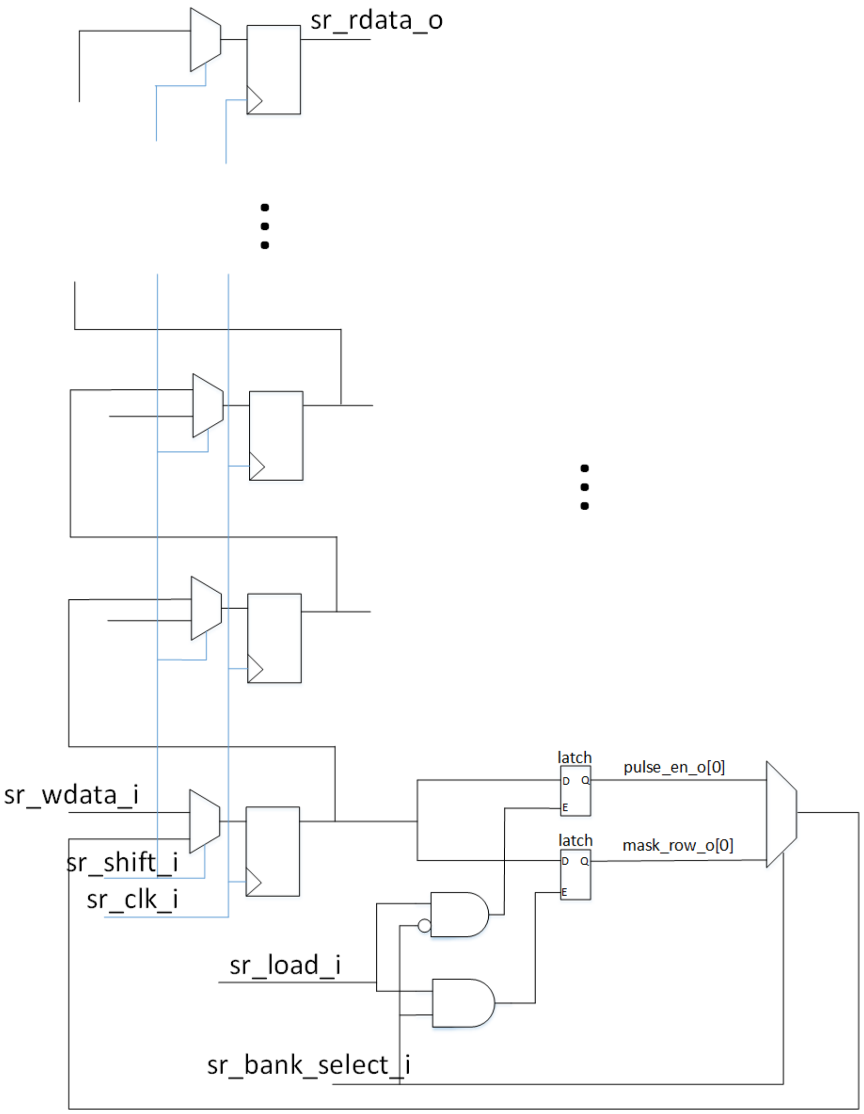
Shift-register control

- Read and write signals for matrix (pulse_en and mask_row)
- Bank select
  - Less DFF ➔ less area
  - Only one shift register
- Use latch to save data
  - Smaller than DFF
  - Less timing restrictive
  - Check timing (no transparent latches):

set_db timing_use_latch_time_borrow true

report_timing –debug time_borrow

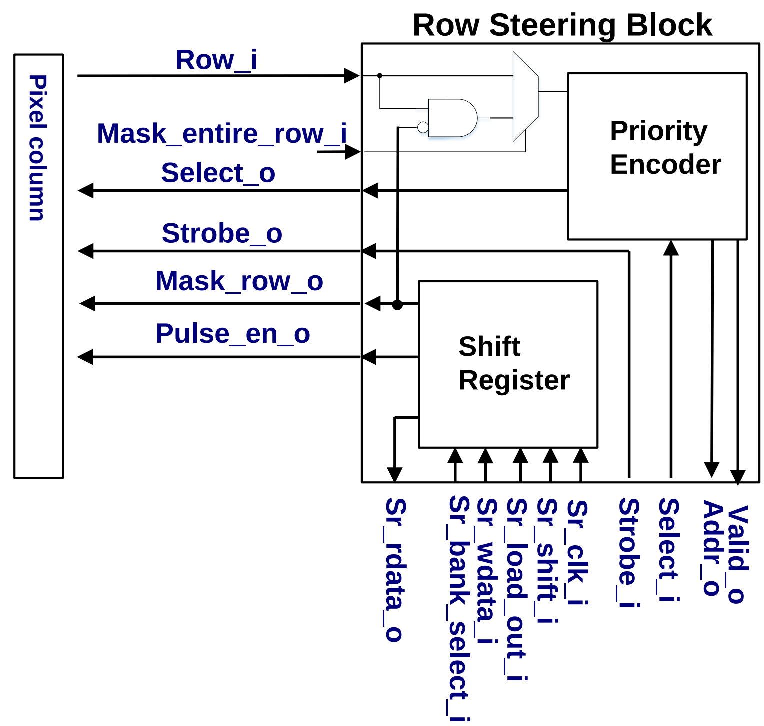
```
                    Capture        Launch
     Clock Edge:+   25.000         0.000
    Src Latency:+   -1.126        -0.978
    Net Latency:+    0.571 (P)     0.518 (P)
        Arrival:=   24.444        -0.461

  Time Borrowed:+    0.000
    Uncertainty:-    0.100
    Cppr Adjust:+    0.000
  Required Time:=   24.344
   Launch Clock:=   -0.461
      Data Path:+    0.335
          Slack:=   24.470
```



Simulation results

- Static timing analysis
  - Post layout, MAX library, CWORST Corner

Arc Source	Arc Destination	Delay[ns]
Strobe_i	Strobe_o	1.791
Select_i	Select_o	2.946
Row_i	Select_o	5.055
Row_i	Valid_o	3.129
Row_i	Addr_o	6.221



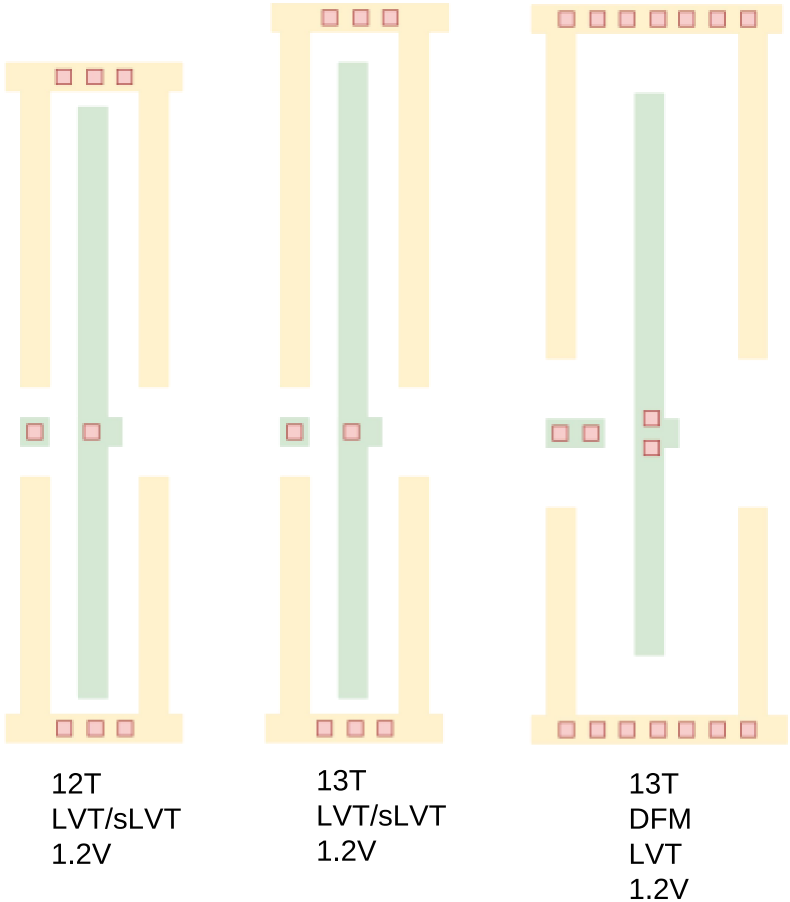
- Static power analysis
  - Row_i is controlled by a clock of 40 MHz
  - With VCD file, TYPICAL Corner
  - 1 hit/2 clocks

```
Total Power
------------------------------------------------------------
Total Internal Power:        0.04975138          41.3350%
Total Switching Power:       0.05609608          46.6064%
Total Leakage Power:         0.01451380          12.0585%
Total Power:                 0.12036127
------------------------------------------------------------
```

⇒ **6.02 pJ/pixel**

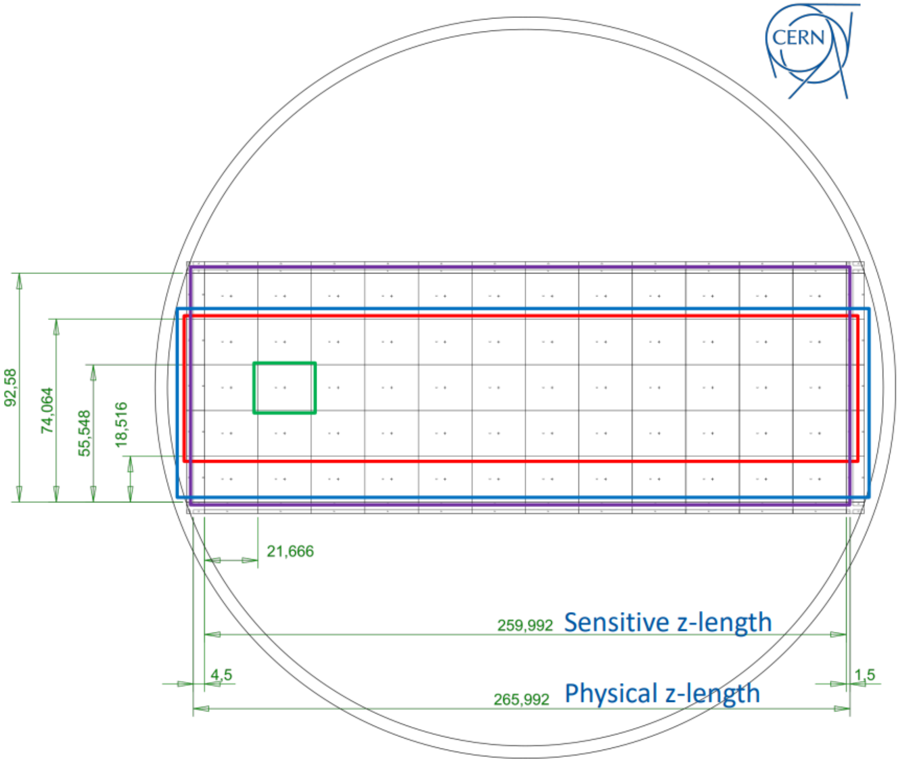
DFM standard cells

- Customized DFM standard cells → to improve yield
  - Add redundancy to single-cut contacts and vias → reduce probability of opens and bad contact
  - Maximize spacing → reduce shorts
  - Maximize width → reduce opens
- Based on the 12 Track standard cells
  - Size of transistors remain unchanged
  - Increase the height of the cells from 12T to 13T



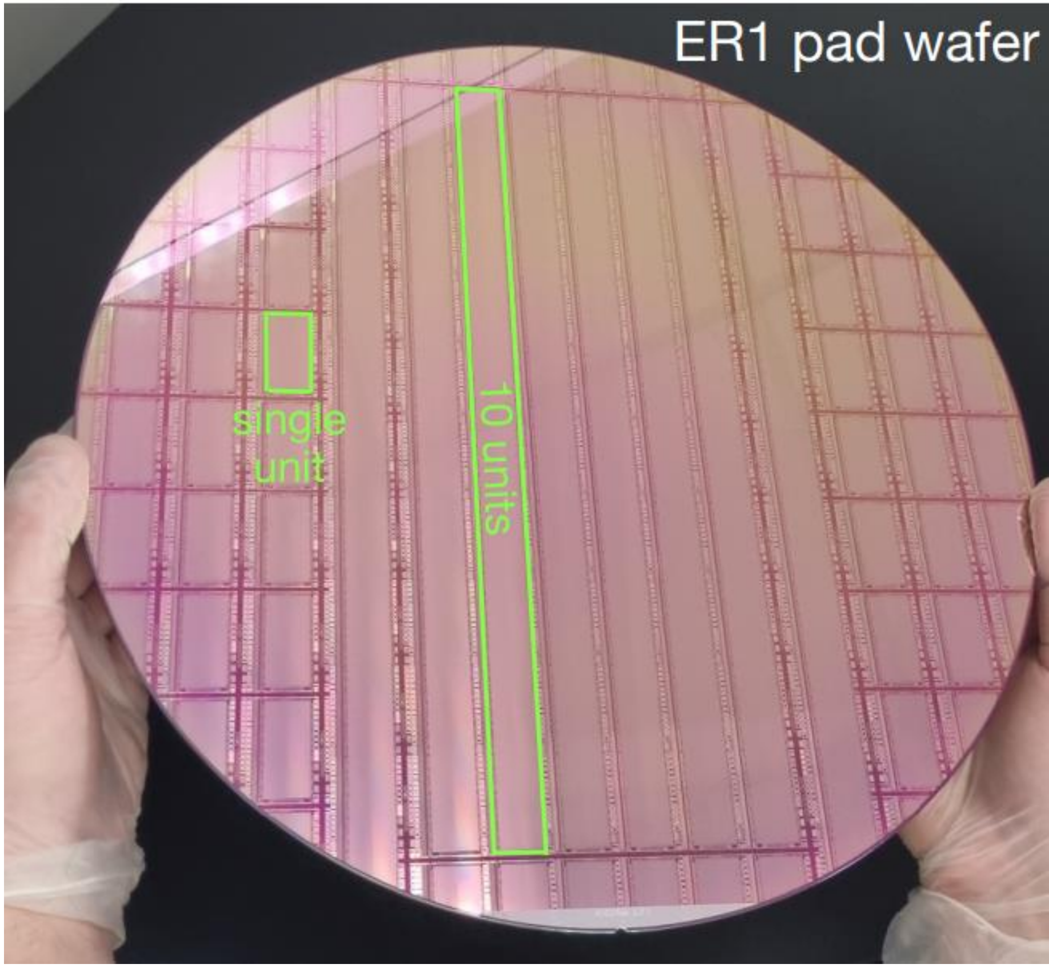
MOSS2 (ER2 Stitched Sensor)

- Layer 0: 12 x 3 repeated units+endcaps
- Layer 1: 12 x 4 repeated units+endcaps
- Layer 2: 12 x 5 repeated units+endcaps
- Repeated (Stitched) Sensing Unit
- ER2 Stitched Sensor is not a direct evolution of MOSS
- ER2 Sensor aims to satisfy ITS3 requirements
  - Existing circuits need substantial redesign
  - New features to be added



Conclusion

- The MOSS prototype tries to answer if a stitched monolithic particle detector is possible
  - Yield improvements
  - Power and data inter stitching connections
  - Stitching methodology
- The MOSS Prototype has been submitted in Q4 2022 with ER1 in the WP1.2 framework
- The test of MOSS has started
  - We can read and write the baby MOSS
- The design of MOSS2 is on going
  - Pre-studies are done
  - Design will start soon



Merci de votre attention