LASP board design for the ATLAS Calorimeter Experiment

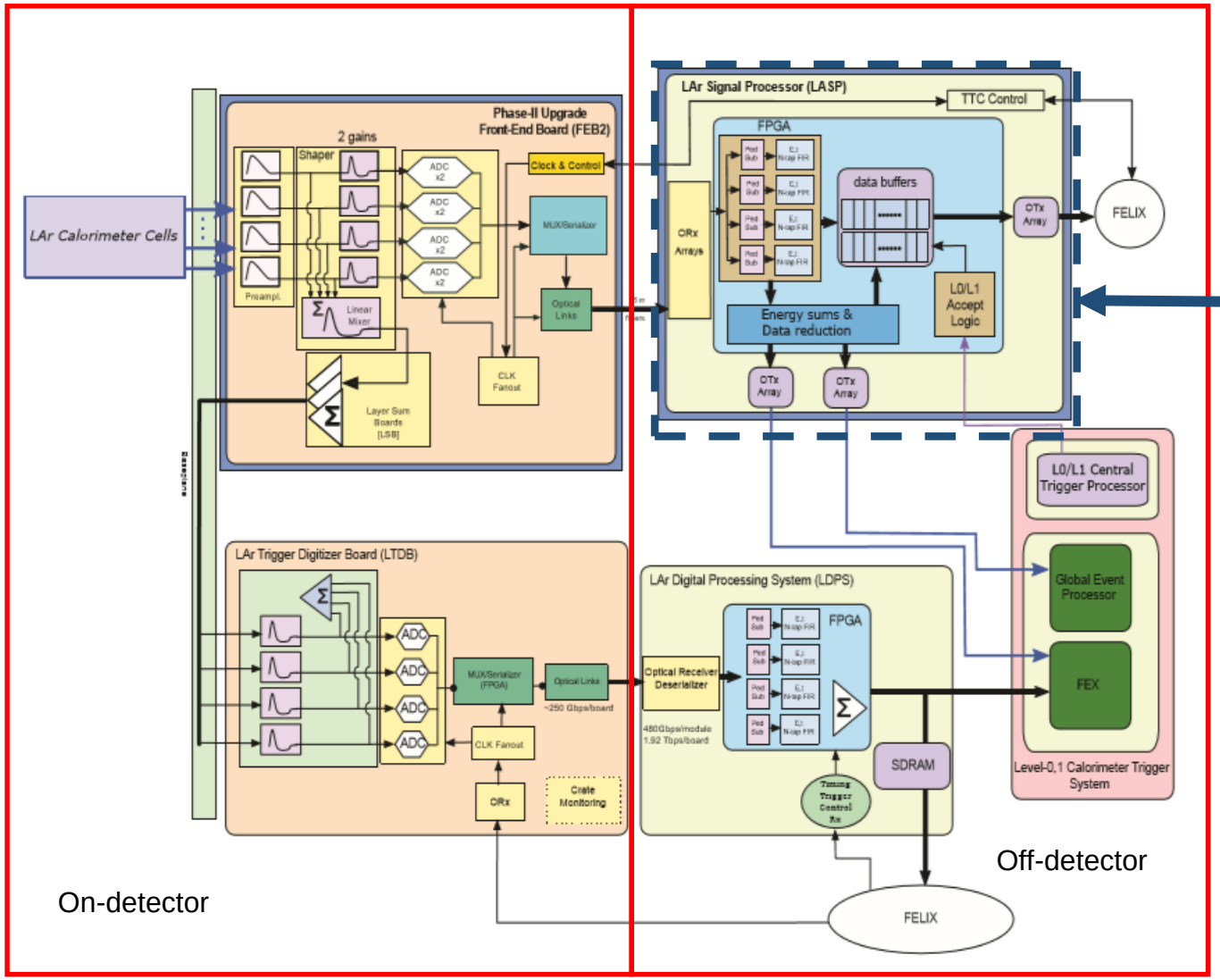
JME 2023

Kevin ARNAUD
On behalf of the CPPM team

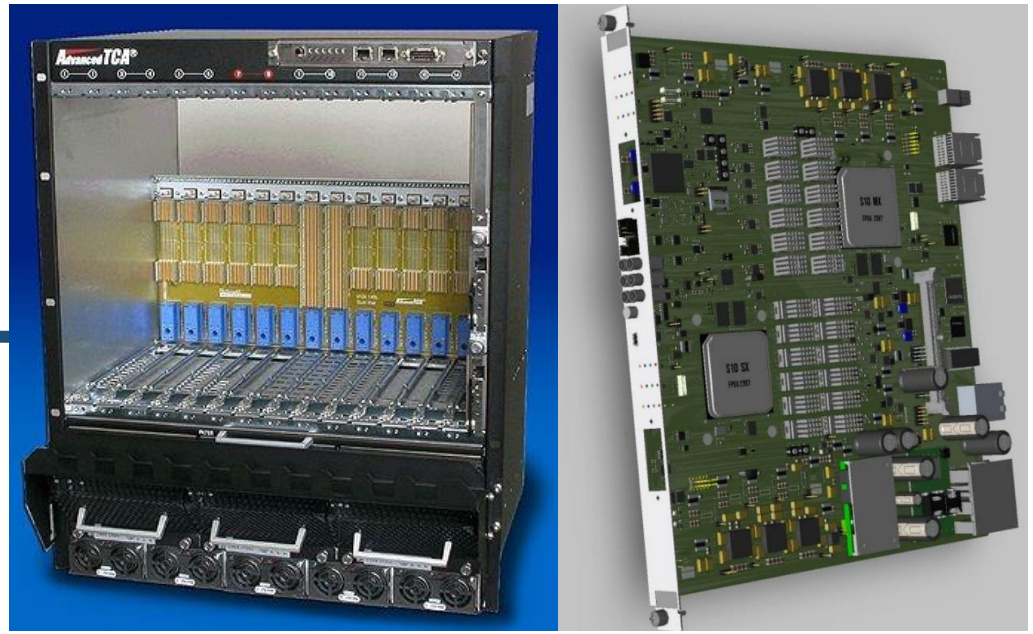
Outline

- Liquid Argon acquisition system
- Functional diagram of LASP board: test board and prototype
- LASP board challenges
- PCB features
- Study and simulations
- Testing the LASP test board
- What is new for the prototype board
- Conclusion

Liquid Argon acquisition system

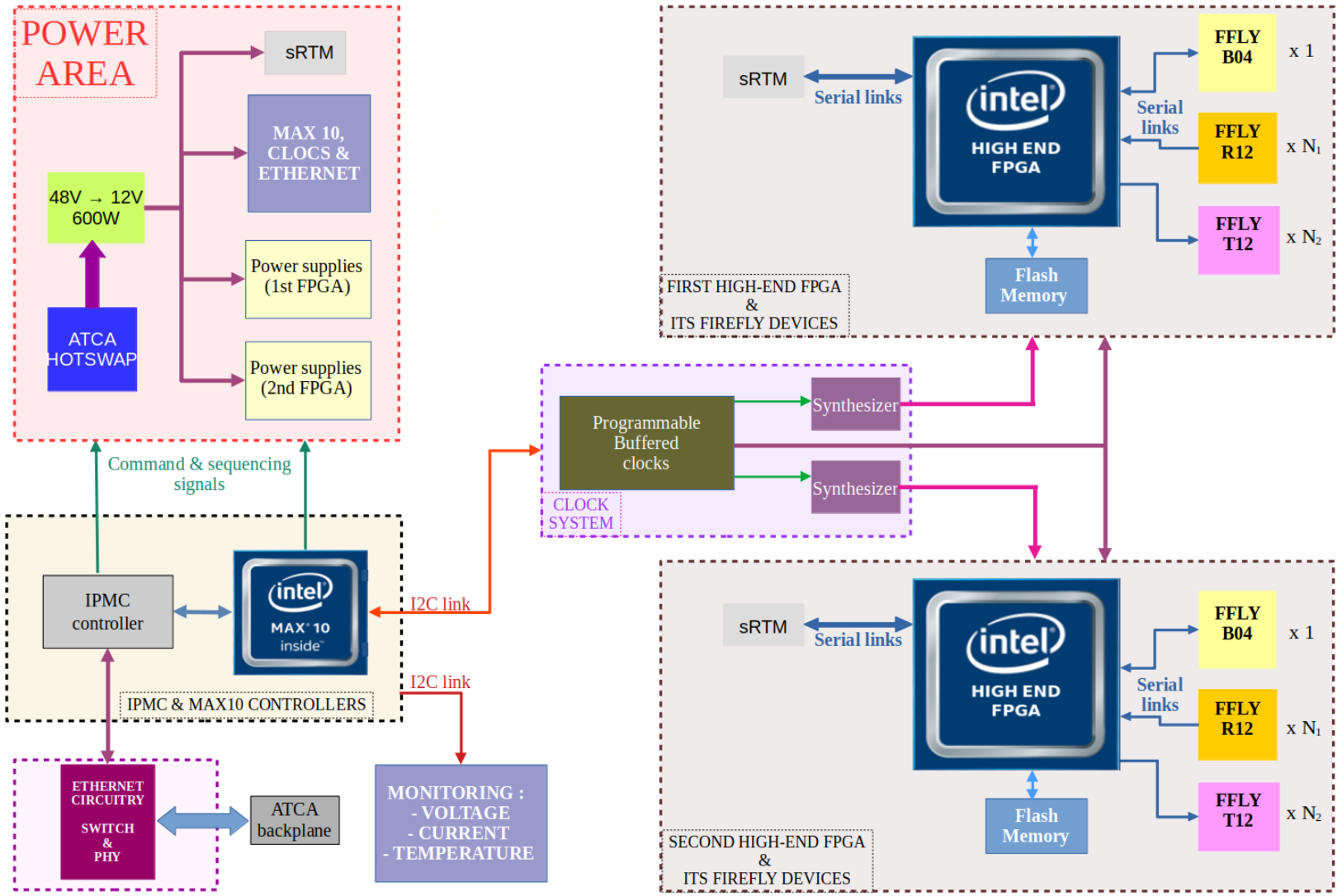


LIQUID ARGON SIGNAL PROCESSOR (LASP)



- **On-detector electronics**
  - 1600 Front End boards FEB2
  - 40000 optical fibers at 10.24Gb/s -> 42To/s
- **Off-detector electronics**
  - 30 ATCA crates
  - 334 ATCA main boards associated with smart Rear Transition Modules
  - Thermal dissipation : 70kW

Functional diagram of two LASP board versions

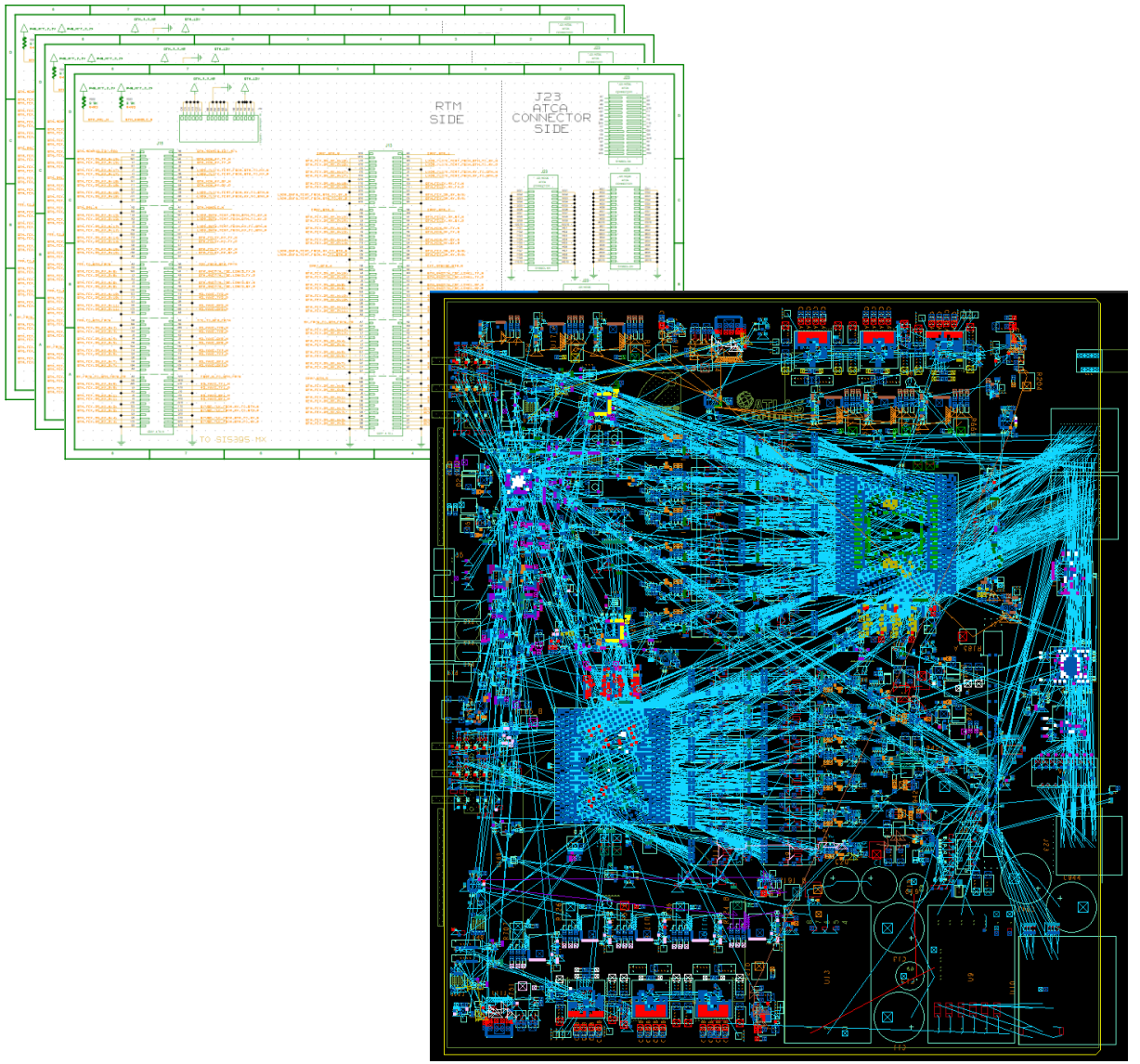


Functional diagram of the LASP board simplified

Components	Test board (2021)	Prototype board (2024)
High-end FPGA	STRATIX-10	AGILEX-7
DDR4	Yes	No
FIREFLY R12 / FPGA	8 (14 Gbps)	6 (25 Gbps)
FIREFLY T12 / FPGA	3 (14 Gbps)	2 (25 Gbps)
FIREFLY B04 / FPGA	1 (28 Gbps)	1 (28 Gbps)

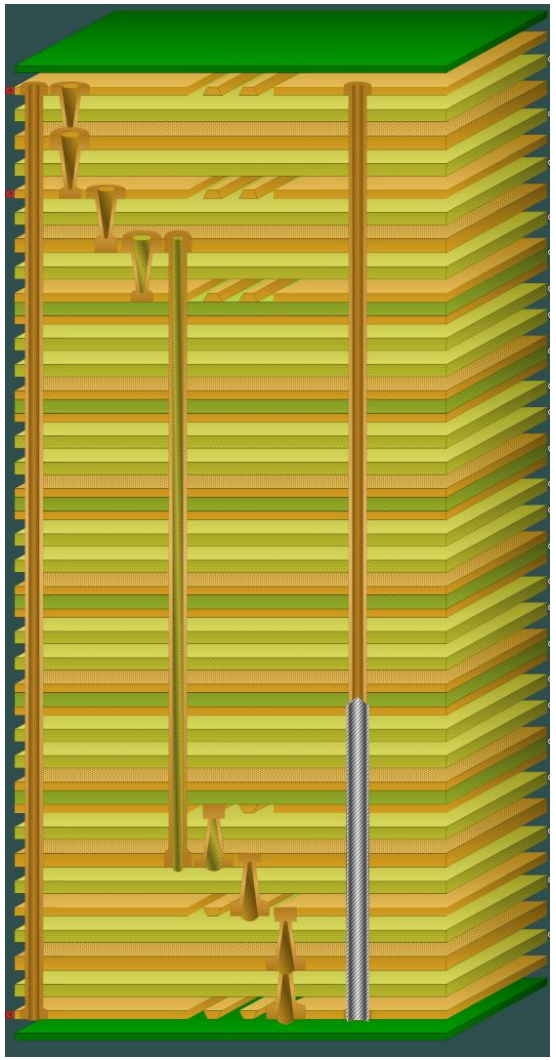
Challenges for both LASP versions

- More than 140 schematics pages
- 16000 connections
- Data rates : 25 Gb/s (with different lengths)
  - 56 links at 25 Gb/s
  - 192 links at 10.24 Gb/s
- Power
  - VCC Core :
    - Up to 120A for the test board
    - Up to 240A for the prototype board
  - Authorized maximal power: 350W
- High component density: around 4000
- Various packages(BGA , TQFP , DFN ,0201,…),
- Press fit connectors
- ATCA format : 280 mm x 322.25 mm
- PCB thickness : 2.4 mm



PCB features

- **20-layer HDI PCB** (High-Density Interconnection)
  - 6 signal layers
  - 14 power layers
- **Selected technologies**
  - Micro Via Stacked and Staggered
    - Signal integrity
    - No stub effect
    - Recommended for high signal density
    - Recommended for power distribution
  - Backdrill technique for Press fit connectors (high speed)
- **Selected materials**
  - Dielectric
    - Test board: Megtron6 (adapted for high speed designs)
    - Prototype board: EM-528K (**halogen free** as requested by CERN)
  - Copper quality
    - Test board: standard quality
    - Prototype board: highest quality (HVLP)



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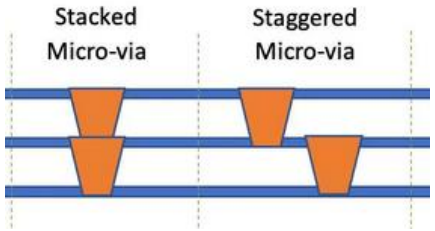
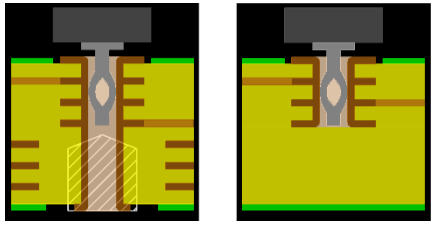
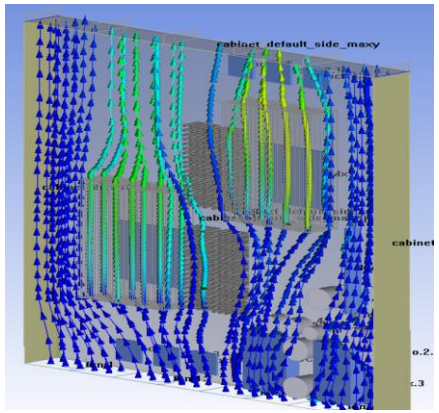


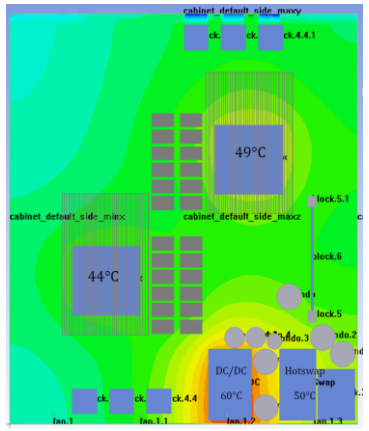


Backdrill

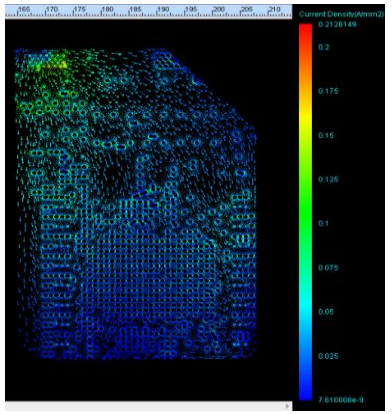
Simulations and designs

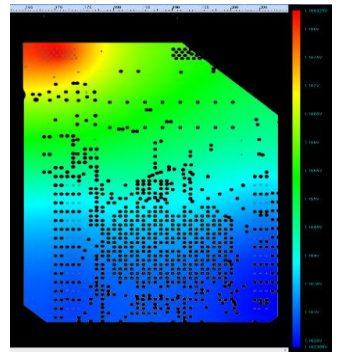
- **Thermal study with ANSYS**



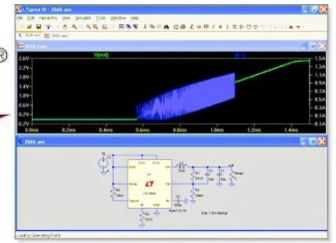


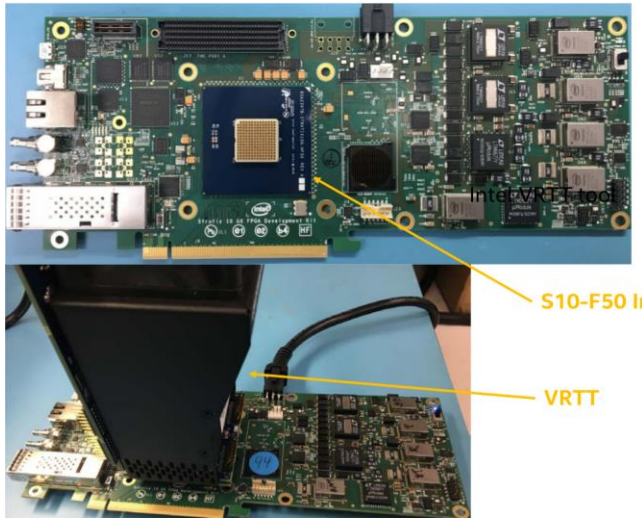
- **Power shape simulations with Cadence SIGRITY**





- **Power supplies: Spice simulation, design & test**
  - Testing with devkits
  - Simulation with LTSPICE (Linear Technology)
  - VRTT tool



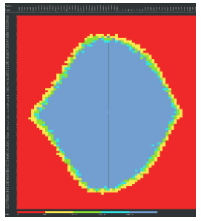


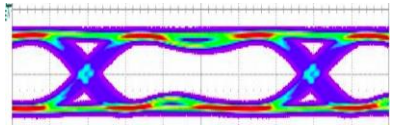
Testing LASP testboard produced in 2021

- **Electrical Tests OK**
  - Power
    - 48V to 12V converter
    - 12V distribution
    - Powering STRATIX 10
    - STRATIX-10 power sequence
    - Stress test FPGA by augmenting occupancy:
      - Vary number of FW slices and processing slice
        - 25%, 50%, 75% and 99% FPGA core used
        - Both FPGA's on
  - I^2C links
    - Temperatures
    - ADC (voltage/current monitoring)
    - Clock (Jitter Cleaner)
  - STRATIX-10 JTAG programming through direct links
  - UART SLOW-Control monitoring with MAX10
  - SLOW-Control IPMC with the shelf manager

- **Optical tests : evaluate eye diagram**
  - FIREFLY on LASP test board
    - Optical loop from B04 TX to B04 RX @ 26 Gbps : 62% to 67%
    - Optical loop from TX to RX at 12.5Gb/s: 68% to 80%

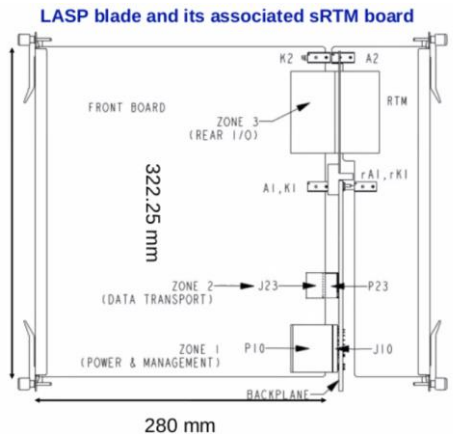
Example opening of 75 % at 12.5 Gb/s





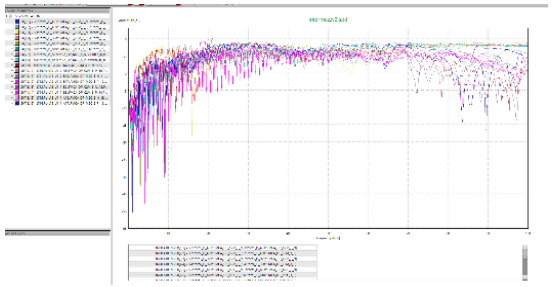
Mesure oscilloscope

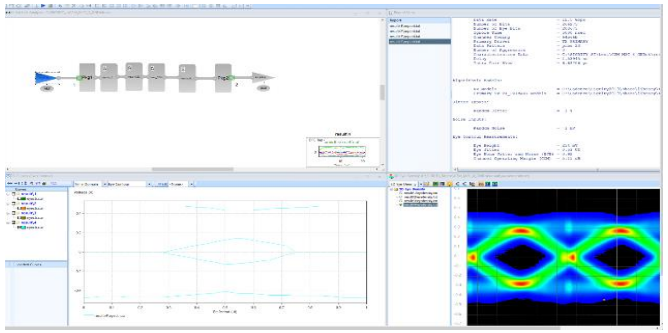
  - From LASP STRATIX-10 transceivers to sRTM FIREFLY
    - For tracks 30 to 40 cm long, the eye diagram opening is less than 30%.

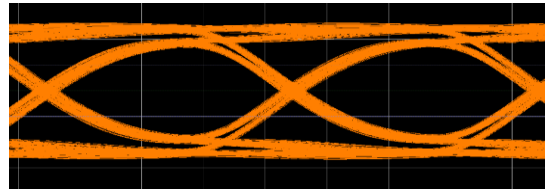


Eye diagram simulations for long traces

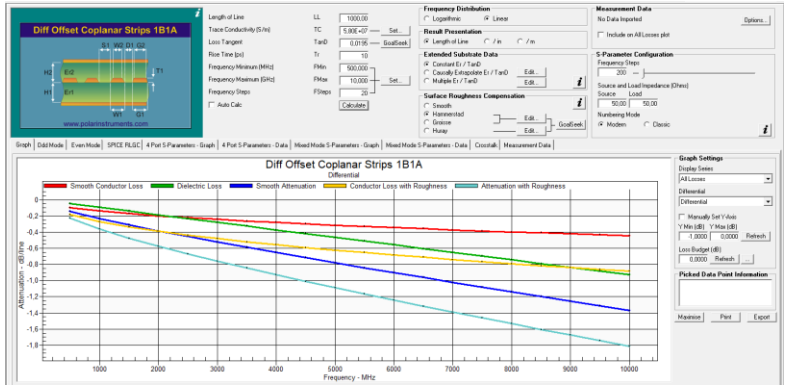
- **SIGRITY and Hyperlynx simulations**
  - Simulation of different high speed links at 12.5 and 25 Gb/s

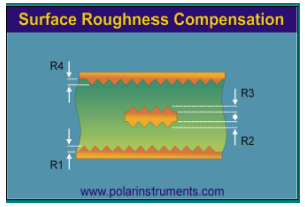




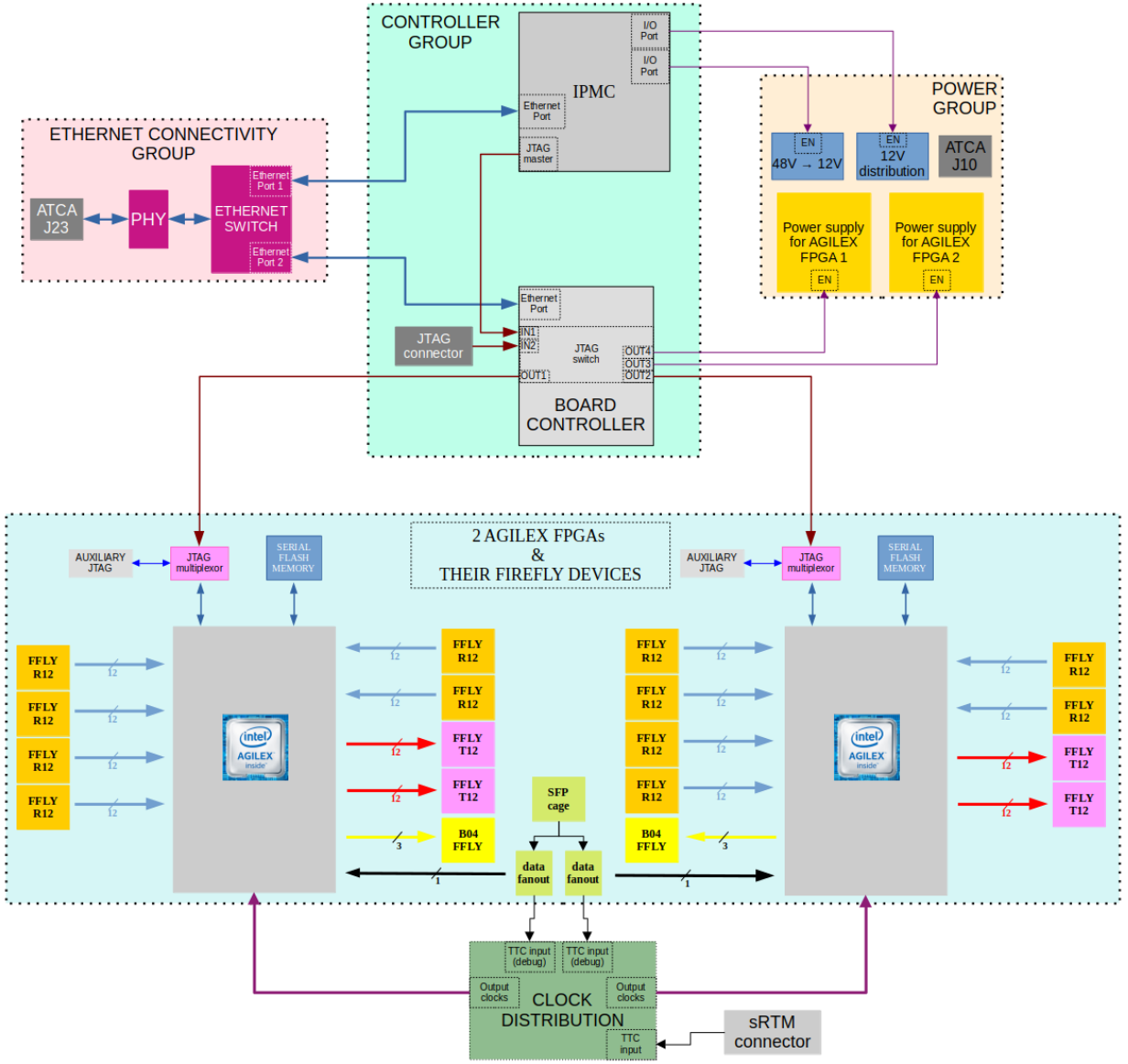


- **Tests of links longer than 30 cm show bad results**
  - Confirmed in simulation when playing with the roughness parameter (PolarInstrument)
  - Copper issue identified



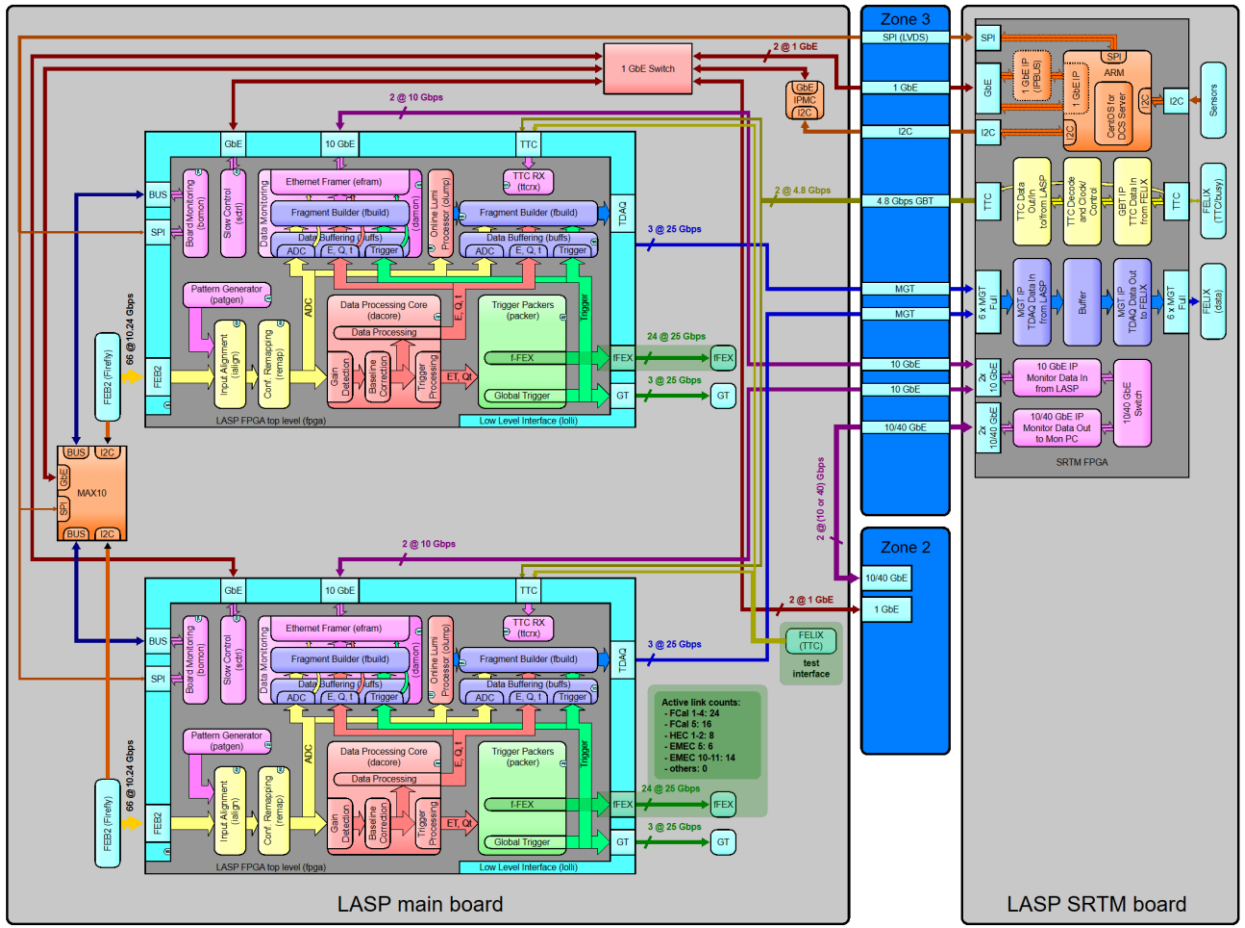


LASP PROTOTYPE board: under development



- **What's new compared to the test board**
  - Components
    - Processing FPGA : STRATIX-10 -> AGILEX-7
      - 40 % less energy consumption
      - 2 to 3 times more ressources for our needs
    - 25 Gbps Ffex firefly on LASP
    - Updated Zone 3 interface with sRTM (no Ffex data, changed transceiver link counts)
    - Removing DDR4
  - Electronic architecture:
    - Processing data from 3 FEB2/FPGA instead of 4
    - New power block for AGILEX FPGA
    - New dynamic JTAG chain: no more star connection of TMS & TCK signals
    - Clock distribution reviewed: no more VCXO tracking
  - PCB
    - Halogen free material (CERN requirement): EM-528K
    - HVLP copper quality

New LASP + sRTM interfaces overview



- FEB2 Input to each FPGA (2/LASP)
  - Up to 384 Calo channels from 3 FEB2's
  - 66 Links @ 10.24 Gbps input (per LASP + SRTM)
  - 1 TTC GBT link @4.8 Gbps (or alternatives @9.6 Gbps)
  - SFP on SRTM with serial fanout to LASP
- Output for L1 (per FPGA)
  - Forward Feature Extractor: ≤24 @25.781 Gbps
  - Global Trigger: ≤ 3 @ 25.781 Gbps
- Output for TDAQ (per FPGA)
  - 1 Interlaken link @ 25.781 Gbps via SRTM
- + monitoring (10 GbE) and ATCA infra

LASP prototype: decisions in past year

- Several design issues addressed
  - FFex output fireflies moved from SRTM to LASP (shorter traces, greater reliability)
  - TTC distribution choice determined (mentioned on previous slide)
  - Updated interface LASP<->SRTM. Expect this to be final version.
  - FELIX output will use Interlaken
  - 3 FEBs/FPGA
  - Switch from Stratix to Agilex family FPGA (ATLAS LAr approval)

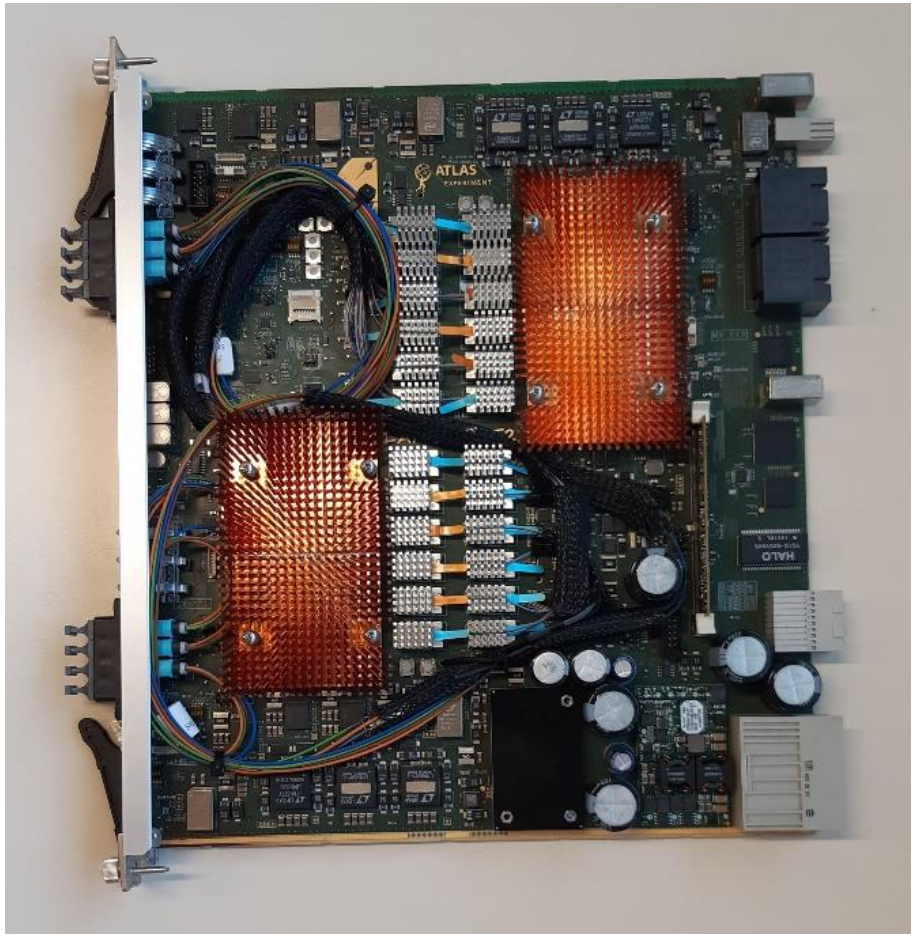
	STRATIX 10	STRATIX 10	STRATIX 10	Agilex	Agilex
	option 1	option 2	option 3	option 4	option 5
Nb FEBs / FPGA	4	3	2	4	3
FW resources	TIGHT	OK	High margin	OK	High margin
Power	Too High	OK	High margin	OK	High margin
Fmax (MHz)	600	600	600	850	850

Original baseline

- Had successful specs review (15 Sep. ‘22) and PDR (17 Jan. ‘23).

Conclusion

- LASP testboard
  - Design and successful development of the testboard based on STRATIX-10
  - Production of 6 LASP testboards in total
    - 4 already produced operationnal
      - Distributed at CERN / CEA Saclay / StonyBrook
    - 2 already produced and being tested



- LASP prototype board
  - Design status of the LASP prototype board
    - Schematic capture being finalized
    - Starting thermal simulations
    - Study of optical fiber routing over the board
  - Routing expected in 2023 Q4
  - Will be tested in 2024
  - Production: 334 boards will be produced by 2026 including 1/4 at CPPM