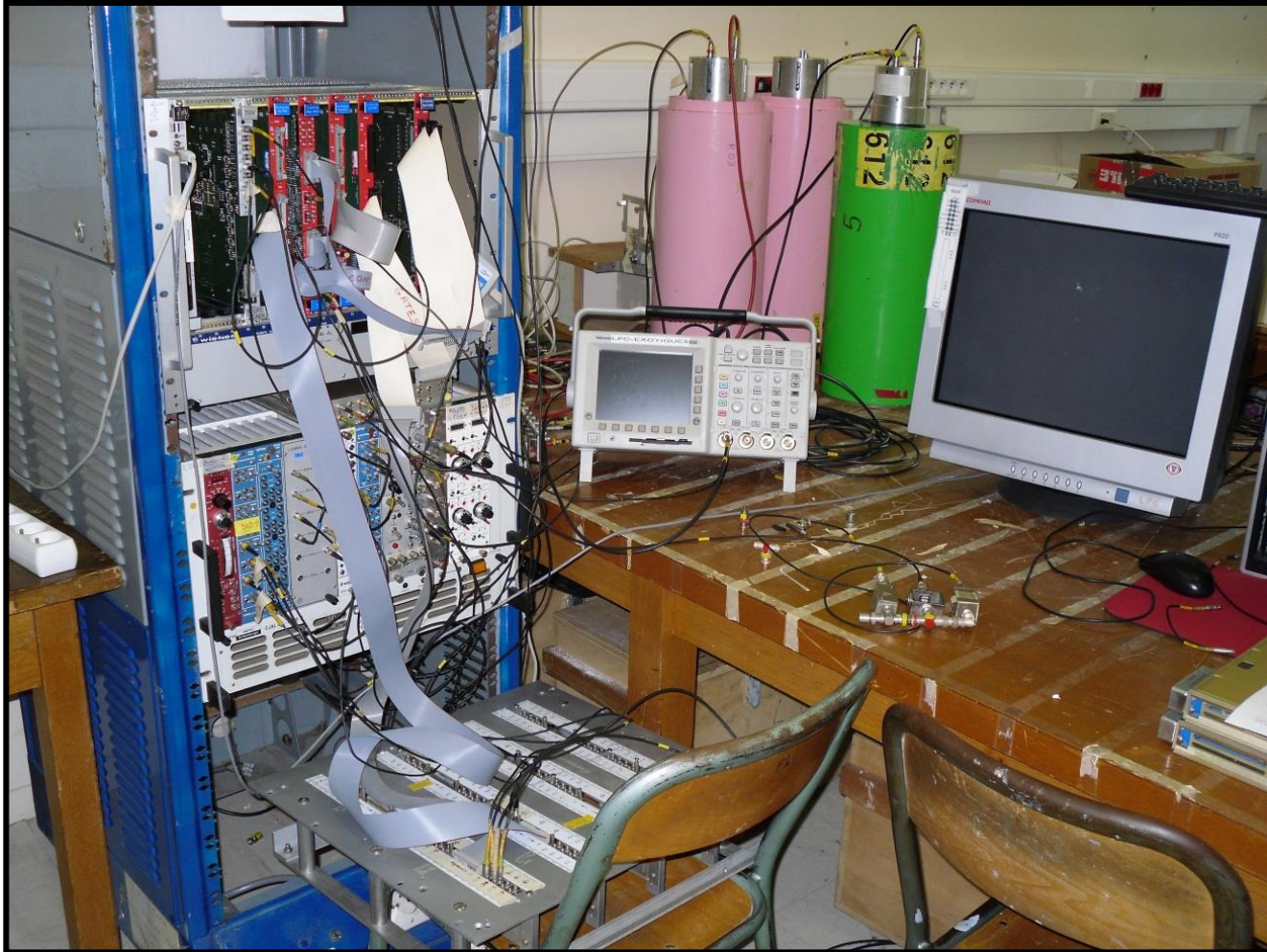


FASTER

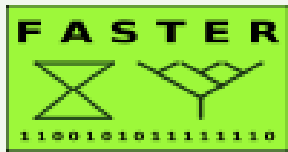
Fast Acquisition SysTEM for nuclEAR Research

**Assemat Julian, Carniol Benjamin,
Chaventré Thierry, Cussol Daniel,
Fontbonne Cathy, Fontbonne Jean-Marc,
Harang Julien, Hommet Jean, Ingouf François,
Langlois Jérôme, Poincheval Jérôme,**

David Etasse

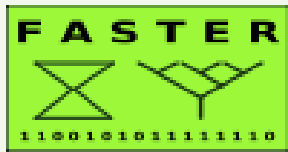






The aim of FASTER is to build a new digital acquisition system with the following constraints:

1. Ensuring at least real time function such as charge, amplitude and time measurements using digital technologies,
2. Use of the most recent commercial components,
3. Use of all modern acquisition techniques (digitalization, data time stamping, serial bus)
4. Use of commercial chassis,
5. Build an adaptable and modular system which can fulfill small size experiments (1 or 2 detectors) requirements as well as much larger experiments (few hundreds of detectors) requirements.



FASTER-V2

1. FASTER-V2 OVERVIEW
2. FASTER-V2 SOFTWARE
3. FASTER-V2 REAL TIME ALGORITHMS

FASTER-V3

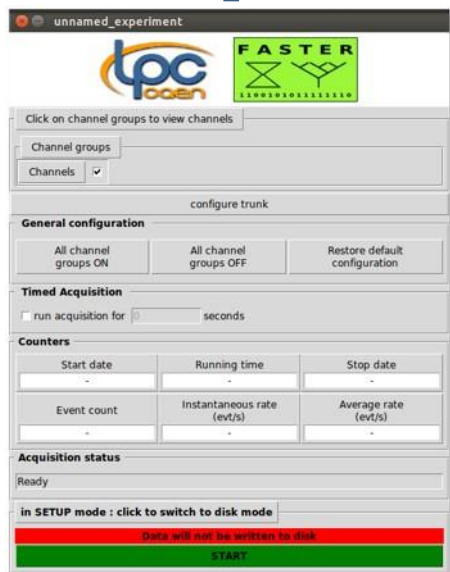
1. FASTER-V3 OVERVIEW
2. FASTER-V3 HARDWARE

SUMMARY



FASTERv2 Overview

Offline Analysis



Ubuntu repository

Real Time Algorithms



Modular Electronic

RHB



Based on Root

STANDALONE SYSTEM



MULTI-CHANNEL SYSTEM



- 4 FADC (125MHz@14bits)
- $\pm 1V$, $\pm 2V$, $\pm 5V$, $\pm 10V$ input range
- 25 MHz Bandwidth



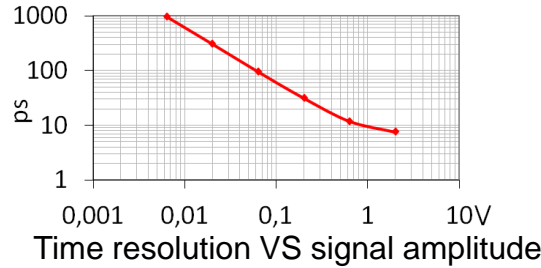
- 2 FADC (500MHz@12bits)
- $\pm 1V$ input range
- $\pm 1V$ input adjustable Offset
- 100 MHz Bandwidth




- DDC316 from TI
- 32 channels
- I-TO-V conversion front end
- 3pC to 12 pC (full scale)
- Integration time range from 10us to 10 ms




- ISEG BPS-Serie - 4W
- $\pm 500 V$ to $\pm 6 KV$







FASTER-CRRC4
FASTER-TRAPEZ-TDC




FASTER-QDC-TDC_{HR}
FASTER-QT2T
FASTER-RF
FASTER-SCALER
FASTER-SAMPLER

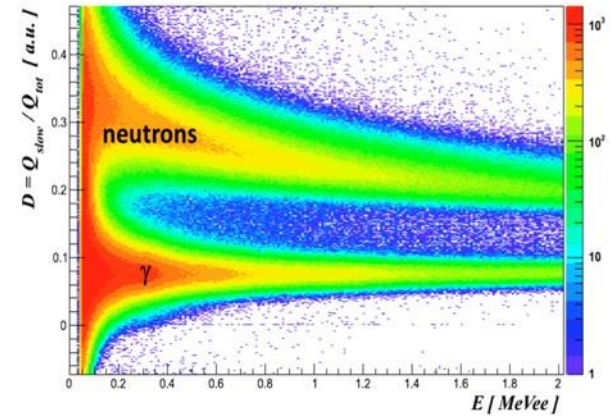




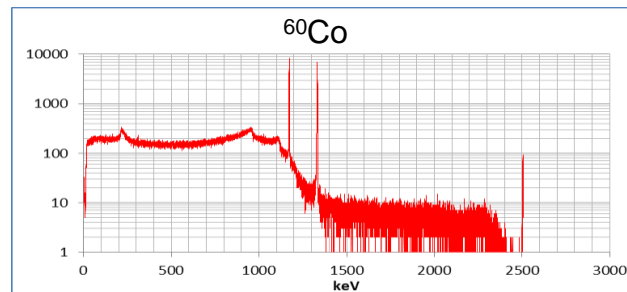
FASTER-ELECTROMETER



FASTER_HV



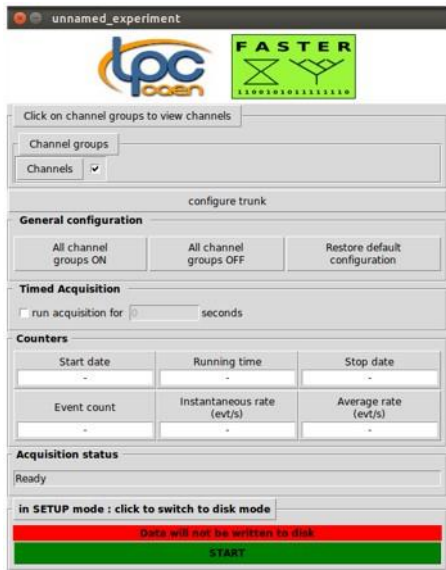
Demon detector, CARAS board,
FASTER-QDC-TDC_{HR}



pic keV	FWHM keV
1173,21	1,71
1332,48	1,90
2505,69	2,41

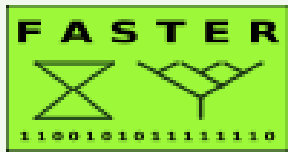
HPGe detector, MOSAHR board, **FASTER_ADC**

Offline Analysis



Ubuntu repository

- Ubuntu 20.04 and 22.04 LTS 64 bits
- ADA, C and Python
- Software trigger multi levels
- Faster repository on LPC Server
 - `sudo apt_get install fasterv2`
- Update the software and the FIRMWARE at the same time
- Offline analysis package
- List of available packages
 - fasterv2, fasterac, rhb,
 - faster-rhb-xxx-demo (xxx=qdc, crc4, trapez, rf,)



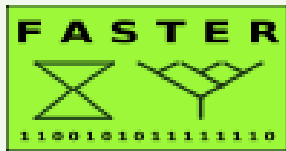
FASTER-V2

1. FASTER-V2 OVERVIEW
2. FASTER-V2 SOFTWARE
3. FASTER-V2 REAL TIME ALGORITHMS

FASTER-V3

1. FASTER-V3 OVERVIEW
2. FASTER-V3 HARDWARE

SUMMARY



FASTERv2 is a digital modular acquisition system from the electronic front end to the histogram builder software developed at LPC.

FASTERv2 is very easy to install, to use with great performances.

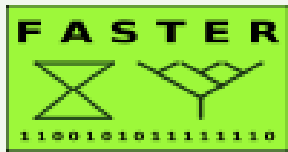
FASTERv2 is able to perform the main nuclear functions with a set of hardware very reduced.

FASTERv2 is wireless 😊.

FASTERv2 is designed to handle medium size experiment (from one to few hundred channels).

FASTERv2 in few numbers

- 80 Systems used (~400 Modules),
- 12 Chassis, 50 Modules (December 2023),
- 2 M€,
- 3.5 FTE,
- 20 Laboratories , 3 Universities



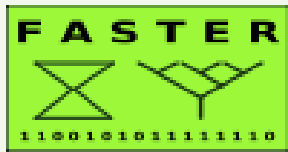
FASTER-V2

1. FASTER-V2 OVERVIEW
2. FASTER-V2 SOFTWARE
3. FASTER-V2 REAL TIME ALGORITHMS

FASTER-V3

1. FASTER-V3 OVERVIEW
2. FASTER-V3 HARDWARE

SUMMARY



FASTERv3 Overview

- Increase number of channels per board,
- Decrease Cost per channel,
- Increase flexibility,
- Ubuntu LTS 64 bits,
- C, C++ and Python,
- First release in 2024-2025.

FASTER-V3

A New real time, digital acquisition platform

Same real time FPGA algorithms as FASTER-V2

+

User algorithms

+

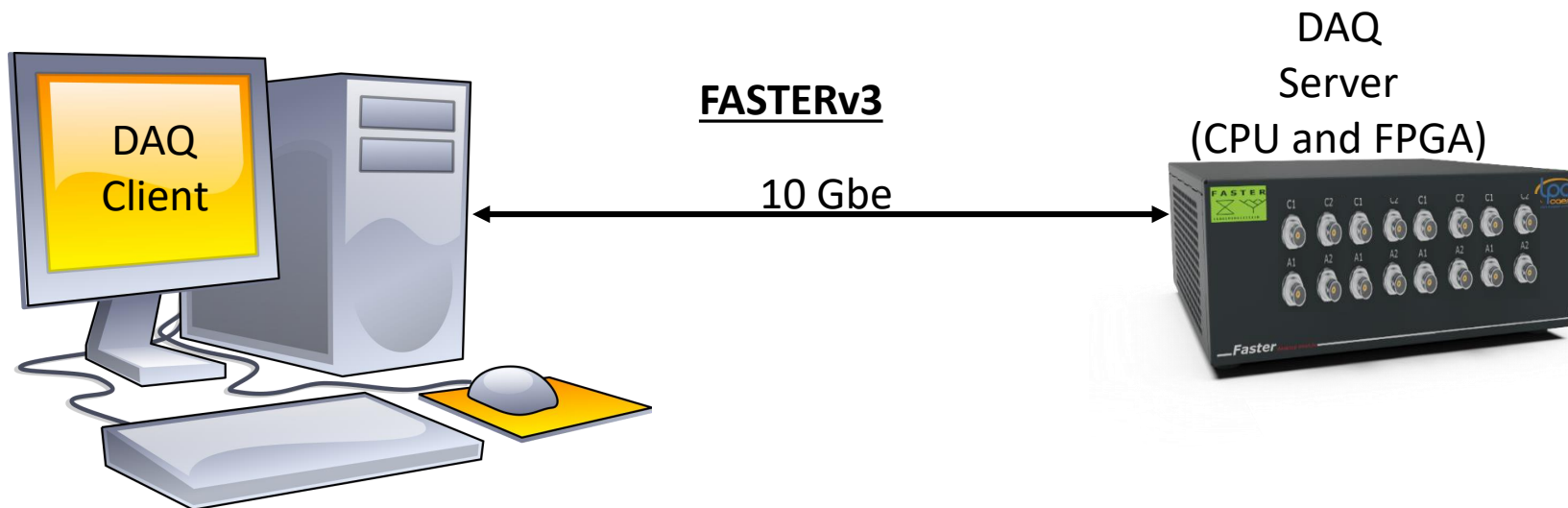
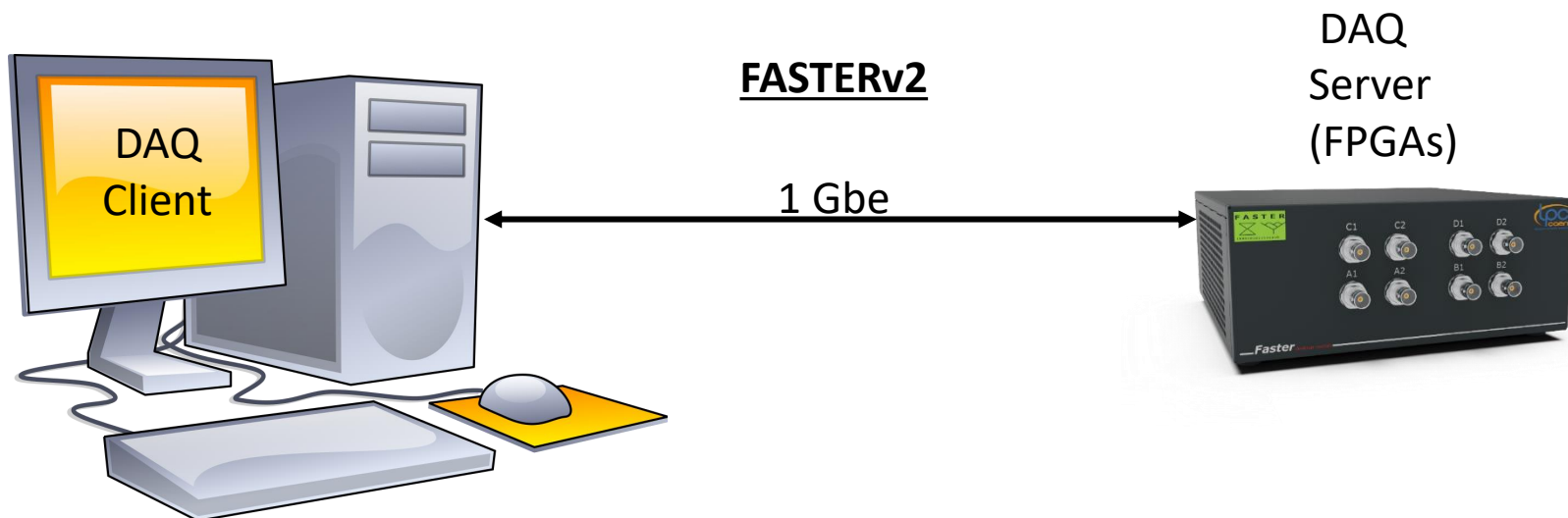
News digitizers (16bits@125 Msps-> 10bits@5 Gsps)

+

TimeD synchronisation

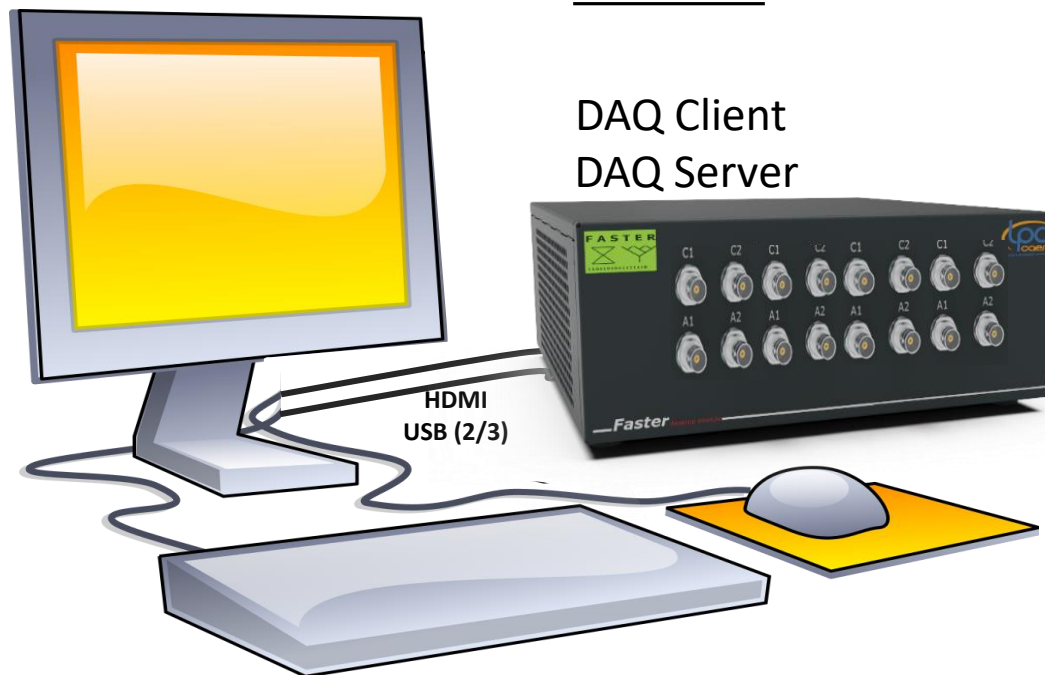
+

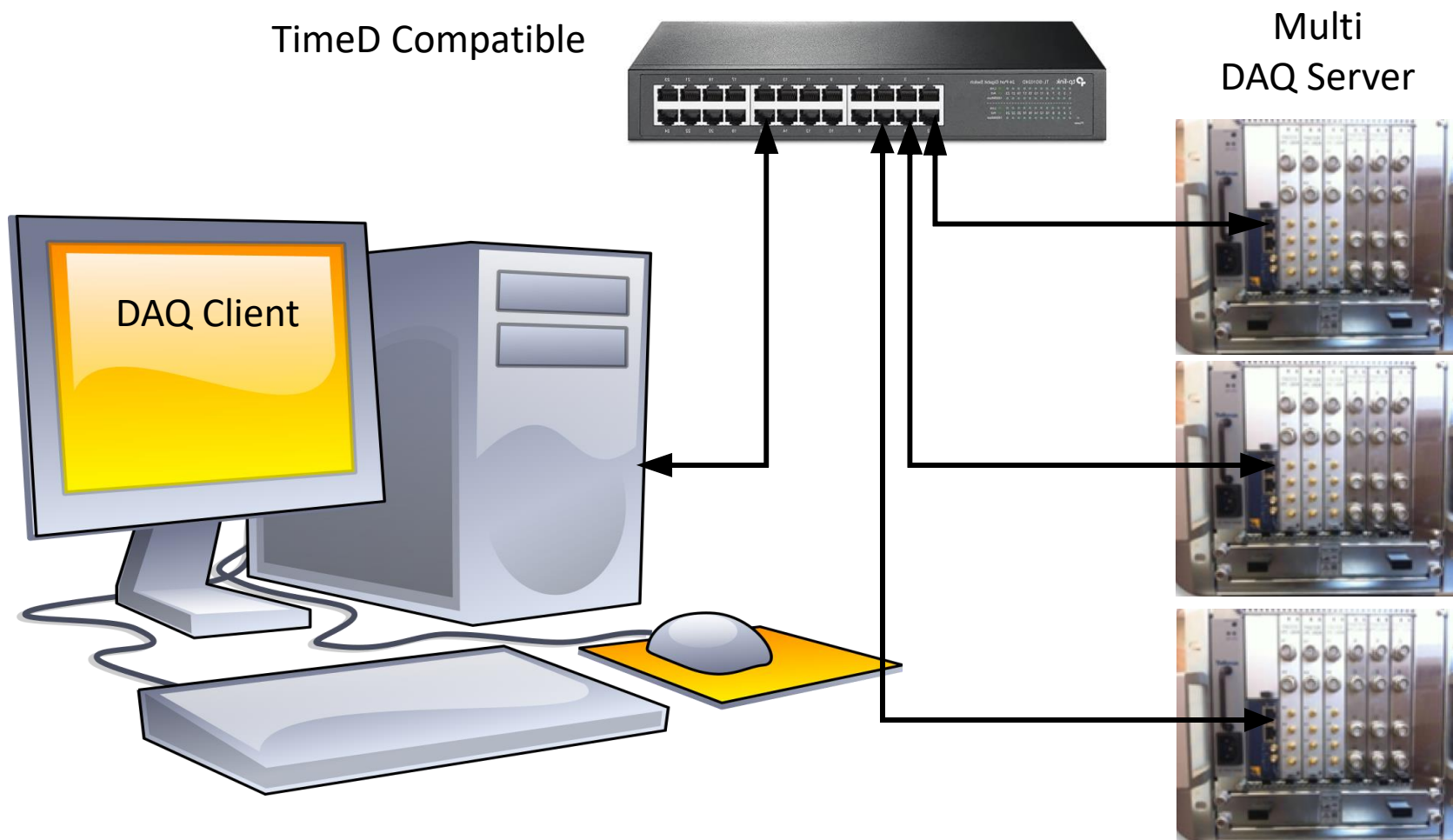
Epics compatible



FASTERv3

DAQ Client
DAQ Server





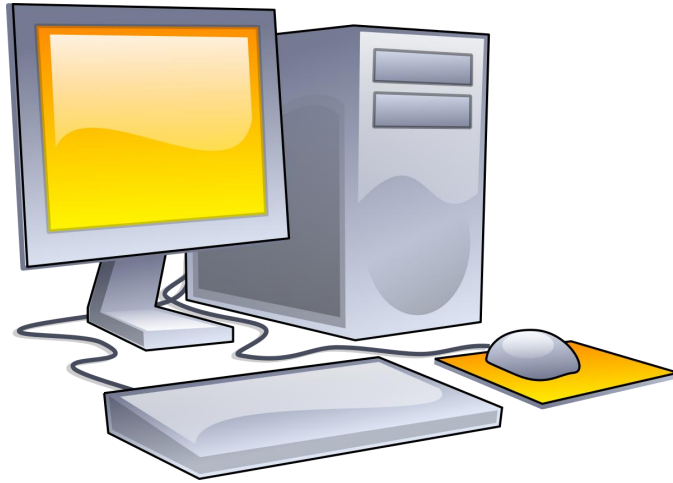
FASTER-V2

1. FASTER-V2 OVERVIEW
2. FASTER-V2 SOFTWARE
3. FASTER-V2 REAL TIME ALGORITHMS

FASTER-V3

1. FASTER-V3 OVERVIEW
2. FASTER-V3 HARDWARE

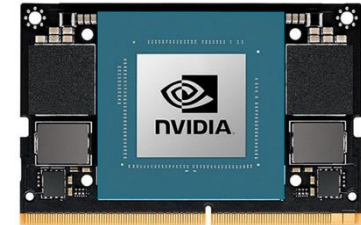
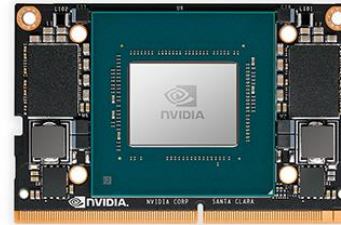
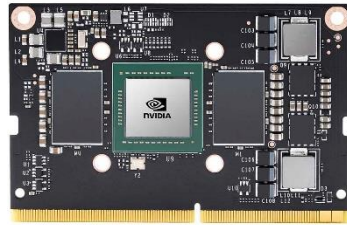
SUMMARY



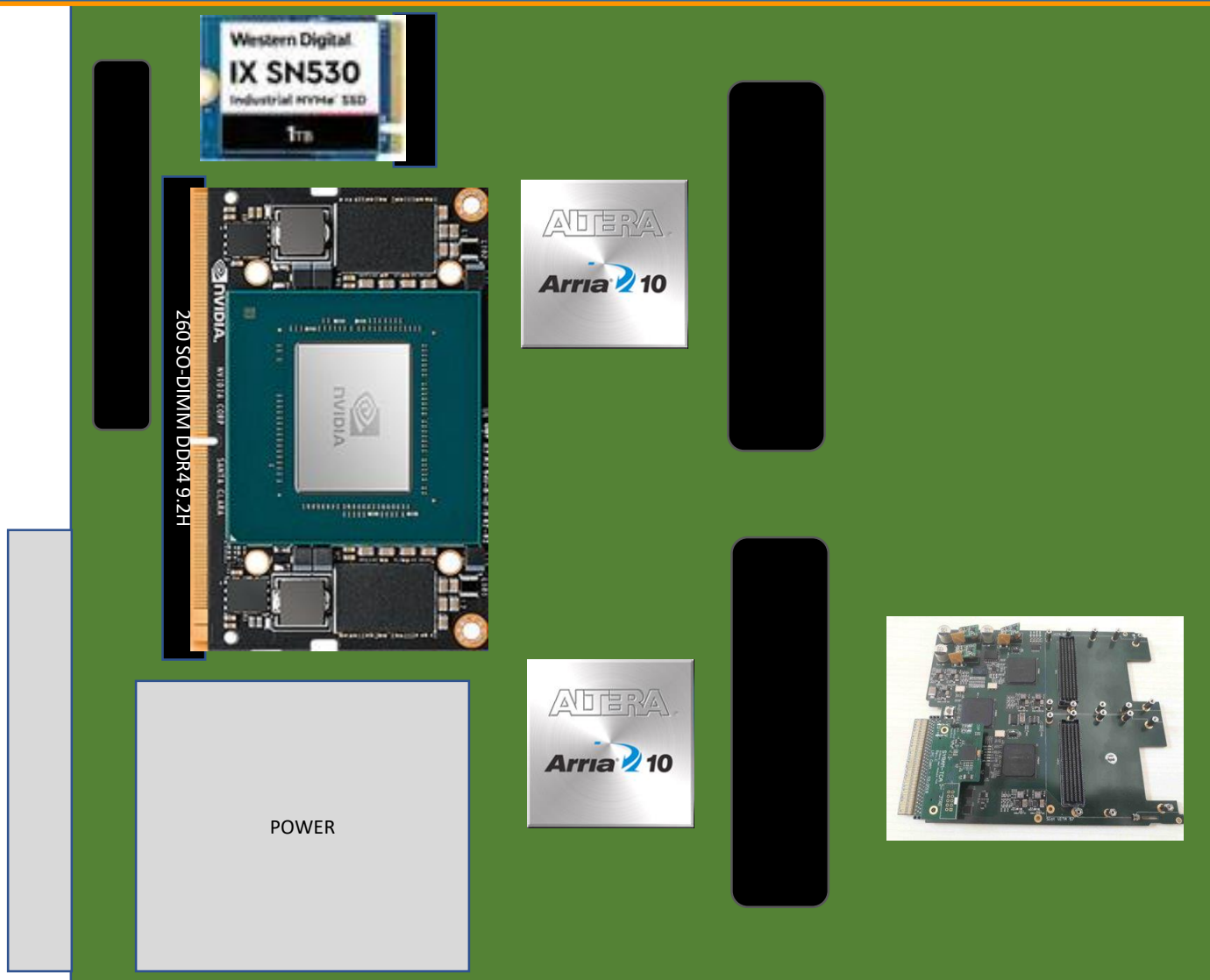
Software
Environnement

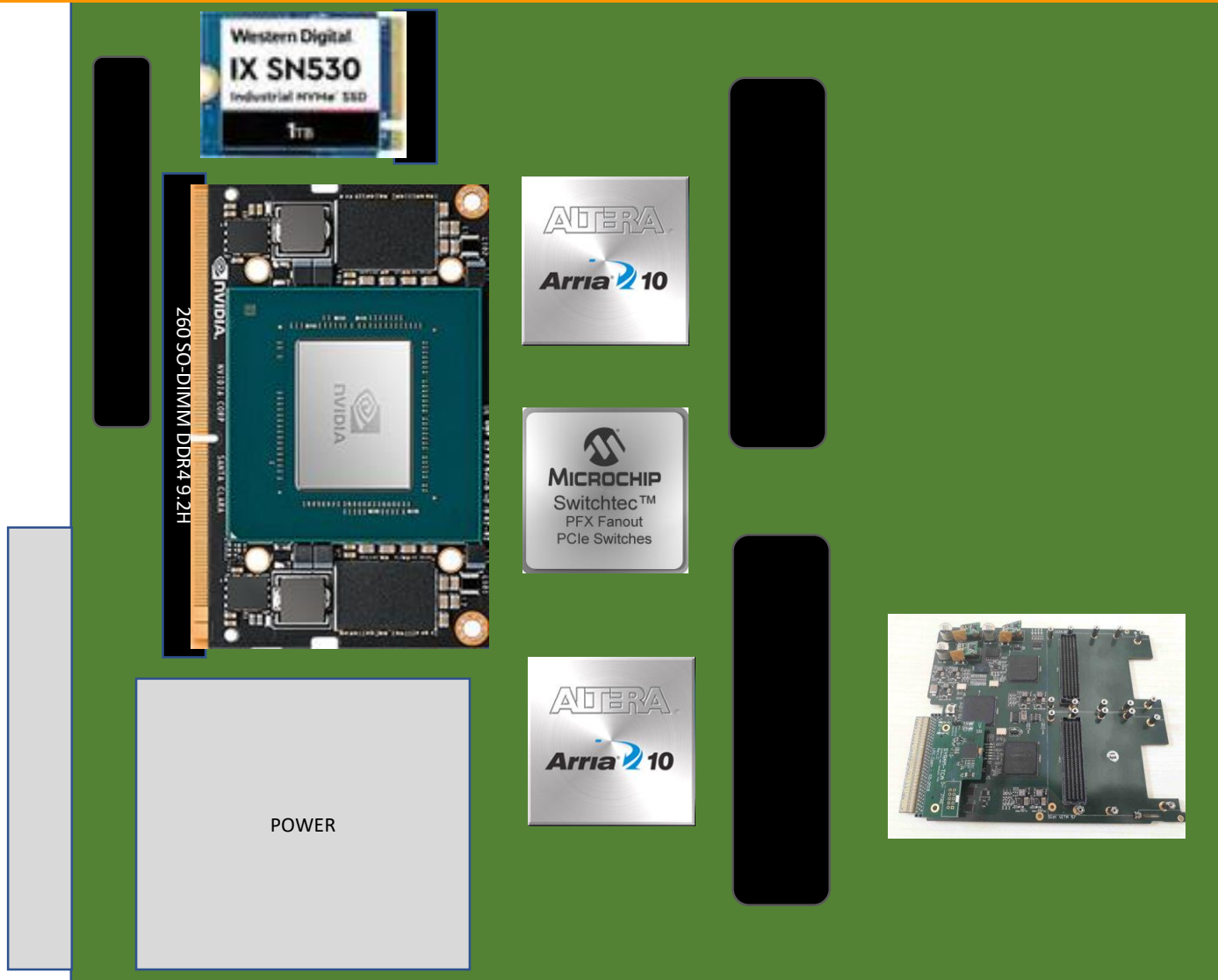
- Ubuntu 20.04
- Cuda 10
- PyTorch
- TensorFlow
- TensorRT
- C/C++





	Jetson TX2 NX 4GB 2017	Jetson Xavier NX 16GB 2020	Jetson Orin NX 16GB 2023
AI Performance	5 TOPS	21 TOPS	100 TOPS
Power	7.5- 15 W	10 W 15 W 20 W	10W - 25W
Cost (HT)	188 €	549 €	663 €

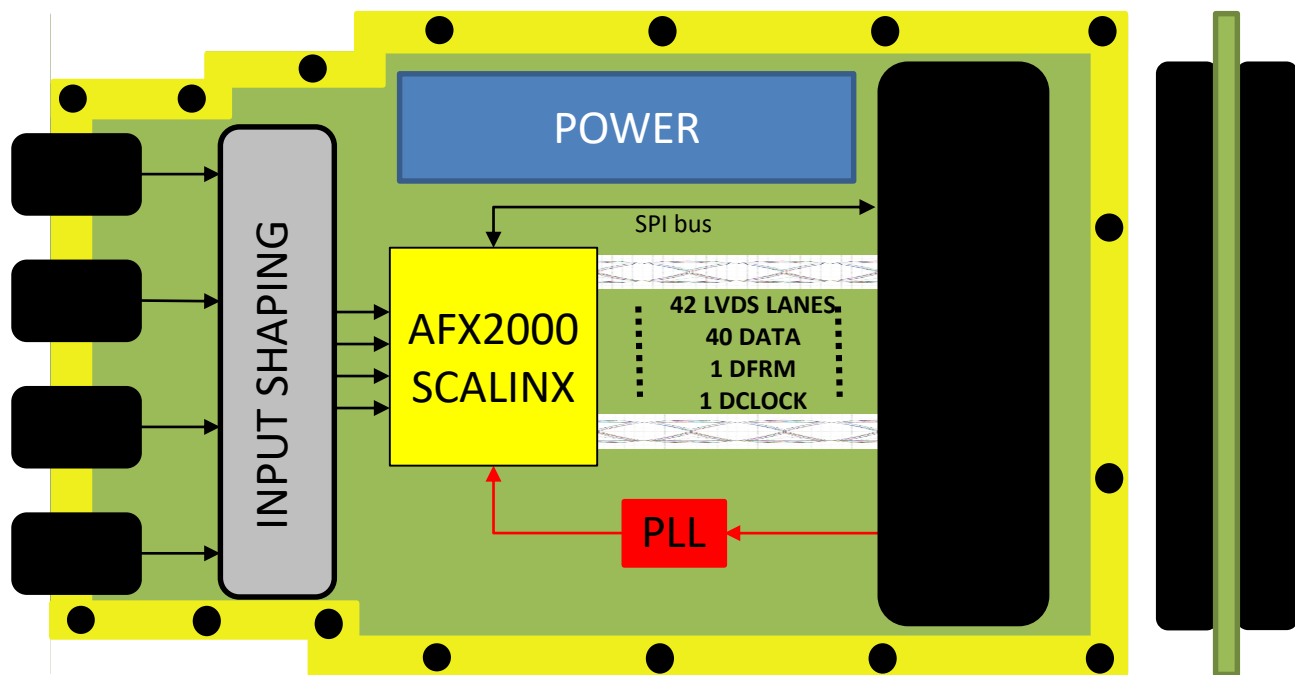
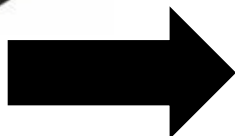






AFX2000
Quad Analog Front-End with 5GSPS ADC
Resolution up to 16-bit and BW up to 300MHz

- 2 FADC (500MHz@12bits)
- $\pm 1V$ input range
- $\pm 1V$ input adjustable Offset
- 100 MHz Bandwidth





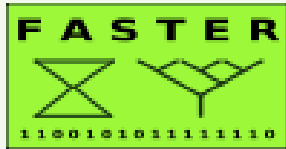
- 7 Double Mid-Size AMC Modules
- 3 FASTER-v3 modules (7 FASTER-v2)
- 48 Channels (28 CARAS, 56 MOSAHR)
- 24 CPU Cores@2Ghz, 3072 GPU Cores@918Mhz, 96 Tensor Cores
- 300 TOPS
- 48 GB RAM
- 3 TB SSD Pcie- Gen4



- 12 Double Mid-Size AMC Modules
- 6 FASTER-v3 modules (12 FASTER-v2)
- 96 Channels (48 CARAS, 96 MOSAHR)
- 48 CPU Cores@2Ghz, 6144 GPU Cores@918Mhz, 192 Tensor Cores
- 600 TOPS
- 96 GB RAM
- 6 TB SSD Pcie- Gen4



- 12 Double Full-Size AMC Modules
- 12 FASTER-v3 modules (12 FASTER-v2)
- 192 Channels (48 CARAS, 96 MOSAHR)
- 96 CPU Cores@2Ghz , 12288 GPU Cores@918Mhz, 384 Tensor Cores
- 1200 TOPS
- 192 GB RAM
- 12 TB SSD Pcie- Gen4



Thank you for
Your Attention