Chips for calibration of the ATLAS LAr calorimeter

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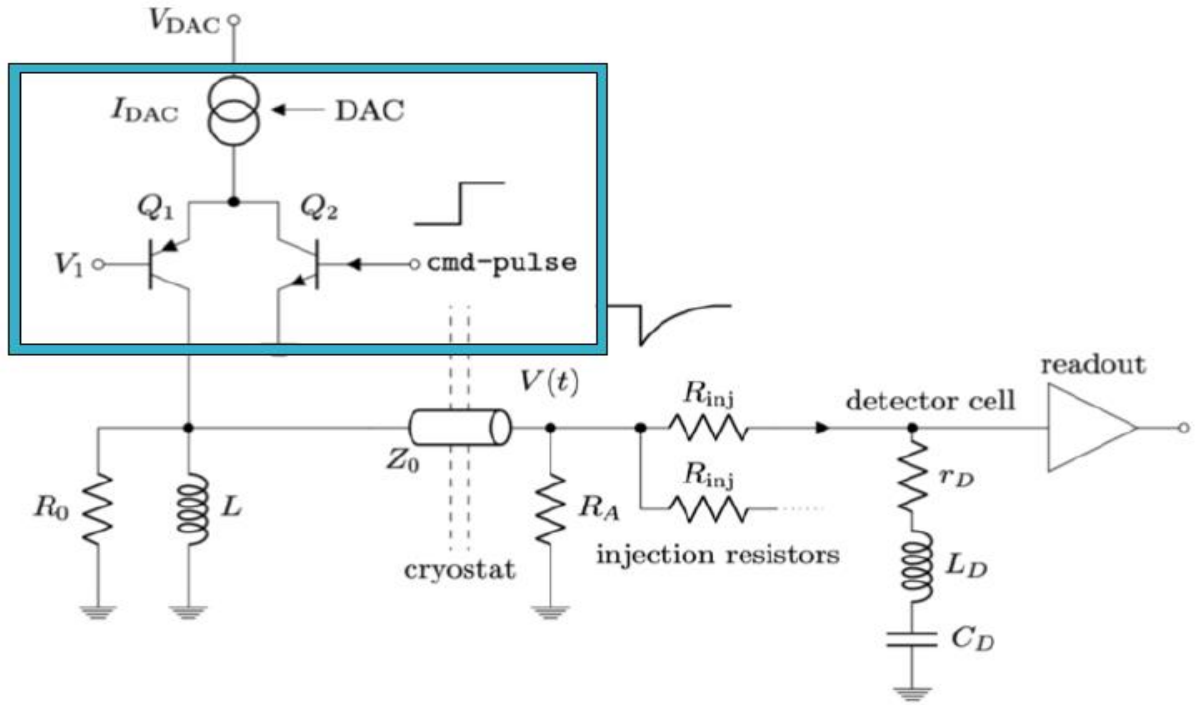
Organization for Micro-Electronics desiGn and Applications

Calibration principle and specifications

The calibration system must provide a high precision test pulse in each channel of the electromagnetic LArg calorimeter.



Pulse specifications:

- High dynamic range : 16 bits

Current from 0 to 320mA divided in 3 ranges

(0-15mA, 15-250mA and 250-320mA)

→ Maximum signal 320mA : 8V on 25 Ohms

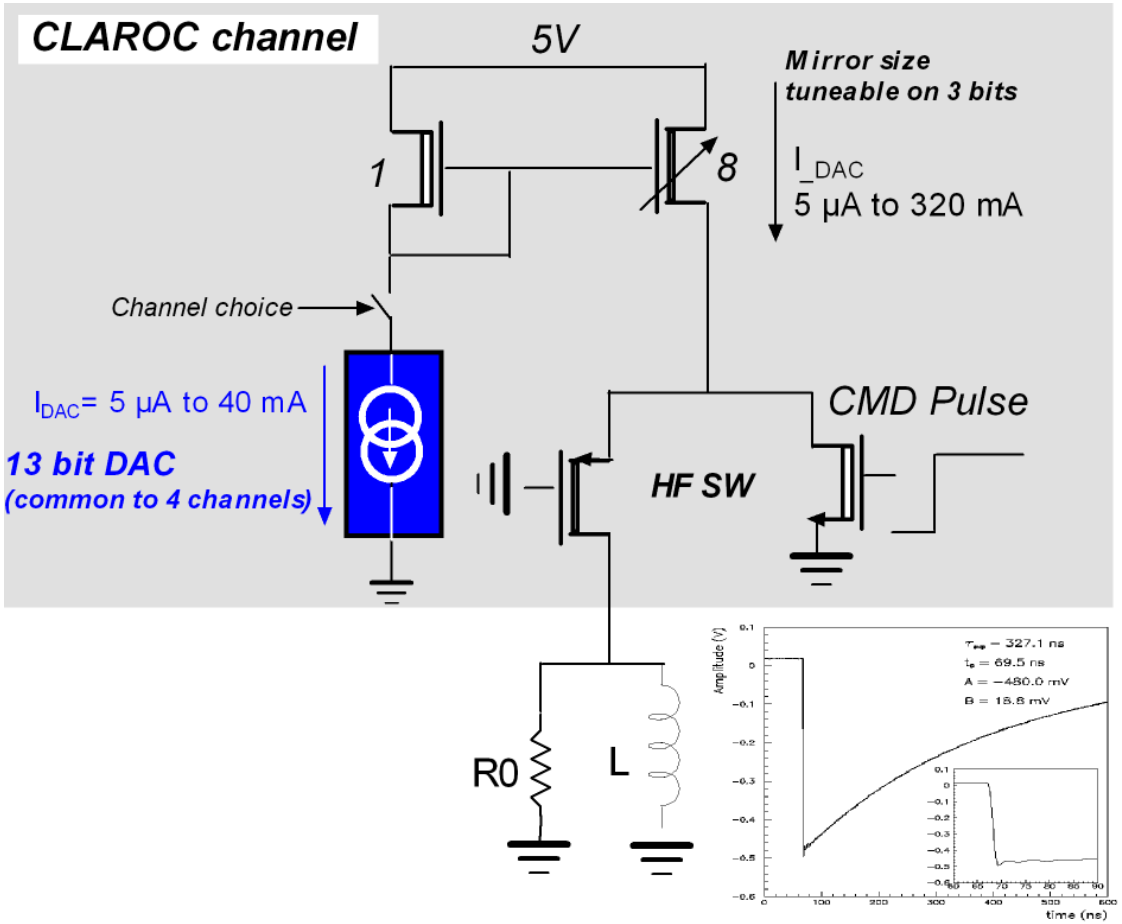
- INL : 1‰ for small range, 2‰ for medium range and 1% for the large range
- Non uniformity between channels < 2.5‰ (< 1‰ out DAC)
- Rad hard : Stable until 1.4 kGy (TID) and 4.1×10^{13} neq/cm^2 (NIEL)
- Drived by new control system (lpGBT)

Keep same calibration board with 128 channels

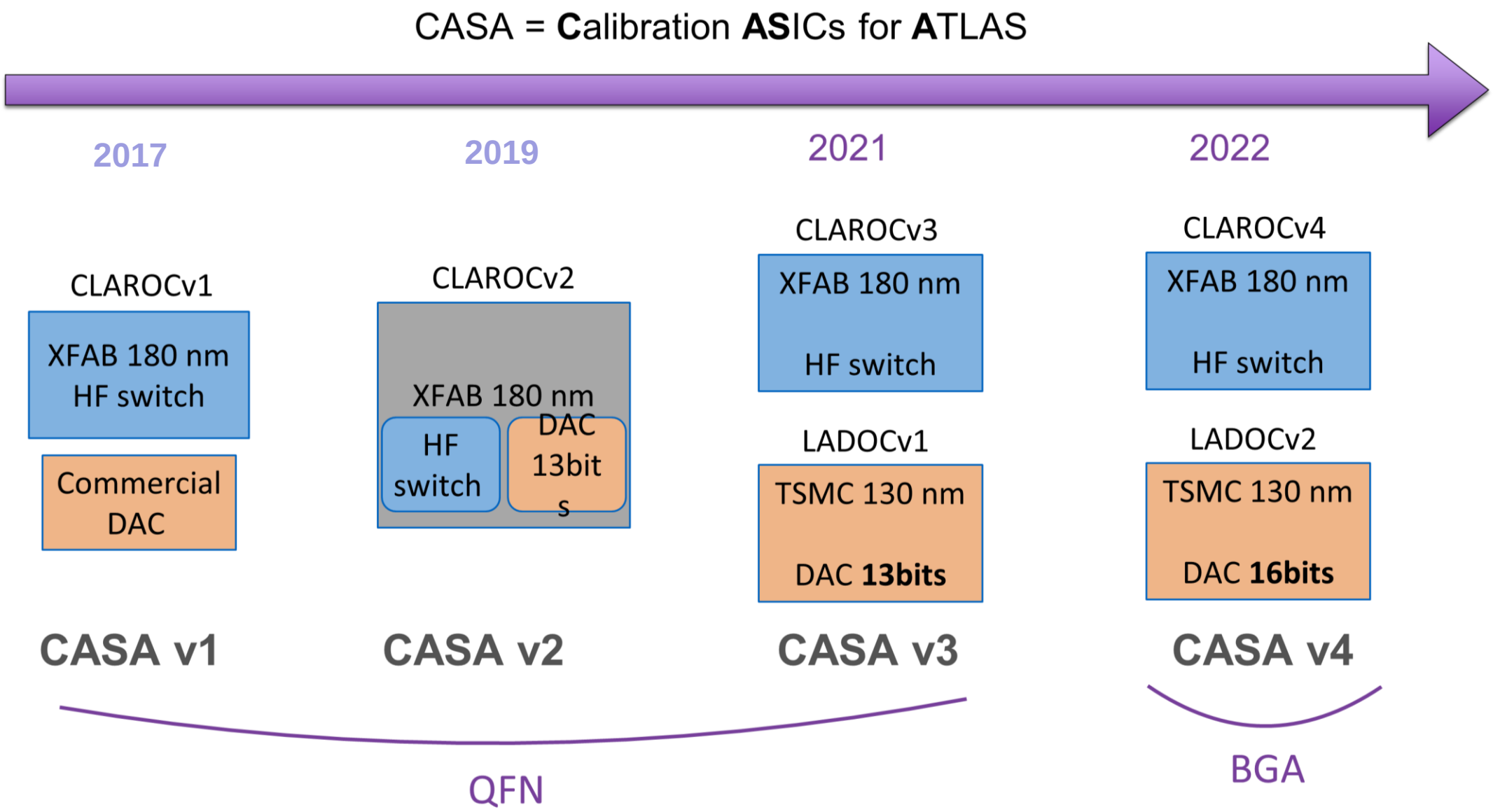
CLAROC : Calibration of Liquid ARgon Output Chip

→Chosen technology : **XFAB**
XT018 180nm CMOS HV SOI

- Deep trench isolation
- Low (1.2V) and medium voltage (5 and 10V) MOS
- 6 metal layers : 4 standard (90mΩ/□ - 1mA/µm) + 2 thick layers (45mΩ/□ - 1.6 mA/µm + 10mΩ/□ - 6mA/µm)



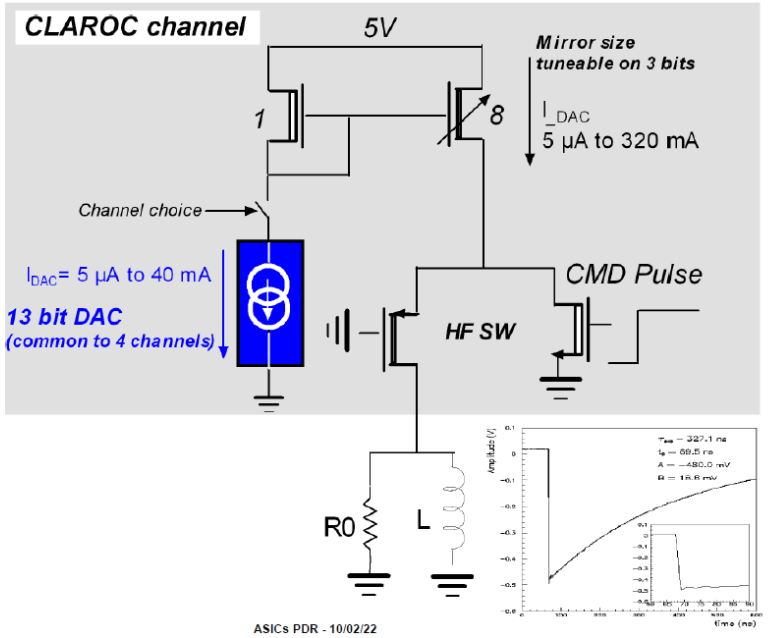
Developments for calibration upgrade : ASICs evolution

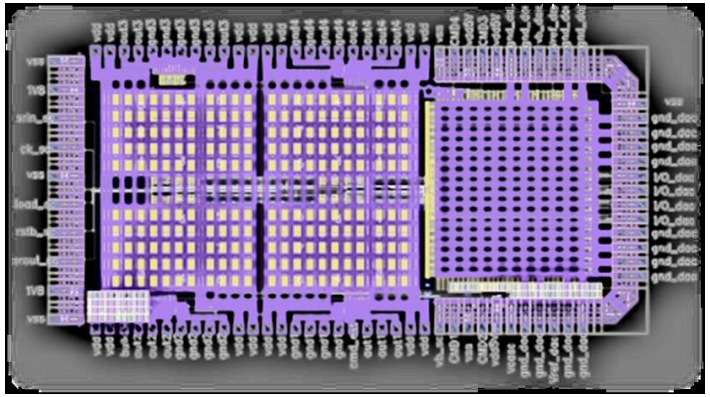


CLAROC2 principle:

In June 2019 : **CLAROC2** complete chip in XFAB :

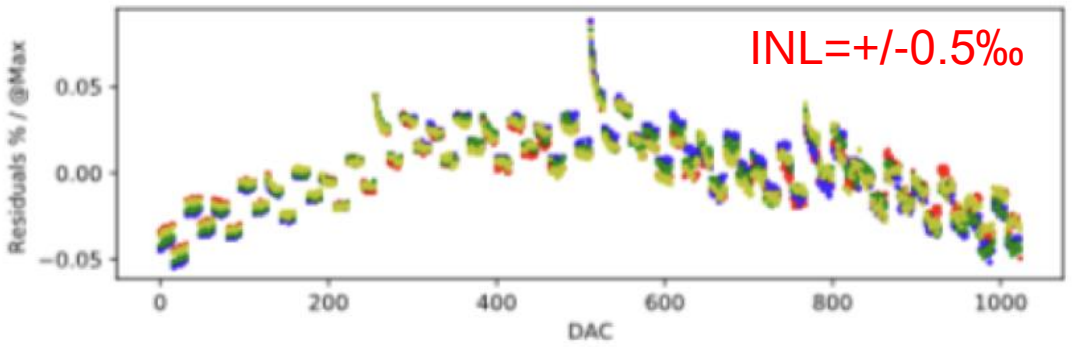
- 4 HF switches
- 16-bit DAC current :
  - A common 13-bit DAC = 10-bit DAC made by scaled current mirrors for the 10 LSB (5µA to 5mA) for precision + 7 current mirror thermometers for the 3 MSB (5mA to 40mA) (Ludovic Raux)
  - 3-bit tuneable gain (1 to 8) current mirror in each channel to choose the dynamic range (0 to 40mA, to 80mA, …to 320mA)
- shift register as slow control for chip configuration (29 SC bits in 1.2V)
  - 17 bits for 13-bit DAC
  - 8 bits for current mirror (common for the 4 channels)
  - 4 bits to validate the 4 channels
- Chips received december 2019



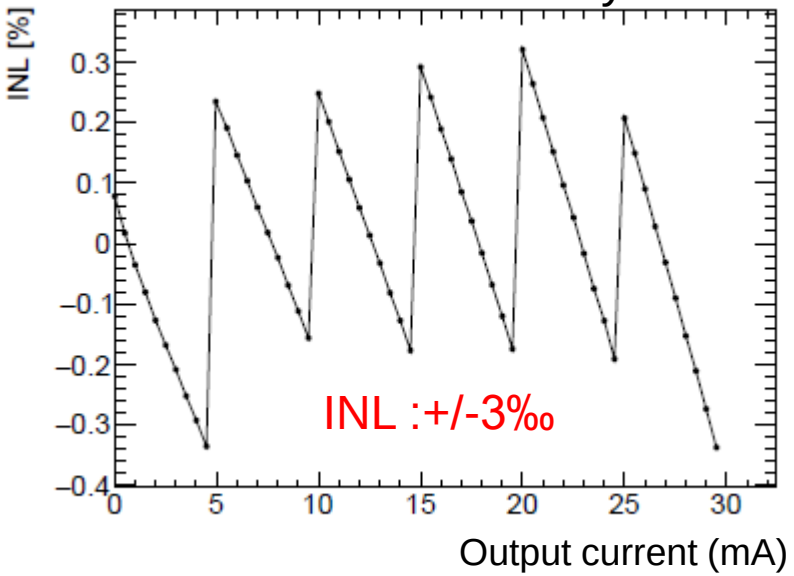


CLAROC 2 DAC measurements

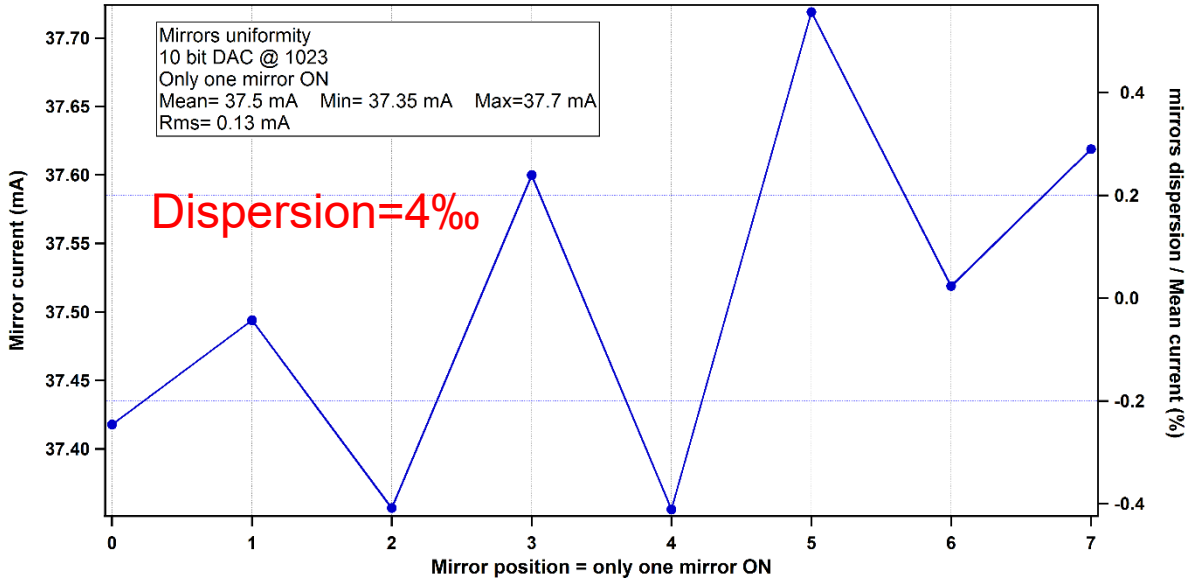
10-bit DAC INL (%)



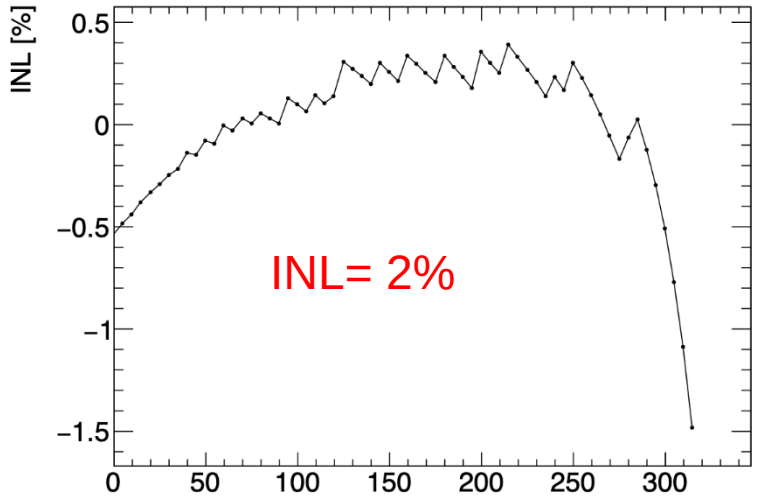
13-bit DAC linearity



current mirrors gain dispersion



16-bit DAC linearity



CLAROC2 main results

Many measurements was done on testbench and under irradiation (X-ray and protons).

- The HF switch passes the specification in the whole current range but linearity is not good enough (-> improve mirror layout).
- Injected charge is under control
- After irradiation, the HF switches are still OK.

The results show 2 main problems :

- Non linearity on the 16-bit DAC is larger than expected : +/-1%

  Mainly due to steps between each thermometer and each mirror

  →The layouts of DACs and mirrors could be improved to avoid steps

- And above all, under irradiation, the 1.2V MOS Vt shifts a lot and slow control become non operational.

  → We can't use this kind of SC and shifts may affect the 13-bit DAC accuracy

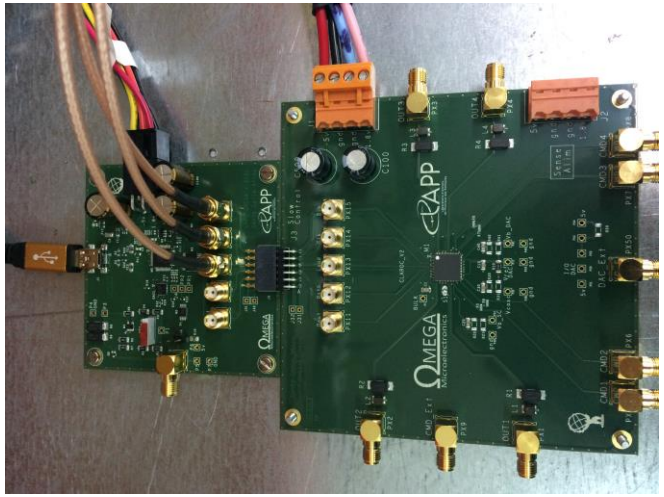
→ Proposed solution: separate the 2 functions

- The HF switches remain in XFAB(we need the 5V and 10V MOS)

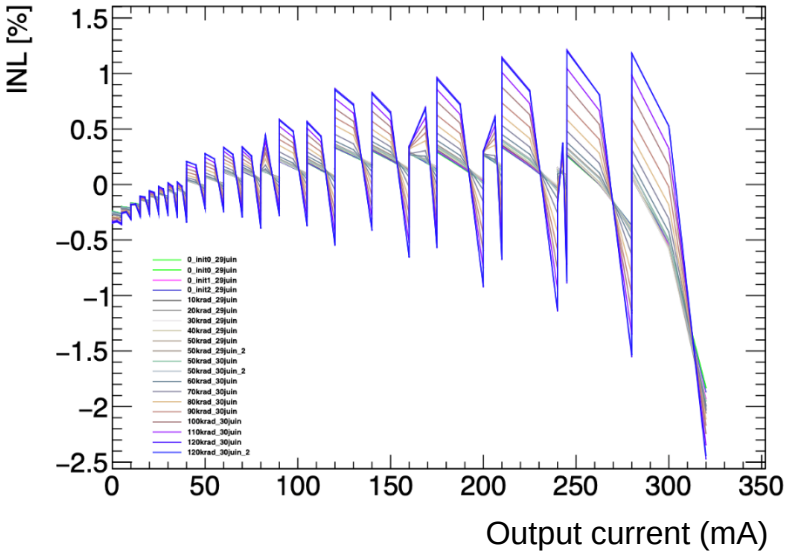
  ➡ **CLAROC3**

- The 13-bit DAC is done in the well known TSMC130

  ➡ **LADOC**

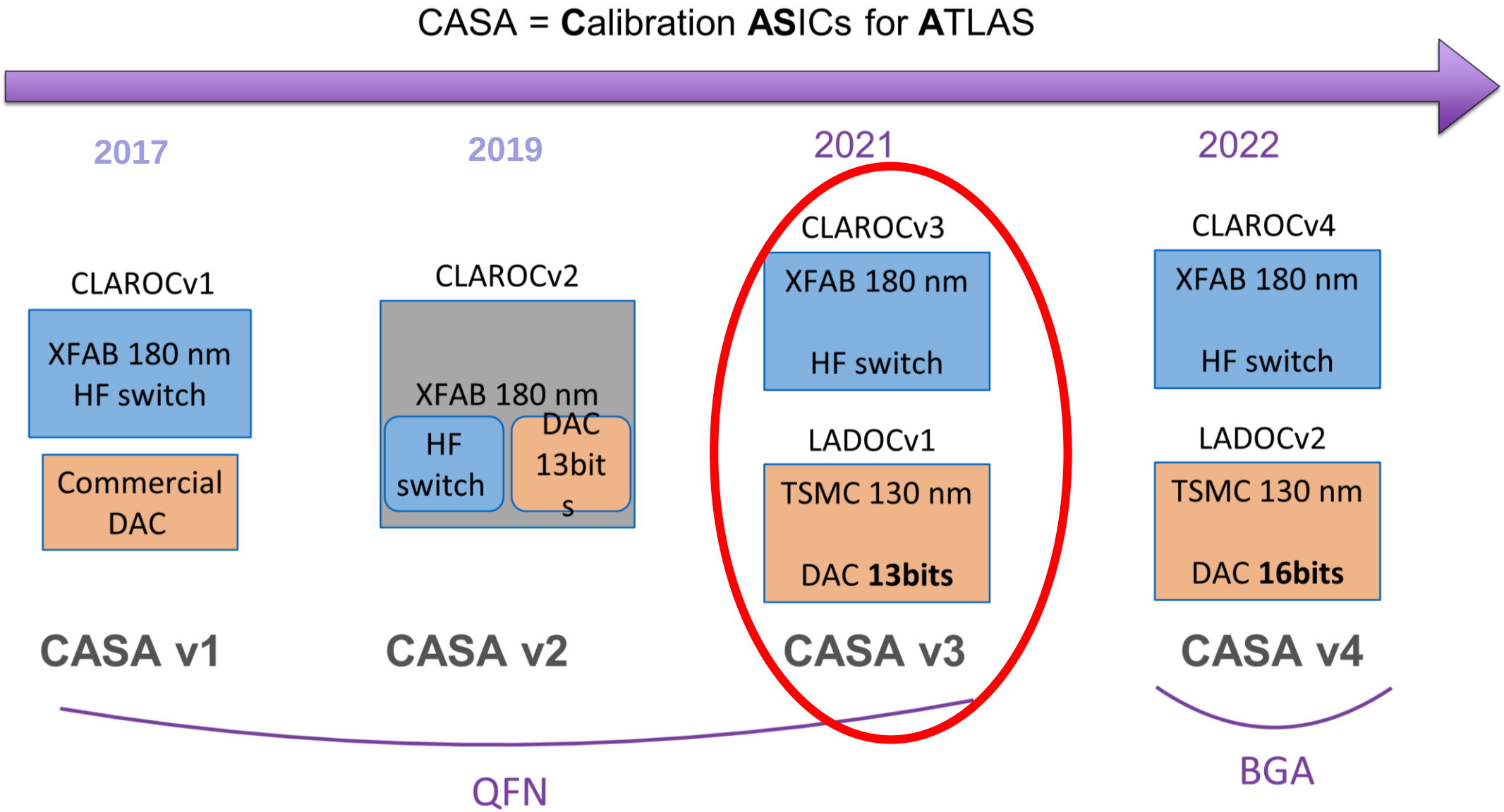


Test board CASA1 (LAPP)



INL under irradiation

Developments for calibration upgrade : ASICs evolution

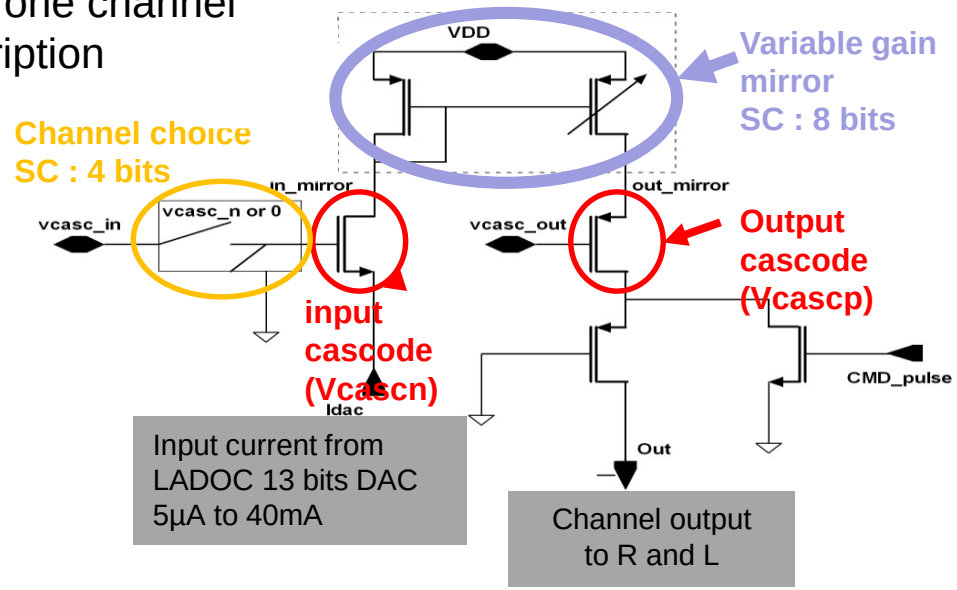


CLAROC3 + LADOC1 principle

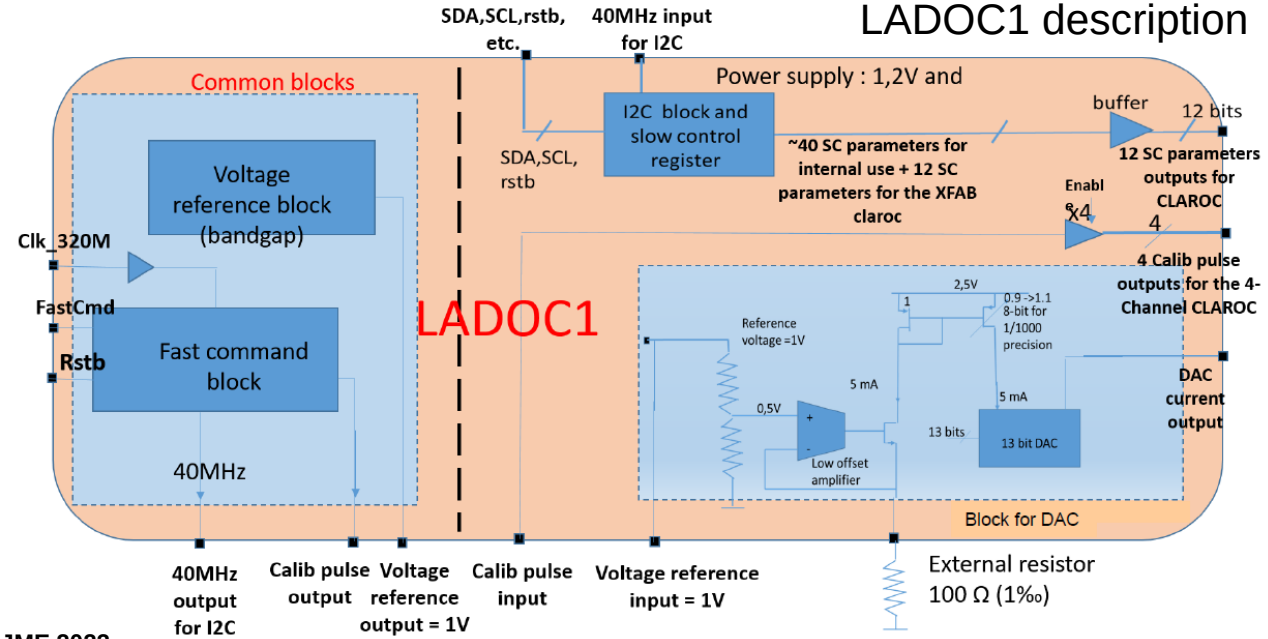
- In August 2020 : **CLAROC3** in XFAB 180nm
  - 4 identical channels
  - with HF switch and 3-bit DAC (mirror gain)
  - All slow control (12 bits) are provided externally and need level translators (1.2V to 5V)
  - Command pulses need fast translators (1.2V to 5V)

- In December 2020 : **LADOC (**Link And DAC Of Claroc) in TSMC130
  - 13-bit current DAC
    - 13-bit DAC (from 5uA to 40mA) : 2 different types of DAC (LADOC1 and 1A)
    - Accurate 8-bit tuneable current source for the DAC
  - Chip provides reference voltage (CERN Bandgap)
  - Chip provides command pulses via a fast command module (re-used from HGCROC)
  - I2C Slow control for both chips (LADOC itself and and CLAROC) (re-used from HGCROC)

CLAROC3 : one channel description



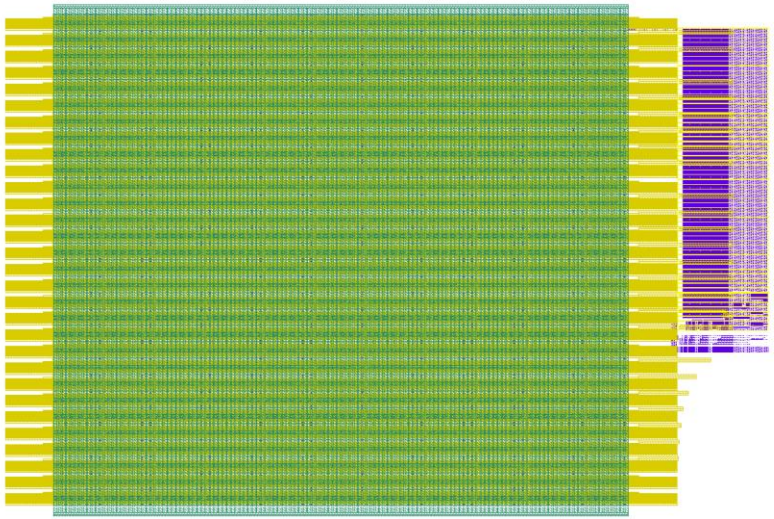
LADOC1 description



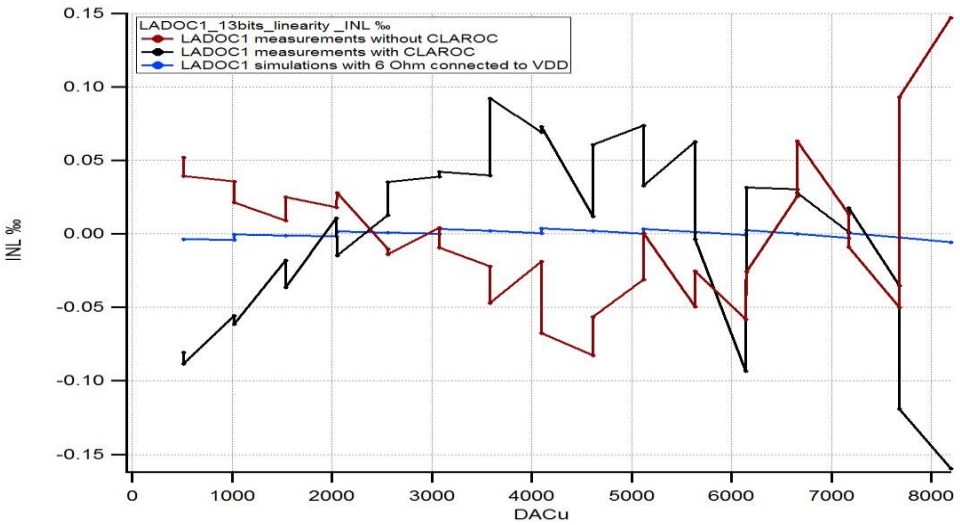
LADOC 13-bits DAC

LADOC1 and LADOC1A : 2 DAC architectures submitted (2 different chips):

- Both are based on a 10-bit DAC with ratioed mirror + 3 bits for MSB with « thermometer » DAC
- One made with very long transistors functionning in triode mode + scaled switches (elementary cell : W=1.5µm ; L=4x20µm) ->LADOC 1
- The other more classical (elementary cell : W=20µm ; L=6µm) with switches connected to the gates ->LADOC 1A

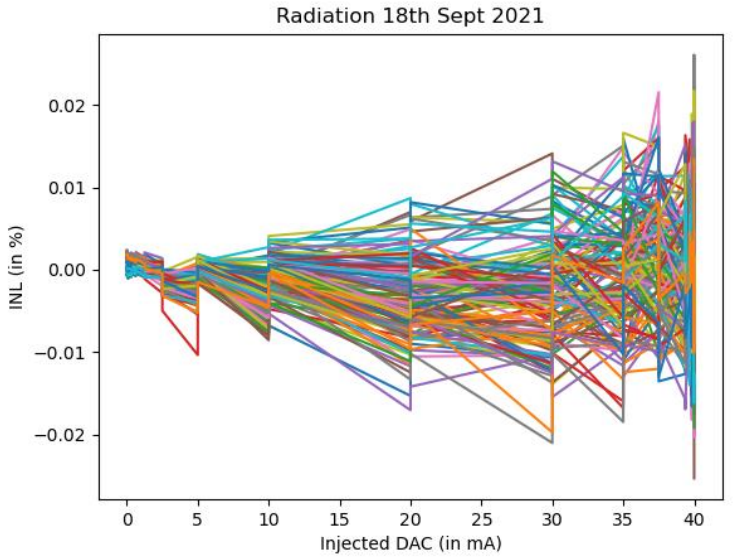


LADOC1 layout (1.9mmX1.4mm)



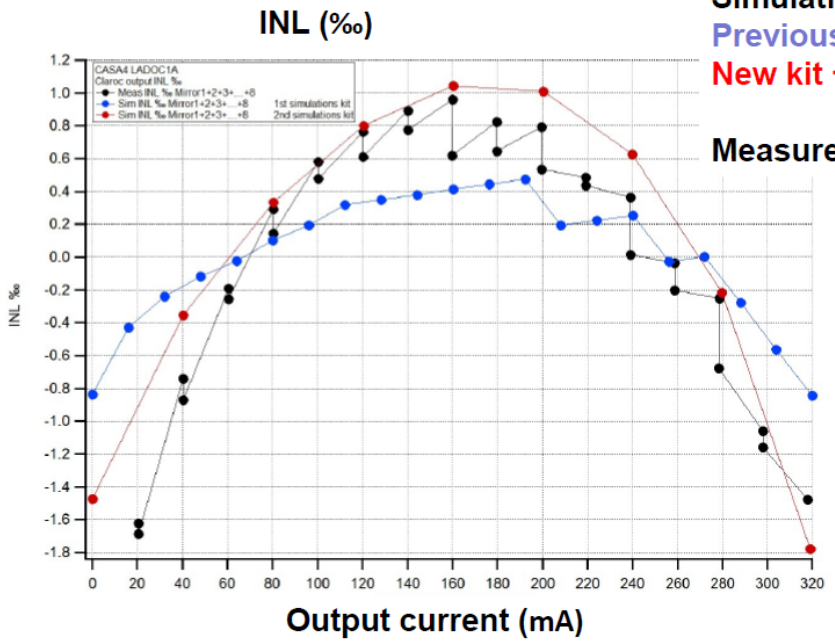
INL LADOC1 13Bit-DAC:

- **LADOC Simulations (blue) → 0.1‰**
- **LADOC output measurements without Claroc connected (red) → +1.5‰ /-0.5‰**
- **LADOC output measurements with Claroc connected (black) → +0.5‰ /-1.5‰**



LADOC1 INL measurements under irradiation

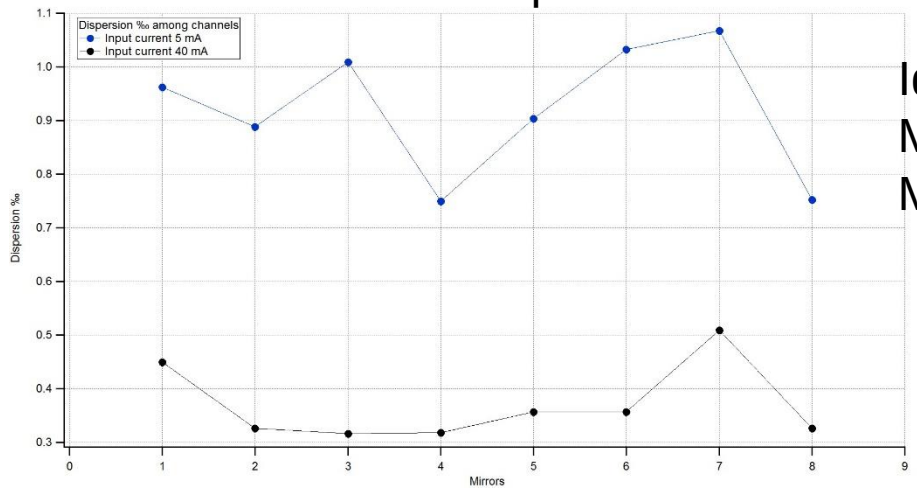
CLAROC3 measurement



Simulations :
Previous kit → INL 1.2 ‰
New kit → INL 2.5 ‰

Measure → INL 2.7 ‰

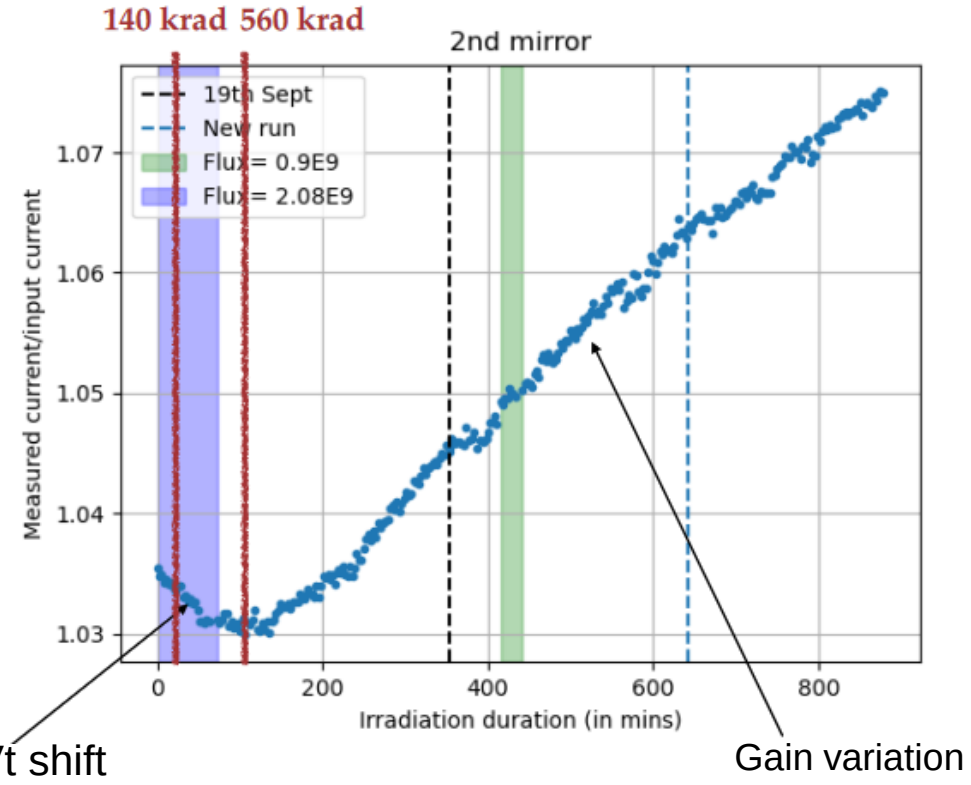
Gain of each mirror dispersion measurement



Idac=5mA
Meas. RMS ~ 1 ‰
MC simu ~ 0.1 ‰

Idac=40mA
Meas. RMS ~ 0.4 ‰
MC simu ~ 0.07 ‰

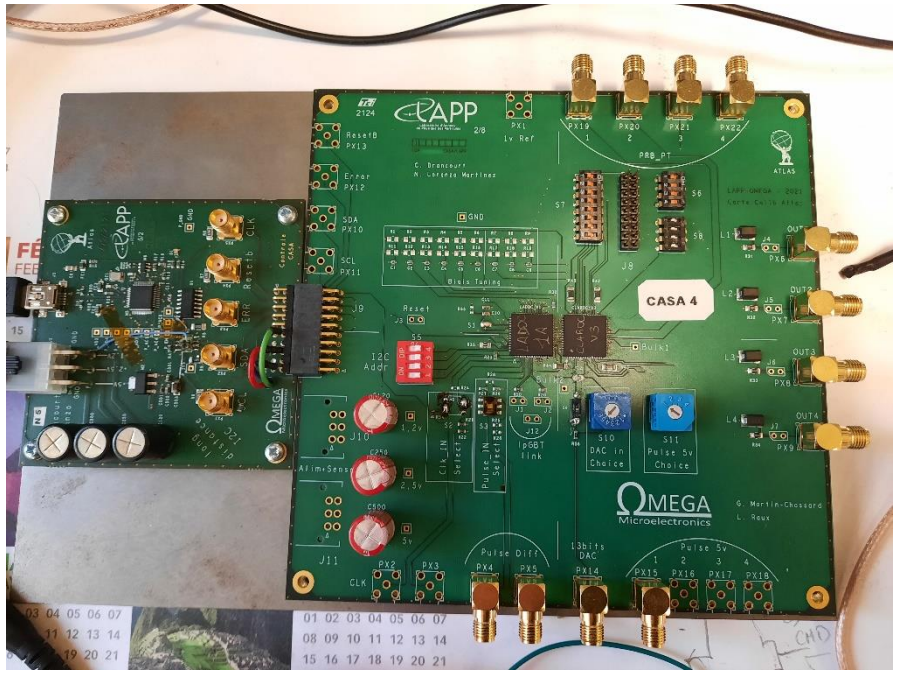
Mirror gain dispersion in irradiation at PSI



The gain increase with dose :
however this effect is not a proton effect but a TID effect, and the corresponding TID dose is 2.5 Mrad
→ Staying in the 140 krad range, no gain increase seen

Measurement results on LADOC1 and CLAROC 3

- LADOC chip now fulfills specifications for both variants
  - All functionalities are OK (I2C, fast command block, etc.)
  - Excellent linearity in its range (0-40 mA), much better than 1‰
  - Excellent radiation resistance
    - no degradation of the linearity seen even after 35 times the required TID dose
    - I2C in its normal autocorrecting mode is not affected by protons beams up to two times the required NIEL dose
  - LADOC1 performs slightly better than LADOC1A



Testboard CASA3 (for CLAROC3 and LADOC1) designed at LAPP

- The CLAROC3 pulser alone (not changed compared to V2) :
  - Non-linearity degrades the LADOC1 good results
  - Good HF switch transistor properties under irradiation
  - Translators for slow control and fast command signals no longer work in radiative environment. (1.2V level not enough against Vt shift)

Propositions for improvement

→ We are not able to compensate the mismatch of the XFAB techno and this mismatch is poorly simulated : we will use the mirror with constant gain and move the high end 3 bits (MSB) of CLAROC to low end 3 bits in LADOC (LSB)

→To improve linearity and compensate the Vt shift of the irradiated transistors we must add an amplifier to improve the mirror gain

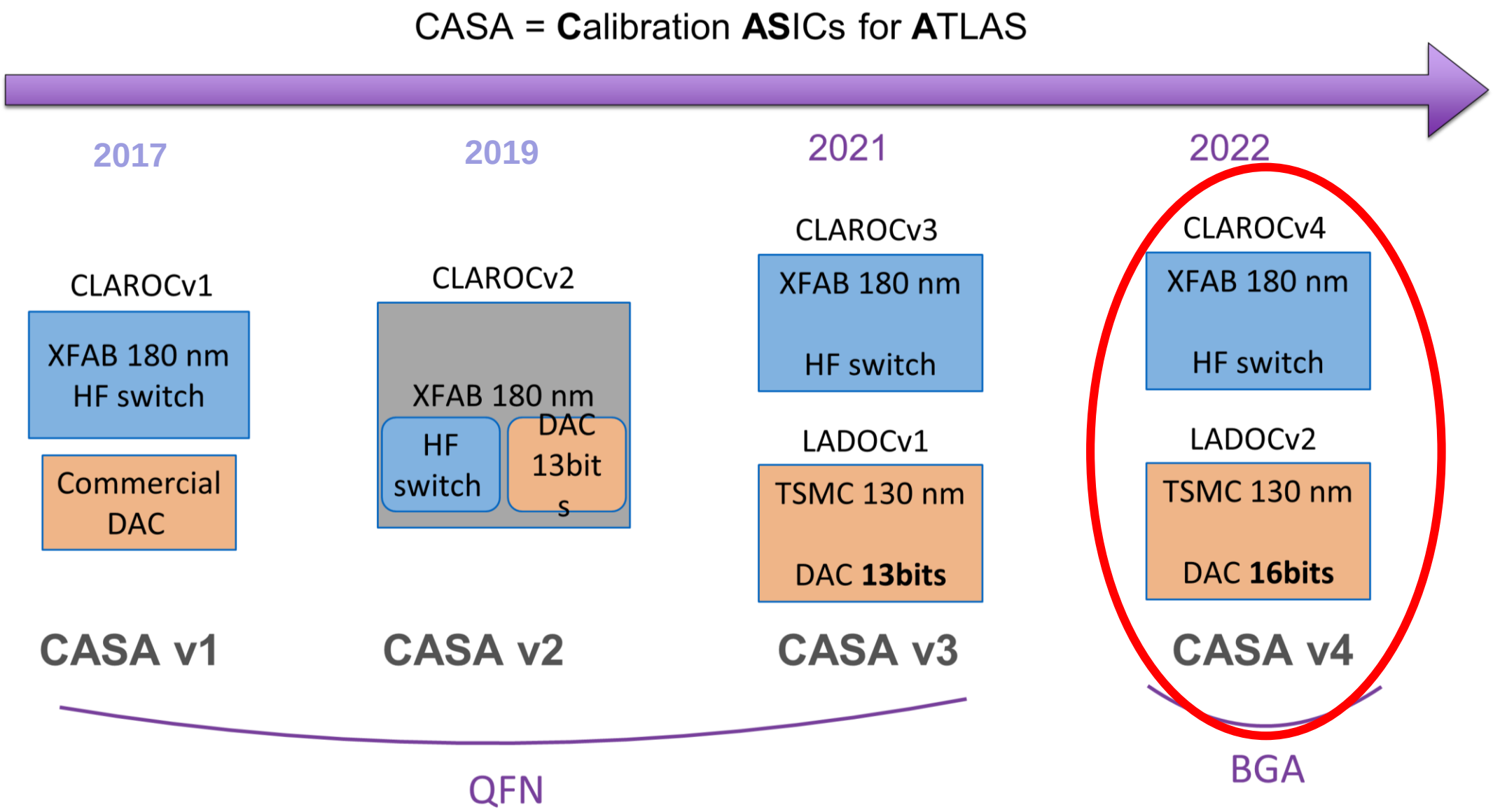
→ To improve the slow control translator and fast command translator we will used 2.5V signals instead of 1.2V one

→ To uniformize the packages used in Larg Calorimetry :

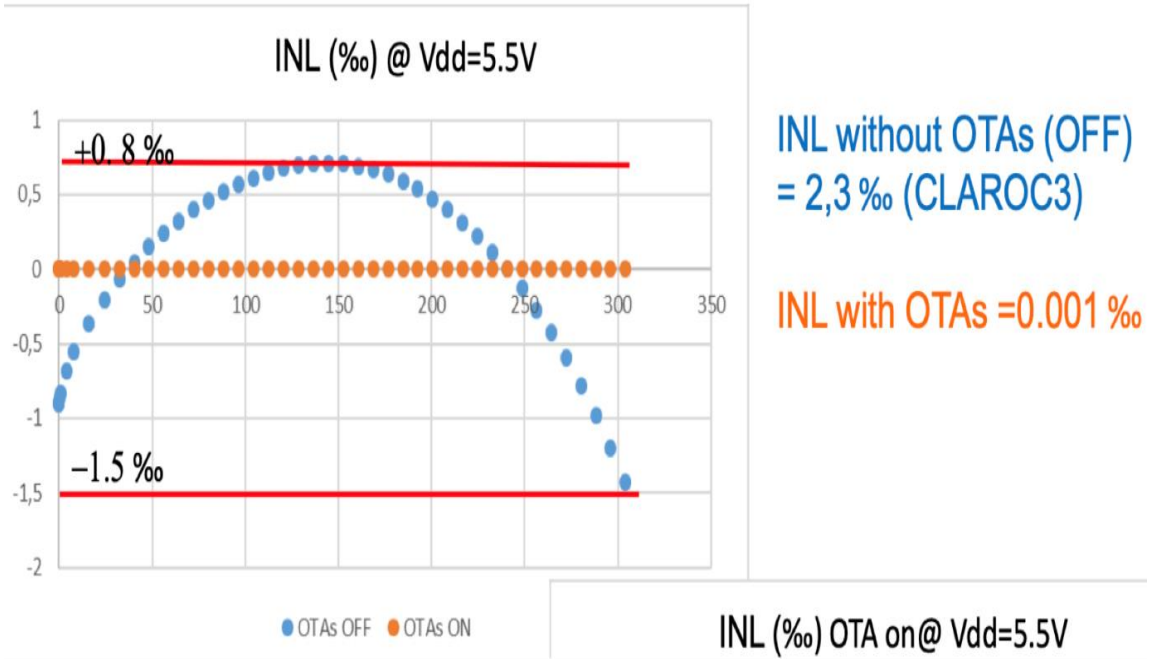
Change the package : QFN100 → BGA196

better for cabling and for serial test

Developments for calibration upgrade : ASICs evolution

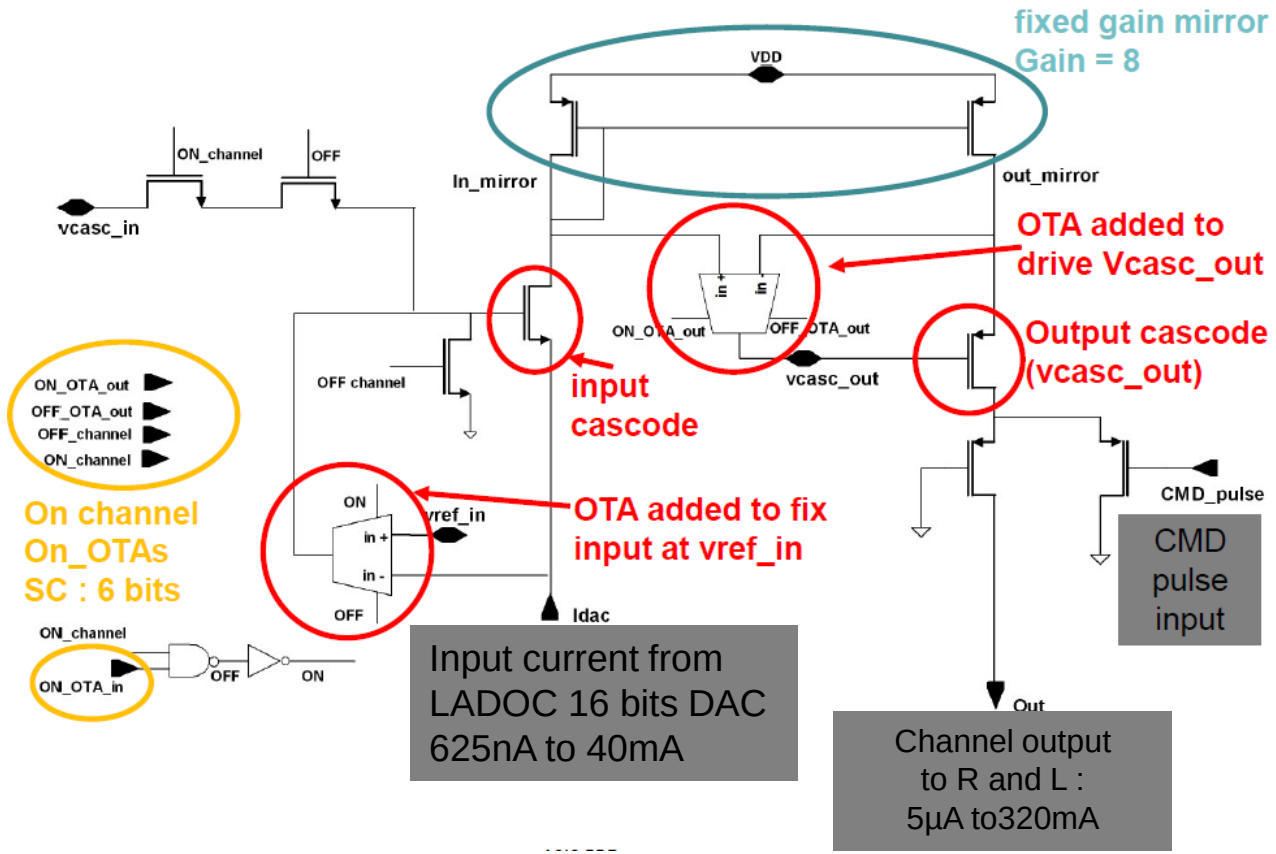


- The mirror gain is constant (= 8)
- Input current from LADOC : 625nA to 40mA
- An OTA is added to improve the mirror gain
- A second OTA is added at the input in order to control the input voltage (at 2.5V) and to keep a good linearity for LADOC



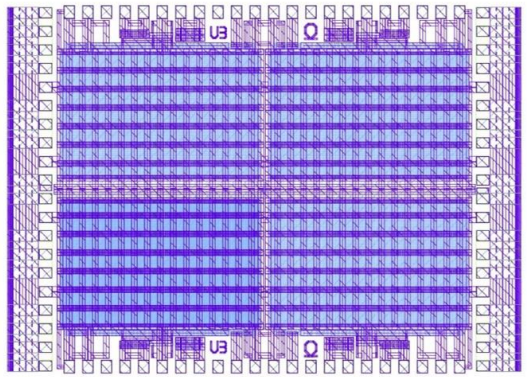
INL without OTAs (OFF) = 2,3 ‰ (CLAROC3)

INL with OTAs =0.001 ‰



CLAROC4

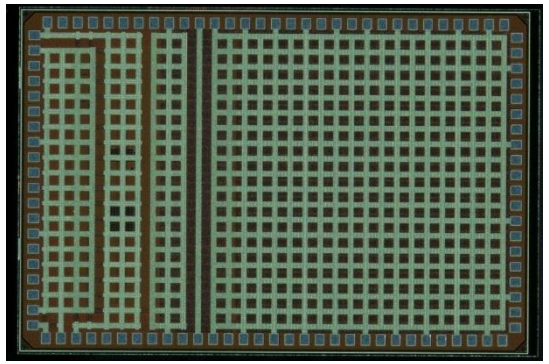
- 2,4mm x 2,3mm
- XFAB180nm
- Submitted in March 2022
- Package : BGA 196

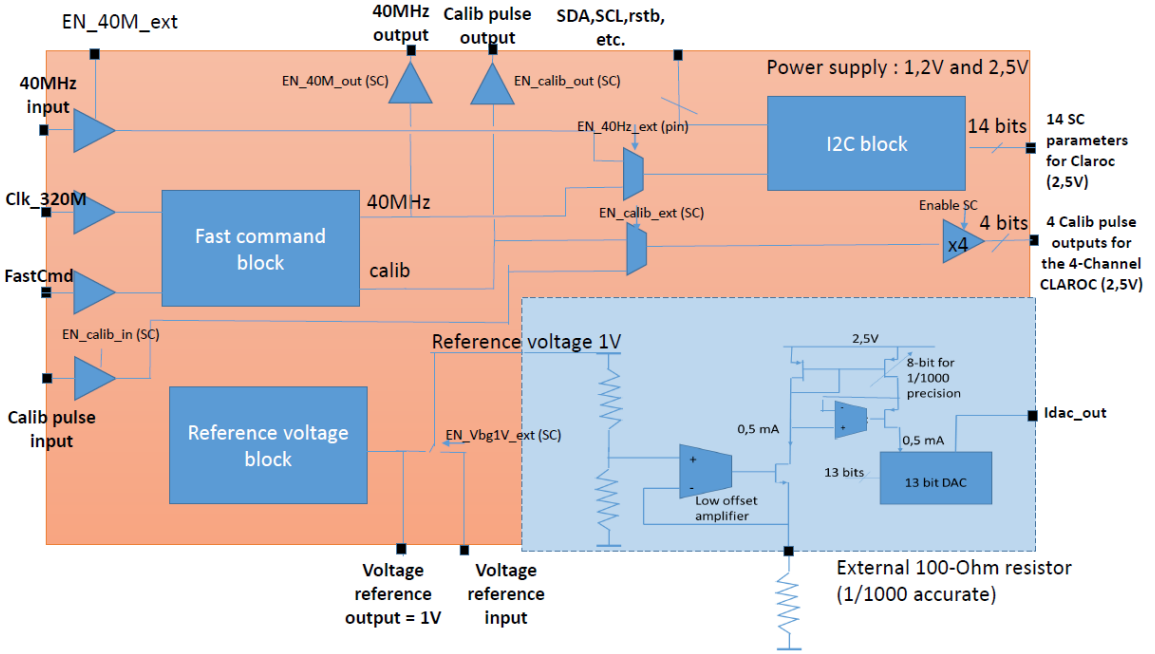


LADOC 2

- LADOC1 DAC will be used (better linearity compared to LADOC1A)
- Extend from 13 to 16 bits: 3 bits LSB will be added. Current from 625nA to 40mA
- Improve the current source: to ensure a better temperature stability
- Provides to CLAROC 2.5V slow control signals (instead of 1.2V in LADOC1)
- Provides to CLAROC 2,5V command signals (instead of 1.2V in LADOC1)
- Provides additional CLAROC SC parameters

LADOC 2
- 3,4mm x 2,3mm
- TSMC130nm
- Submitted in April 2022
- Package : BGA 196



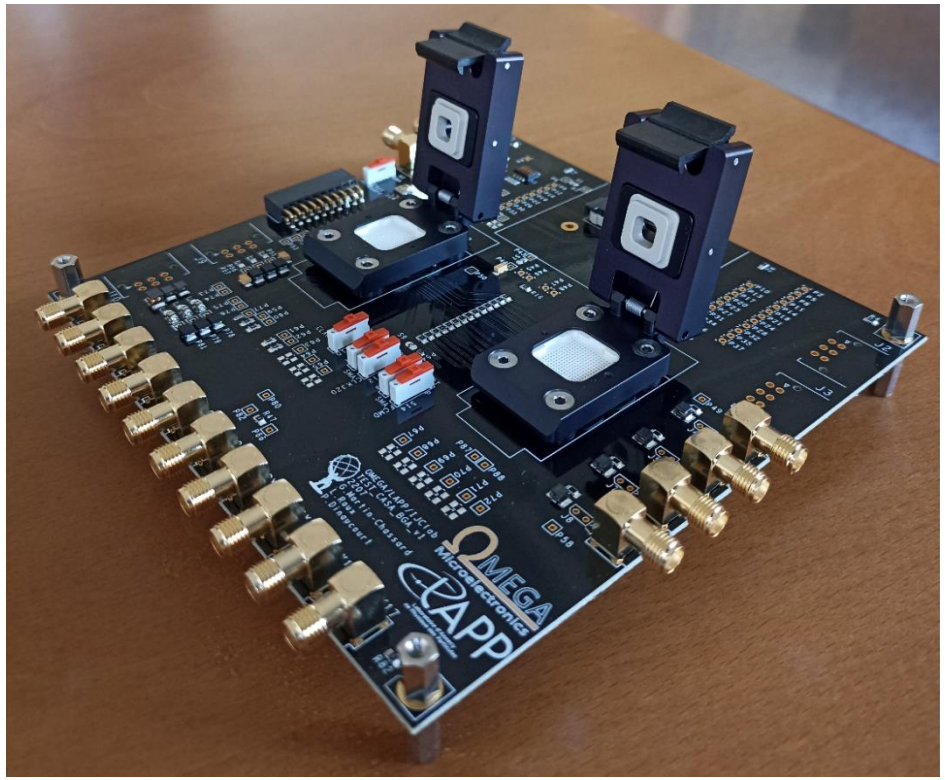


Notice: It is not a true 16-bit DAC we would like to realize, but it is a 16-bit DAC range with 1/1000 accuracy

Chips packaging in BGA and CASA4 testboard

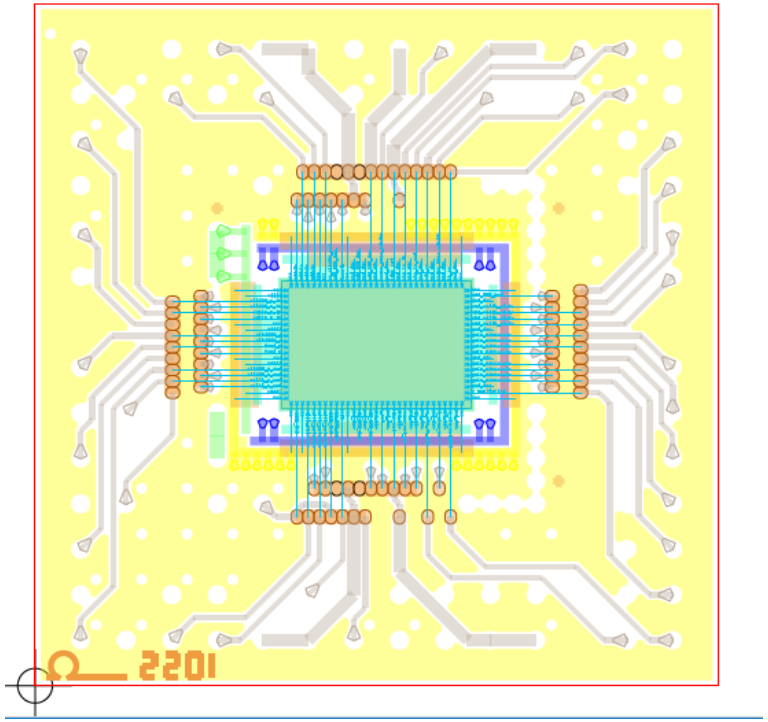
Chips packaging in BGA 196 :

- Necessary to also package CLAROC3 and LADOC1 in BGA in order to be able to compare effect of both packages (QFN/BGA)
- A complex substrat is designed to embed the 4 chips
- Developped by Pierrick Dinaucourt



CASA4 : testboard for LADOC2 and CLAROC4 in BGA

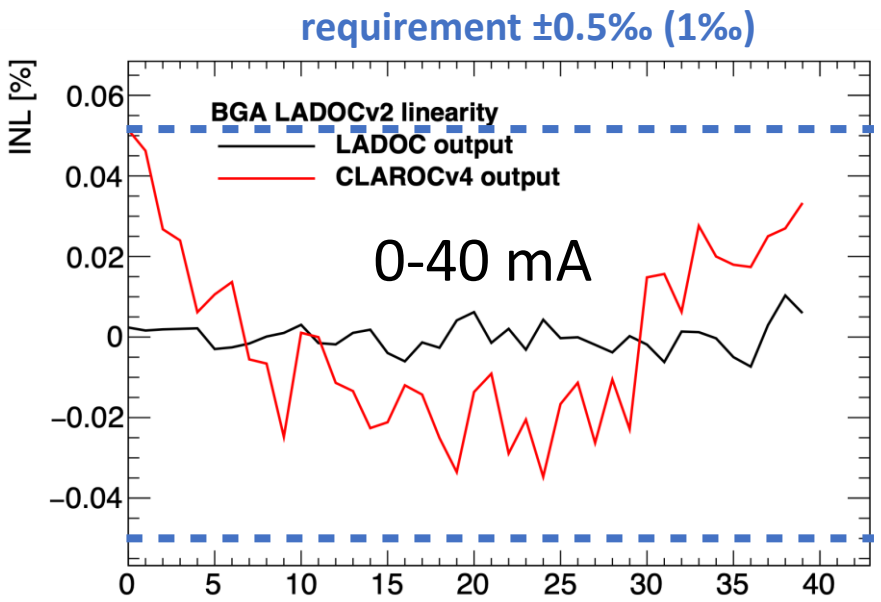
BGA substrat common for the 4 chips



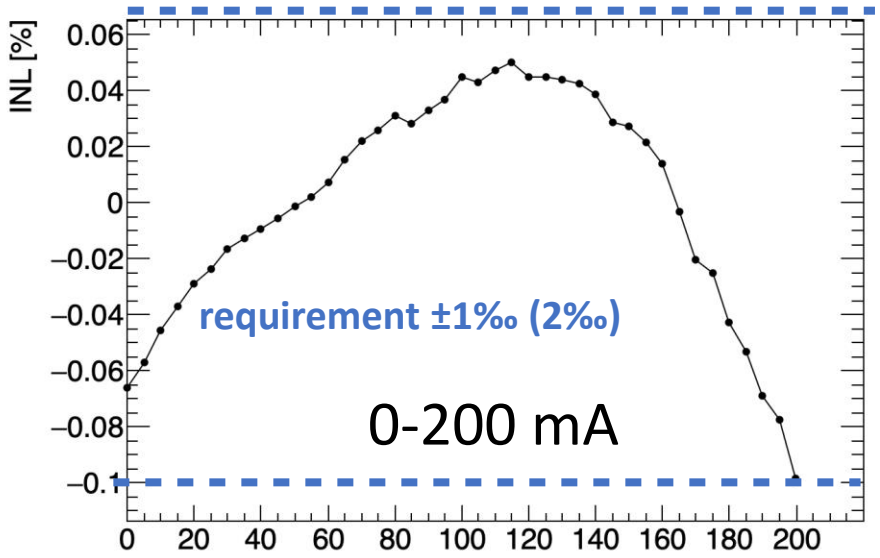
CASA4 testboard :

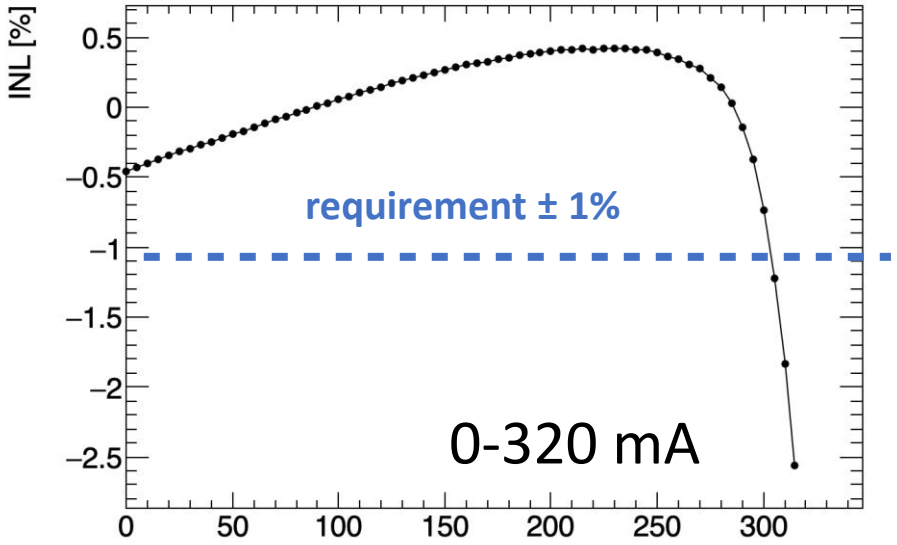
- Many configurations to be able to test both ladoc1 + claroc3 or ladoc2 + claroc4
- Sockets are chosen to be able to test chips on socket or soldered it on the board
- Designed by Pierrick Dinaucourt

CLAROC4 linearity for the different ranges

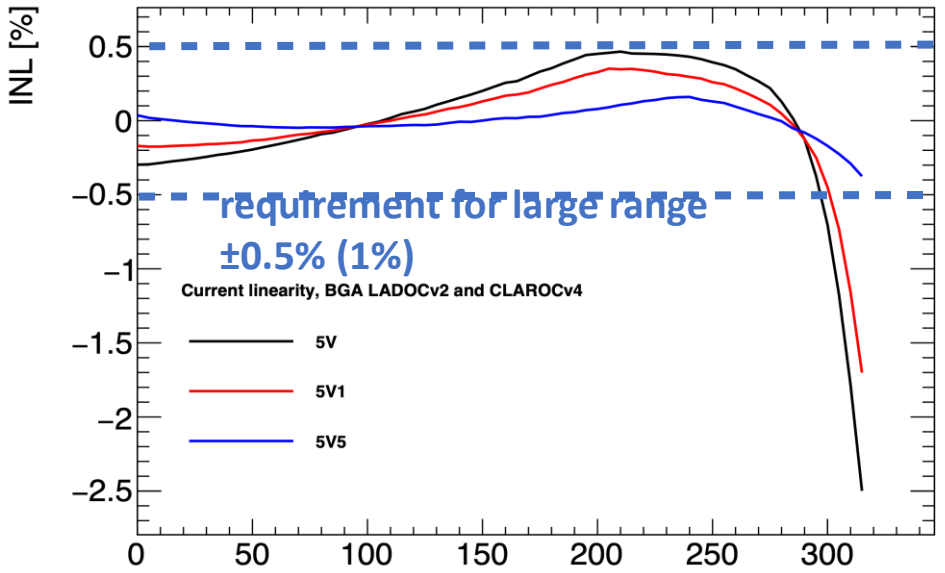


within specification for current< 200 mA but rather good for small range



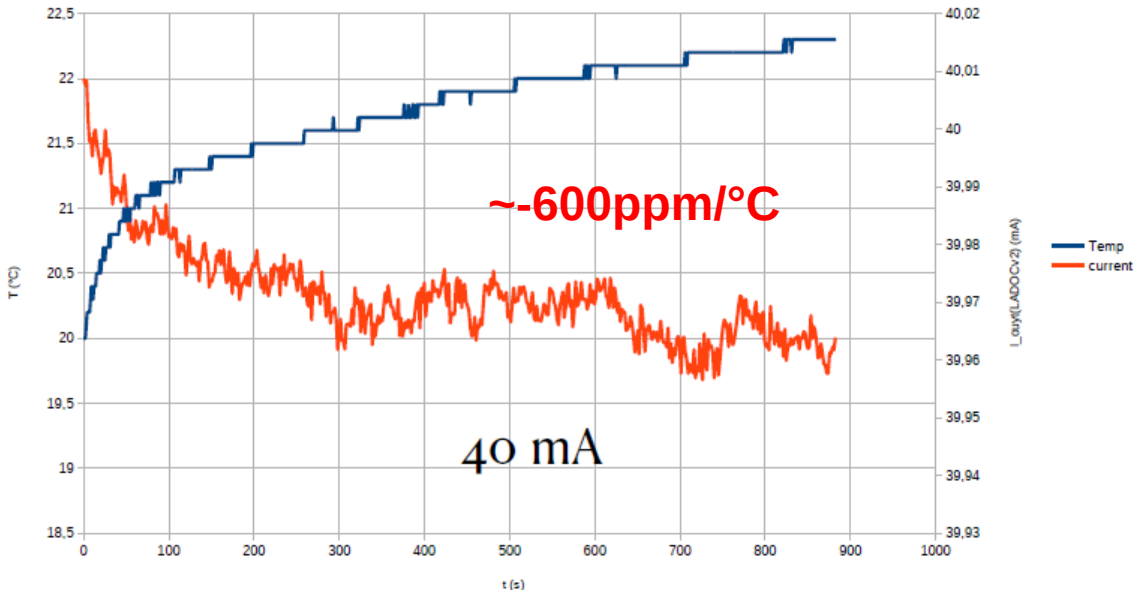


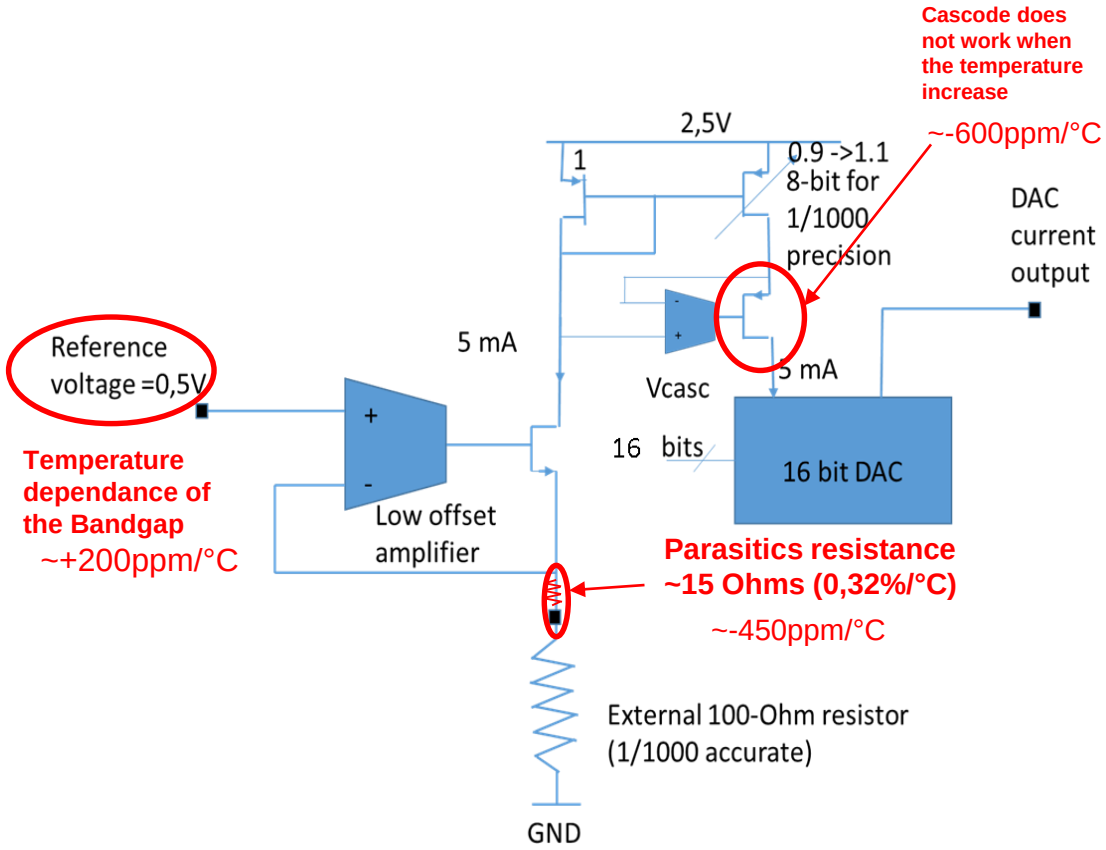
Not within specification for current>200 mA
→ Saturation
Increasing Vdd to 5.5V
→ Within specs



LADOC2 measurements

Output current temperature dependance
Measurement made @LAPP (Lucas Mangin) with a temprature sensor





LADOC2B :
Reduction of the parasitic resistance in the layout
Redimensionning of the 16-bit DAC without degrading the excellent linearity performance :
Reduction of the elementary cell length (L=16µm → 12µm)

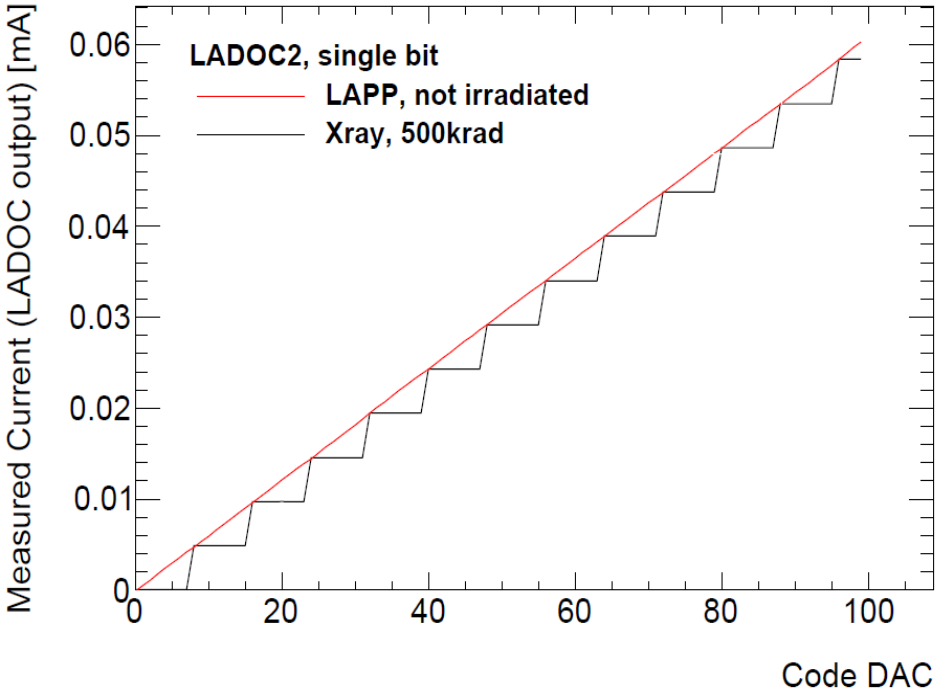
CLAROC4 and LADOC2 irradiation tests

First X-ray campaign at CERN (April 2023) :

• LADOC2 : The DAC giving the 3 LSB bits of LADOC (0-> 5µA) seems to die after only 60 krad

• CLAROC4 :
  • PMOS transistor of the HF switch has only a very tiny VT shift after 200 krad (40 mV)
  • The CLAROC DC output current become zero for small current at low doses (20Krad) and this offset increase when the doses increase. At 200 krad, no more DC current from CLAROC.
  • However pulses are always seen at the output of CLAROC (other channel)

→ **to be understood and redo TID tests for CLAROC**



Second campaign (May 2023) :

Problem understood : the new default configuration for CLAROC4 puts ON the NMOS command for the HF switch.

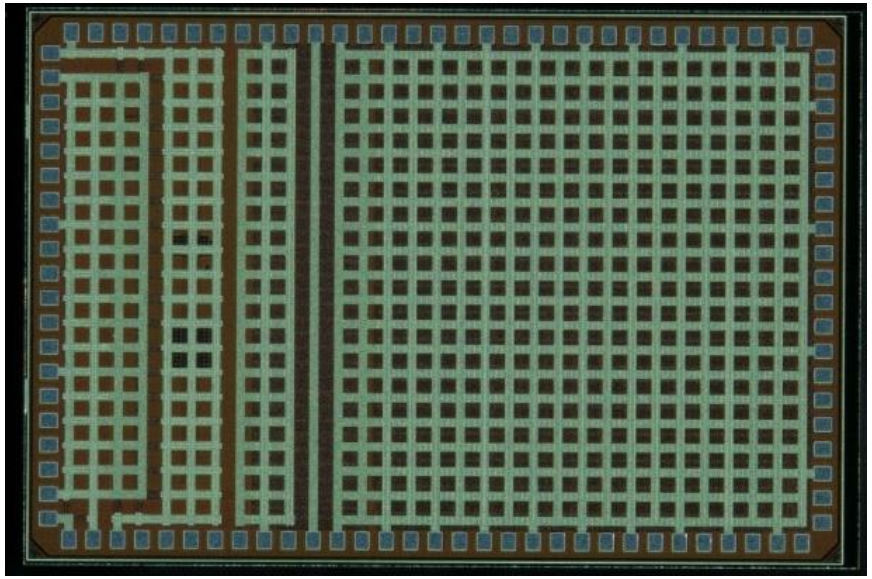
When we switch OFF this NMOS : results of irradiation are again OK and same as the one obtain with CLAROC3

Summary

LADOC2b :

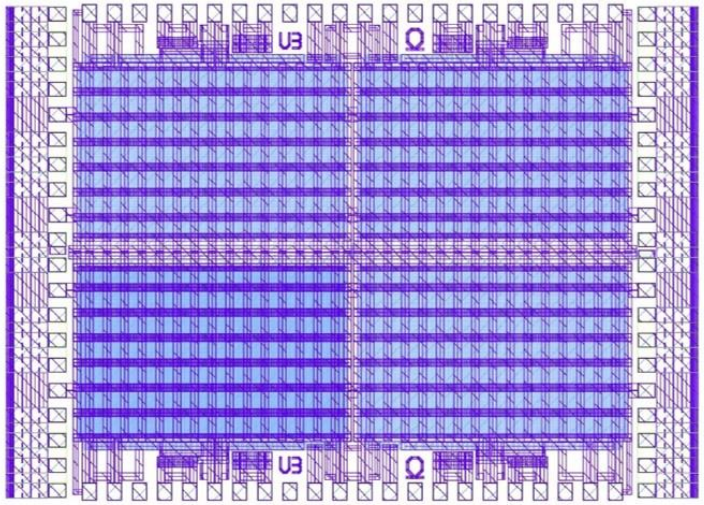
Opportunity to submit it in the run AIDA in March 2023:

- temperature dependance corrected
- small DAC irradiation problems are fixed



CLAROC4 :

- Study last irradiation results in details
- Submit the pre-serie version at the end of year



For the calibration system, we need 5000 dies of each :

→ Series production in 2024