Welcome to

Sfp connectivity and **M**icrotca for **A**dvanced **R**emote **T**rigger

program

A project for GANIL, AGATA, GRIT, GARETS, FASTER …
and available for any Laboratory
(see GANIL Technology Transfer Office)

SMART in terms of manpower

Hardware & Firmware - 4 permanents + 1 CDD

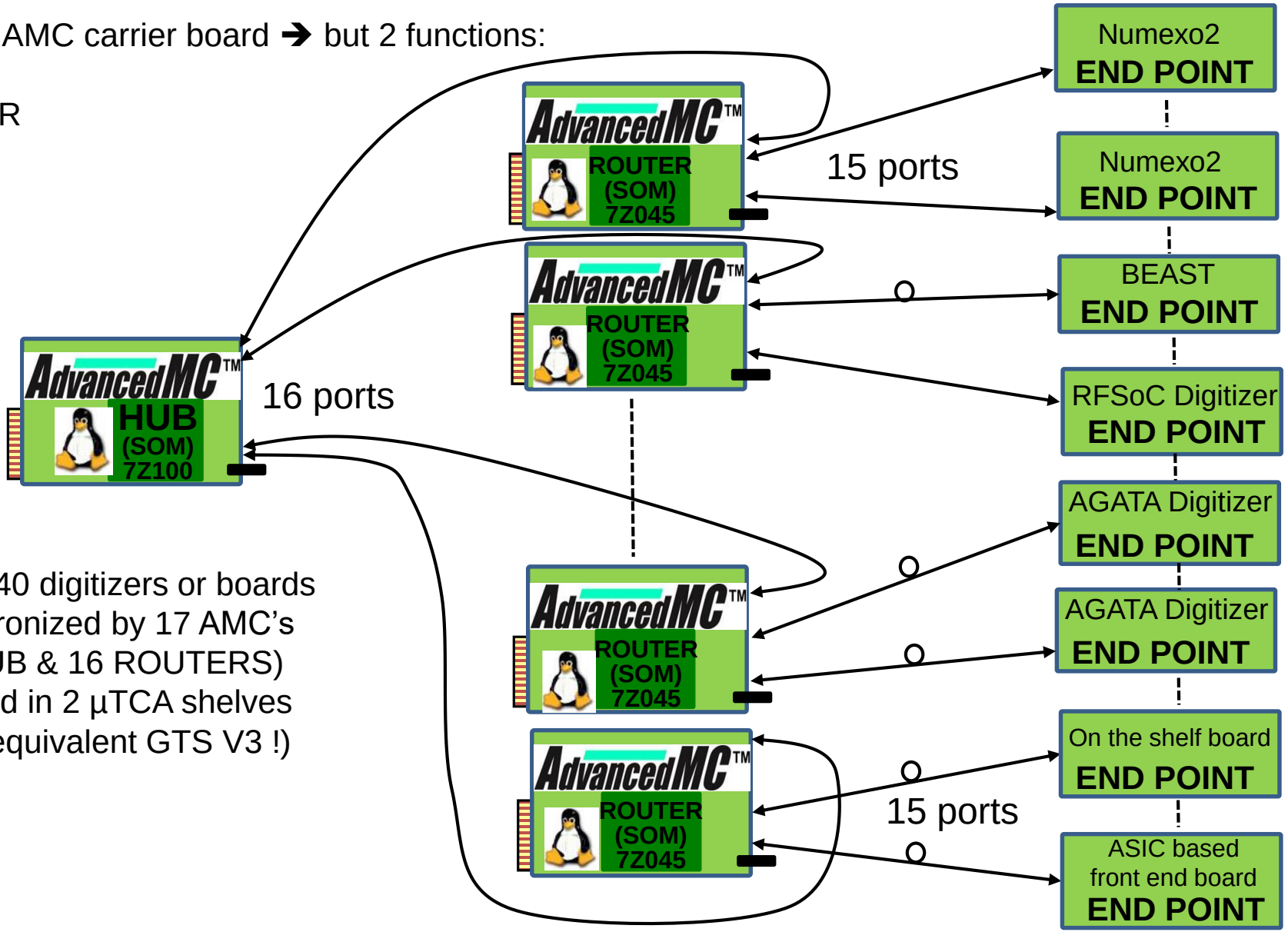
Software - 3 permanents

Maria Blaizot
Patrice Bourgault
Matthieu Bezard
Sébastien Coudert
Blandine Duclos
François Ingouf
Frédéric Saillant
Gilles Wittwer

? ➡ gilles.wittwer@ganil.fr

Global Architecture (Phase 1) & terminology reminder

Only one AMC carrier board ➔ but 2 functions:
- HUB
- ROUTER



Up to 240 digitizers or boards synchronized by 17 AMC's (1 HUB & 16 ROUTERS) housed in 2 µTCA shelves (120 equivalent GTS V3 !)

A - Main characteristics (Phase 1)

COMMUNICATION RATES

- **HUB ↔ ROUTER**: Line Rate = 4 Gb/s; Payload Data Rate = 400 MB/s; Reference Clock = 100 MHz

- **ROUTER ↔ EP's**: Line Rate = 2 Gb/s; Payload Data Rate = 200 MB/s; Reference Clock = 100 MHz

AUTOMATIC ALIGNMENT

- **HUB to EP's** : with external TDC chip

CLOCK & TIMESTAMPING

- **HUB to ROUTER (to EP's)** : 8B/10B encoding/decoding with Recovered Clock = 100 MHz;
  TS on 48 bits/10ns (more than 1 month of experiment)

TRIGGER @ HUB LEVEL

- **Trigger req./val.** : based on uplink and downlink frames (build with ID recognition/digitizer type)
- **Multi-partitions** : 240, 480, up to 720 digitizer channels (typically 45x16ch-NUMEXO2 boards)
- **Multiplicity** : threshold by partition
- **Acceptance window**: for late channels arriving during a trigger cycle
- **Logic Equation** : (OR/AND/NOT) between partitions for the final decision (ACCEPT/REJECT)
- **32 bit Event Number** : for accepted returned frames
- **Max 208 KHz/channel – Total trigger rate @HUB level: 800 Mtrig_req/s**

B - Main characteristics (Phase 1)

COMMUNICATION MEDIA (Interoperability)

- **COPPER**: SFP to SFP or QSFP to 4xSFP; Up to 7 meters with passive Direct Attach Cables (DAC) characterized @ 10Gb/s

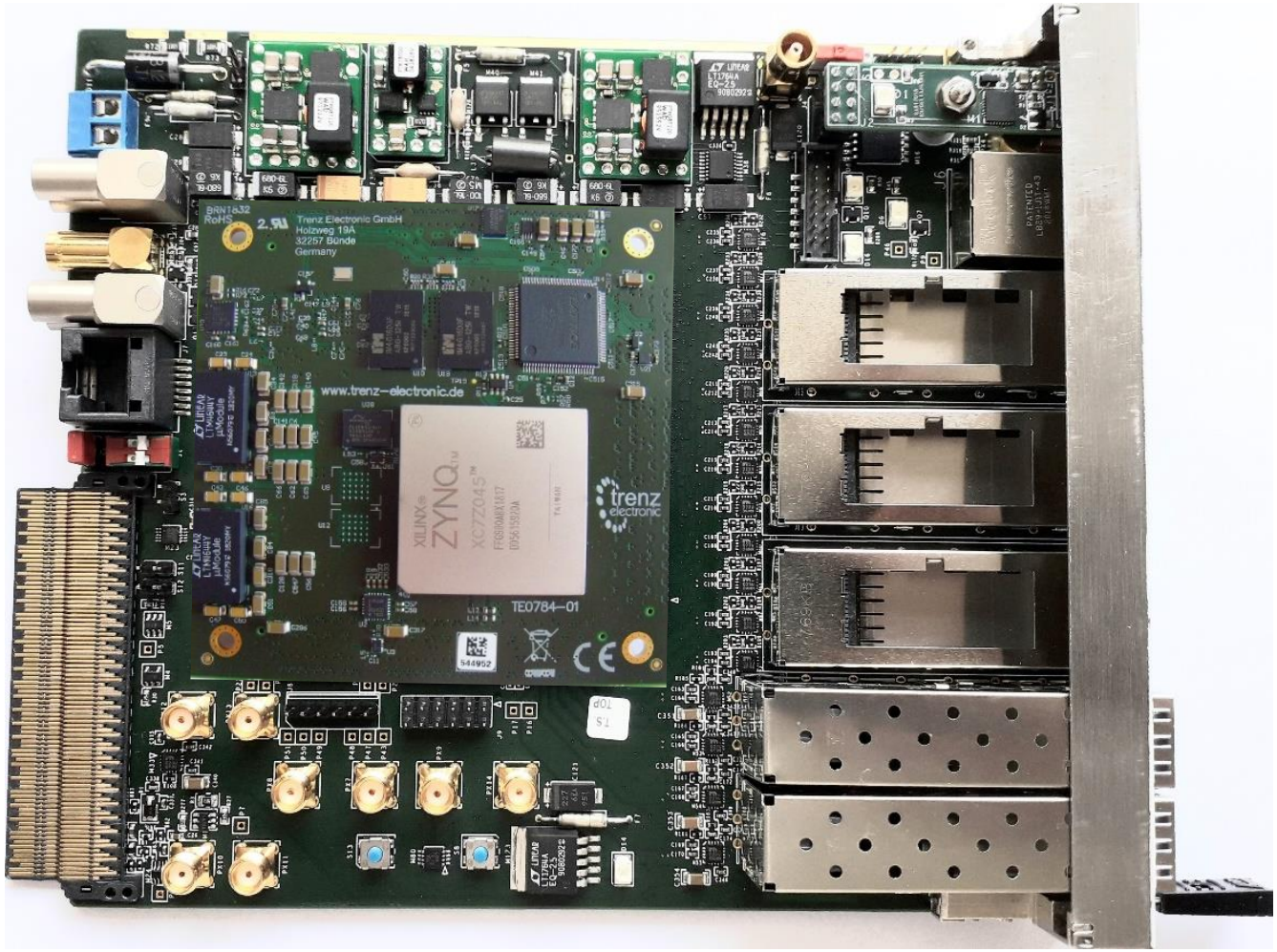
- **FIBER** : SFP transceiver (LC) to SFP transceiver (LC) or QSFP (MPO) to 4xSFP (LC) with optical patch cord; up to 150 meters with OM3/OM4 fibers

SOM and SOC USED on SMART AMC BOARD (Phase 1)

- **HUB**: TE0784-01 from TRENZ Company with Xilinx XC7Z100-2FFG900I

- **ROUTER** : TE0784-01 from TRENZ Company with Xilinx XC7Z045-2FFG900I

SMART AMC in terms of Hardware (Phase 1)



Production: 26 AMC boards (+SOM) in 2024, mainly for GANIL and AGATA

New communication media qualified for SMART

(all them remotely identified by “SFP_QSFP_device_checker”

SFP+ to SFP+
(10Gb/s passive cables)

2 Finisar SFP transceivers
One 6.1 Gb/s and one 8.5 Gb/s
(more than 150 m with OM3 fiber)

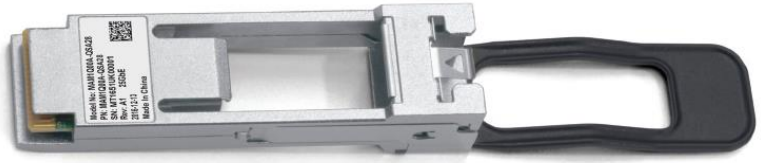
- Four-channel full-duplex transceiver module
- Hot Pluggable QSFP+ form factor
- Maximum link length of 100m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel

QSFP to MPO
(Finisar FTL410 series)

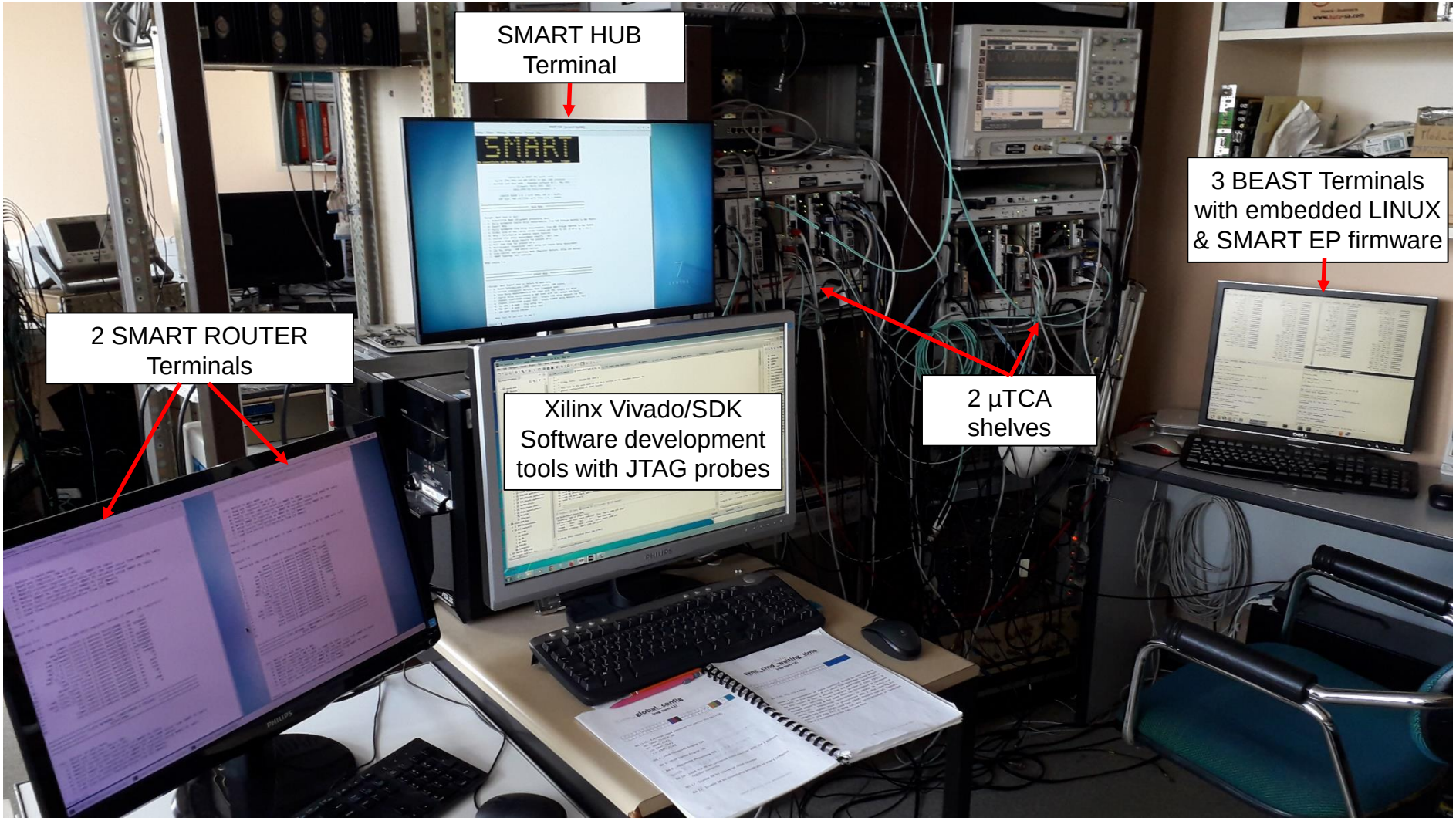
QSFP to 4xSFP+
(40G breakout passive cables)

Fiber MPO to 4 x 2 Fiber MPO Duplex LCs

QSFP(ch.1) to SFP adapter
(Useful with passive cables
or transceivers)

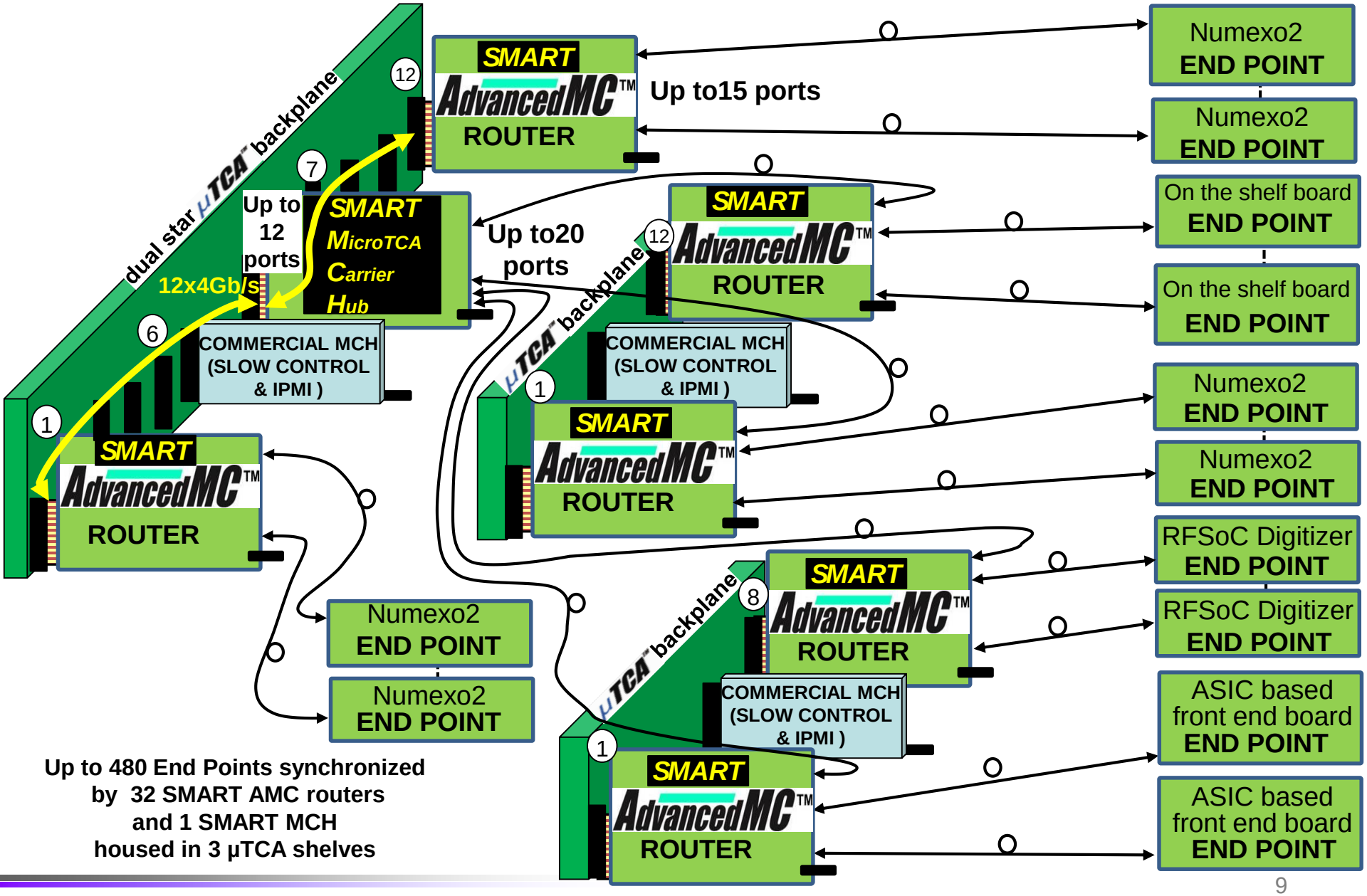


SMART tests - Full test bench overview



Main results: +/- 1 lsb on timestamps between aligned boards

SMART Phase 2 - Full Architecture, twice the phase 1!



Up to 480 End Points synchronized by 32 SMART AMC routers and 1 SMART MCH housed in 3 µTCA shelves

Zynq-7000 vs Zynq UltraSCALE+ ZU19 vs latest Kintex UltraSCALE+ KU19P

Zynq-7000 SoCs

	Device Name	Z-7045	Z-7100
	Part Number	XC7Z045	XC7Z100
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	350K	444K
	Look-Up Tables (LUTs)	218,600	277,400
	Flip-Flops	437,200	554,800
	Block RAM (# 36 Kb Blocks)	19.2 Mb (545)	26.5 Mb (755)
	DSP Slices (18x25 MACCs)	900	2,020
	Peak DSP Performance (Symmetric FIR)	1,334 GMACs	2,622 GMACs
		16 x GTX	16 x GTX

SMART AMC ROUTER | HUB

Zynq® UltraScale+™ MPSoCs

Device Name	ZU19EG	
System Logic Cells (K)	1,143	
CLB Flip-Flops (K)	1,045	
CLB LUTs (K)	523	
Max. Distributed RAM (Mb)	9.8	
Total Block RAM (Mb)	34.6	(984)
UltraRAM (Mb)	36.0	128
Clock Management Tiles (CMTs)	11	
DSP Slices	1,968	
PCI Express® Gen 3x16 / Gen4x8	5	
150G Interlaken	4	
100G Ethernet MAC/PCS w/RS-FEC	4	
AMS - System Monitor	1	
GTH 16.3Gb/s Transceivers	44	
GTY 32.75Gb/s Transceivers	28	

SMART MCH 1st candidate

KINTEX UltraSCALE+

Kintex® UltraScale+™ FPGA

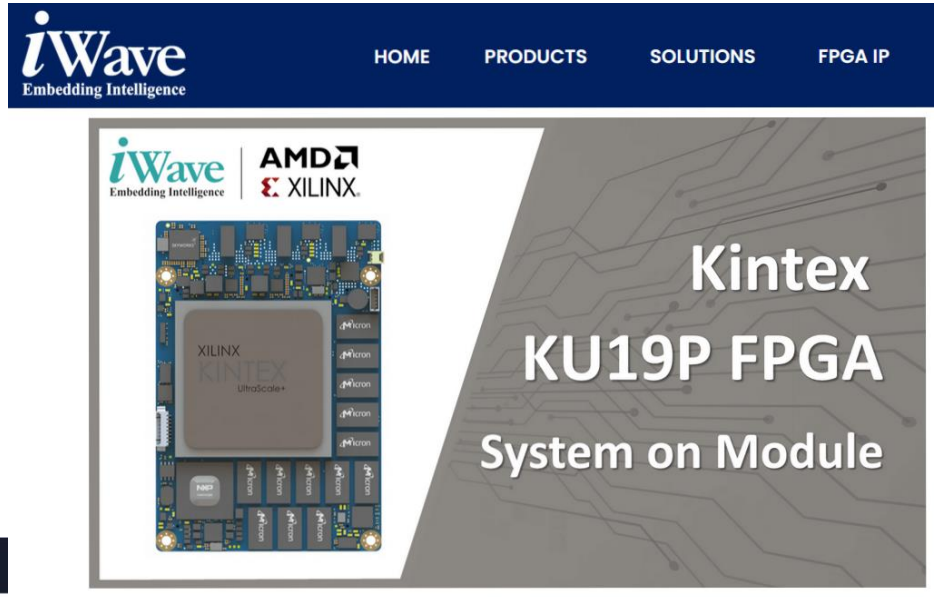
Device Name	KU19P	
System Logic Cells (K)	1,843	
CLB Flip-Flops (K)	1,685	
CLB LUTs (K)	842	
Max. Distributed RAM (Mb)	11.6	
Total Block RAM (Mb)	60.8	1728
UltraRAM (Mb)	81.0	288
Clock Mgmt Tiles (CMTs)	9	
DSP Slices	1,080	
PCIE4 (PCIe® Gen3 x16)	0	
PCIE4C (PCIe® Gen3 x16 / Gen4 x8 /CCIX)	3	
150G Interlaken	0	
100G Ethernet w/ KR4 RS-FEC	1	
Max. Single-Ended HD I/Os	72	
Max. Single-Ended HP I/Os	468	
GTH 16.3Gb/s Transceivers	0	
GTY 32.75Gb/s Transceivers	32	

SMART MCH 2nd candidate

Up to 2016 FIFO's ready to use

Sfp connectivity and Microtca for Advanced Remote Trigger

Phase 2



Nuremberg, Germany 22nd June 2022 – iWave Systems unveils the first look of Xilinx Kintex® UltraScale+™ powered System on Module (SOM) at embedded world 2022.

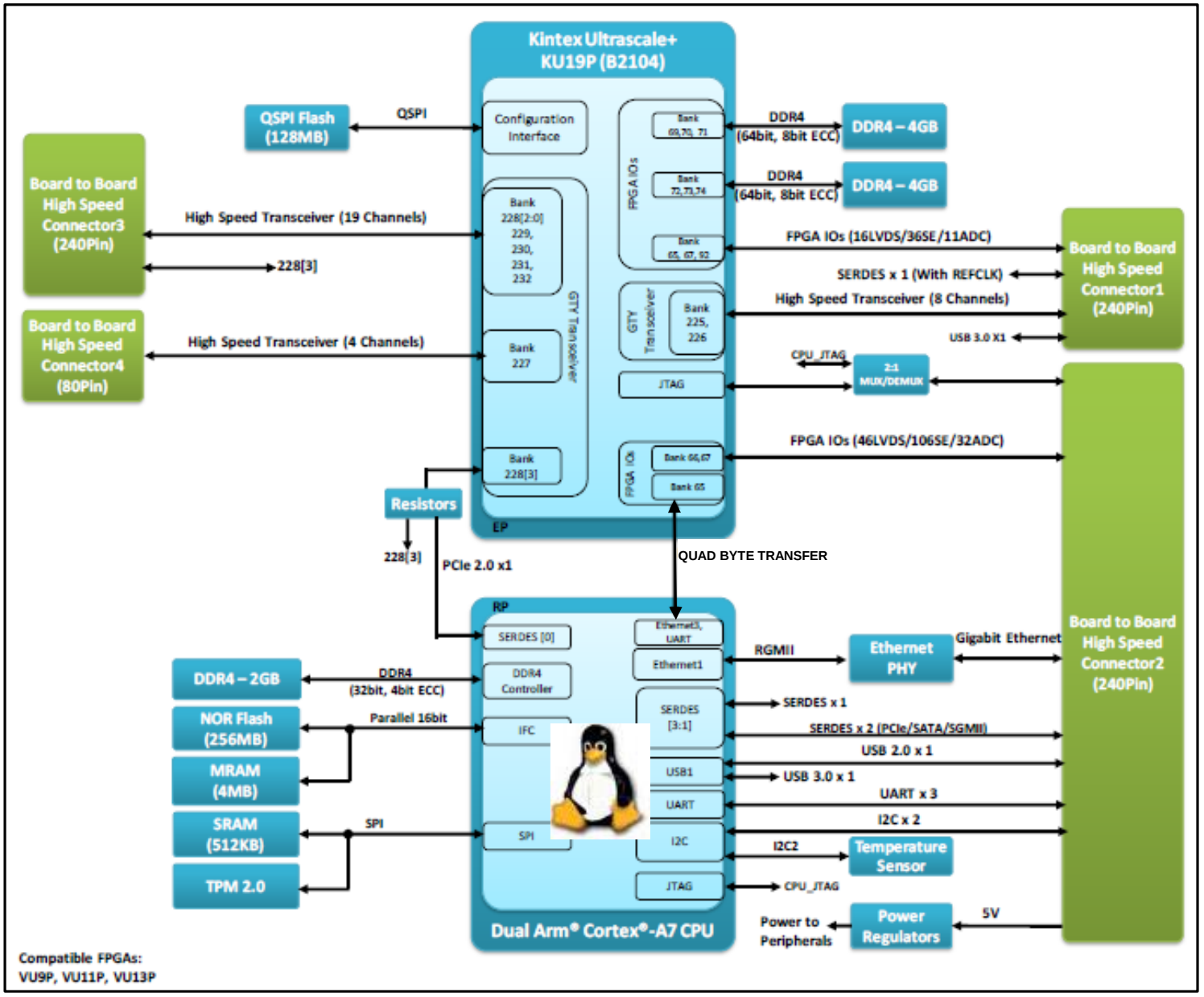
Solutions Products Company AMD XILINX

Introducing the Kintex UltraScale+ KU19P FPGA: Optimized for Network Accelaration - July 22,2020

Kintex UltraScale+ KU19P FPGA Provides Strong Balance of Performance, Price, and Power

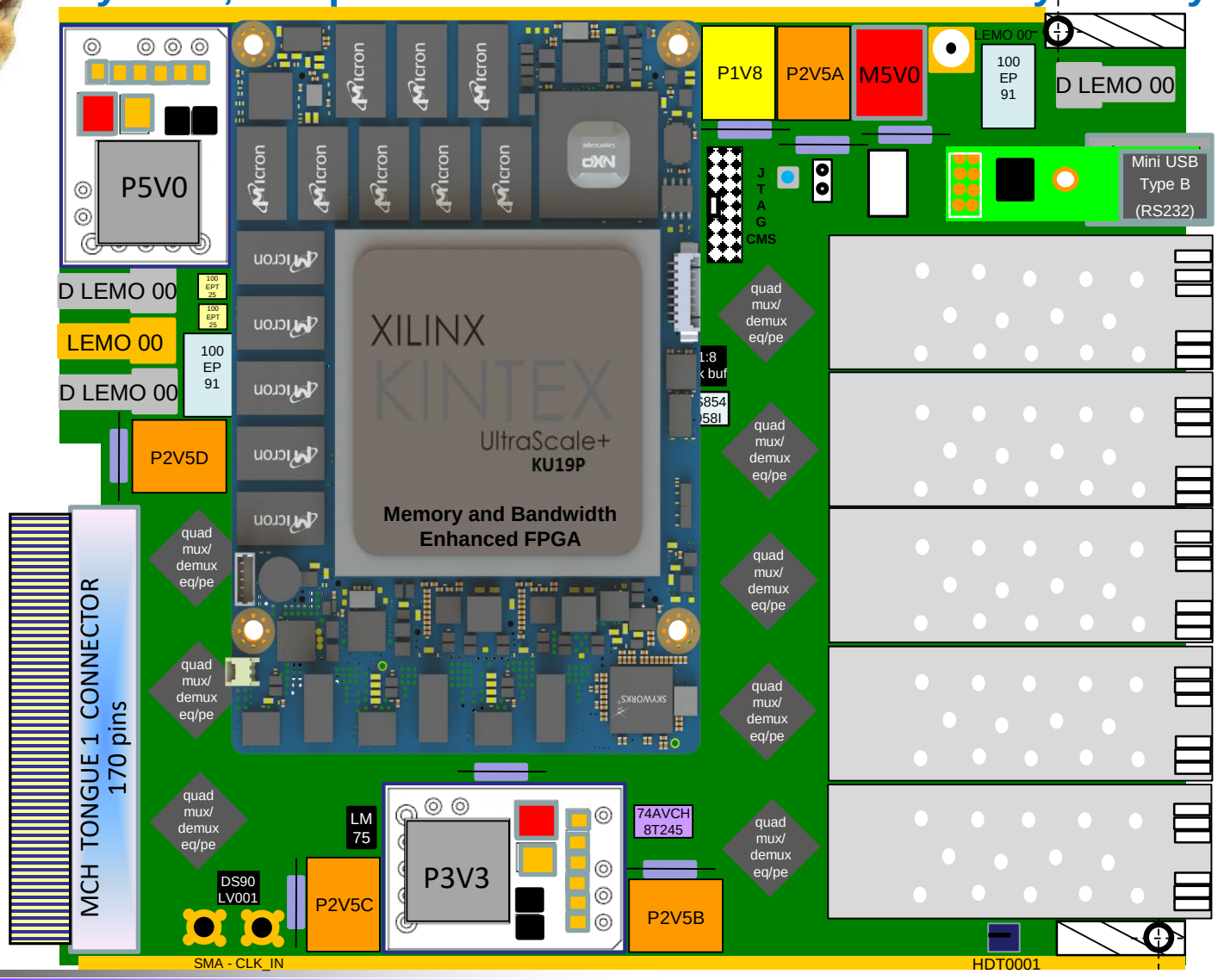
As next-generation networks are deployed to support an increasingly diverse mix of high-bandwidth applications, network vendors and data center operators need to rapidly scale packet processing capability while both minimizing capex/opex and preserving the flexibility to adapt to future connectivity standards. To meet these requirements, Xilinx is excited to announce the latest addition to the Kintex® UltraScale+™ FPGA portfolio: the Kintex UltraScale+ KU19P FPGA. The KU19P FPGA delivers the optimized mix of resources and high-throughput connectivity needed to efficiently accelerate network processing while maintaining the strong balance of performance, price, and power inherent to the entire Kintex FPGA portfolio.

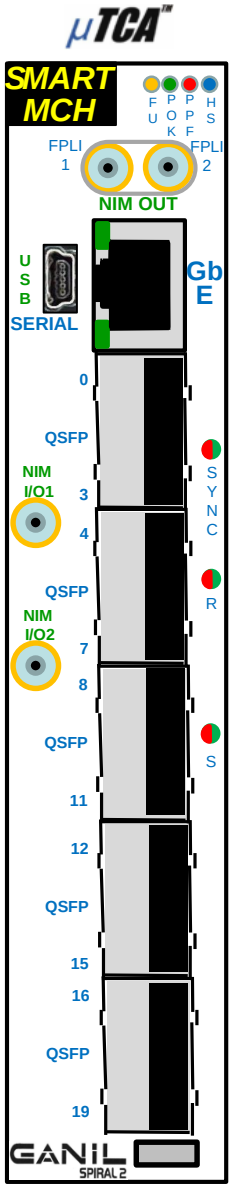
SMART MCH - SOM block diagram



Sfp connectivity and Microtca for Advanced Remote Trigger

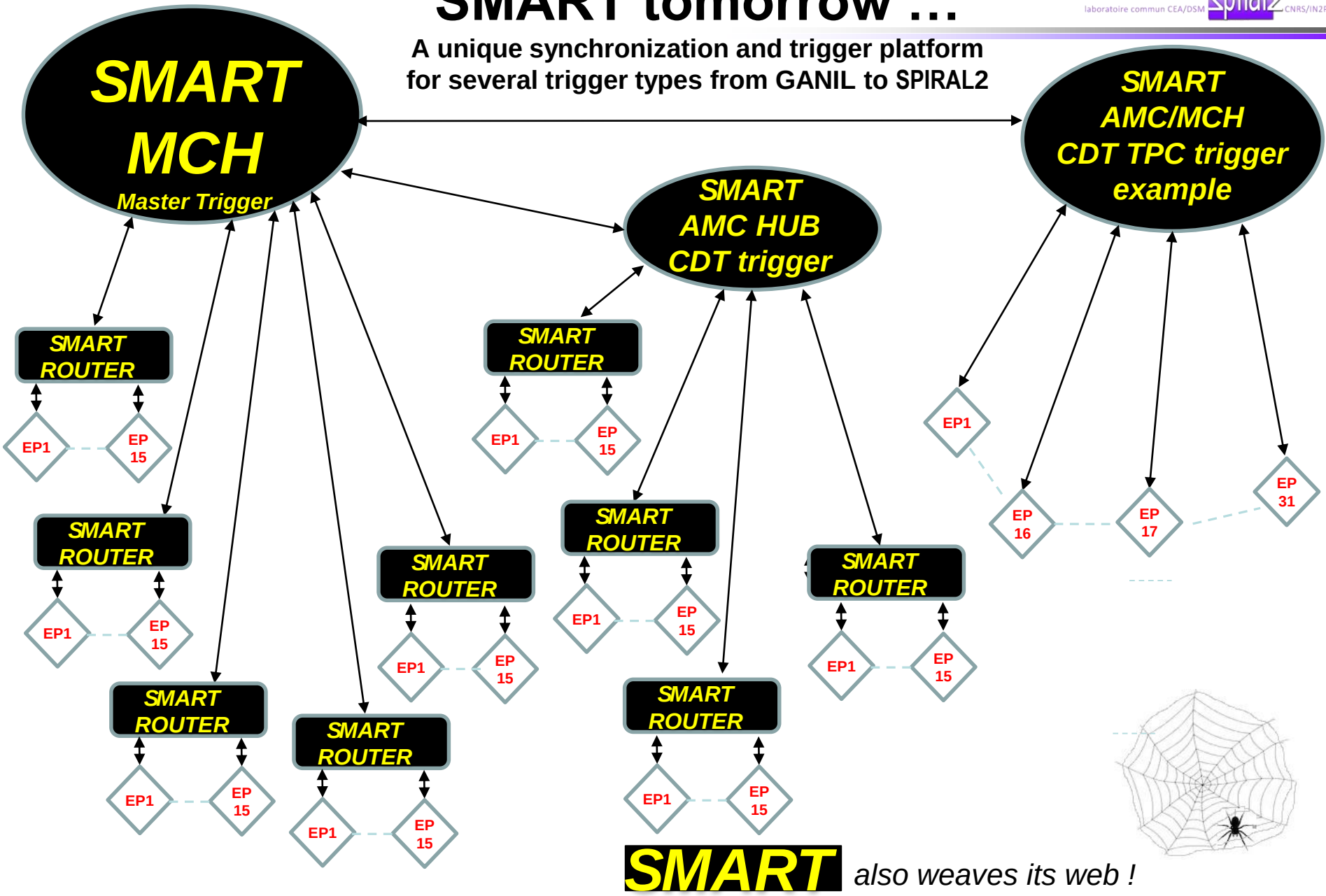
July 2024, a super HUB called SMART MCH is ready for Physics





SMART tomorrow …

A unique synchronization and trigger platform for several trigger types from GANIL to SPIRAL2



SMART *also weaves its web !*

Merci de votre attention