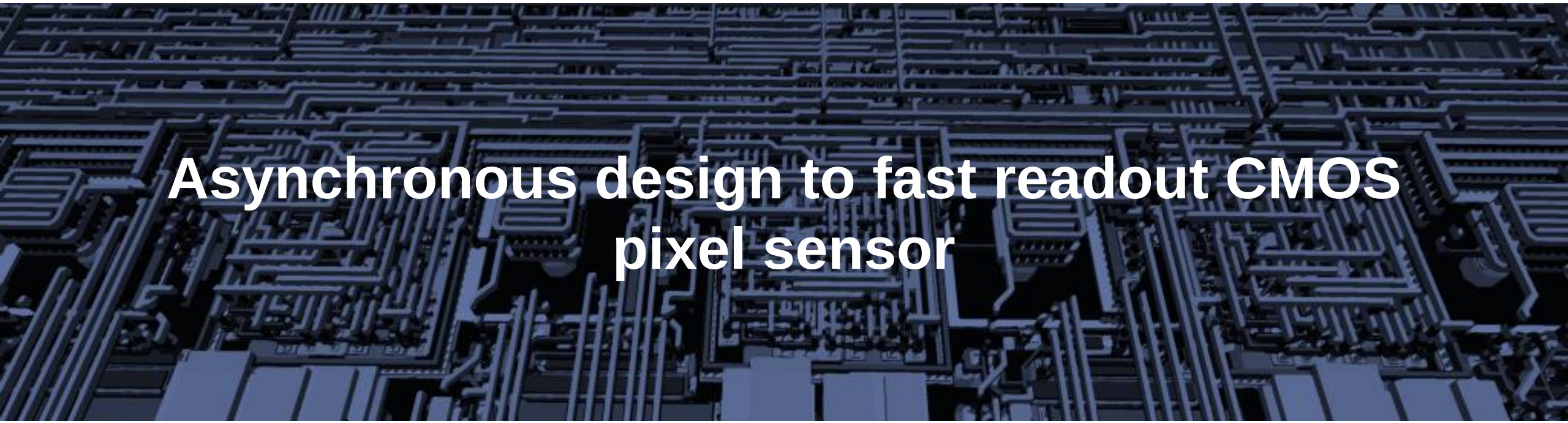


Asynchronous design to fast readout CMOS pixel sensor

PhD Student Jean SOUDIER

Directors: Jérôme BAUDOT & Wilfried UHRING

Supervisor: Frédéric MOREL

Outline

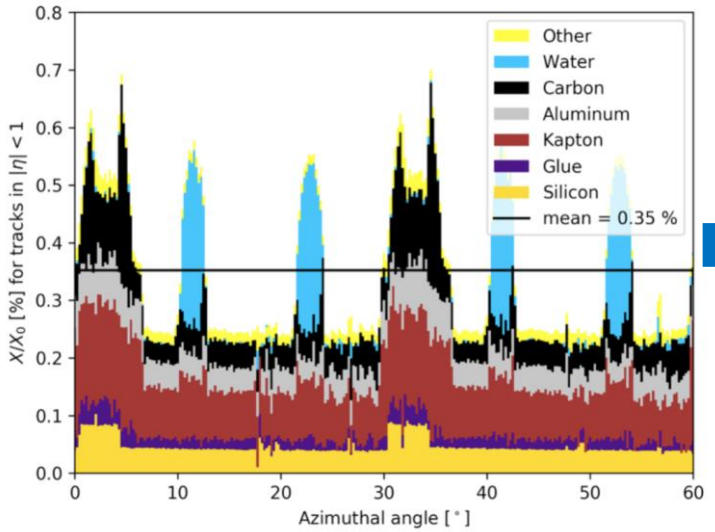
Introduction

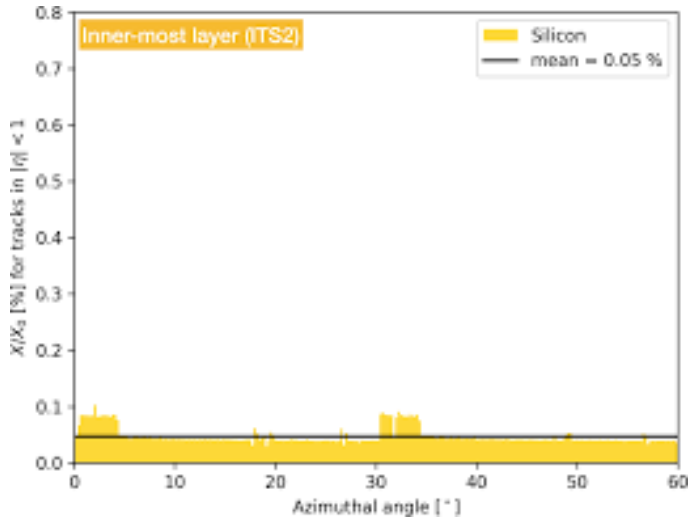
- Asynchronous flow
- Size variation and estimations
- SPARC design

Conclusion

Overview

Divide by 7 the material budget

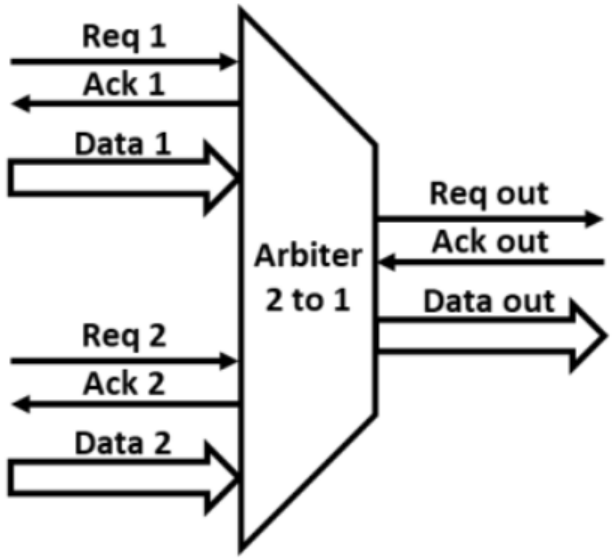




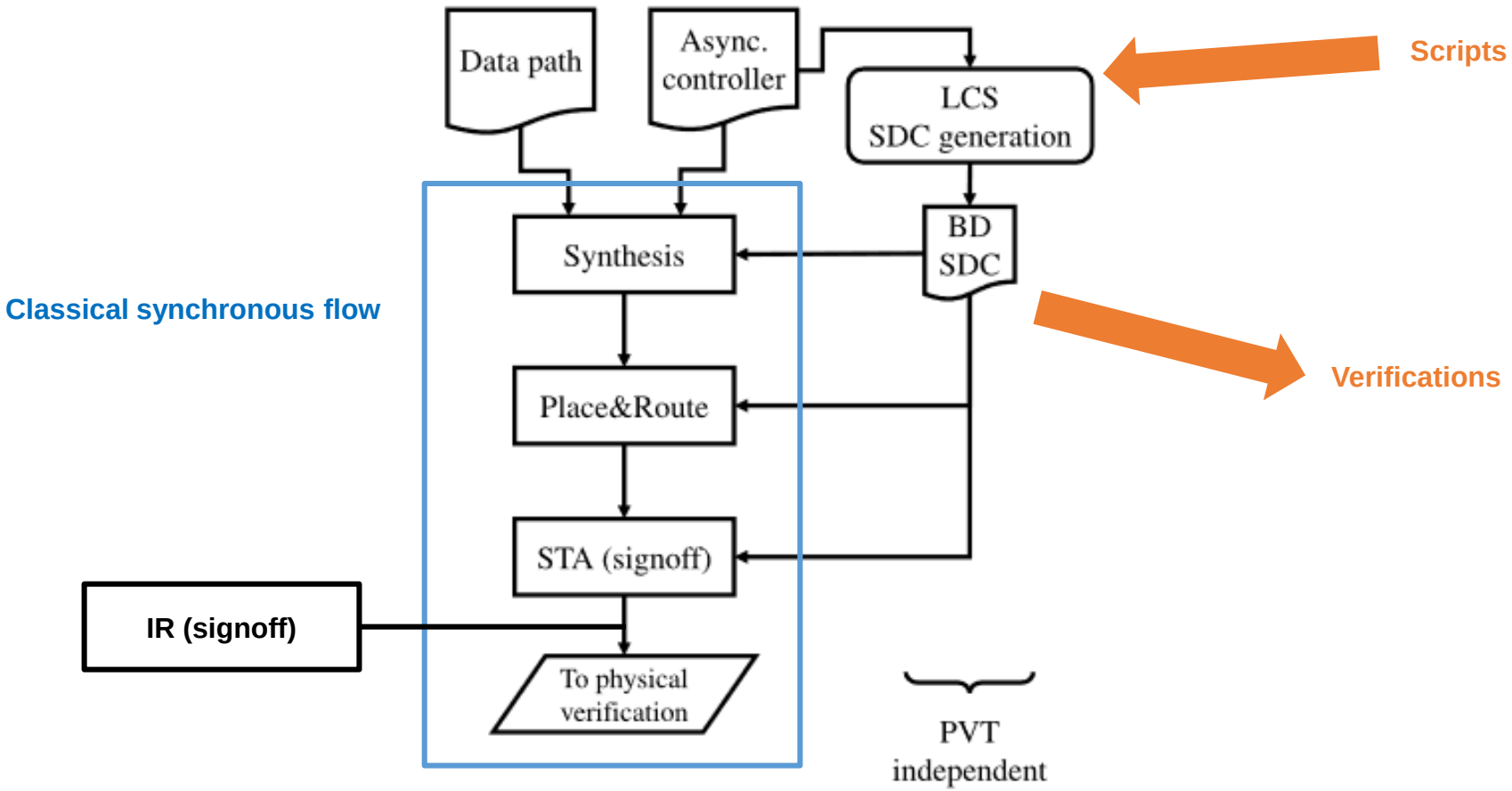
Goal of the thesis

New architecture:
- low-power
- high rate
- small pitch

Asynchronous architecture:
- work when needed
- achieve variable bandwidth
- clock less more localized



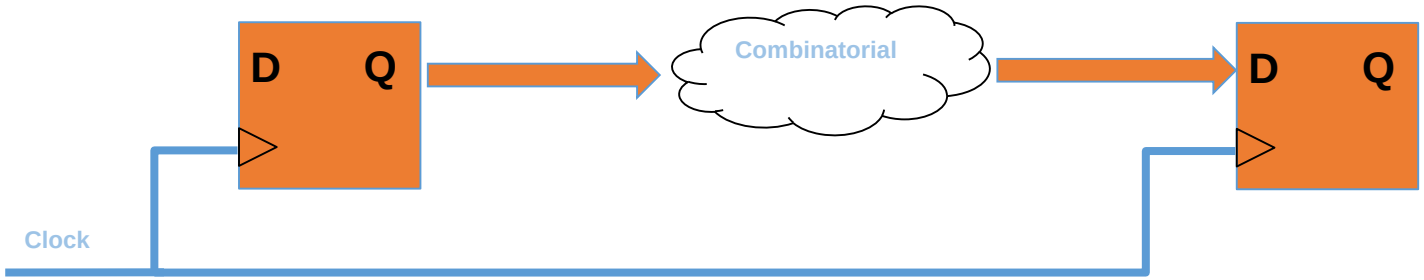
Flowkit, digital on top for asynchronous



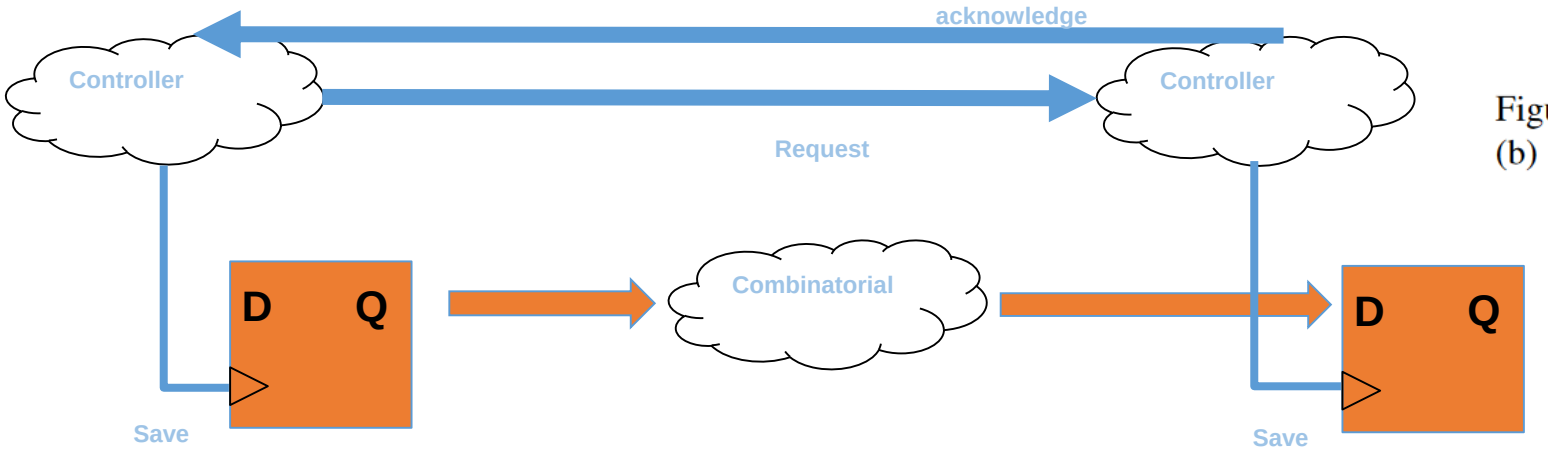
[1] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, mai 2018, p. 110-118. doi: 10.1109/ASYNC.2018.00036.

Synchrone / asynchrone data transfer

Synchrone



Asynchrone



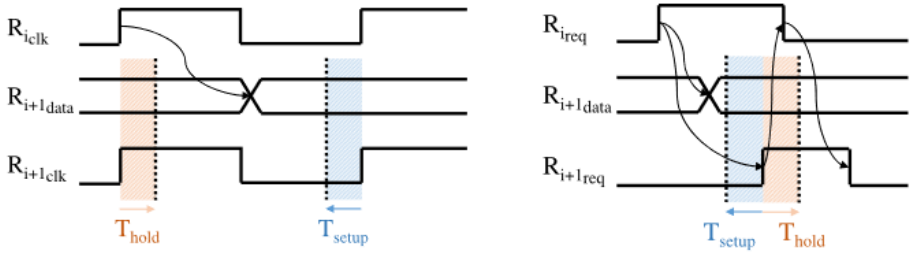
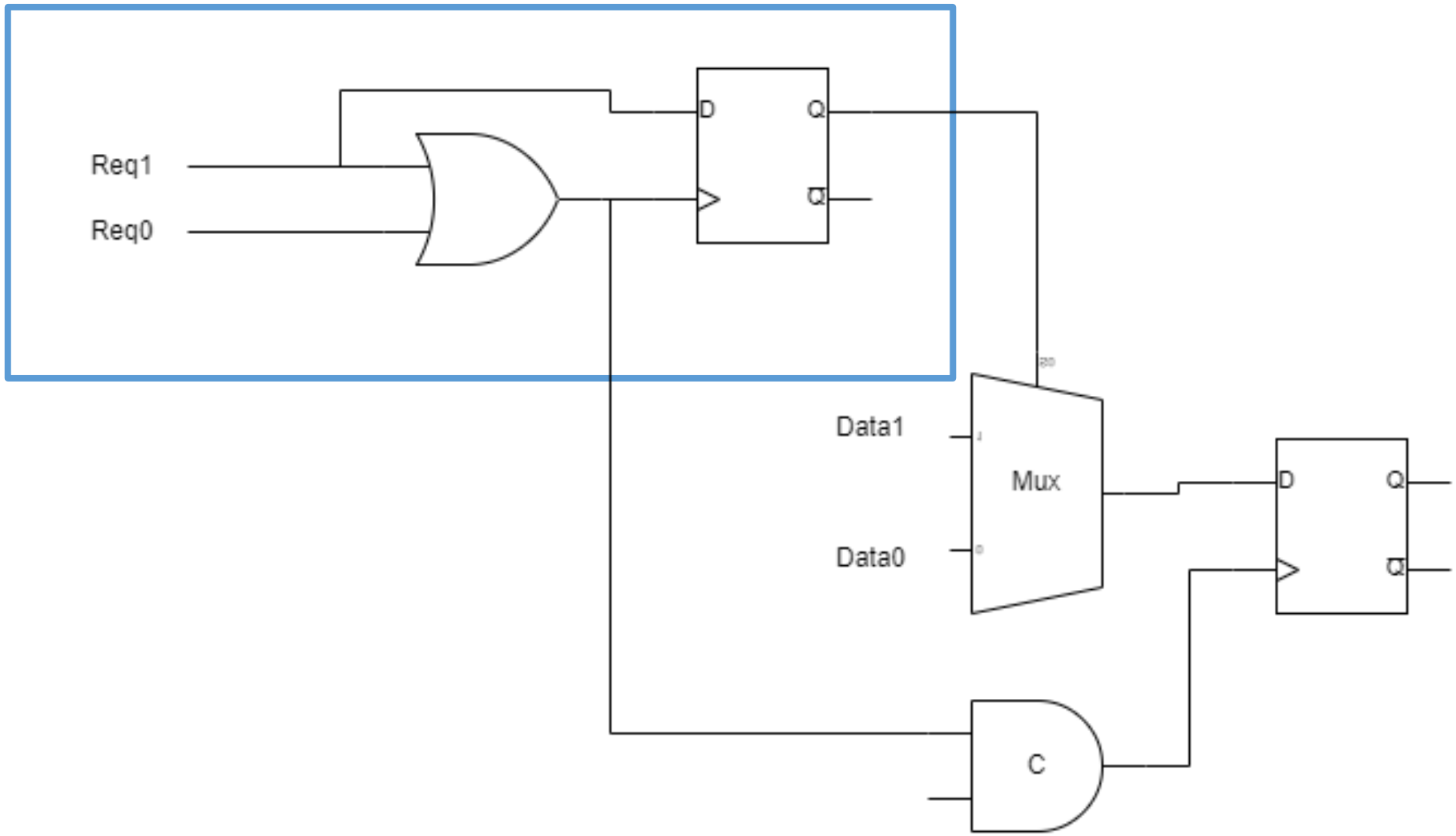


Figure 5: Timing waveform for a 2-stage (a) synchronous and (b) asynchronous pipeline.

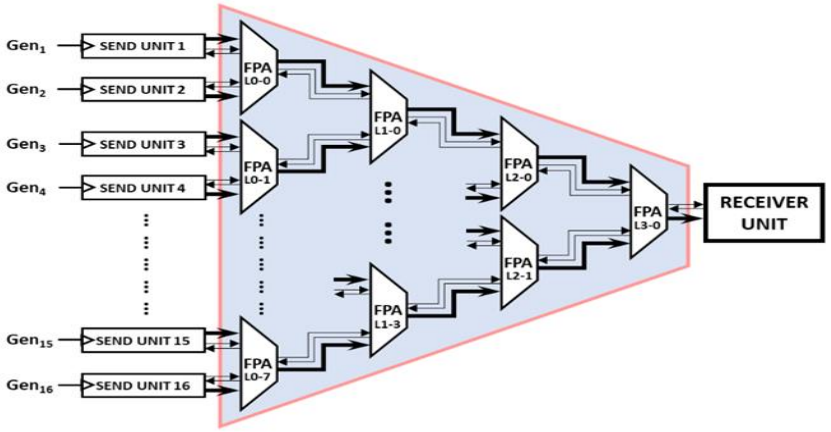
[1] G. Gimenez, A. Cherkaoui, G. Cogniard, et L. Fesquet, « Static Timing Analysis of Asynchronous Bundled-Data Circuits », in *2018 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, mai 2018, p. 110-118. doi: 10.1109/ASYNC.2018.00036.

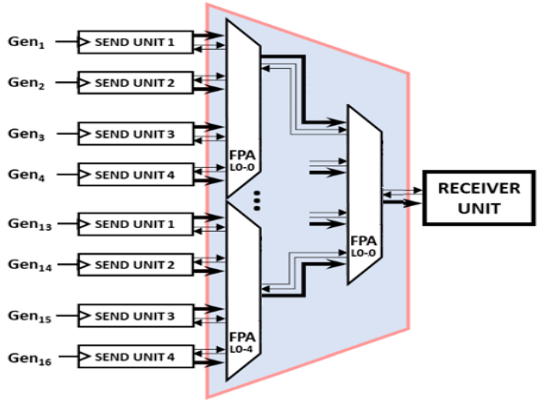
Arbiter design

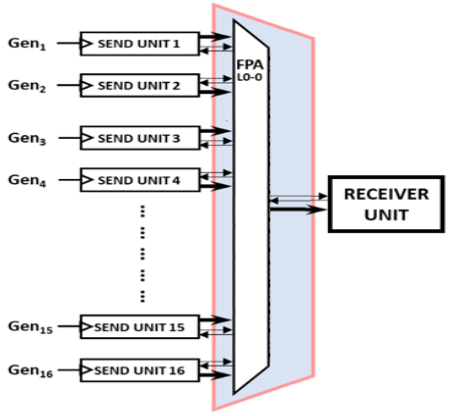


First designing a column

Symbolic view of differents size with 16 pixels (2to1, 4to1 & 16to1)





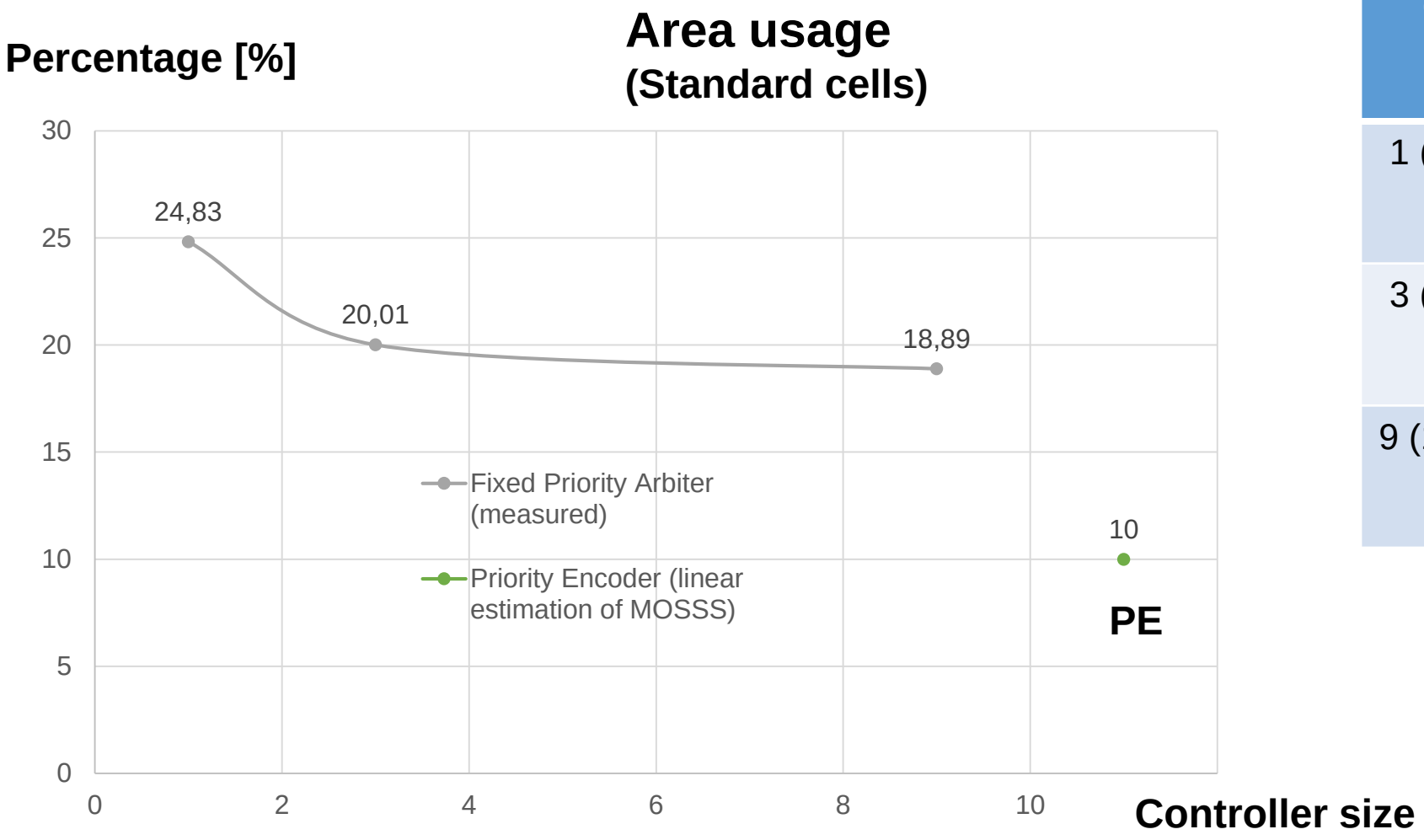


Soudier et al., « Design of chronous ASIC for CMOS sensor readout », 18th nto" Workshop on Advanced on Radiation Detectors

Results of differents size with 512 pixels (2to1, 8to1 & 512to1)

Circuit	9 levels	3 levels	1 level
Area (normilazed)	1	0,81	0,76
Power consumption (normilazed)	1	0,77	0,64
Reading speed (ns)	12,46	5,8	5,49
Estimate reading speed for one level (ns)	1,38	1,93	5,49
Bandwidth (pixels/100ns)	17	14	15

Results on area to fit in small pitch

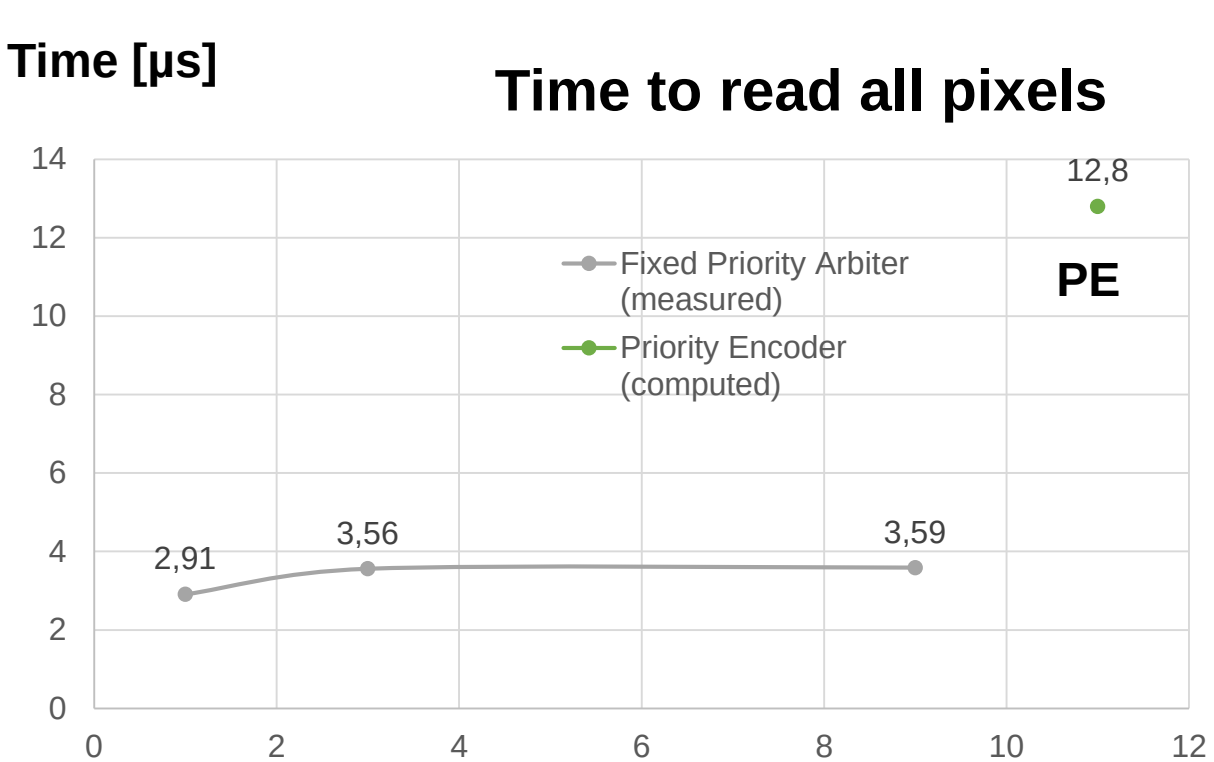


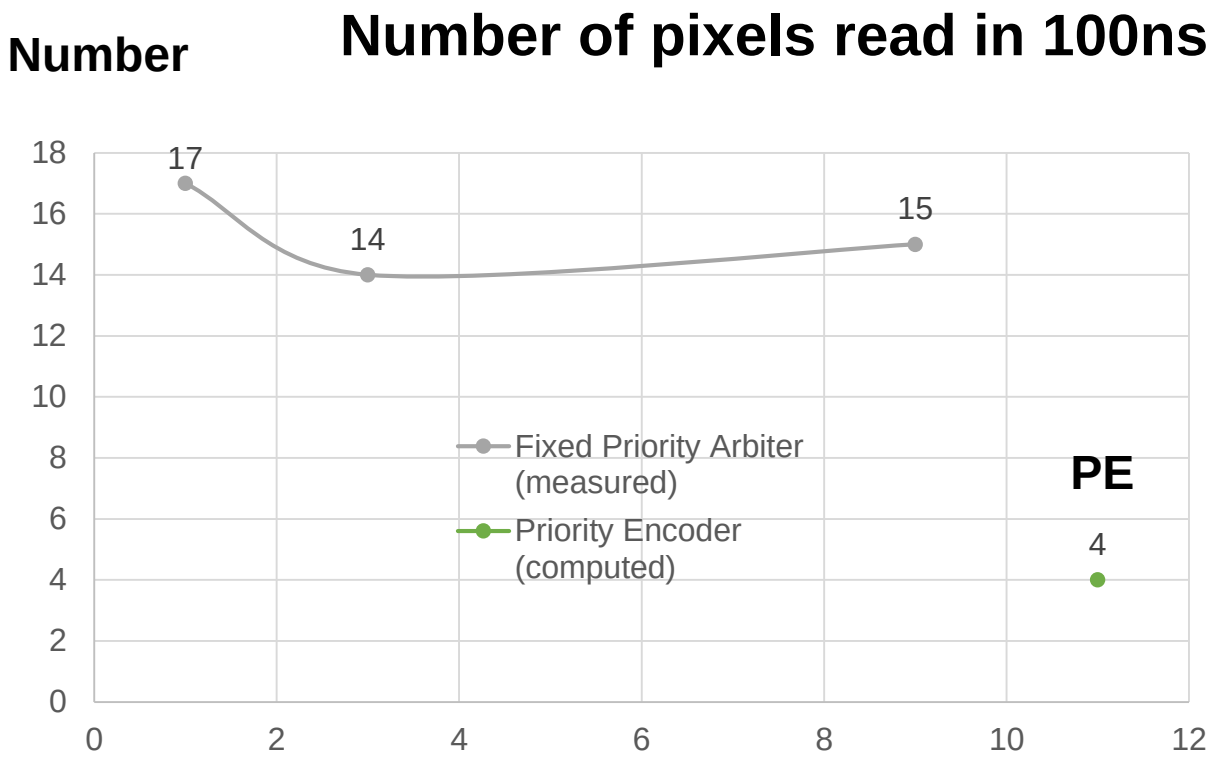
Controller size	Pourcentage of Gcells full (routing cells)
1 (9 levels of 2 to 1)	44,31% (limitation, huge congestion)
3 (3 levels of 8 to 1)	0%
9 (1 level of 512 to 1)	0%

[1] J. Soudier et al., « Design of asynchronous ASIC for CMOS pixel sensor readout », 18th "Trento" Workshop on Advanced Silicon Radiation Detectors

Functional results for 512 pixels

Test name	Description	Type of results
Functional	Firing every pixels to evaluate the bandwidth	Time to read all pixels and number of pixels read in 100ns

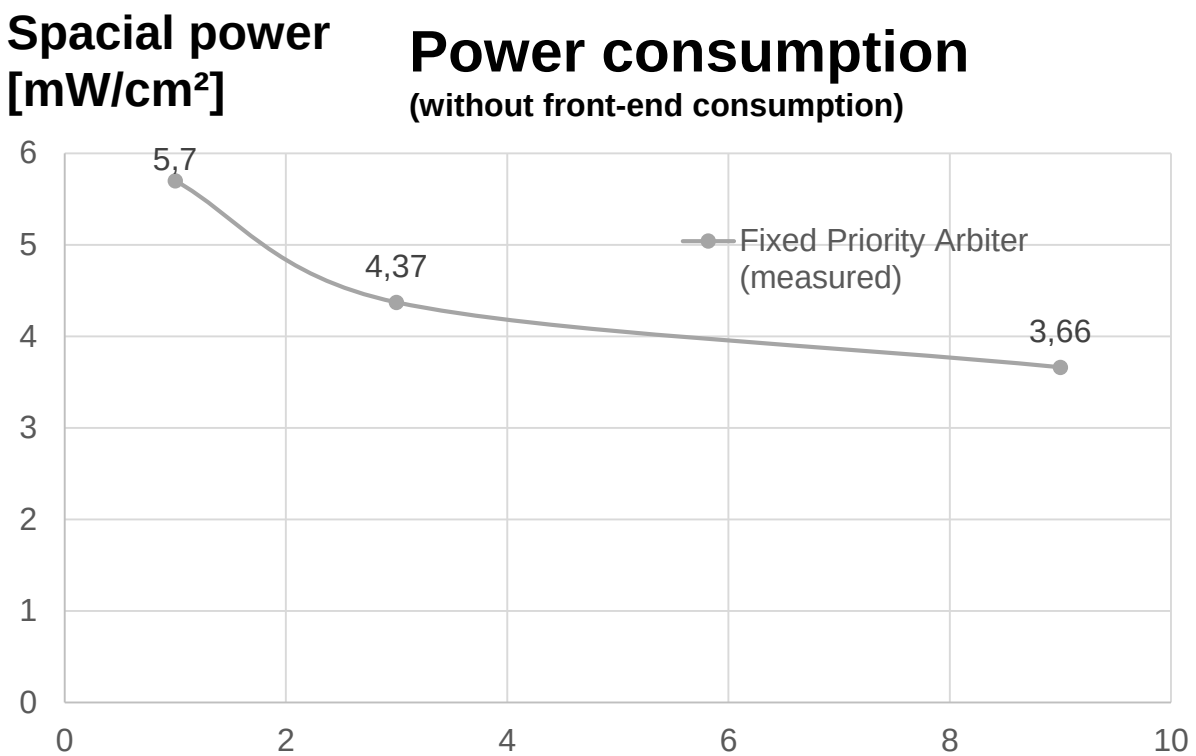


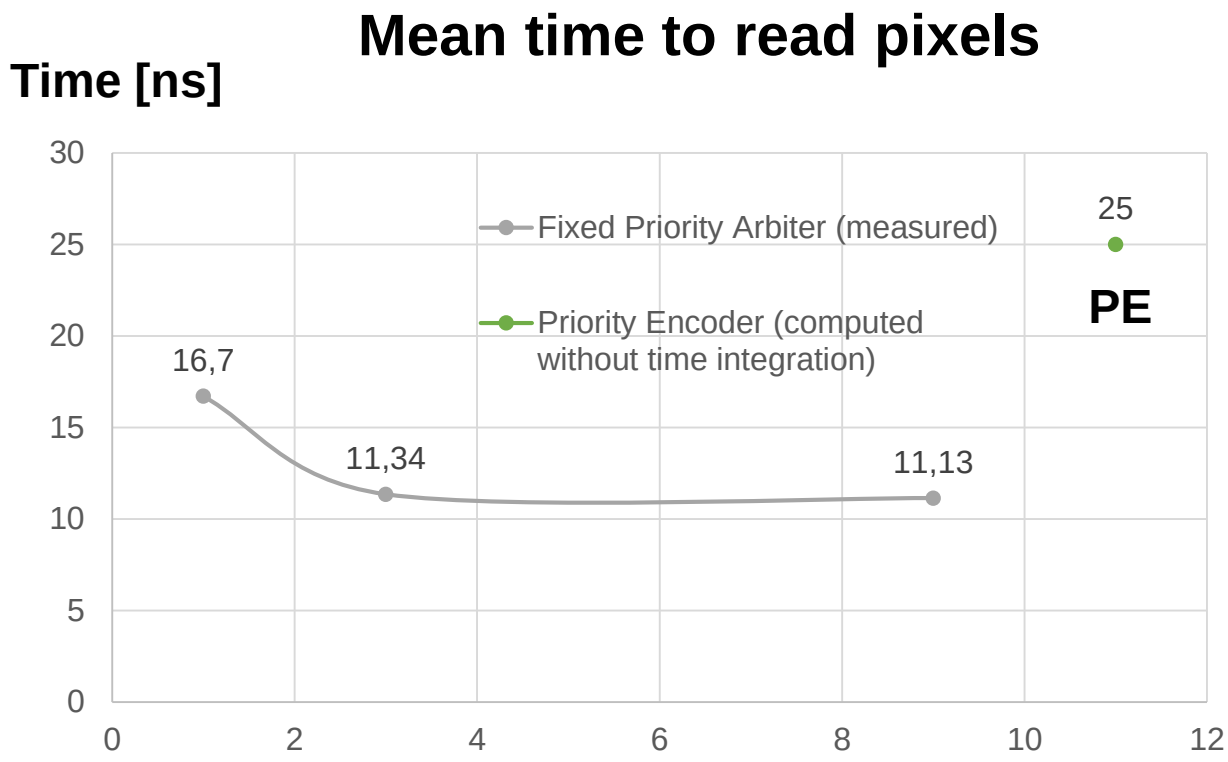


[1] J. Soudier et al., « Design of asynchronous ASIC for CMOS pixel sensor readout », 18th "Trento" Workshop on Advanced Silicon Radiation Detectors

Exploitation results with 330 MHz/cm² hit rate

Test name	Description	Type of results
Classical usage	98 pixels firing during 100 µs	Power consumption and mean hit rate





[1] J. Soudier et al., « Design of asynchronous ASIC for CMOS pixel sensor readout », 18th "Trento" Workshop on Advanced Silicon Radiation Detectors

Specifications

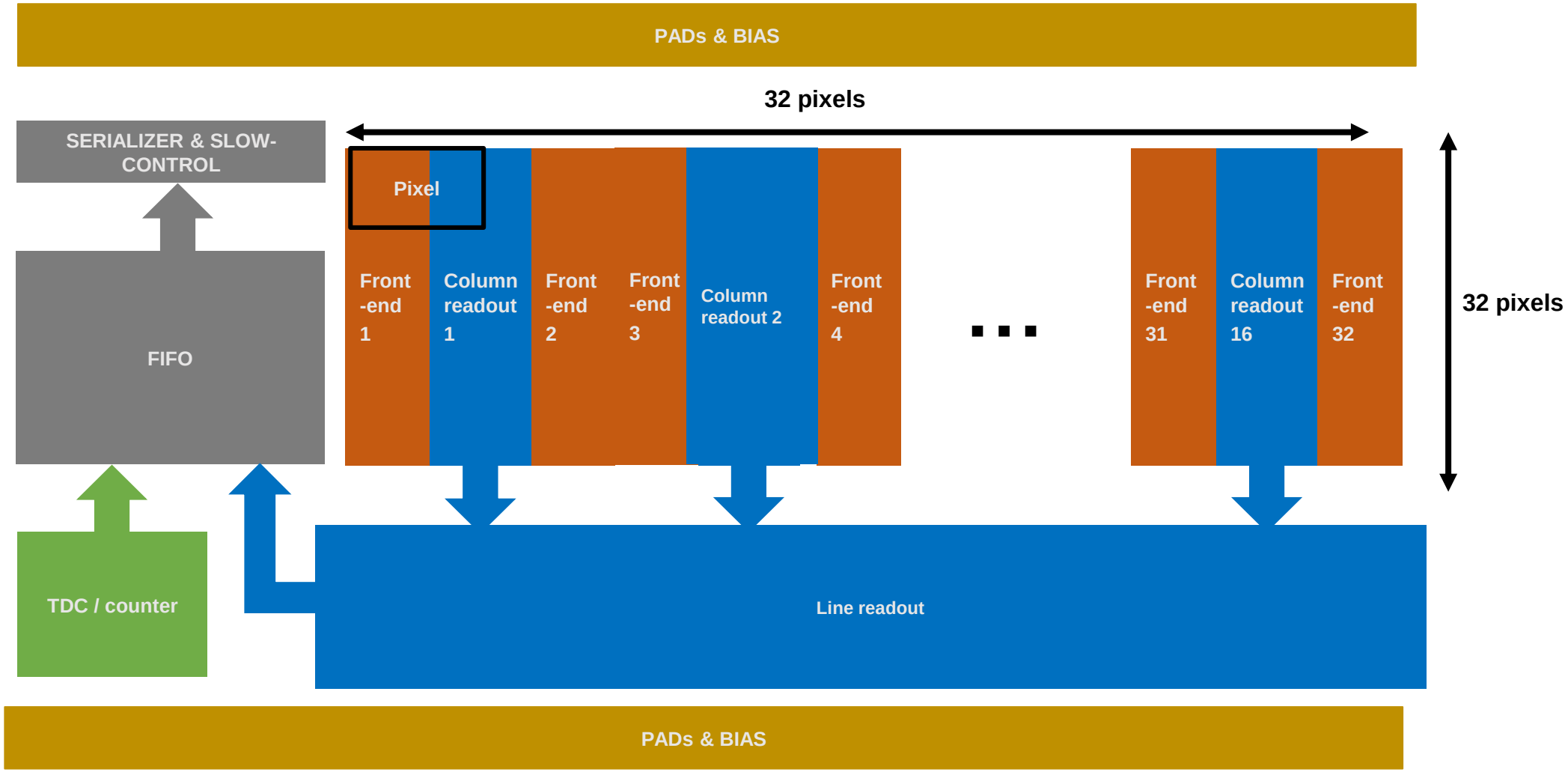
Fixed Priority Arbiter:

- **low-power (no cooling system is needed > 10mW/cm²)**
- **high rate (less than Ghit/cm²)**
- **small pitch (achieve 18µm pixel pitch)**
- **use a 2ns TDC**

Suited for experiments:

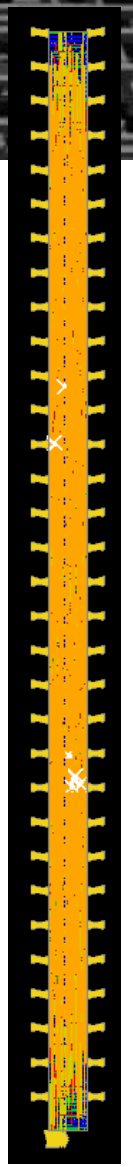
- **ALICE, CMS, ATLAS**
- **BELLE II, FCCee**
- **Quantum physic**

Proposal of a small chip in ER2 (65n)



Column design

Double column signoff design for a 64 to 1



Summary table of the flow

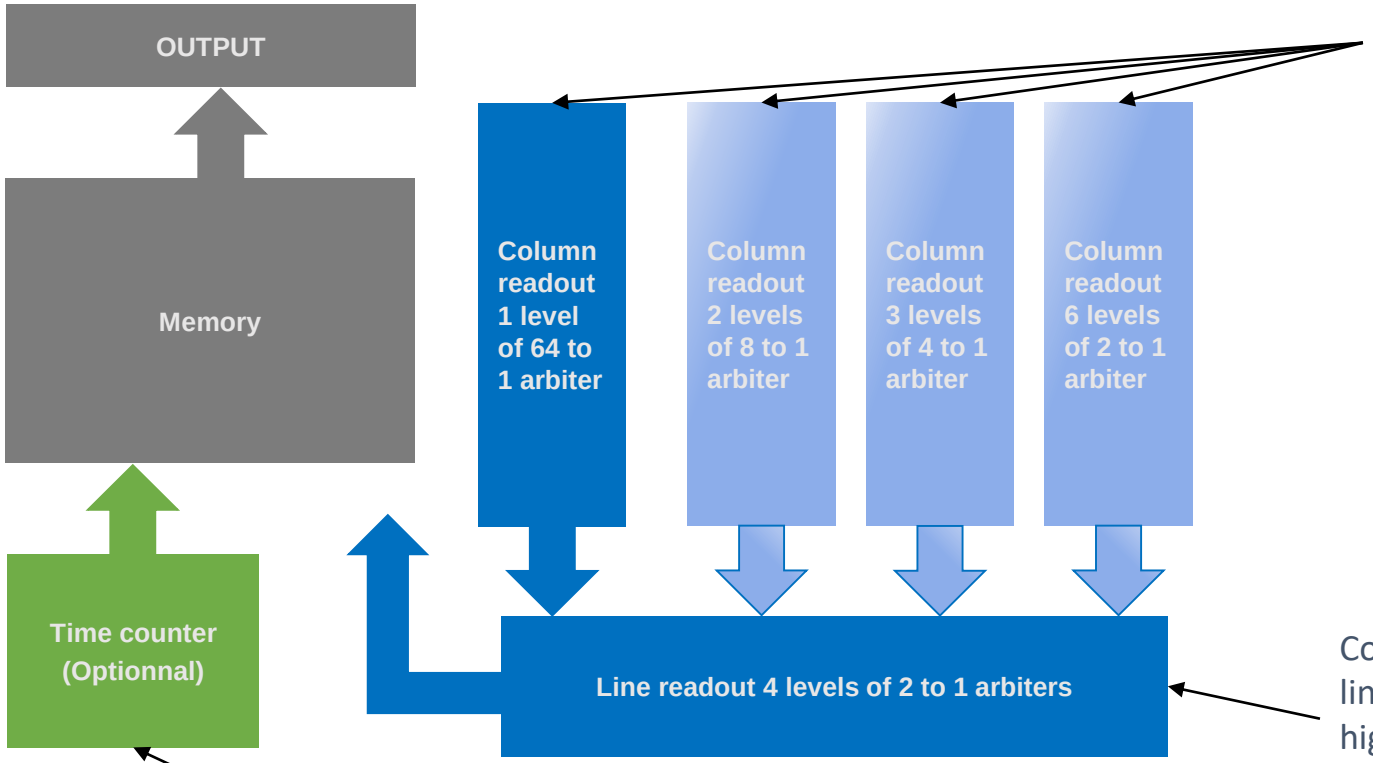
Type	Min (ns)	Mean (ns)	Max (ns)
functionnal	4.29	4.48	4.79

Type	Ratio readed pixels (%)	Mean (ns)	Max (ns)	NB particuls	NB noise	NB events	NB events on col	Rate (MHz/cm^2/s)	Hit/TW (Hits/100ns)
real	100.00	7.79	14.52	31	50	113	7	34.06	18

Snapshots	Setup (all)			Hold (all)			Clock		Design			Power										Congestion	Route	
	WNS (ns)	TNS (ns)	FEPS	WNS (ns)	TNS (ns)	FEPS	Insts	Area (um^2)	Density (%)	Insts	Area (um^2)	Total (mW)	Total/Area (mW/cm^2)	Leakage (mW)	Leak/Area (mW/cm^2)	Internal (mW)	Int/Area (mW/cm^2)	Switching (mW)	SW/Area (mW/cm^2)	Clock (mW)	Clock/Area (mW/cm^2)	Max	Total	DRC	WL (um)
opt_signoff	0.035	0	0	0.262	0	0	334	2865.120	55.13	845	6224	0.00	6.05	0.00	5.89	0.00	0.07	0.00	0.09	0.00	3.89	14.00	28.00	0	71699

The SPARC sensor prototype

Prototype based in an inside matrix shape in 65nm



Design of differents column sizes

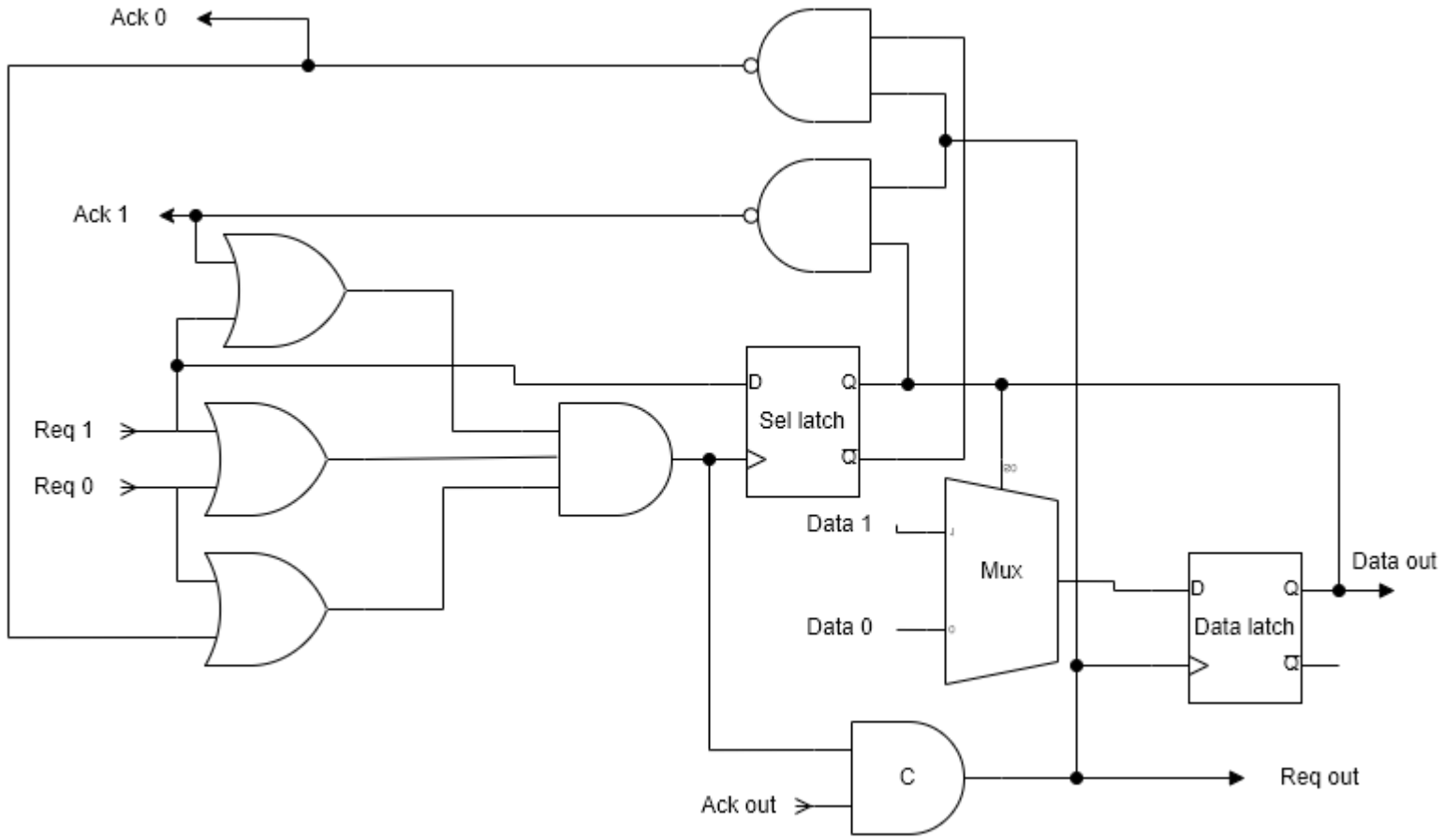
Compromise on the line readout with a higher bandwidth instead of the area

Could come with a time counter to add timestamps on hits

Conclusion

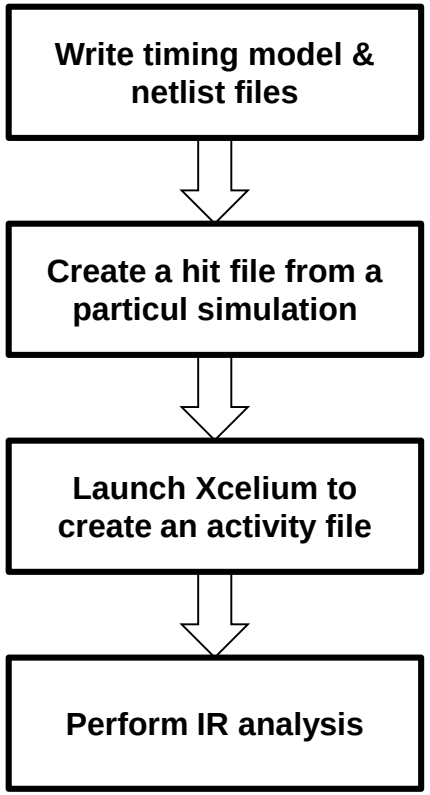
- Creation of an asynchronous digital flow for Cadence tools
- Conception of a prototype for particule physics with differents sizes of controller
- Creation of a flow and reporting for particule physics to analyse and compare differents chips

Timing reduction



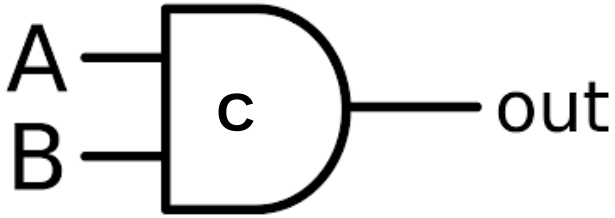
IR signoff

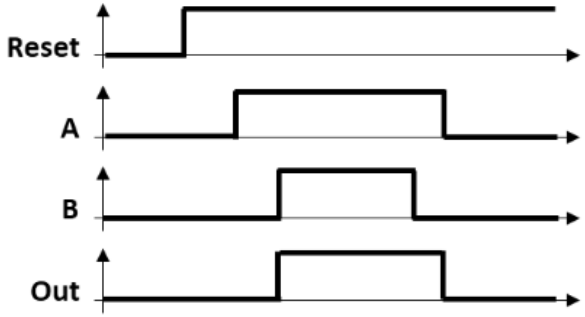
Matrix size
Type of particuls
Time frame
Azimutal angle
Patern IDs
Noise frequency

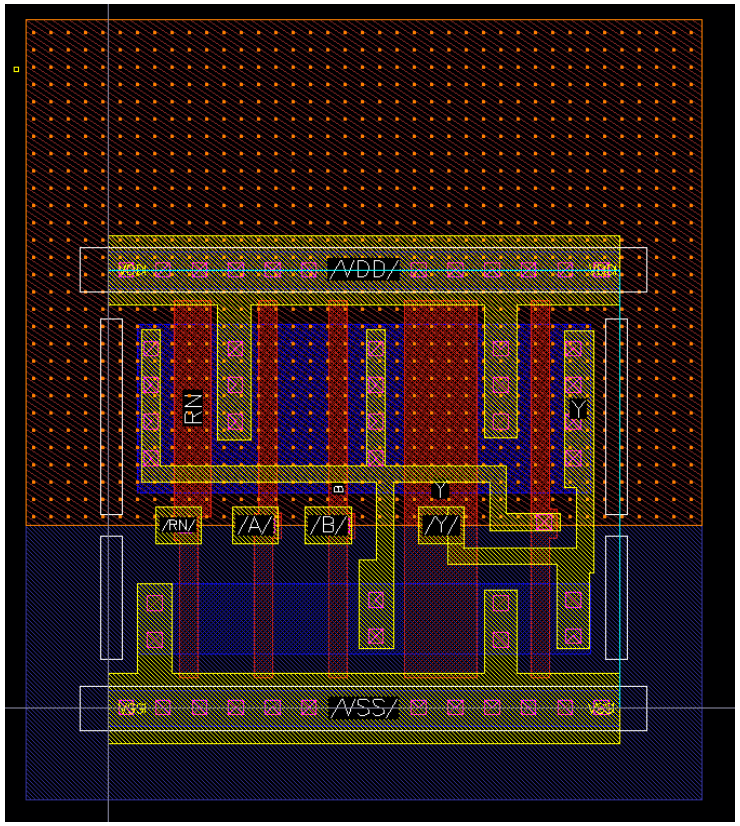


Local synchronization

C gate







[1] E. Aguénounon *et al.*, « Design and Characterization of an Asynchronous Fixed Priority Tree Arbiter for SPAD Array Readout », *Sensors*, vol. 21, juin 2021, doi: 10.3390/s21123949.