SCALINX

NEW ART OF SIGNAL CONVERSION

Standard JESD204B & JESD204C. Implement exemple.

Journées de l'ingénieur IN2P3/CEA

Standard JESD204B & JESD204C. Implement exemple.

R&D Department

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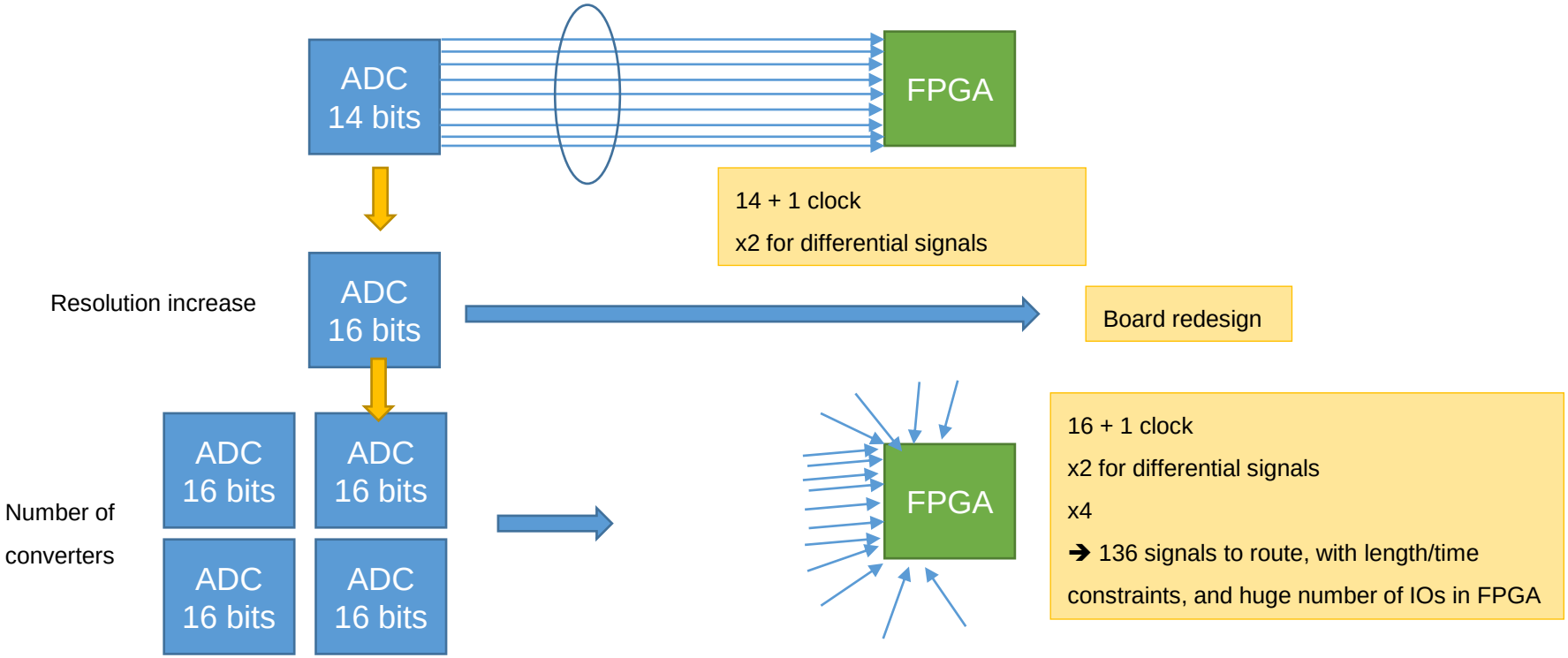
12 Juin 2023

Presentation outline

1. A brief introduction to JESD204 B/C
2. Use cases
3. Validation overview

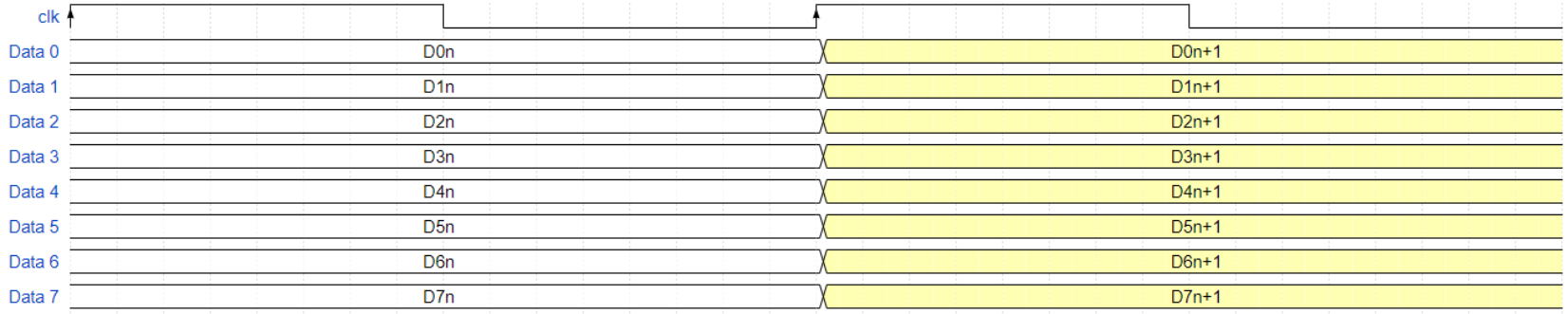
1. Introduction to JESD204 B/C

The problem with parallel interface



1. Introduction to JESD204 B/C

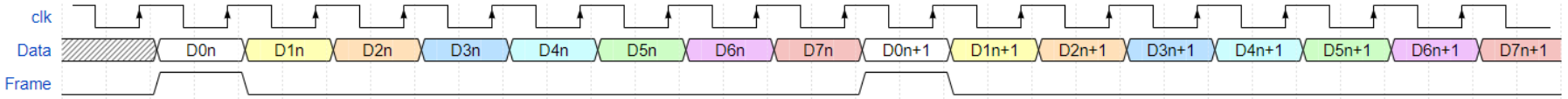
Move to Serial LVDS



Reduce the number of lanes

Increase the data rate of the SLVDS buffer

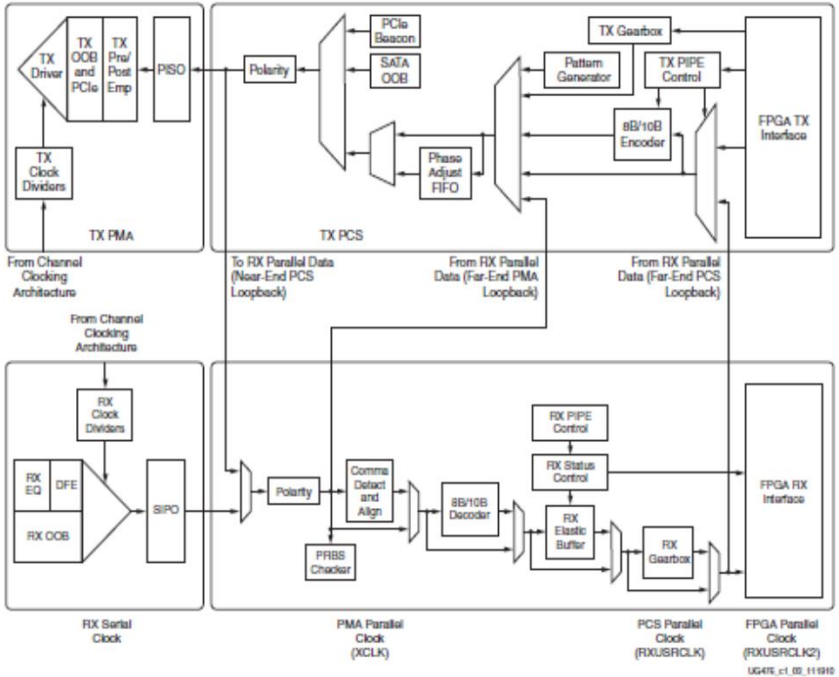
Need an extra signal for the Frame indication



1. Introduction to JESD204 B/C

Move to SERDES

Idea: reuse the bricks already available for the other standard (USB, SATA, Ethernet, etc)

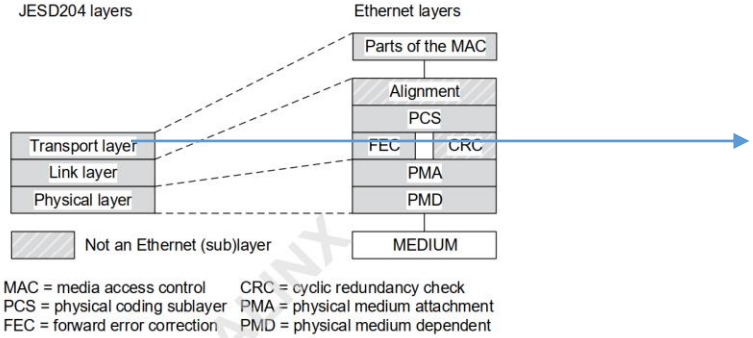


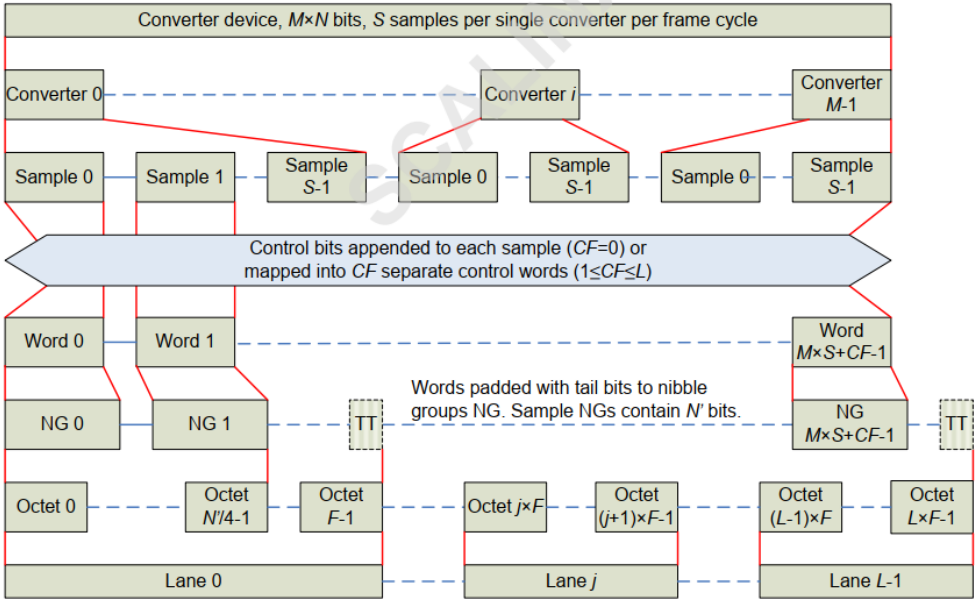
- Clock Data Recovery
- Multi Lane alignement
- 8b/10b – 64b/66b encoding
- Pre-emphasis/Equalizer
- BIST (pattern Generator/checker)
- Clock synchronization

Already available in FPGA from low range to high range

3.12Gbps, 6.25Gbps, 11Gbps, 17Gbps, 24Gbps, 32 Gbps +

Transport Layer

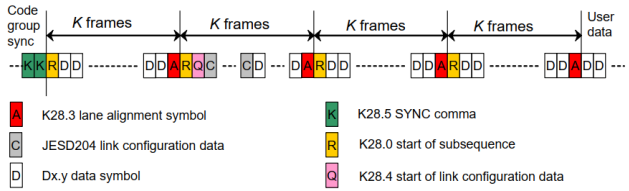


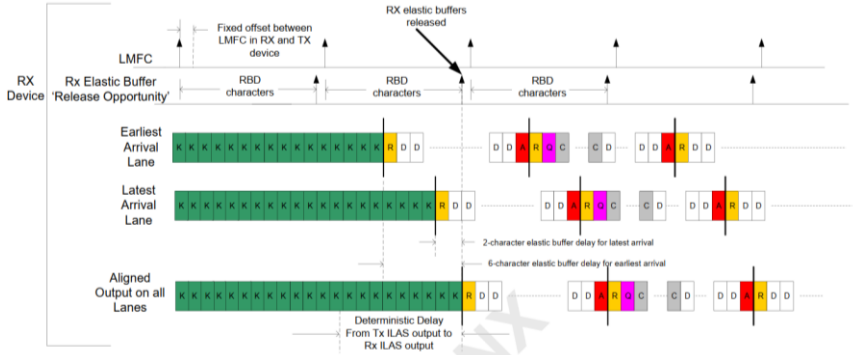


1. Introduction to JESD204 B/C

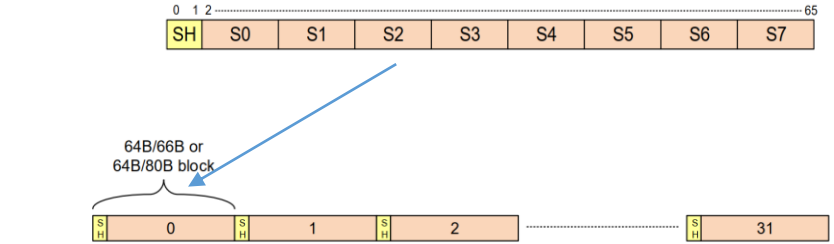
Link Layer JESD204B/C

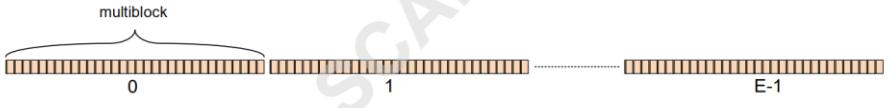
- 8b10b encoding
- Komma characters
- Inter Lane Alignement Sequence





- Block / Multiblock / Extended Multiblock format
- Scrambled data
- Sync header
- 64b/66b 64b/80b





No retransmission of error. Error detection available, Error correction possible (FEC/CRC)

1. Introduction to JESD204 B/C

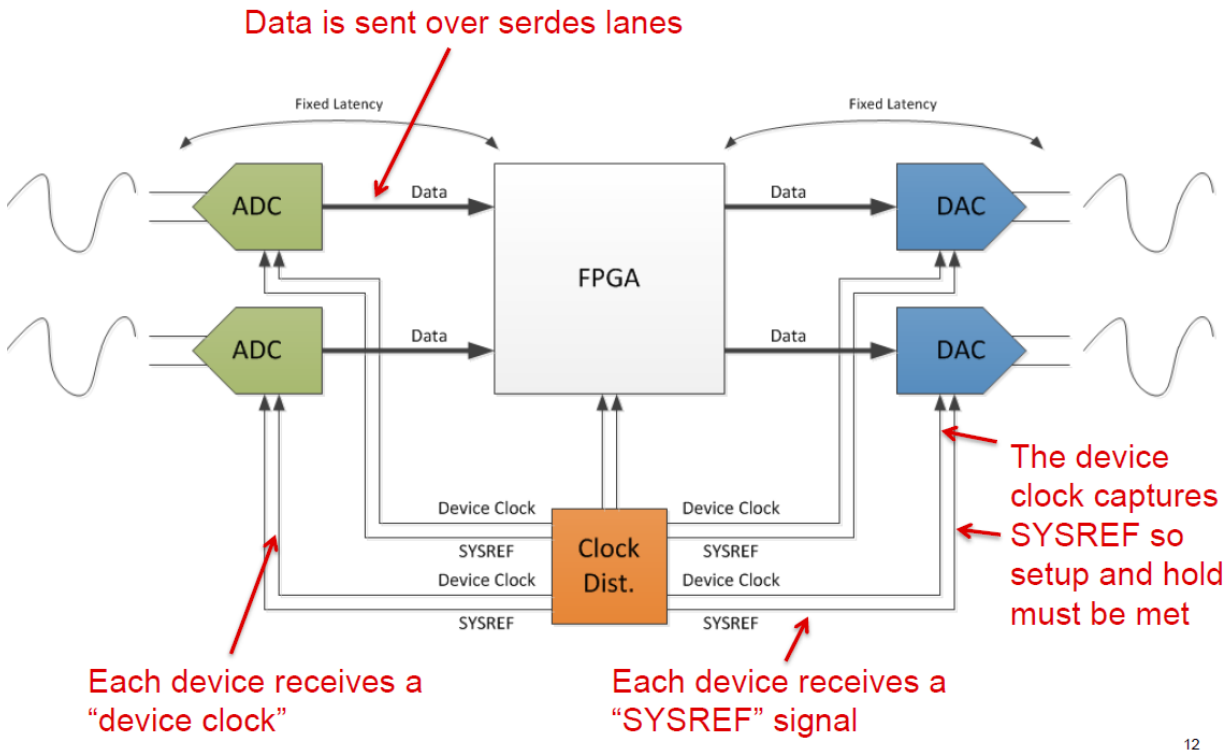
Physical Layer

CML interfaces

Eye diagram / return loss adjusted with data rate + transport channel length

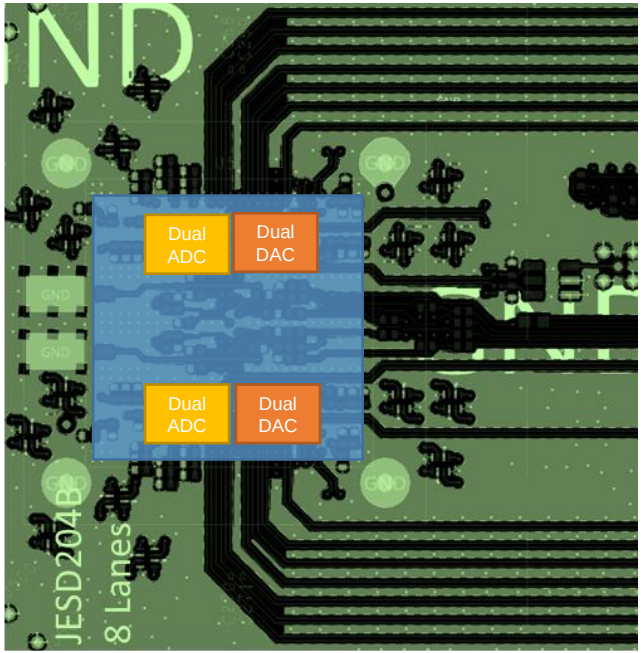
Data interface class	Minimum data rate (Gbps)	Maximum data rate (Gbps)
B-3	0.3125	3.125
B-6	0.3125	6.375
B-12	6.375	12.5
Category C	6.375	32

Devices synchronization



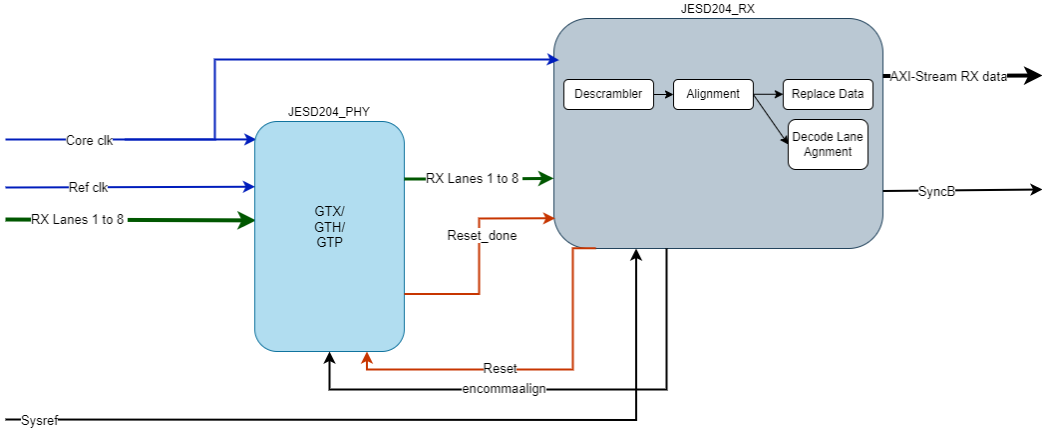
2. Use cases Example

- Example #1 JESD204B :
  - 2 x Dual ADC 16 bits: TX serializer 2x2 Lanes
  - 2 x Dual DAC 16 bits: RX deserializer 2x2 Lanes
  - Max Sampling Frequency : 208 MSPS
  - Max DataRate: 4.16 Gbps
- Example #2 JESD204B
  - Dual ADC 16 bits: TX serializer 4 lanes
  - Max Sampling Frequency : 500 MSPS
  - Max DataRate: 13.3 Gbps

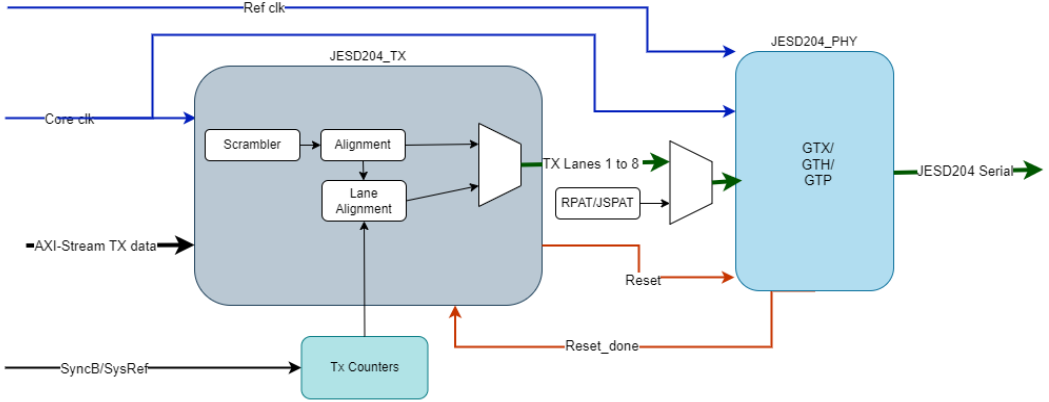


2. Use cases Example

- RX FPGA Implement

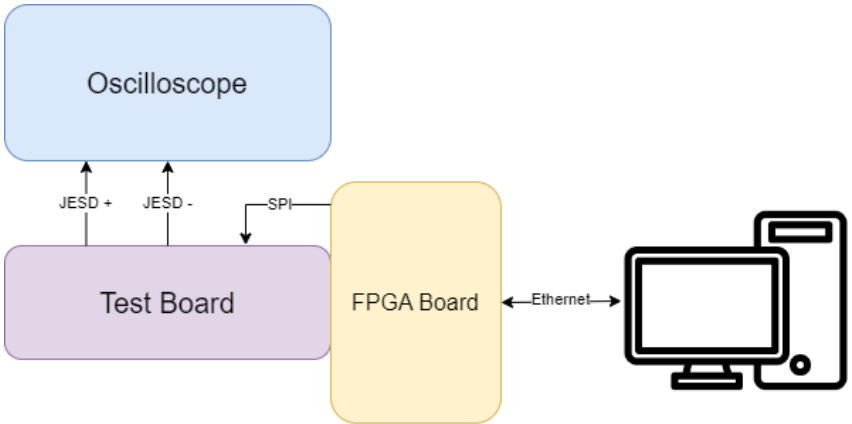


- TX FPGA Implement

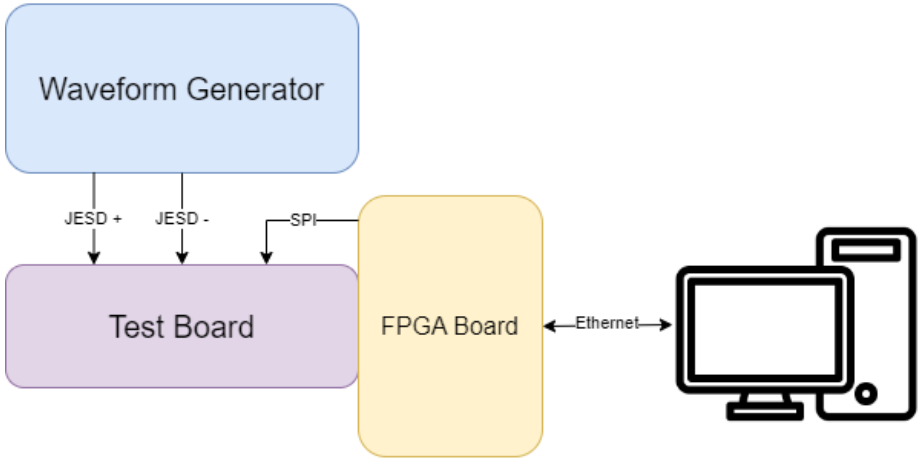


3. Validation overview

- Setup TX measurements :
  - Tektronix DPO73304SX
  - FPGA Xilinx



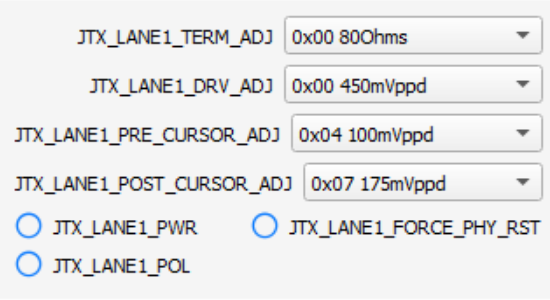
- Setup RX measurements :
  - Tektronix AWG70001B
  - FPGA Xilinx



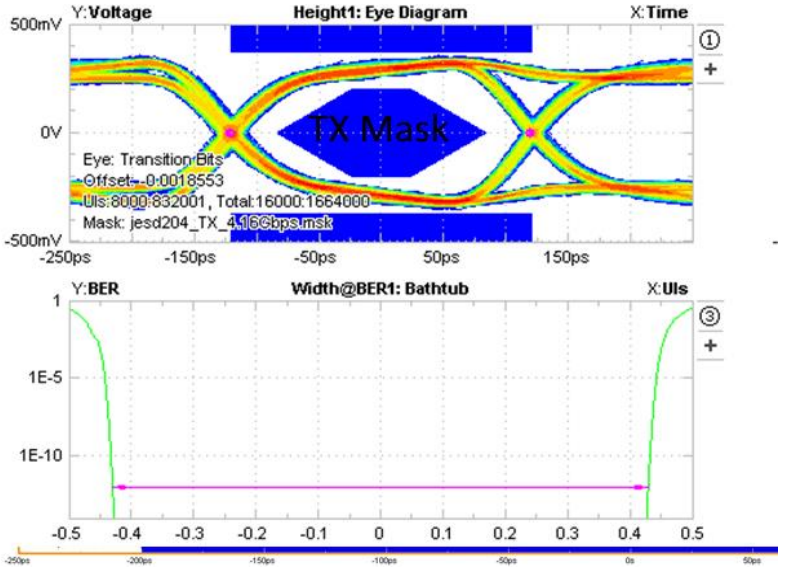
3. Validation overview

- Eye diagram measurements

- Adjust PHY Serializer :
  - Pre-emphasis
  - De-emphasis
  - Termination
  - Voltage Drive
  - Current Drive

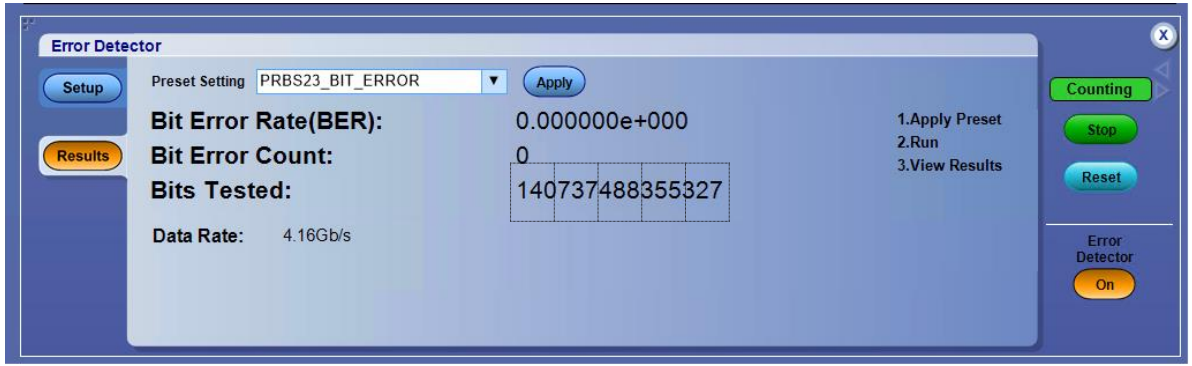


- Test sequence :
  - Pattern used was JSPAT.
  - Oscilloscope was set to Eye diagram measurement. (Tektronix DPO73304SX)



3. Validation overview

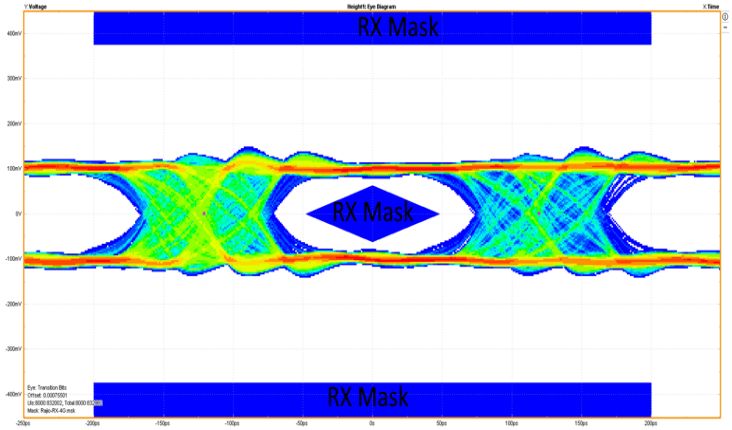
- BER TX measurements
  - BER objective is ≤ 1e-15
  - Test was run for ~70 hours and no errors were detected.



3. Validation overview

BER TX

- Configure AWG eye diagram for RX BER test



Signal from AWG to DPO

Tektronix AWG70001B

Tektronix DPO73304SX