SPIDER “Swift Pipelined DigitizER”

for timing path measurement of upgrade II LHCb

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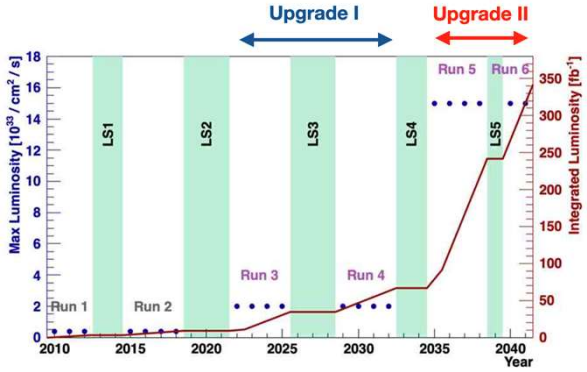
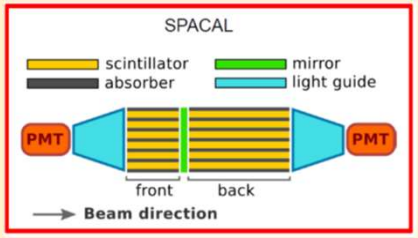
Plan

- ✓The U2 detector
  - Detection, Electronics
  - Requirements for new timing path
- ✓How to achieve the specifications
  - Digital TDC vs Waveform TDC
- ✓New Electronics chain
- ✓SPIDER “Swift Pipelined Digitizer” ASIC
  - Concept, architecture, performances
- ✓Status of SPIDER development
- ✓Summary

The Upgrade 2 (II) detector 1/3

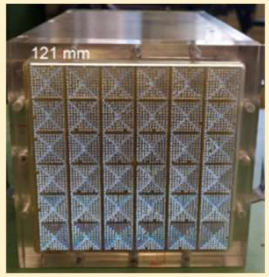
Integrated lumi:
from 50 fb^{-1} in run 3
to 300 fb^{-1} in runs 5 + 6

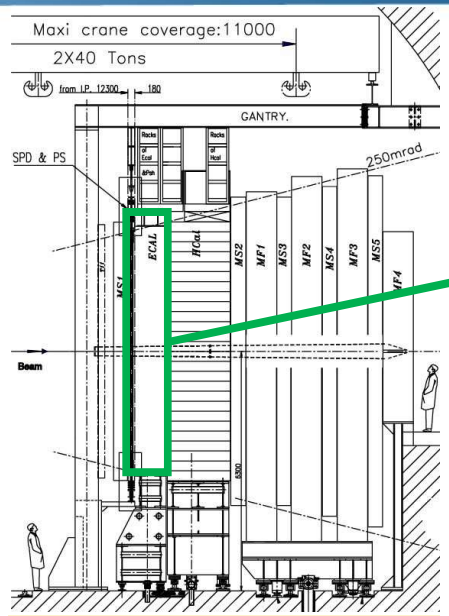




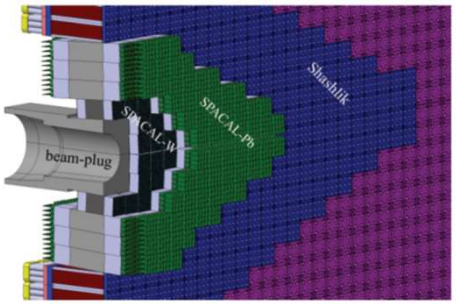
SPACAL W-Polystyrene
20ps@20GeV, 10ps@100GeV

Technologies for PicoCal R&D

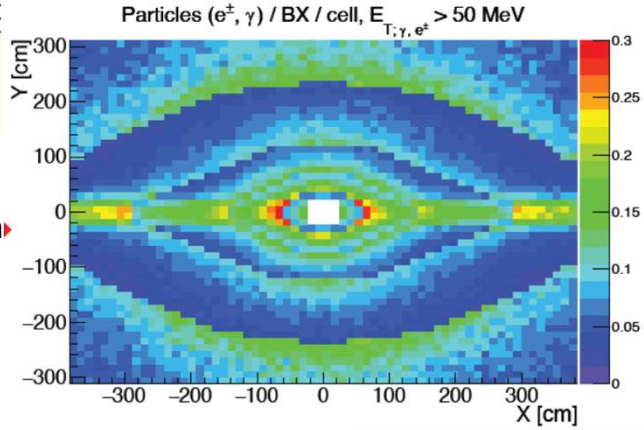




The future UII detector:
« **PicoCal** »

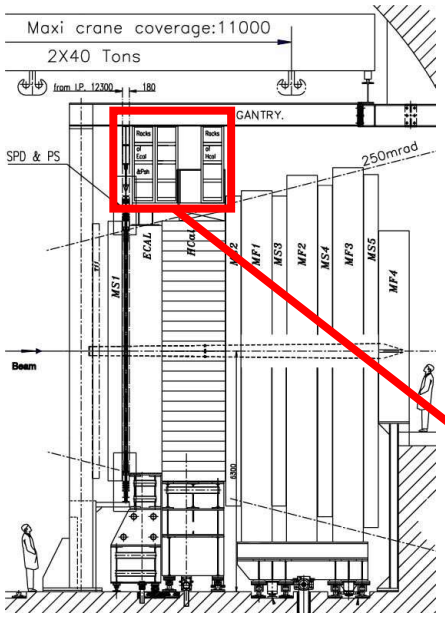


UII detector occupancy



- For the phase 2 upgrade, the central part of the detector will be equipped with SPACAL modules to deal with radiation (up to 1MGy).
- Shashlik will remain in the outer part (< 40kGy).
- **In order to limit the occupancy, the size of the modules will be reduced thus their number increased → from 6,000 to ~ 15,000 channels**
- Introduction of longitudinal segmentation and double sided readout => **~ 30,000 channels** (baseline option)

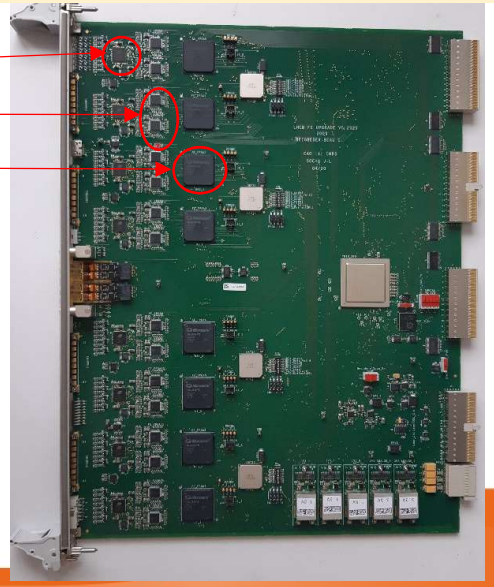
Current electronics



- The 10 electronics racks are located on the platform => 12 to 20m cables but low radiation level (400 Gy for UII)
- **18 crates**
- Currently **256 front-end boards** (32-channel each)

The original front-end board (2008-2020)

The new front-end board since phase1 upgrade in 2020



New Front-end electronics expected : 64 channels per FE board

➢ Requirements for new timing path

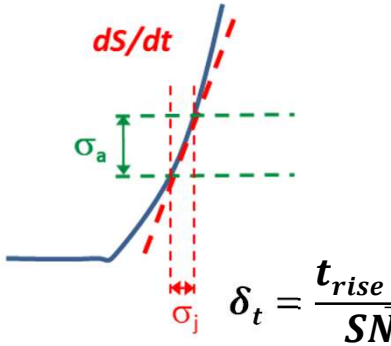
- **Target time resolution of 15ps rms @ [1-5 GeV] to distinguish multiple interactions**
- Target **energy range** for time measurement => **E_T = [50MeV-5GeV] => range of 100** …
- Deal with **maximum possible channel occupancy : 10% required originally but 50% would be much safer**
- If you look at the current modules and electronics: rise time of 5ns with 1mV rms noise → jitter of 250ps rms !

⇒ We have to reduce **both rise time and noise**

⇒ To give an idea, to get a resolution of 20ps rms with a rise time of 1ns and a noise of 1mV rms, you need a 50 mV pulse

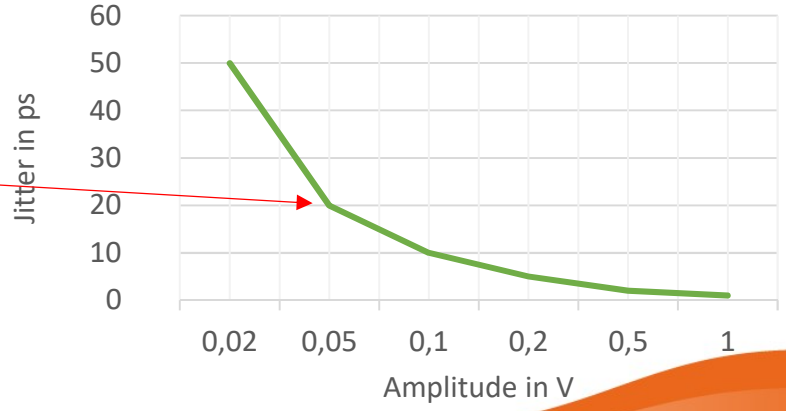
- 1ns seems to be a (below the ?) limit for the PMTs so we have to do our best concerning the noise to get the largest possible dynamic range
  - Noise is **the sum of detector and electronics contributions**

Theoretical electronics time resolution:



$$\delta_t = \frac{t_{rise\ time}}{SNR} = \frac{Noise}{Slope}$$

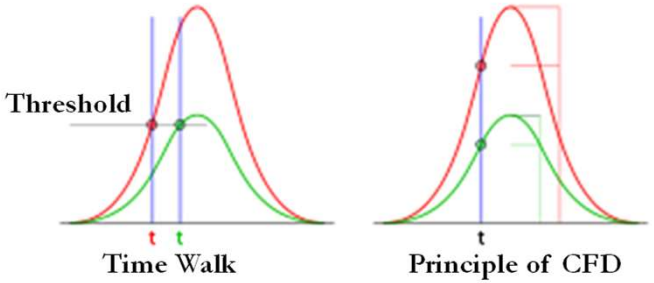
Evolution of the jitter with the signal amplitude (rise time = 1 ns, noise = 1mV)



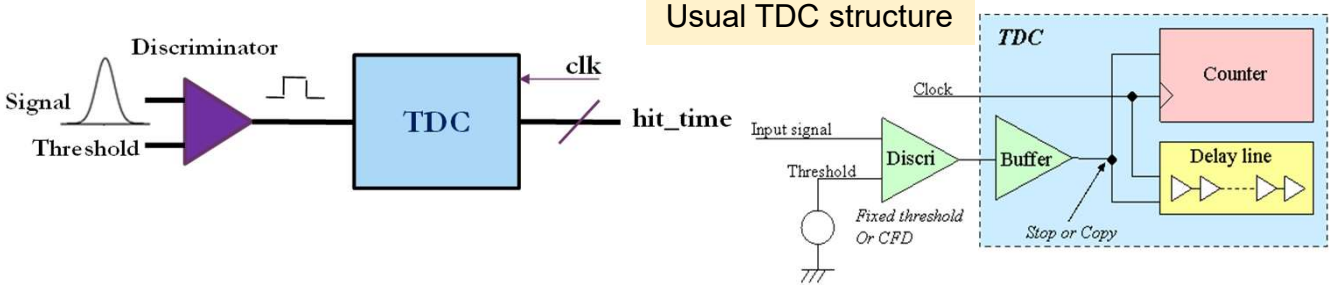
➢ Standard Time to Digital Converters chain (TDCs)

- The usual candidates for time stamping of fast signals. They are designed either in the form of **dedicated ASIC** or integrated inside **high-end FPGAs**.
- They are self-triggering and can withstand high counting rates
- A TDC has a strictly digital input => **a discriminator** has to be present to transform the **analog signal into digital**. It introduces **additional jitter and residues of time walk** => the overall timing resolution is degraded to **the quadratic sum of the discrimination and TDC contributions**.

When sending a signal to a discriminator, the time instant "t" of the output level toggling will depend on the amplitude of the signal
→ **"Time Walk"** effect

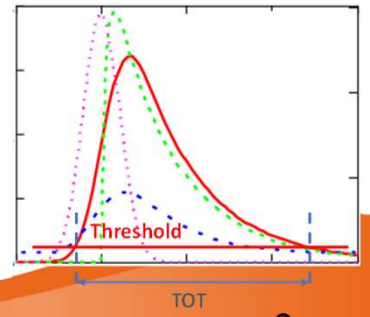


Usual TDC structure



To avoid the Time Walk effect, one has to use a Constant Fraction Discriminator (CFD)

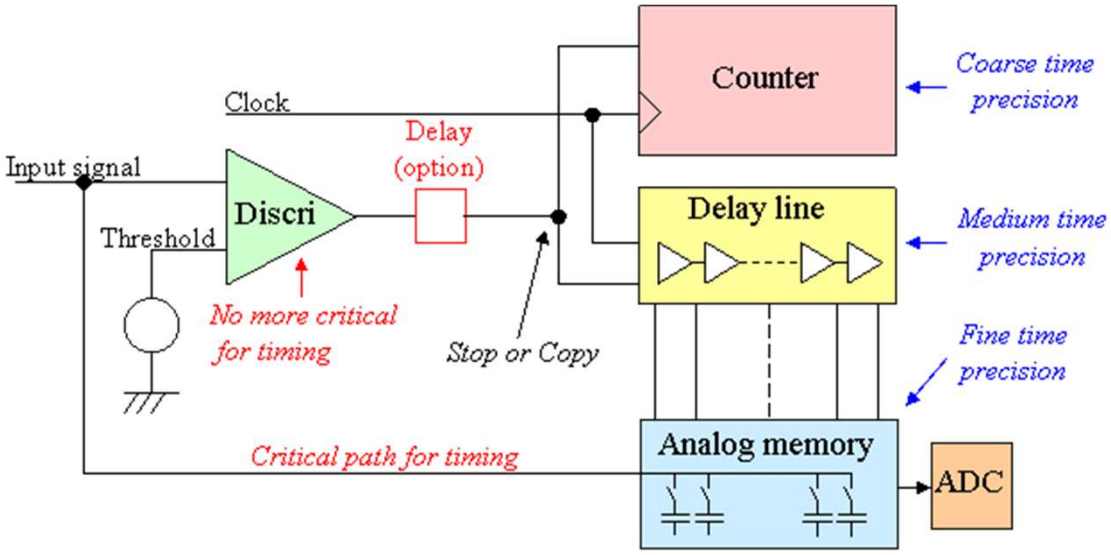
- But this implies that **you need to know the value of the peak** to apply the threshold !
- Ok for firmware or software when the signal has been digitized but **not in a TDC which does not provide information on waveform**, except under the derivate form of time over threshold (**TOT**) thus with a limited precision (especially because of the asymmetry of the signal edges).



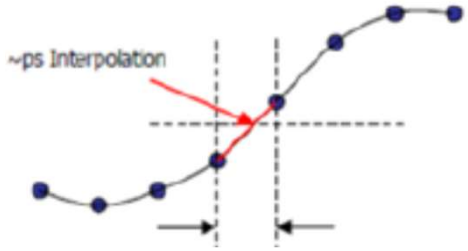
➢ « Waveform TDC » chain

- **concept introduced by LAL/IRFU in 2009: association of DLL-based TDC and of analog-memory based Waveform Digitizer**

- The TDC gives the coarse time of the samples and the samples give the final time precision after **CFD interpolation** => **resolution of a few ps rms**
- Digitized waveform gives **access to signal shape**…
- All channels are self-triggering, conversely to TDC, discriminator is used only for triggering, **not for timing**

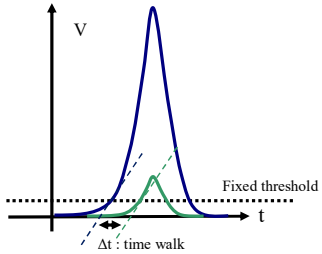


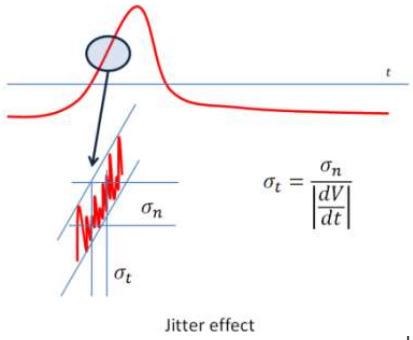
16 bits in the chip
+ 24 bits in the FPGA



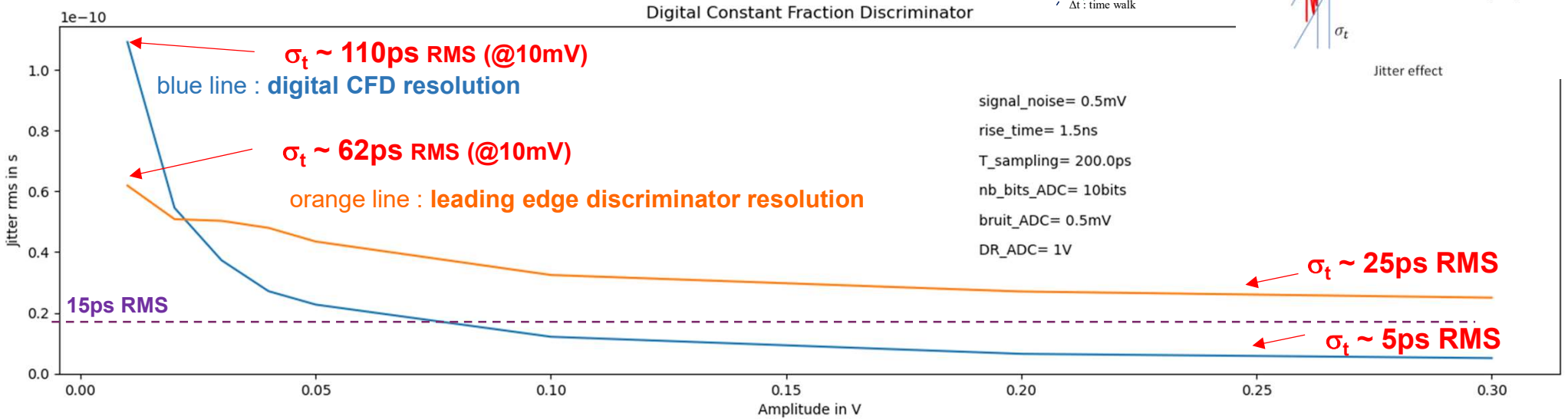
➢ Timing jitter versus signal amplitude for large dynamic 100

Set-up : rise time = 1.5ns ; σ_{noise}= 500µV RMS





V_{in} ranges from 10mV to 1V
→ discriminator threshold is set to **5mV** (half the minimum signal)



Digital CFD required to achieve the time resolution <15ps for a large dynamic : waveform TDC, a good candidate but limited in counting rate !!

➢ Concept of the « pipelined digitizer »

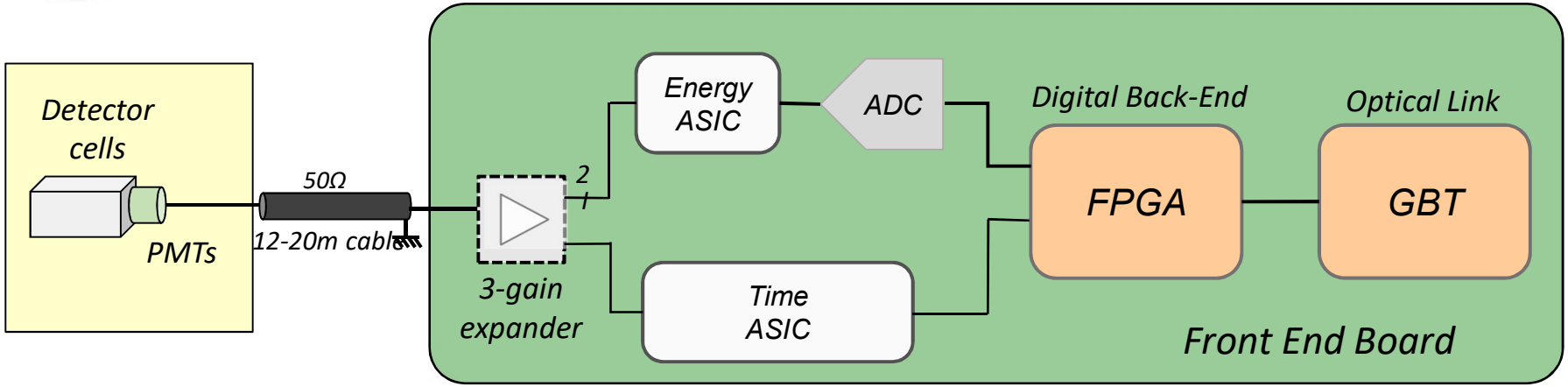
A standard digitizer (like Sampic) is made of a single circular memory bank with a sampling depth of N signal points which limits the counting rate due to conversion dead time

- **To increase the counting rate, a multi-bank memory working like a pipeline is required and must run sequentially**
- **To implement multi-bank memory with a reasonable size per channel (physical constraints), we define a optimized sampling window to deal with only the interesting part of the signal, which consequently reduces the size of each memory bank**
- **To reduce the channel data rate, only the necessary samples (8 ?) for making the dCFD calculation possible are sent to the companion FPGA**

With this improvements, the pipelined waveform TDC is a good way to address the requirements on timing path

New electronics chain

➢ Chosen architecture

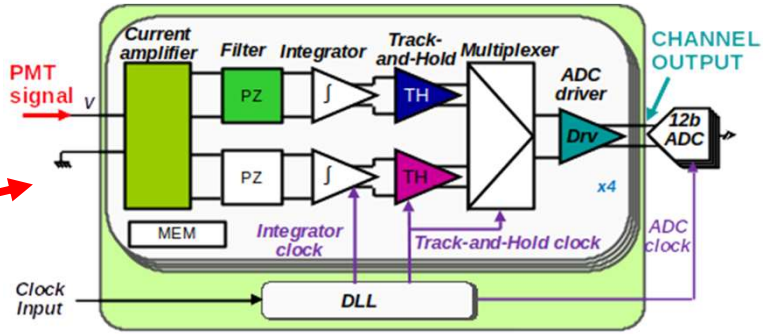


➢ Two separated processing paths with dedicated ASICs in the same technology: **CMOS 65 nm**

- ➢ **Energy path** close to the current ICECAL scheme (mostly analog processing)
- ➢ **Independent timing path** based on SPIDER waveform TDC

=> can be **used for other application or type of detector**

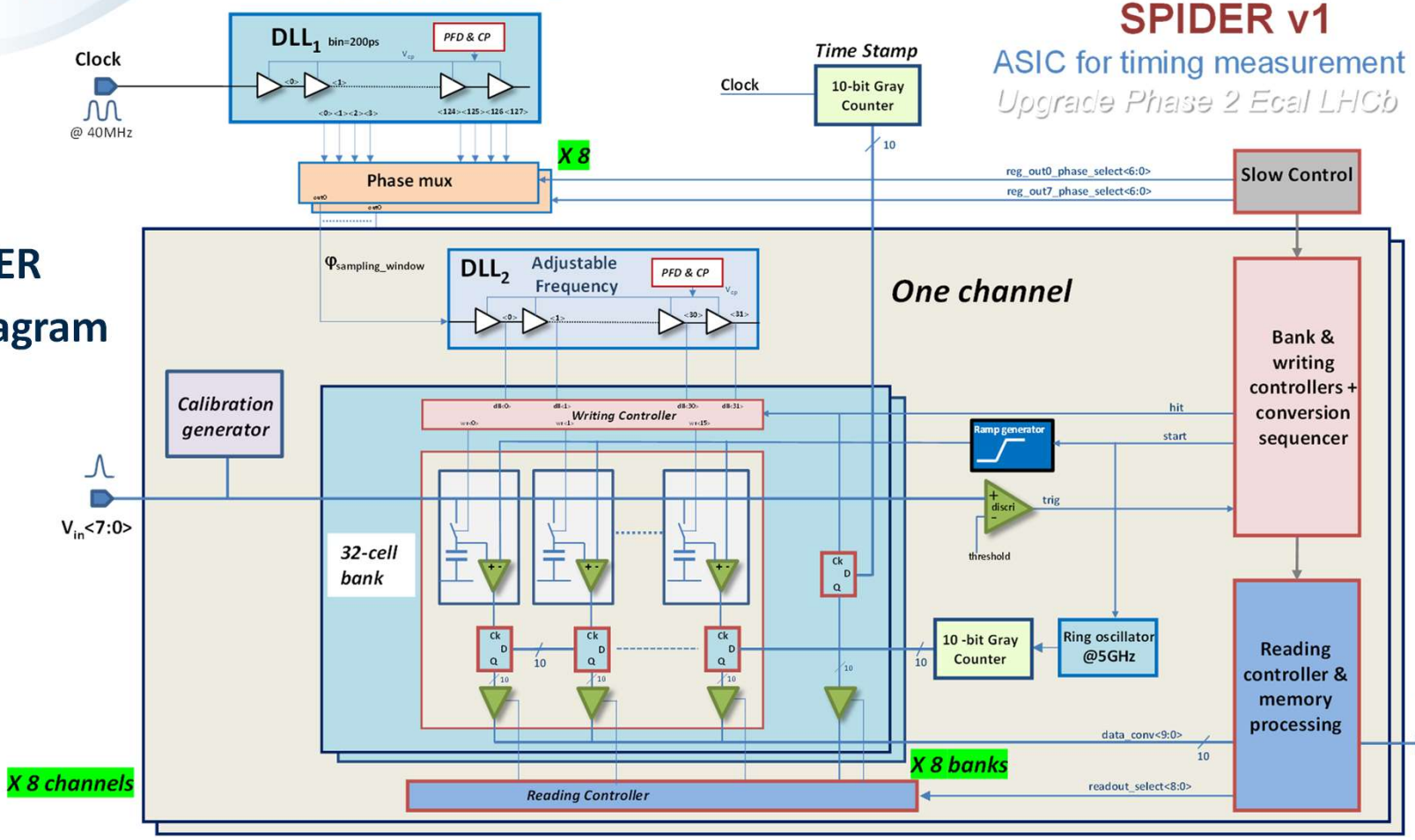
- ➢ For dynamic range compatibilities, **3 different gains** must be provided
  - ➢ 50MeV to 100GeV over 2 gains for energy measurement
  - ➢ 50MeV to 5GeV (single gain) for time measurement



SPIDER "Swift Pipelined Digitizer" ASIC 1/4

➢ Architecture

SPIDER block diagram



8 samples +

1 Time Stamp +

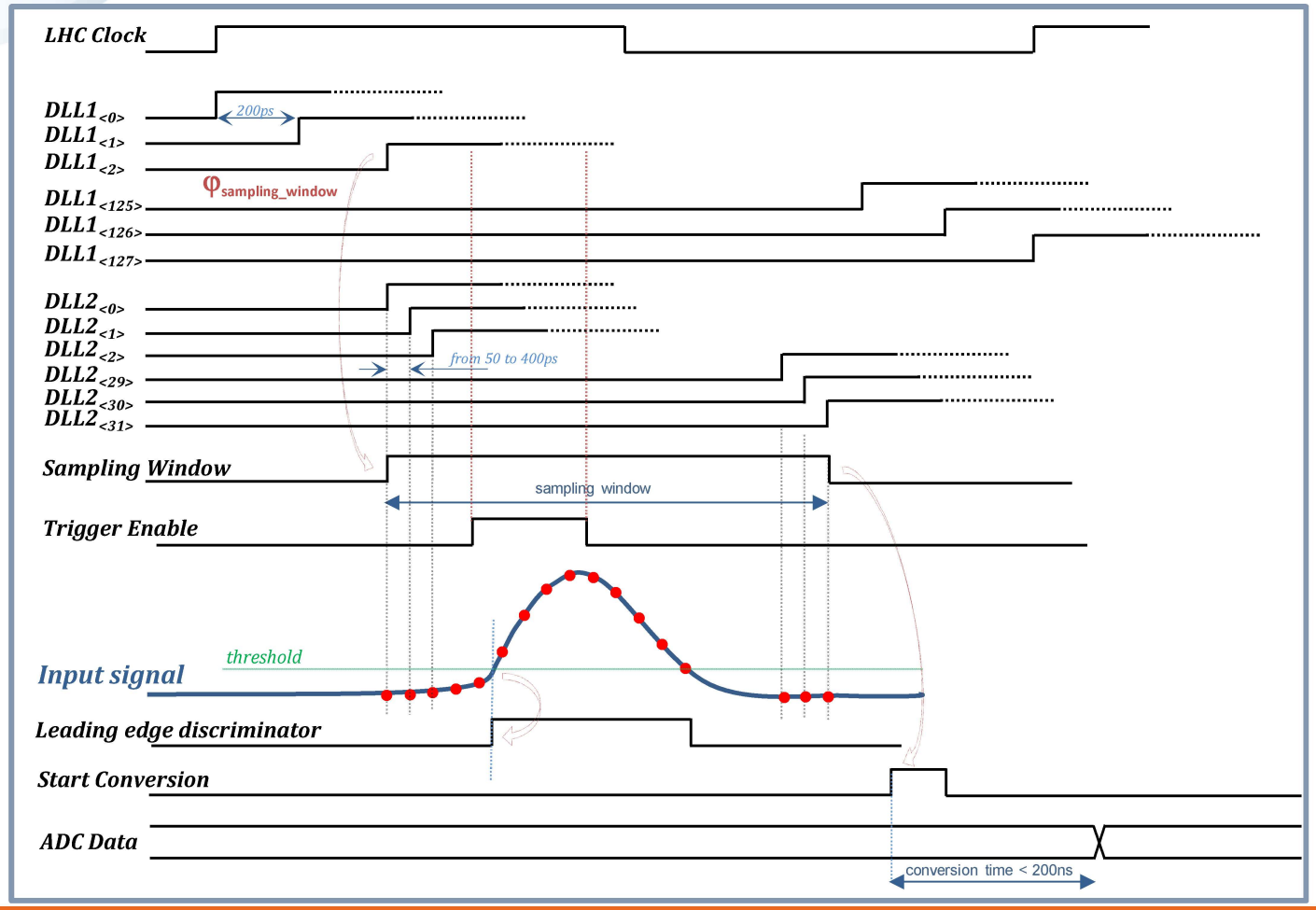
1 id_bank

= 10 data words of 10 bits

X 20Mevt/s (50% occupancy)

= up to 2Gb/s per channel

➢ Architecture



SPIDER chronograms

➢ Main specifications

- ➢ **Technology: 65nm (the most lasting technology, 10 years (?)), 1.2V power supply**
- ➢ **Input signal : rise time from 1ns to 1.5ns, dynamic range V_{in}=[10mV-1V]**

To achieve the time resolution of 20ps, the requirements are:

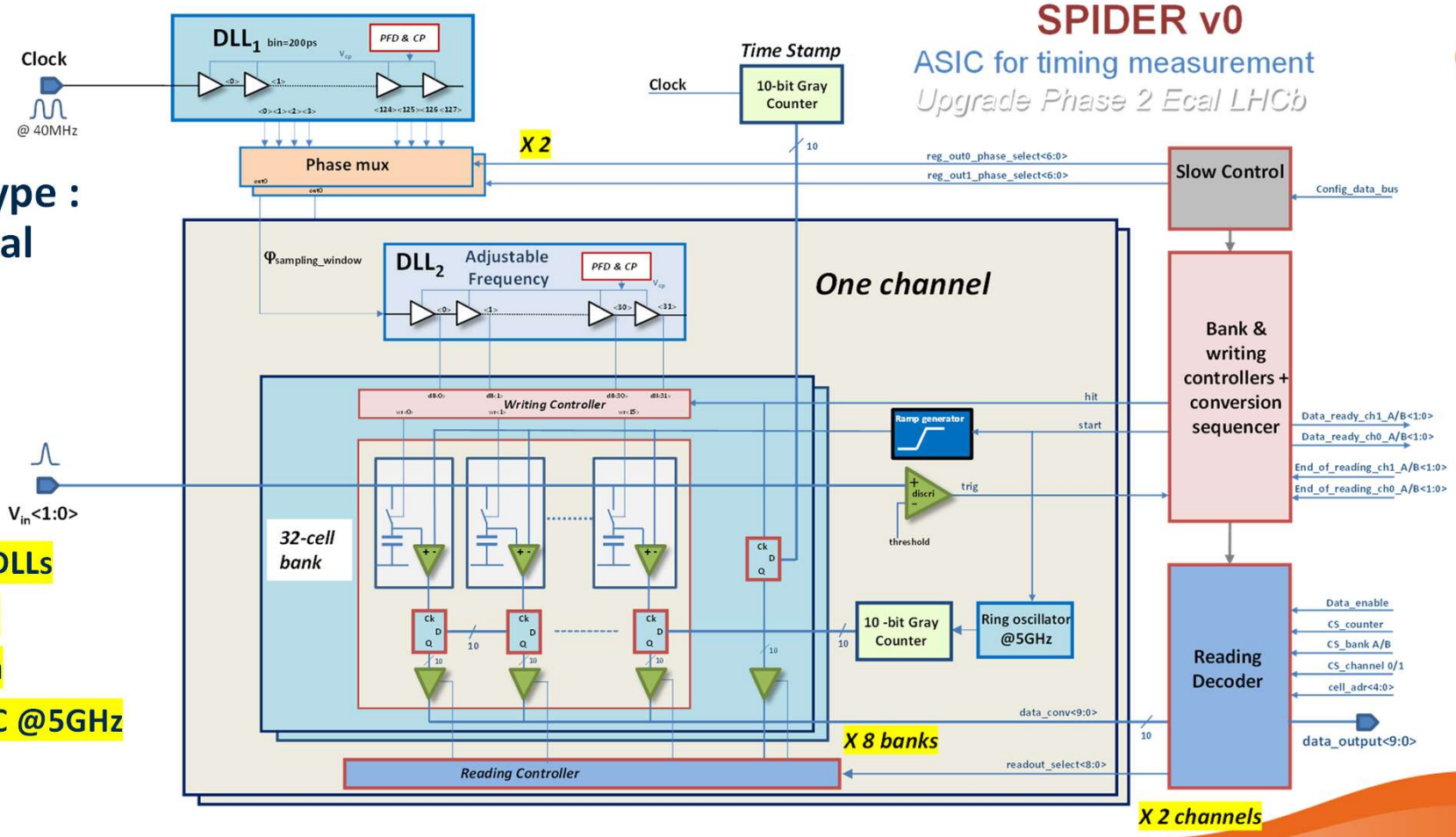
- ➢ **Need for a memory cell (switches & capacitor) compatible with a noise voltage around 0.5mV**
- ➢ **Need of a resolution of 10 bits for the sampling : 10-bit Wilkinson ADC@5GHz to reduce the conversion time (200ns for 10bits i-e 8 clock periods)**
- ➢ **Need for 128-delay-cell DLL1 running @40MHz → bin ≈ 200ps to tune the beginning of the sampling window**
- ➢ **Need for 32-delay-cell DLL2 running from 80MHz to 640 MHz → bin ≈ 50ps to 400ps to select the sampling frequency between 2.5GHz and 20GHz**

➢ **First prototype architecture: «2 eightfold-bank channels»**

SPIDER first prototype : contains all critical blocks

Proof of concept :

- ✓ **Clock distribution & DLLs**
- ✓ **Memory cell in 65nm**
- ✓ **Multi-bank operation**
- ✓ **10-bit Wilkinson ADC @5GHz**



Status of SPIDER development

➢ **R&T project @IN2P3 2021-2023** (*RS: P.Robbe & RT: C.Beigbeder*)

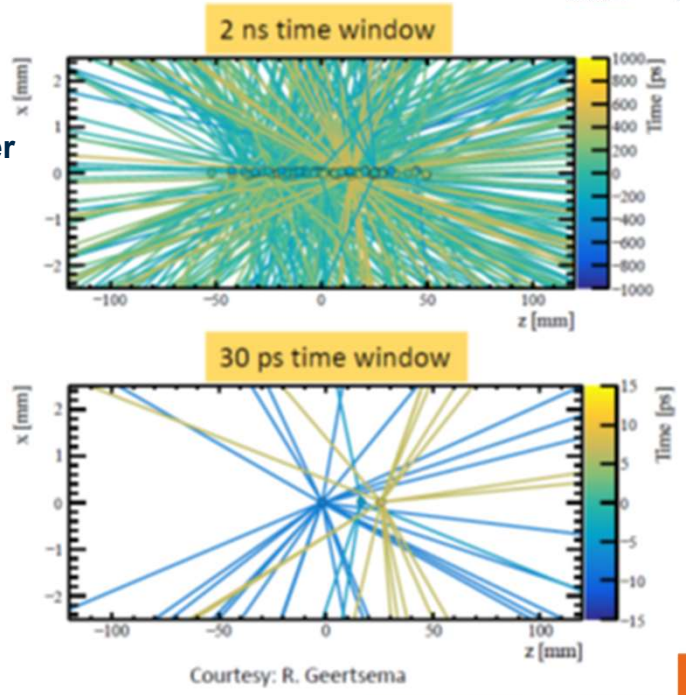
- Collaboration of **4 IN2P3 labs** (Orsay, Clermont-Ferrand, Caen, Lyon) led by IJCLab and LPC Clermont.
- Very challenging design! Has started six months ago.
- Repartition in **work packages** for:
  1) Delay Locked Loop (DLL1 & DLL2)
  2) Analog part (memory cell, trigger comparator, ADC comparator, ramp generator) + Sampling & ADC management (bank & write controller + conversion sequencer)
  3) Counting digital part for "10-bit Wilkinson ADC & coarse time" (Gray counters, ring oscillator)
  4) Slow control & Readout management part (read decoder)
  5) Phase Locked Loop (not critical for first prototype)

  ⇒ The first prototype submission is expected at the **end of 2023**

The idea is to start with few channels of new electronics during run 4: **front-end boards, ICECAL65 & SPIDER…**

Summary

- For 4D calorimetry, we need to develop electronics with **large dynamic range** and **very good time resolution**
  - As shown, the association of the two requirements is **a challenge…**
- Based on our long experience in the design of **analog memories**, we feel like the **Waveform TDC** can be an adequate solution to face this challenge
  - Waveform indeed contains all information
  - A low threshold has **no impact on time resolution**
  - Extracting only the most useful samples for the time extraction limits the readout time
  - There is **a lot of bandwidth margin for faster signals** which may **directly reduce the jitter**
  - This solution can work for **many other types of detectors** …
- Our main targets:
  - **Short term**:
    - Reduce the electronics noise and increase the dynamic range
    - Reduce the conversion time while keeping the massive parallelism of the ADC
    - Get the best possible time INL and jitter for the analog memory
    - Optimize the output dataflow
  - **Longer term**:
    - Perform on-chip data compression still allowing external feature extraction
    - Get closer to 100% occupancy
    - Measure **both amplitude and time** …



Courtesy: R. Geertsema

Thank you for your attention!