

numériseur GHz+traitement du signal NEGMA+REActif

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CNRS/IN2P3/GANIL/DPHY/GT**Acquisition**

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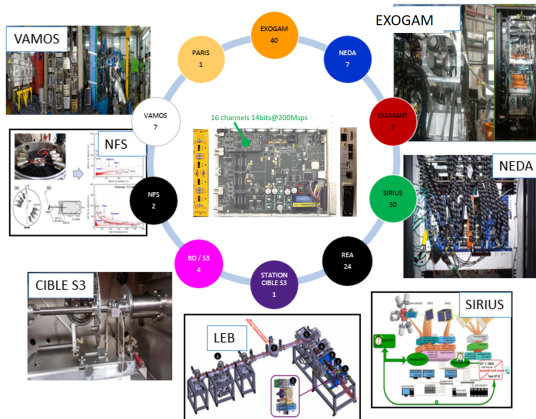
- 1 NEGMA
 - Introduction et contexte
 - Technologie choisie-caractéristiques
 - Premiers pas
 - Déroulement
- 2 NEGMA + REActif
 - acquisition GHz
 - matériels
- 3 REActif
 - traitement du signal
 - code informatique
 - carte HACKtif
 - performance
- 4 conclusion et perspectives

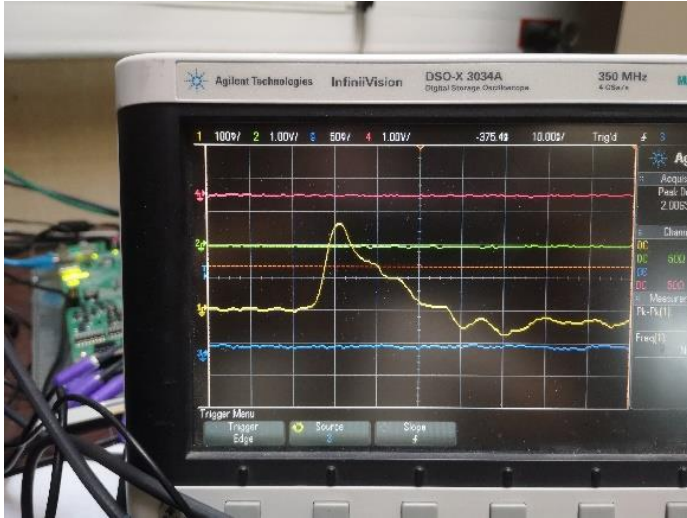
Introduction

NUMEXO2: Numériseur généraliste

Caractéristiques générales

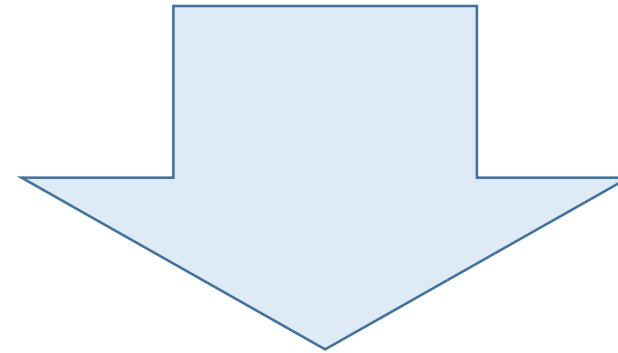
- ❑ Numériseur 14 bits / 200 Mhz (+/- 4 volt)
- ❑ 16 voies (ADC,QDC, TDC/TAC) ou
2048 voies multiplexées (Chambres à fils /
Chambres à dérivés VAMOS)
- ❑ Mesure de temps
 - ❑ TDC numérique (1ns), TAC (qq10ps)
- ❑ Discrimination numérique (seuil < 20 KeV)
- ❑ Inspections logiques/ analogiques chaînables
- ❑ Système embarqué Linux
- ❑ Ethernet @ 6 Mo/s
- ❑ Time stamp (GTS)
- ❑ Fort taux de comptage (qq 10 KHz à qq 100KHz)



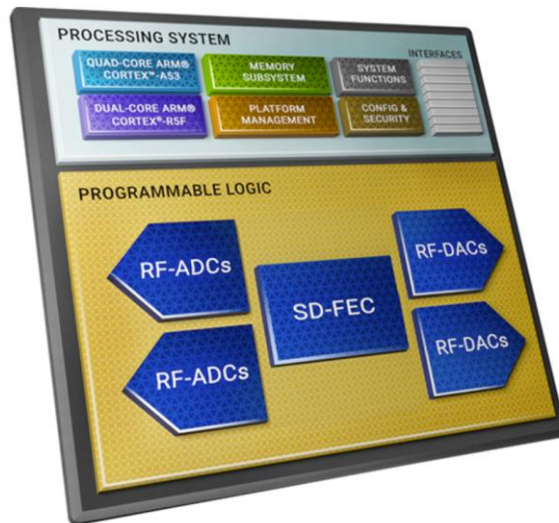


Le contexte

- 1- Besoin de mesure sur signaux rapides (*qq ns*)
- 2- Des taux de comptage élevé (*>100 kHz*)
- 3- Transmission rapides des données vers serveurs (*qq GETH*)
- 4- Des algorithmes complexes déportés



ZYNQ[®]
RFSoc



Ce que nous proposons:

- 1- Des ADC *14b/2.5 GHz* (FPGA_RFSOC) & DAC *16b/10 GHz*
- 2- Processeurs Temps Réel intégré aux FPGA
- 3- Transmission optique (*jusqu'à 10 Gbits*)
- 4- Time Stamp via SMART (*en développement au GANIL*)

Famille FPGA_RFSOC

Device Name		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	ZU65DR	ZU67DR	
		Gen 1					Gen 2	Gen 3					DFE			
RF Data Converter	Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5F MPCore up to 533MHz															
	12-bit RF-ADC w/DDC	# of ADCs	0	8	8	8	16	16	-	-	-	-	-	-	-	
		Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	-	-	-	-	-	-	-	
	14-bit RF-ADC w/DDC	# of ADCs	-	-	-	-	-	-	8	2	4	8	4	8	8	
		Max Rate (GSPS)	-	-	-	-	-	-	2.5	5.0	5.0	2.5	5.0	5.0	5.0	
	14-bit RF-DAC w/DUC	# of DACs	0	8	8	8	16	16	8	4	12	8	8	16	6	
		Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	9.85 ⁽³⁾	10.0 ⁽⁴⁾	
		SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0	0	
		Digital Front-End (DFE)	-	-	-	-	-	-	-	-	-	-	-	-	✓	
		Number of DDCs per RF-ADC ⁽¹⁾	0	1	1	1	1	1	1	2	1	1	1	1	1	
	RF input Freq max. GHz	4					5	6					7.125			
	Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x			
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930	489	489	
	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425	224	224	
	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0	6.8	6.8	
	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0	22.8	22.8	
	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5	45.0	45.0	
	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272	1,872	1,872	
	GTy Transceivers	16	8	16	16	16	16	8	16	16	16	16	16	8	8	
	PCIe® Gen3 x16	2	1	2	2	2	2	-	-	-	-	-	-	-	-	
	PCIeGen3 x16/Gen4 x8 / CCIX ⁽²⁾	-	-	-	-	-	-	0	2	2	2	2	2	0	0	
	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1	0	0	
	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2	1	1	
	System Monitor	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
		Speed Grades	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-1E, -1I, -1L, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1E, -1I, -1L, -2E, -2I, -2LI	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI
	Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	
	D1156	35x35	214, 72, 208 4, 16 0, 0													
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8		214, 24, 130 4, 8 6, 6	214, 24, 130 4, 8 10, 8	
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16			
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12						

Zynq® UltraScale+™ RFSOCs

1. This value applies when all RF I/O of an RF-ADC tile are used. 2. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213. 3. For operation up to 10GSPS, contact your local Xilinx Sales Representative. 4. 10GSPS RF-DAC operation is available in -2I speed grade.

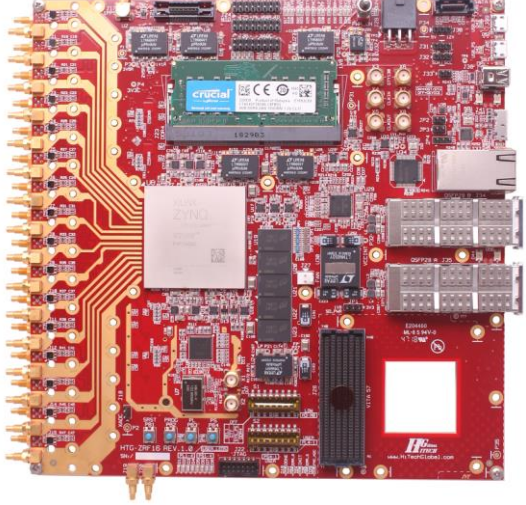
Caractéristiques

Featured Xilinx Devices

Featuring the Zynq UltraScale+ **XCZU49DR-2FFVF1760** RFSoc













14-bit, 2.5GSPS RF-ADC	16
14-bit, 9.85GSPS RF-DAC	16
Max. RF input Frequency (GHz)	6
System Logic Cells (K)	930
Memory (Mb)	60.5
DSP Slices	4,272
33G Transceivers	16
Maximum I/O Pins	408

Modules et Kits commerciaux



VP430 RFSoc board.

Zynq® UltraScale+™ RFSoc Boards & Kits Portfolio

Gen 1 4GHz		Gen 2 5GHz		Gen 3 6GHz	
<p>ZCU111 Evaluation Kit</p>  <p>ZU28DR Application Development and Performance Evaluation of: ADCs: 8x 12-bit 4.096GSPS DACs: 8x 14-bit 6.554GSPS SD-FEC: 8</p> 	<p>Avnet RFSoc Kit Development Kit</p>  <p>ZU28DR Wireless Application Development Leveraging: Xilinx ZCU111 Evaluation Kit Avnet Qorvo 2x2 Small Cell RF Front End 1.8GHz Card Avnet RFSoc Explorer with MATLAB and Simulink</p> 	<p>ZCU1275 Characterization Kit</p>  <p>ZU29DR Ideal for Tone Testing and Data Sheet Verification of: ADCs: 16x 12-bit 2.058GSPS DACs: 16x 14-bit 6.554GSPS</p> 	<p>ZCU1285 Characterization Kit</p>  <p>ZU39DR Ideal for Tone Testing and Data Sheet Verification of: ADCs: 16x 12-bit 2.220GSPS DACs: 16x 14-bit 6.554GSPS</p> 	<p>ZCU208 Evaluation Kit</p>  <p>ZU48DR Application Development and Performance Evaluation of: ADCs: 8x 14-bit 5.0GSPS DACs: 8x 14-bit 10.0GSPS SD-FEC: 8</p> 	<p>ZCU216 Evaluation Kit</p>  <p>ZU49DR Application Development and Performance Evaluation of: ADCs: 16x 14-bit 2.5GSPS DACs: 16x 14-bit 10.0GSPS</p> 



ZCU216 les éléments du kits

Featuring the Zynq® UltraScale+™ XCZU49DR-2FFVF1760 RFSoc



01

02



04



03



05



06



07



08



09



10



11



12



13



14



15

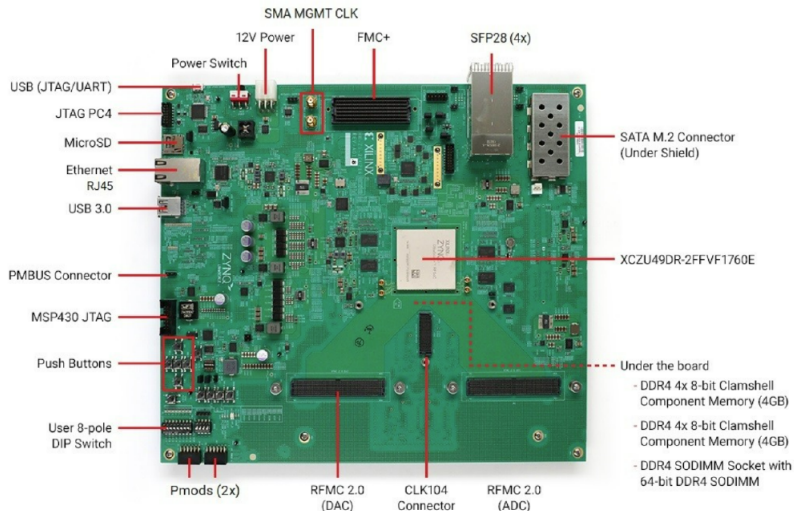


- 01 ZCU216 Evaluation Board
- 02 XM655 16T16R Breakout Add-On Card
- 03 XM650 16T16R N79 Band Loopback Add-On Card
- 04 CLK104 RF Clock Add-On Card
- 05 **6 Filters**
 - 2 Low Pass: DC-2500MHz
 - 2 Mid-Band Pass: 3000-4300MHz
 - 2 High-Band Pass: 4900-6200MHz
- 06 **2 Carlisle SMA 8 Cable Assemblies**
- 07 **2 SMA Cables**
- 08 **4 SSMP to SSMP Cables**
- 09 **4 Joy Signal Jumper Cables**
- 10 **Ethernet Cable**
- 11 **2 Micro USB Cables**
- 12 **MicroSD Card**
- 13 **Power Cords and Adapters**
- 14 **Vivado® Design Suite: System Edition Voucher**
- 15 **Hand Tools**

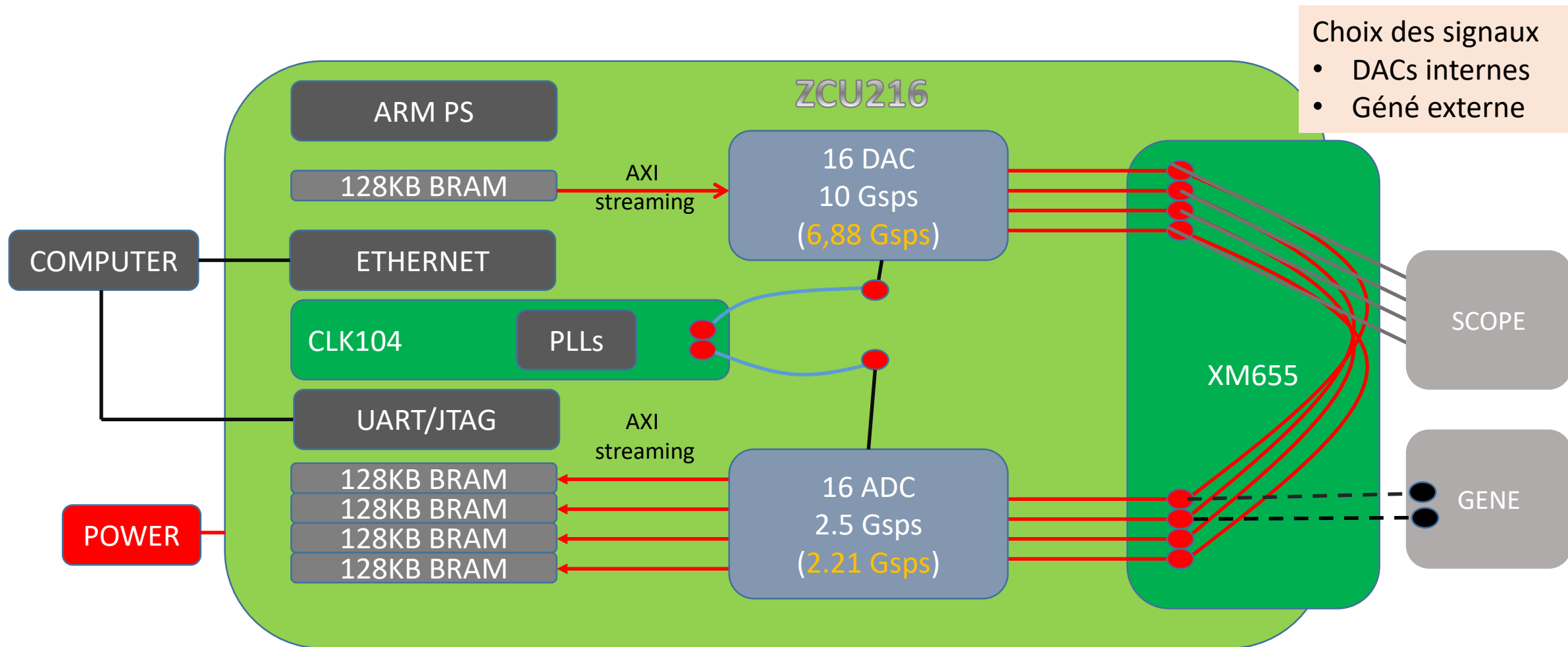
Front-end NEGMA (∠ Charles HOUARNER, Maria BLAIZOT)

The screenshot displays the Altium Designer PCB layout environment. The central workspace shows a detailed PCB layout for a front-end circuit, with components and traces rendered in green. The layout is densely packed, particularly in the lower right quadrant. The interface includes a standard Windows-style menu bar and toolbar at the top. On the left, the 'Design Information' panel lists various design aspects such as 'Workspace Name', 'Setup', 'Database Preparation', 'Placement', 'Constraints', 'Inplacement', 'Manufacturing Preparation', 'Manufacturing Deliverables', and 'Utilities'. On the right, the 'Options/Visibility' panel provides controls for 'Global visibility' and a 'View' section with a grid of checkboxes for different design layers like 'Layer', 'Coversure', 'Planes', 'Holes', and 'Holes'. A 'Through H!' option is also visible at the bottom of the grid.

Premiers pas



ZCU216 Synoptique banc de test



RF Data Converter Evaluation User Interface EUI

Configuration des ADCs et des DACs

Paramètre des PLLs

PC/Win10
EUI Client

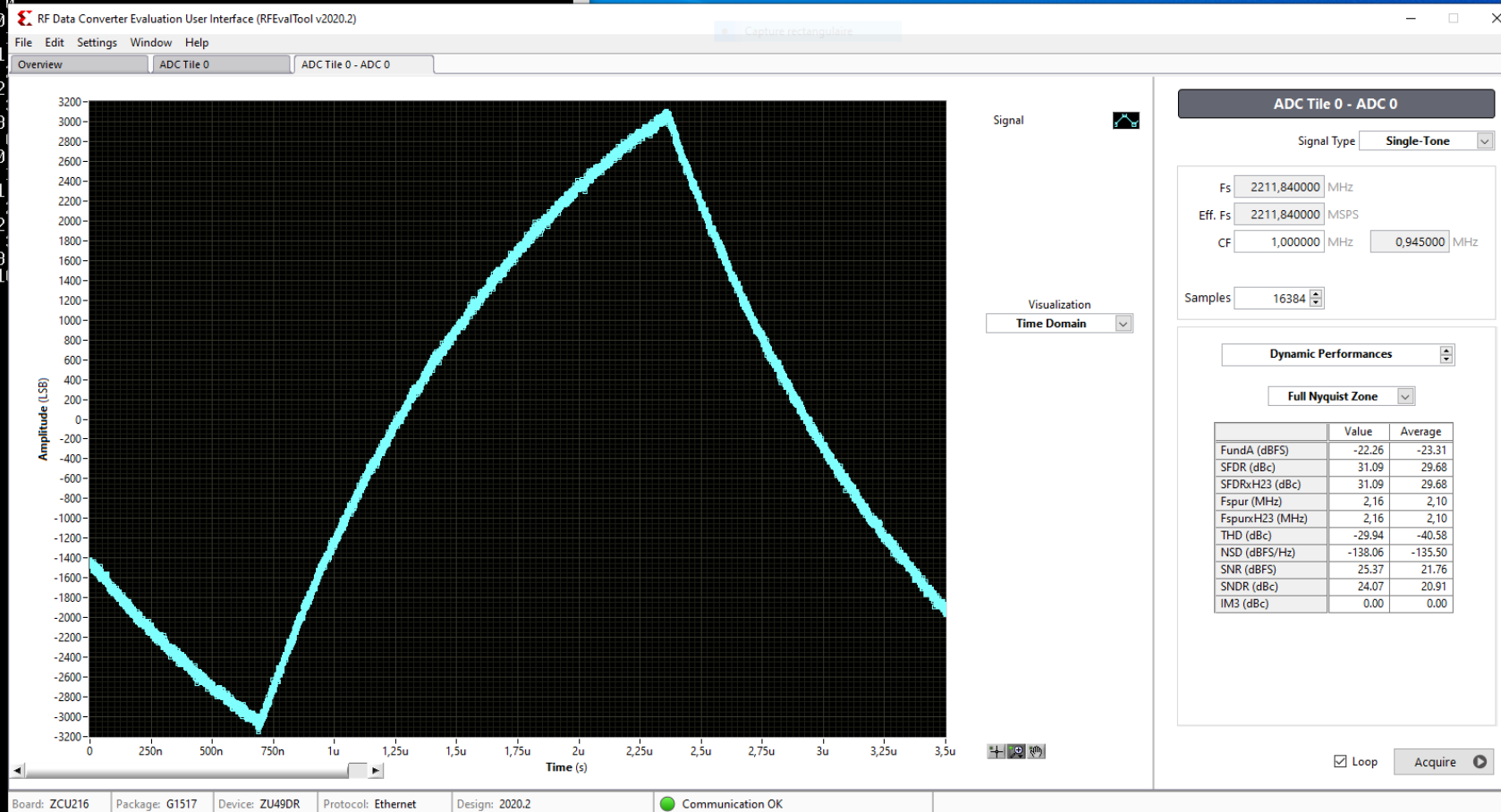
ZCU216
RFTOOL (Server)

Ethernet

The screenshot displays the RFEvalTool v2020.2 interface. The main window is titled "Board ZCU216" and shows a hierarchical view of the hardware configuration. The "Processing System (PS)" contains "Programmable Logic (PL)", which includes an "RF Data Converter Subsystem : DAC" and an "RF Data Converter Subsystem : ADC". Each subsystem is divided into four tiles (Tile 0 to Tile 3). Each tile contains a "PLL" block and a set of DACs (DAC 0, DAC 1, DAC 2, DAC 3) for the DAC subsystem, and a set of ADCs (ADC 0, ADC 1, ADC 2, ADC 3) for the ADC subsystem. A "Clock Distribution" section is also visible. On the right side, the "OnboardPLL" configuration panel is open, showing the "Onboard PLL" settings. It includes fields for "LMK REF Clock", "LMX ADC RFPLL", and "LMX DAC RFPLL". Below these fields is a diagram of the clock distribution network, showing "Clock 104" and "LMK" blocks. The diagram shows "ClkOut0" (245,760 MHz) connected to "Fosc" of "ADC LMX" and "DAC LMX". "ClkOut4" (245,760 MHz) is connected to "Fosc" of "DAC LMX". "ClkOut6" (245,760 MHz) is connected to "DAC REFCLK". "ClkOut12" (245,760 MHz) is connected to "ADC REFCLK". "ClkOut8" (122,880 MHz) is connected to "PL CLK (MMCM Fin)". "ClkOut3" (7,680 MHz) is connected to "AMS SYSREF". "ClkOut9" (7,680 MHz) is connected to "PL SYSREF". A note at the bottom right of the diagram states "All values are in MHz". At the bottom of the interface, there are "Power Settings" and "Clock Settings" buttons, and a status bar showing "Board: ZCU216", "Package: G1517", "Device: ZU49DR", "Protocol: Ethernet", "Design: 2020.2", and "Communication OK".

RF Data Converter EUI

```
COMS - Tera Term VT
Fichier Edition Configuration Contrôle Fenêtre(W) Aide
ZCU216 datapathmode for block_id 2
ZCU216 Interpolation for block_id 3
ZCU216 datapathmode for block_id 3
ZCU216 Interpolation for block_id 0
ZCU216 datapathmode for block_id 0
ZCU216 Interpolation for block_id 1
ZCU216 datapathmode for block_id 1
ZCU216 Interpolation for block_id 2
ZCU216 datapathmode for block_id 2
ZCU216 Interpolation for block_id 3
ZCU216 datapathmode for block_id 3
ZCU216 Interpolation for block_id 0
ZCU216 datapathmode for block_id 0
ZCU216 Interpolation for block_id 1
ZCU216 datapathmode for block_id 1
ZCU216 Interpolation for block_id 2
ZCU216 datapathmode for block_id 2
ZCU216 Interpolation for block_id 3
ZCU216 datapathmode for block_id 3
ZCU216 Interpolation for block_id 0
ZCU216 datapathmode for block_id 0
ZCU216 Interpolation for block_id 1
ZCU216 datapathmode for block_id 1
ZCU216 Interpolation for block_id 2
ZCU216 datapathmode for block_id 2
ZCU216 Interpolation for block_id 3
ZCU216 datapathmode for block_id 3
IP Address of the board: 169.254.1
Server Init Done
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Closed data and command sockets
Accepted data connection
Accepted command connection
Start data processing thread
Type: 0 Tile_Id: 0 Enable: 1
Type: 0 Tile_Id: 0 Enable: 1
Type: 0 Tile_Id: 1 Enable: 1
Type: 0 Tile_Id: 1 Enable: 1
Type: 0 Tile_Id: 2 Enable: 1
Type: 0 Tile_Id: 2 Enable: 1
Type: 0 Tile_Id: 3 Enable: 1
Type: 0 Tile_Id: 3 Enable: 1
Type: 1 Tile_Id: 0 Enable: 1
Type: 1 Tile_Id: 0 Enable: 1
Type: 1 Tile_Id: 1 Enable: 1
Type: 1 Tile_Id: 1 Enable: 1
Type: 1 Tile_Id: 2 Enable: 1
Type: 1 Tile_Id: 2 Enable: 1
Type: 1 Tile_Id: 3 Enable: 1
Type: 1 Tile_Id: 3 Enable: 1
```



EUI Xilinx

Vivado

The screenshot shows the RFEvalTool interface with a block diagram of DAC and ADC tiles and a configuration table below it.

Tile	Sample Clock (MHz)	PLL	Ref. Clock (MHz)	Output Divider (M)	Source Tile	Distribute Clock
DAC Tile 3	7864,320000	<input checked="" type="checkbox"/>	245,760	1	DAC Tile 2	None
DAC Tile 2	7864,320000	<input checked="" type="checkbox"/>	245,760	1	DAC Tile 2	Input Ref. Clock
DAC Tile 1	7864,320000	<input checked="" type="checkbox"/>	245,760	1	DAC Tile 2	None
DAC Tile 0	7864,320000	<input checked="" type="checkbox"/>	245,760	1	DAC Tile 2	None
ADC Tile 3	2211,840000	<input checked="" type="checkbox"/>	245,760	4	ADC Tile 2	None
ADC Tile 2	2211,840000	<input checked="" type="checkbox"/>	245,760	4	ADC Tile 2	Input Ref. Clock
ADC Tile 1	2211,840000	<input checked="" type="checkbox"/>	245,760	4	ADC Tile 2	None
ADC Tile 0	2211,840000	<input checked="" type="checkbox"/>	245,760	4	ADC Tile 2	None

The screenshot shows the Vivado IDE configuration for the Zynq Ultrascale+ RF Data Converter (2.4). The 'Tile Clocking Settings' table is visible.

Tile	Sampling Rate (G SPS)	Max Fs (G SPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)	Clock Source	Distribute Clock
ADC 224	2.21184	2.500	<input checked="" type="checkbox"/>	245.760	245.76	1	276.480	276.480	ADC224	Off
ADC 225	2.21184	2.500	<input checked="" type="checkbox"/>	245.760	245.76	1	276.480	276.480	ADC225	Off
ADC 226	2.21184	2.500	<input checked="" type="checkbox"/>	245.760	245.76	1	276.480	276.480	ADC226	Input Retick
ADC 227	2.21184	2.500	<input checked="" type="checkbox"/>	245.760	245.76	1	276.480	276.480	ADC227	Off
DAC 228	6.88128	7.000	<input checked="" type="checkbox"/>	245.760	245.76	1	573.440	107.520	DAC230	Off
DAC 229	6.88128	7.000	<input checked="" type="checkbox"/>	245.760	245.76	1	573.440	107.520	DAC230	Off
DAC 230	6.88128	7.000	<input checked="" type="checkbox"/>	245.760	245.76	1	573.440	107.520	DAC230	Input Retick
DAC 231	6.88128	7.000	<input checked="" type="checkbox"/>	245.760	245.76	1	573.440	107.520	DAC230	Off

Reverse Engineering:
Transposition des paramètres EUI dans Vivado

Configuration ADC/DAC

Reverse Engineering:
Transposition des paramètres EUI dans Vivado

ADC

Component Name: usp_rf_data_converter_0

Basic System Clocking Advanced

Converter Setup

Converter Setup: Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

Zynq Ultrascale+ RF Data Converter (2.4)

Multi Tile Sync Converter Band Mode Link Coupling

Enable Multi Tile Sync Band Single Link Coupling AC

Converter Configuration

ADC Pair 0,1 ADC Pair 2,3

ADC 2

Enable ADC Invert Q Output

Dither Enable ADC Observation Channel Ports

Enable TDD Real Time Ports Off

Data Settings

Digital Output Data Real

Decimation Mode 1x

Samples per AXI4-Stream Cycle 8

Required AXI4-Stream clock: 276.480 MHz

Mixer Settings

Mixer Type Coarse

Mixer Mode Real->Real

Frequency 0

Analog Settings

Nyquist Zone Zone 1

Calibration Mode Mode2

ADC 3

Enable ADC Invert Q Output

Dither Enable ADC Observation C

Enable TDD Real Time Ports Off

Data Settings

Digital Output Data Real

Decimation Mode Off

Samples per AXI4-Stream Cycle 8

Mixer Settings

Mixer Type Off

Nyquist Zone Zone 1

Calibration Mode Mode2

DAC

Component Name: usp_rf_data_converter_0

Basic System Clocking Advanced

Converter Setup

Converter Setup: Advanced

Changing Converter Setup to Simple will cause current Advanced IP configuration to be lost.

RF-ADC RF-DAC

Zynq Ultrascale+ RF Data Converter (2.4)

Multi Tile Sync Converter Band Mode Variable Output Current

Enable Multi Tile Sync Band Single Output Power 20.0 [2.25 - 40.5]

Converter Configuration

DAC Pair 0,1 DAC Pair 2,3

DAC 0

Enable DAC Invert Q Output

Inverse Sinc Filter

Enable TDD Real Time Ports Off

Data Settings

Analog Output Data Real

Interpolation Mode 1x

Samples per AXI4-Stream Cycle 12

Required AXI4-Stream clock: 573.440 MHz

Datapath Mode DUC 0 to Fs/2

Mixer Settings

Mixer Type Coarse

Mixer Mode Real->Real

Frequency 0

Analog Settings

Nyquist Zone Zone 1

Decoder Mode SNR Optimized

DAC 1

Enable DAC Invert Q Output

Inverse Sinc Filter

Enable TDD Real Time Ports Off

Data Settings

Analog Output Data Real

Interpolation Mode 1x

Samples per AXI4-Stream Cycle 12

Required AXI4-Stream clock: 573.440 MHz

Datapath Mode DUC 0 to Fs/2

Mixer Settings

Mixer Type Coarse

Mixer Mode Real->Real

Frequency 0

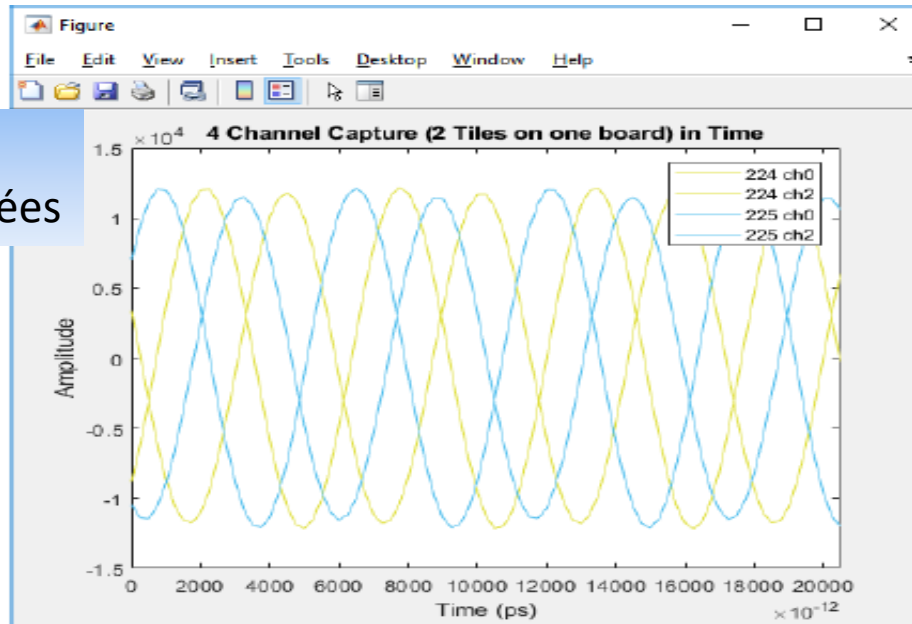
Analog Settings

Nyquist Zone Zone 1

Decoder Mode SNR Optimized

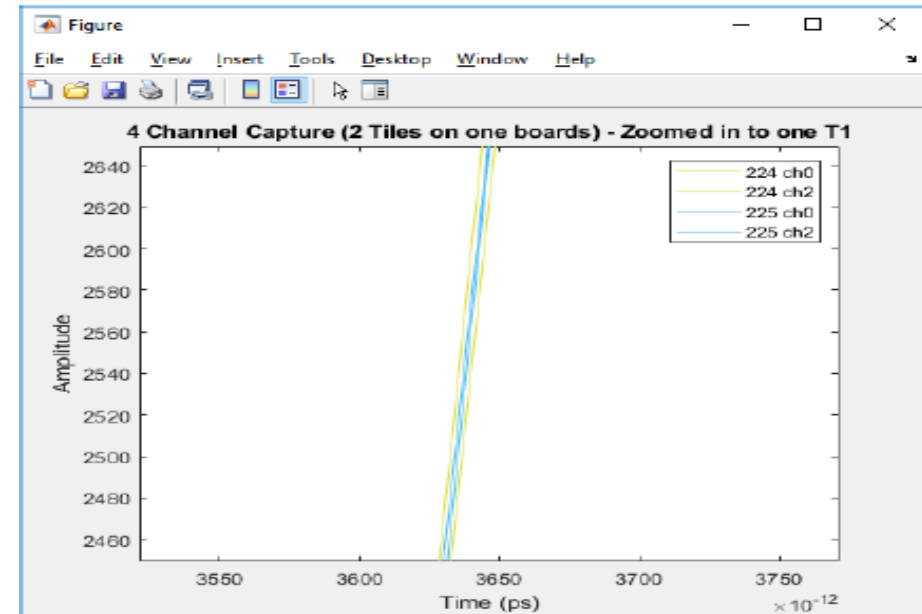
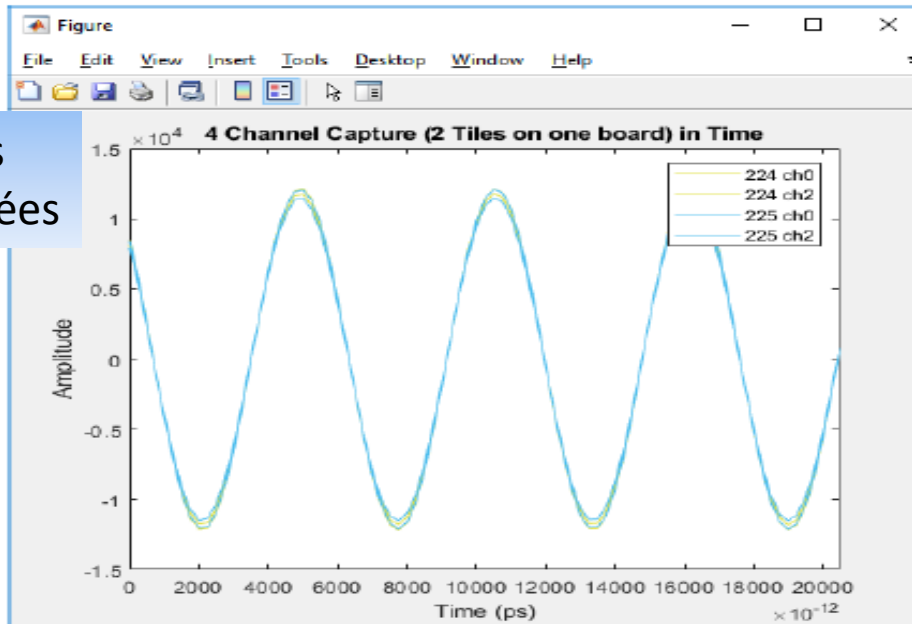
Capture ADC après MTS *Multi Tile Synchronization*

Voies
non alignées



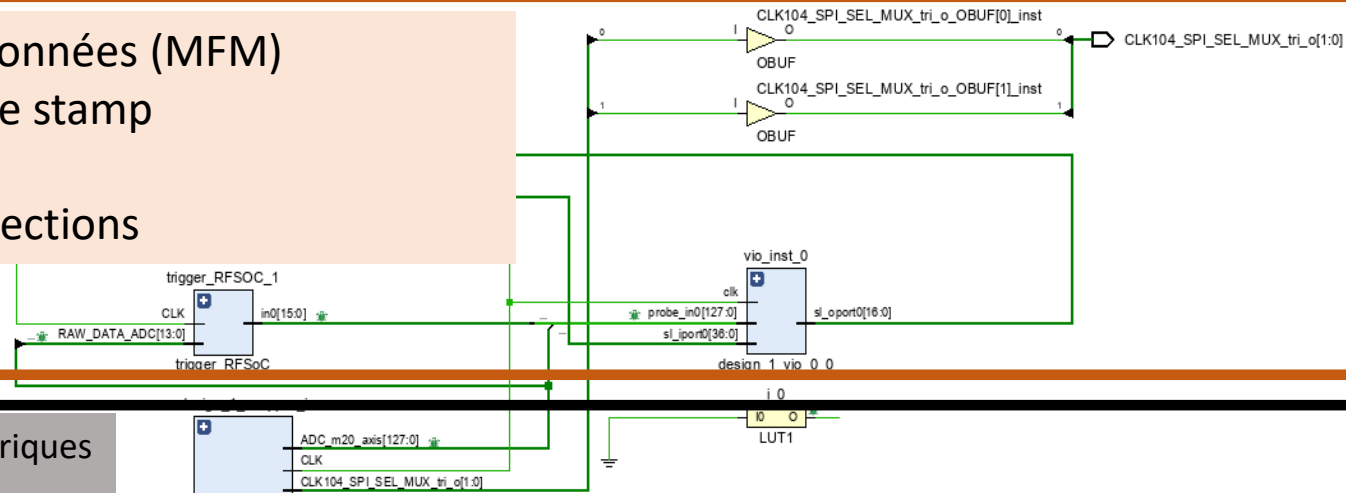
Octave
Alignement des voies

Voies
alignées



Top Level RFSOC Trigger

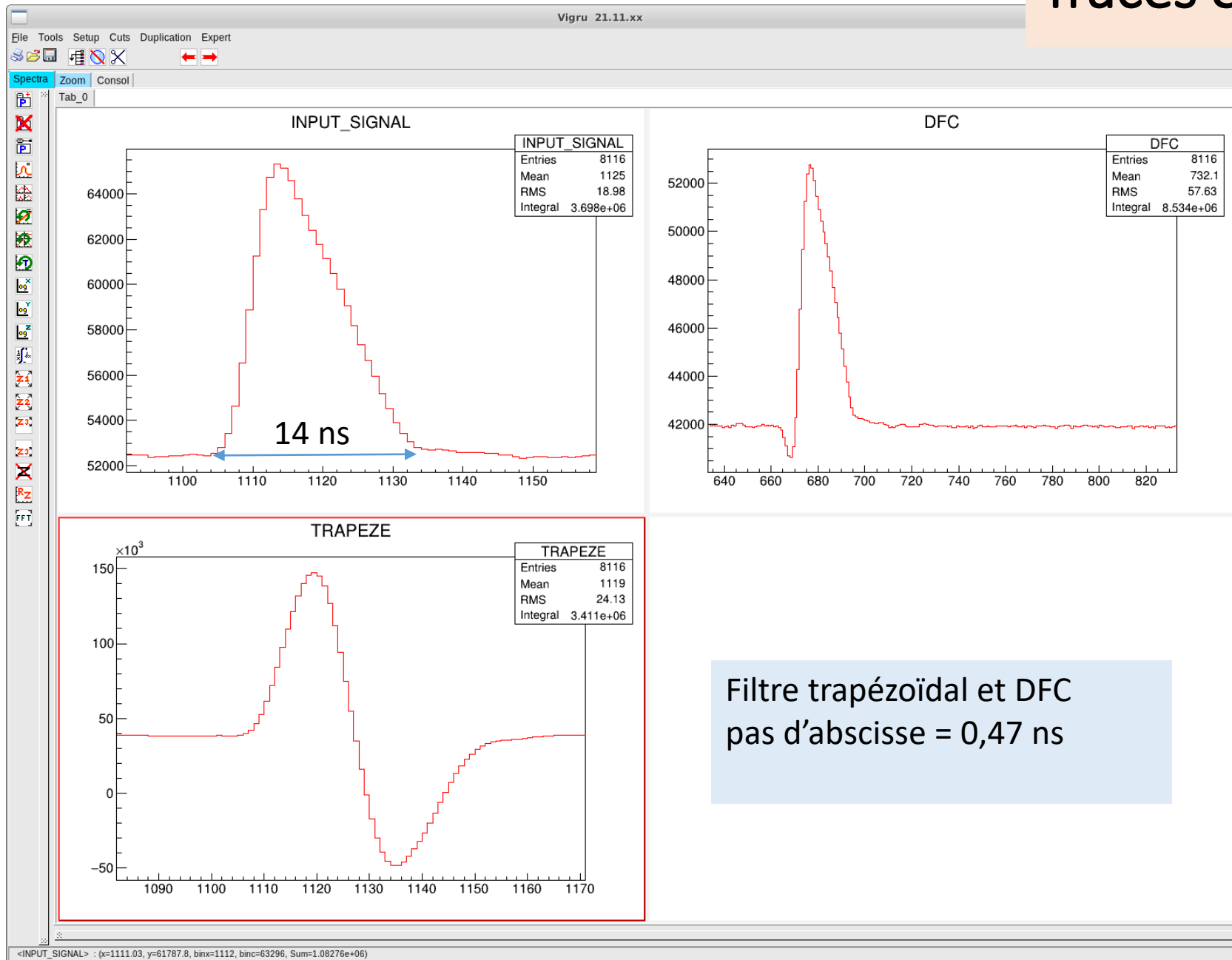
- Formatage données (MFM)
- Trigger / Time stamp
- Liens Gbits
- Debug / Inspections



- ARM PS / Périphériques
- RF-ADC / RF-DAC



Traces & TNS VIGRU



Déroulement

Phase 1

- Finalisation des programmes soft
- Firmware:
 - Time Stamp : prêt pour des tests avec SMART
 - Trigger : quelques ajustements en cours
 - Transmission optique : tests en cours
- Carte Front-End (Amplis d'entrées): routage de la carte en cours
- Mécanique du démonstrateur
- Validation du démonstrateur (ZCU216)

Phase 2

- Lancement et réalisation du projet final NEGMA
 - Nombre de modules, standard, partenaires...

Equipe actuelle (Démonstrateur)

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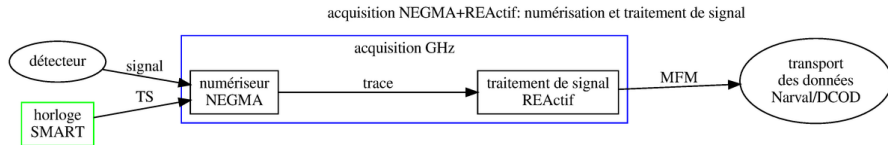
Equipe actuelle (Démonstrateur)

- **Hard** : A. Boujrad, C. Houarner, M. Blaizot, P. Bourgault
- **Soft** : L. Legeard, S. Coudert

flux d'acquisition

NEGMA + REActif

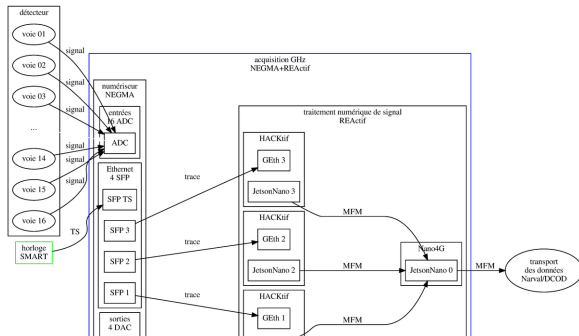
- NEGMA: numérisation + horodatage
- REActif: traitement du signal



matériels d'acquisition

NEGMA + REActif

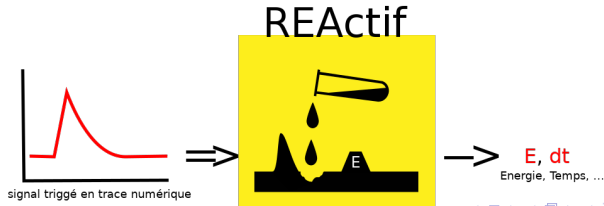
- NEGMA: 1 kit de développement RF-SOC ZCU-216 (Xilinx)
- REActif: 3 cartes HACKtif (GTA -open source-), 1 kit de dev.



REActif: traitement informatique du signal

REActif

- réaliser le traitement du signal de manière \oplus souple et \oplus rapide dans un co-processeur facilement programmable
- traitement du signal triggé en provenance du numériseur sur co-processeur en langage informatique (C++)
- plateforme embarquée afin d'être \oplus proche du numériseur avec un encombrement minimal et \ominus énergivore
- transfert NEGMA \Rightarrow REActif en GEthernet (16kB MFM)



REAction: traitement du signal sur co-processeur

code informatique

- traitement du signal sur GPU en langage informatique (CUDA=C++) 1 coeur par trace (ex. calcul d'énergie)
- plusieurs traces en parallèle (ex. 128 traces sur JetsonNano)

calcul de l'énergie d'un signal: code de filtrage trapèzoidal (CUDA)

```

__global__ void trapezoidal_filter(const float *e, *s , int dimX, dimY
, const int ks, const int ms, const float alp, const int decalage)
{
const int si = threadIdx.y*dimX, ei = si+dimX, pi = si+decalage-1;
//create a filter
for(int n=pi;n<ei;++n)
s[n]=2*s[n-1]-s[n-2] + e[n-1]-alp*e[n-2] -e[n-(ks+1)]
+alp*e[n-(ks+2)]-e[n-(ks+ms+1)]+alp*e[n-(ks+ms+2)]
+e[n-(2*ks+ms+1)]-alp*e[n-(2*ks+ms+2)];
}
    
```

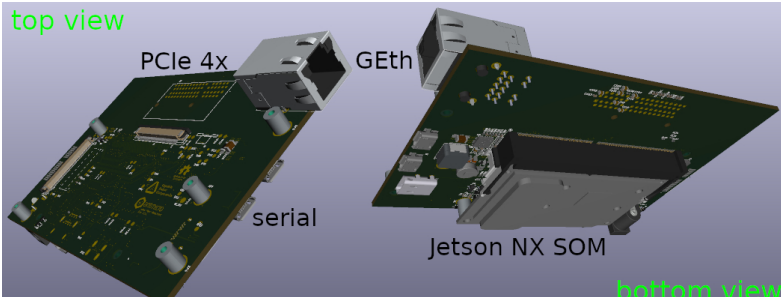

carte HACKtif (∠ Patrice BOURGAULT)

dim. 120x85mm pour les chassis NIM, μ TCA, ... ou sur table.

matériel

- carte mère open source (GANIL/DPHY/GTA)
 - dessin sous KiCAD (projet open source)
 - SOM Jetson NX sur connecteur SODIMM: Nano, TX2 ou xNX
- carte fille GEthernet PCIe 4x

top view

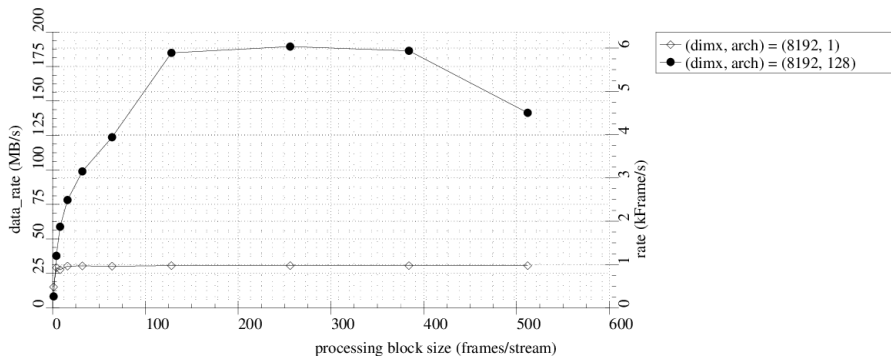


bottom view

performance JetsonNano

calcul d'énergie: Jetson Nano

perf.: 6k frame/s, 200 MB/s, >1GEth (16kBoF=8kS on 128 GPU cores)

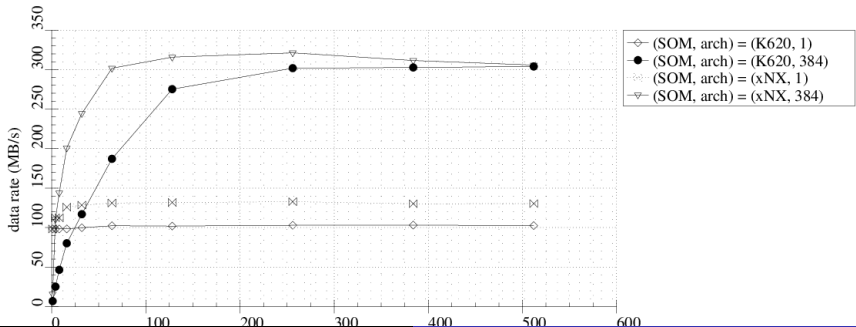


data rate (and frame rate) vs. 8kS frames per stream (1 str. on 128 cores in mode 10W) arch.=Nano

performance énergétique et encombrement

calcul d'énergie sur 384cores: Jetson xNX vs i5+K620

- performance identique entre embarqué/PCle
- 10 fois moins de consommation électrique (10W vs 100W)
- 10 fois moins d'encombrement (1L vs 10L)



conclusion et perspectives

NEGMA

- numériseur GHz+TS (carte RF-SOC)
- carte front-end DC (au lieu de RF)
- traces triggées sur 3 liens SFP

REActif

- traitement du signal en langage simple, souple et REActif
- tests préliminaires convainquants en parallélisation naive
- gains en prix, énergie et encombrement (carte HACKtif)

NEGMA+REActif

- rassemblement de RF-SOC + HACKtif via lien SFP
- tests, tests, tests.